Virtual Display Color Processor

Disclaimer

Overview

The Virtual Display Color Processor (VDCP) is a hardware tool for monitoring the pixel data sent from the computer to the display via the Digital Video Interface (DVI) cable. The VDCP is a circuit board to be connected between the DVI cable and the DVI port. The VDCP circuit retrieves the red, green, and blue subpixel values of the target pixel and then show the subpixel values on the display. The hardware portion of VDCP consists of a field programmable gate array (FPGA) board (Cyclone III QB3, Altera) and a DVI daughter board (DVI-HSMC, Terasic). The software portion of VDCP, as described in this document, was designed with the Verilog hardware description language.

Functions

- By pressing a button, it switches between 8 lookup tables for emulating various tone reproduction curves.
- It shows the RGB values of a center pixel for the last 4 frames. The pixel location is centered enough to be included in the test patterns generated by the color

calibration kit but not underneath the sensor to hinder the measurement.

- The color processor writes the 256-byte EDID information into the DVI receiver such that the computer can retrieve the information of available resolutions.

Target System Requirements

- A display using a single-channel DVI port
- A computer (or image device) driving the display through a DVI port
- A fully-pinned DVI cable

System Requirements

- Cyclone III FPGA Starter Kit (QB3), Altera. Ordering code: DK-START-3C25N.

  http://www.altera.com/products/devkits/altera/kit-cyc3-starter.html
- DVI transmitter/receiver board (HSMC-DVI), Terasic. Part No: P0017.

  http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&No=359

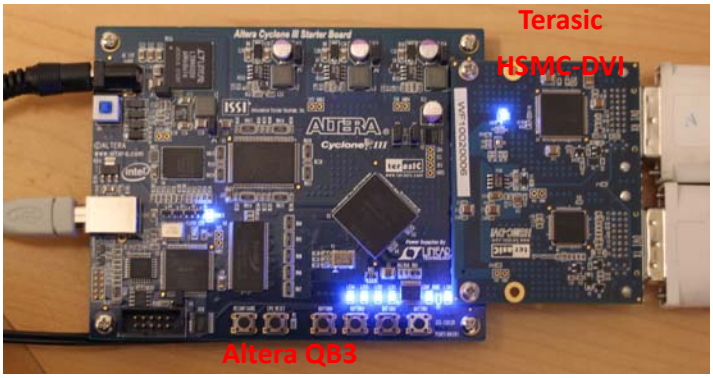

Figure 1: Cyclone III FPGA Starter Kit (left) and DVI board (right).

- Altera Quartus II Web Edition Software (Version 13, free download)

  http://www.altera.com/products/software/quartus-ii/web-edition/qts-we-index.html
- VPCP code developed by FDA/CDRH/OSEL/DIAM

Installing Quartus II Web Edition:

(1) Download Quartus II Web Edition Software from http://dl.altera.com/?edition=web

Figure 2: Download screen for Quartus II Web Edition.

(2) Install Quartus II Web Edition Software

Downloading VDCP Software

Download VDCP software from code.google.com/p/vdcp including the following files:

- VDCP.v
- DVI_Demo.v

Compiling VDCP Software

Create a new folder and copy the files from the “DVI_Demo” project on the CDROM that comes with the HSMC-DVI board

Copy the two files “VDCP.v” and “DVI_Demo.v” into the new folder such that:

The “VDCP.v” is added, and

The old “DVI_Demo.v” is replaced

Open the “DVI_Demo” project

Compile the project

If the compilation is successful, a binary file “DVI_Demo.sof” will be generated in the same folder

Uploading VDCP Software onto QB3

(1) Run Quartus II Web Edition and find “Programmer” in the “Tools” tab

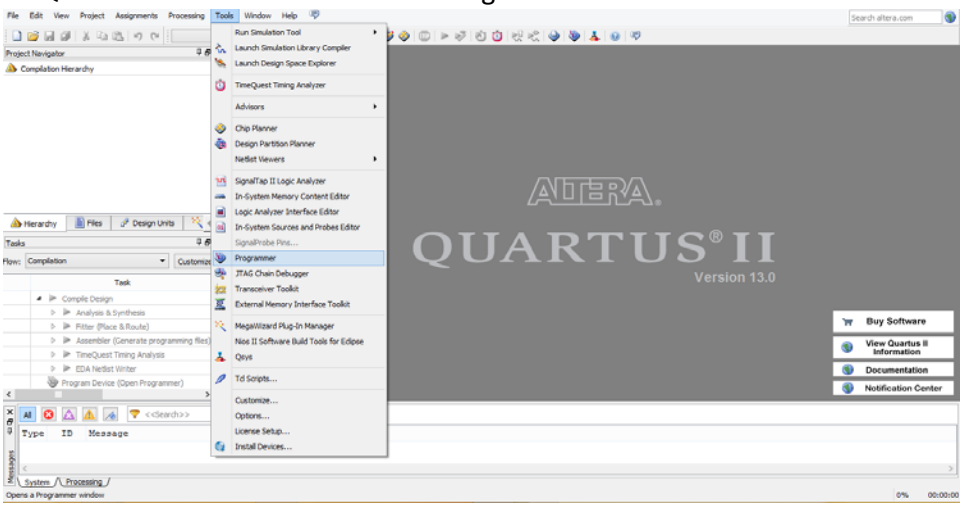

Figure 3: Locate the “Programmer” menu.

(2) Open the “Programmer” and click on the “Add File…” button

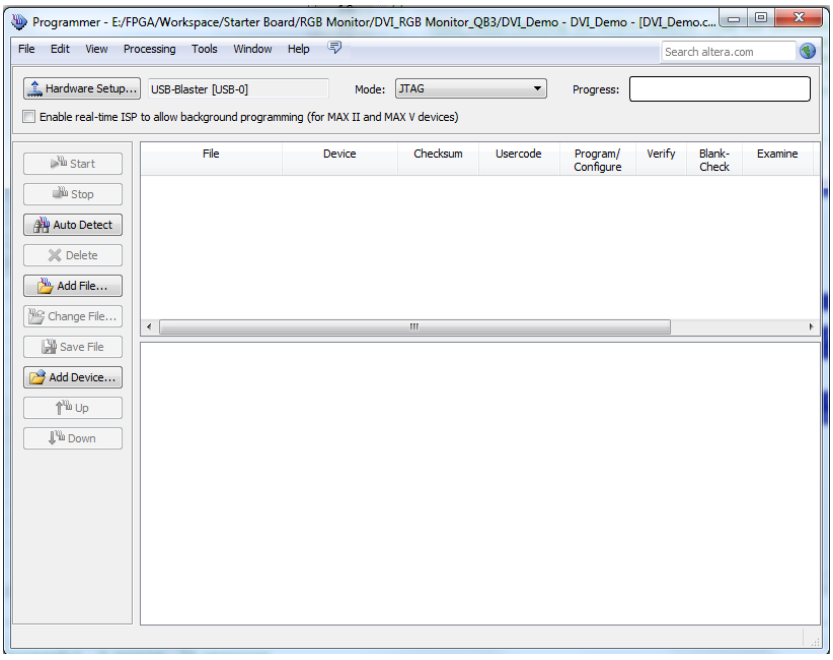

Figure 4: The Programmer is used to upload code onto the FPGA board.

(3) Choose the “DVI_Demo.sof” file

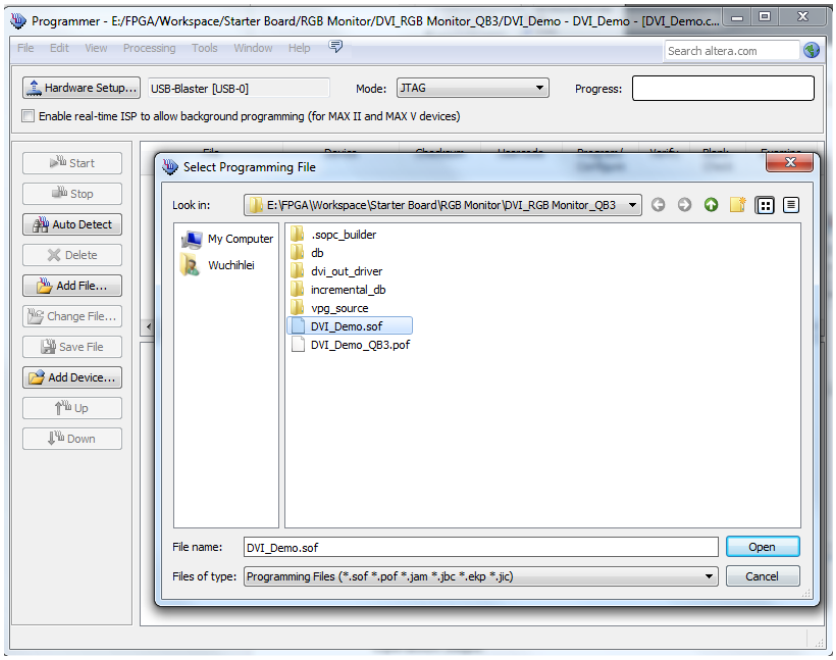

Figure 5: Choose the binary file for uploading.

(4) Press the “Start” buttom to start program.

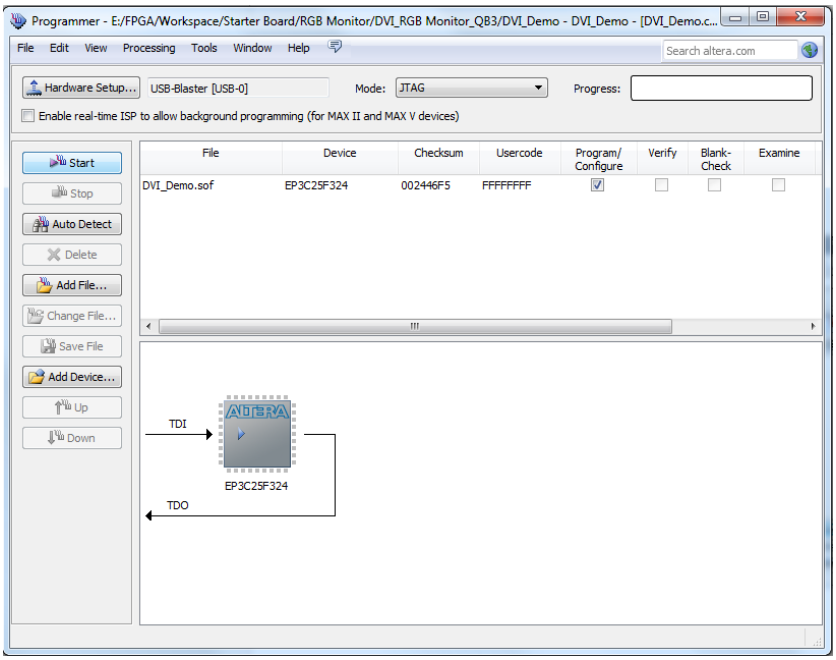

Figure 6: Click Start to start uploading.

Using VDCP

(1) The FPGA will restart after the programming finishes

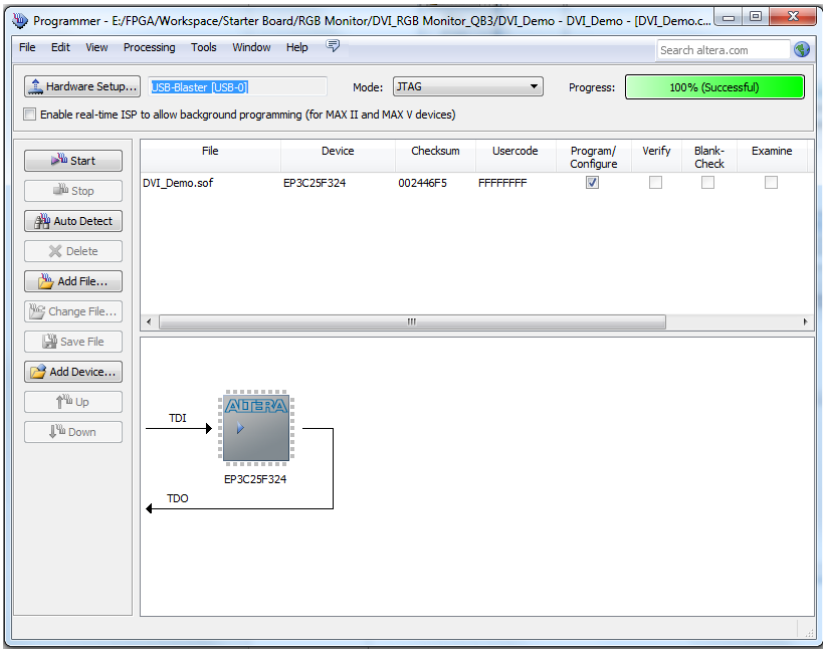

Figure 7: The FPGA board is reset after the uploading completes.

(2) The first image shown on the screen is the following color chart

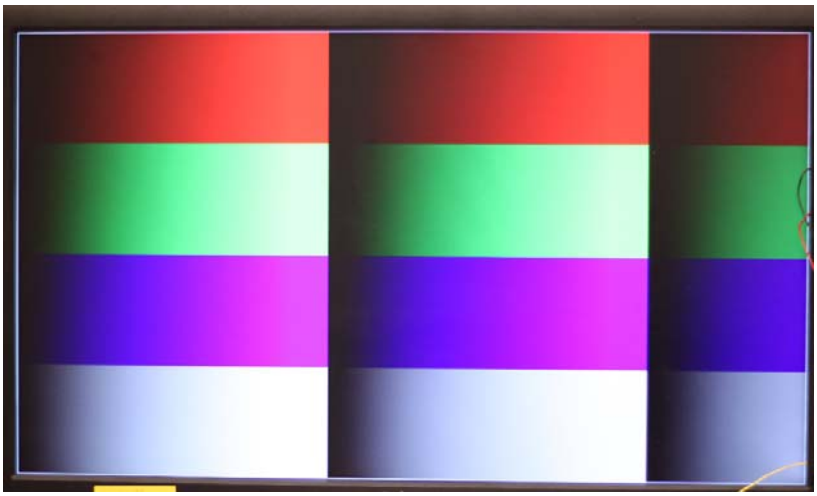

Figure 8: The FPGA shows a color chart if the code is uploaded successfully.

(3) Briefly press the “BUTTON3” button on the FPGA board

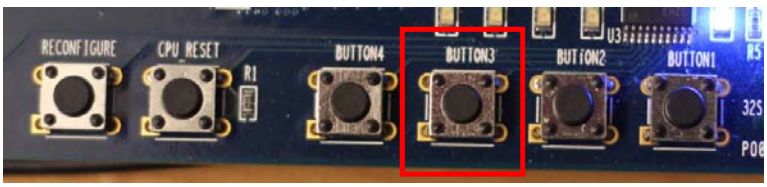

Figure 9: Press Button3 to bring the DVI image content back to the display.

(4) The display will show the image content from the DVI input

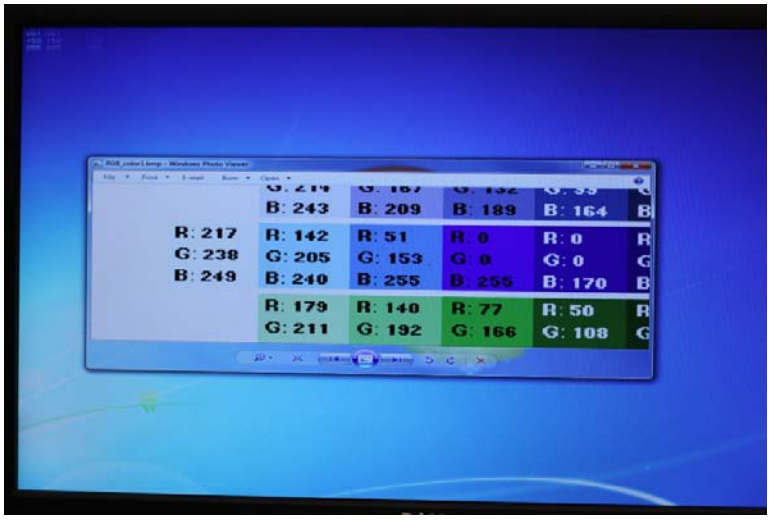

Figure 10: The display shows the image content from the computer, which is a test pattern for verifying the VDCP.

(5) The target pixel in the center is marked by a red box

Figure 11: The target pixel is surrounded by a red box. Move the color patch of interest to cover this target pixel and its subpixel values will be read and shown on the top left corner.

(6) The red, green, and blue subpixel values are shown on the top left corner. There are 4 columns. Each column, from top to bottom, consists of the red, green, and blue subpixel values of the target pixel at time t when the frame is refreshed. The 4 columns, from left to right, represent time t, t+1, t+2, and t+3, respectively. In other words, the 4 columns represent the subpixel values in the last 4 consecutive frames.

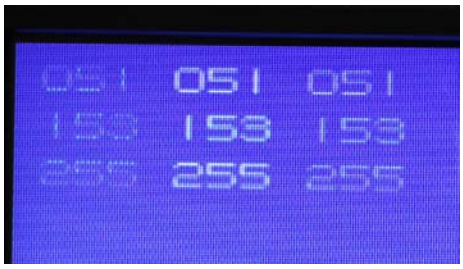

Figure 12: The VDCP shows the pixel read-out as 4 columns of red, green, and blue subpixel values.

(7) The VDCP code needs to be uploaded again once the FPGA power is turned off

Citation

70.2: Virtual Display: A Platform for Evaluating Display Color Calibration Kits
WC Cheng, A Badano
SID Symposium Digest of Technical Papers 42 (1), 1030-1033

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