Department of Electrical EngineeringCity University of Hong Kong

EE 1001 Foundations of Digital Techniques

Laboratory Manual

Aims:

- 1. To familiarize simple logic circuits
- 2. To get acquaintance with logic ICs (integrated circuits)
- 3. To implement logic circuits with bread board

Laboratory Sessions:

LAB1 Familiarization of simple logic circuits

LAB2 Using logic gates to fabricate a 4-bits adder

Notes:

1. Student is required complete the experiment within 3 weeks.

Components (per Student):

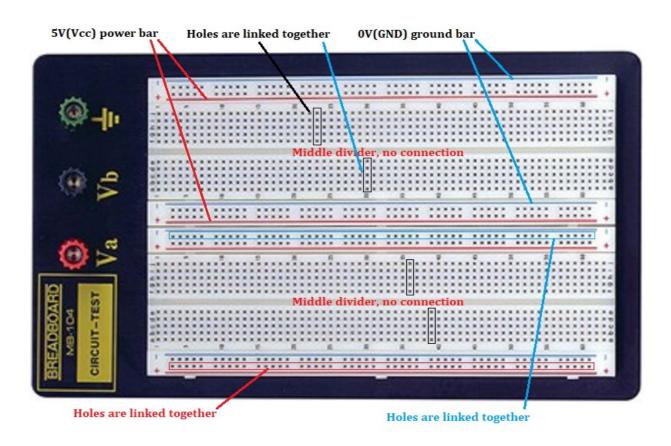
1
2
1
1
2
8
2
10
10
1
0.5M
0.5M
2M
2M

Submit your work to laboratory supervisor

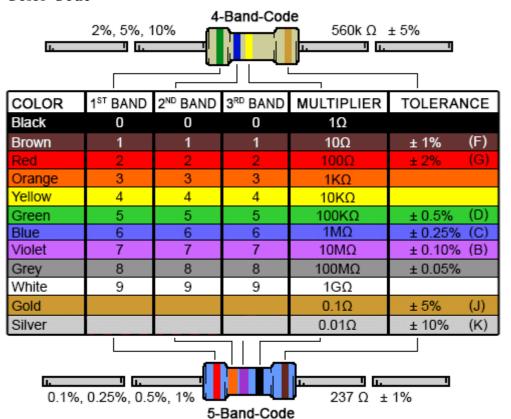
Experiment 1: pages 7-8

Experiment 2: Pages 9-10

Introduction to bread board:

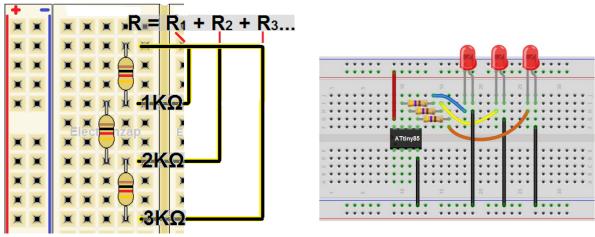


Resistor Color Code



Examples of circuit connection:

Series three 1K Ω resistors to obtain 3 K Ω resistance



Tutorial on how use bread board is available on youtube:

https://www.youtube.com/watch?v=6WReFkfrUIk

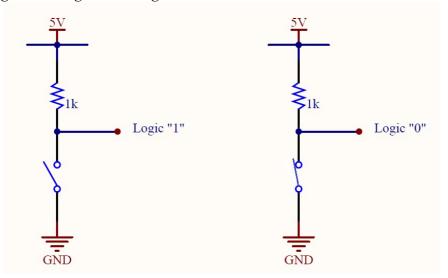
A few tips for logic circuit implementation:

Use the following circuit to produce logic "1" and logic "0" as input to the logic circuit.

$$5V \longrightarrow 1 \text{ K}\Omega$$

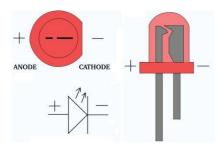
IMPORTANT: NEVER directly connect to 5V to obtain logic "1", the logic gate IC may easily be damaged.

2. Using switch to generate Logic "1" & "0"

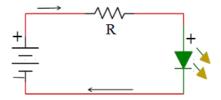


3. Use LED to indicate Logic "1" & "0"

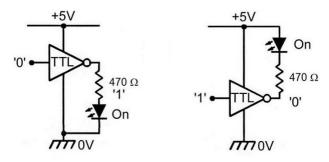
LED is with polarity, with long leg representing anode and short leg representing cathode.



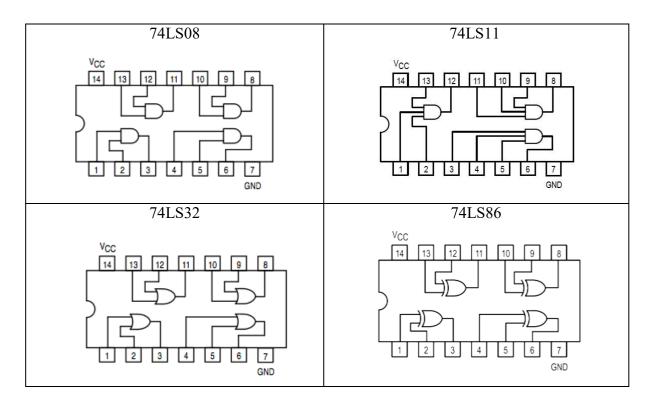
To turn a LED, the LED should be forward-biased as shown below:



The following circuit shows the TTL output circuits for turning on the LED with either logic "1" output or logic "0" output. The function of the resistor is to limit the current passing through the LED to avoid damage.



TTL Logic IC Pin assignment:



For detail data sheet, search from Google to obtain on-line.

For example: Type "74LS86 datasheet pdf" to search for detail information for 74LS86 IC.

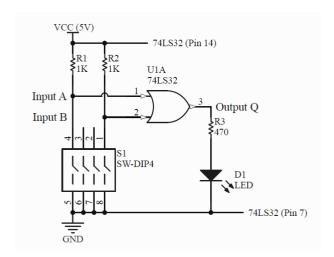
Name:	.SID	:

Experiment 1: Familiarization of simple logic circuits

Refer to Pages 3 to 6 and watch the youtube clip for breadboard fundamentals.

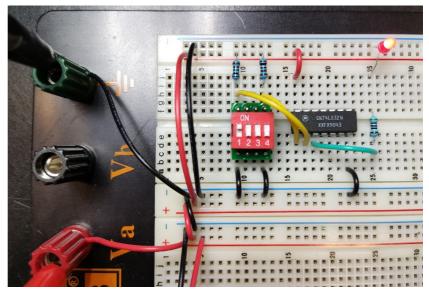
74LS32:

Connect the circuit as shown below schematic diagram and complete the logic table.



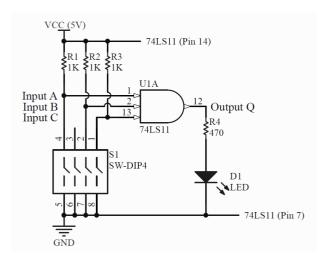
74LS32

Inp	Output					
Α	A B					
0	0					
0	1					
1	0					
1	1					



74LS11:

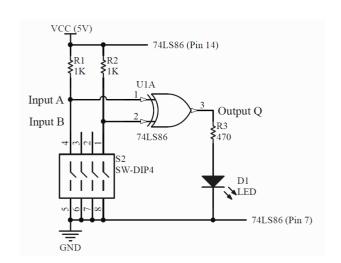
Connect the circuit as shown below schematic diagram and complete the logic table.



74LS11			
	Output		
Α	В	С	Q
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

74LS86:

Connect the circuit as shown below schematic diagram and complete the logic table.



74LS86

Inp	Output	
Α	В	Q
0	0	
0	1	
1	0	
1	1	

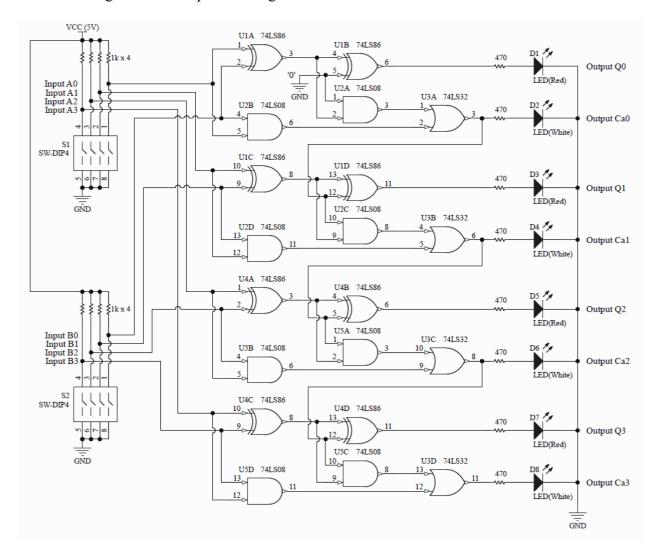
Show your results to Laboratory Supervisor.

Items	Grade
Attitude and progress (1 – 10)	
Quality of implementation (1 – 10)	
Completion % (0% – 100%)	
Supervisor Signature	

Name:	.SID:	
rame.	.SID.	

Experiment 2: Using logic gates to fabricate a 4-bits adder

Student need to watch a youtube video (https://www.youtube.com/watch?v=wvJc9CZcvBc) of a 4-bit adder and fully understand the working principle. Connect the circuit as shown below schematic diagram and complete the logic table.



N.T.	CID	
Name:	.SID:	

	Input										Out	tput			
А3	В3	A2	В2	A1	B1	Α0	В0	Ca3	Q3	Ca2	Q2	Ca1	Q1	Ca0	Q0
0	0	0	0	0	0	0	0								
0	0	0	0	0	0	0	1								
0	0	0	0	0	0	1	0								
0	0	0	0	0	0	1	1								
0	0	0	0	0	1	0	0								
0	0	0	0	1	0	0	1								
0	0	0	0	1	1	1	0								
0	0	0	0	1	1	1	1								
0	0	0	0	1	0	0	0								
0	0	0	1	1	0	0	1								
0	0	1	0	1	0	1	0								
0	0	1	1	1	0	1	1								
0	0	0	0	1	1	0	0								
0	1	0	1	1	1	0	1								
1	0	1	0	1	1	1	0								
1	1	1	1	1	1	1	1								

4-bit	s Ado	der (fo	or dei	mons	tratio	n)									
	Input										Out	put			
А3	В3	A2	B2	A1	B1	Α0	В0	Ca3	Q3	Ca2	Q2	Ca1	Q1	Ca0	Q0
0	0	0	0	0	0	0	0								
0	0	0	0	0	0	0	1								
0	0	0	0	0	0	1	0								
0	0	0	0	0	0	1	1								
0	0	0	0	0	1	1	1								
0	0	0	0	1	1	1	1								
0	0	0	1	1	1	1	1								
0	0	1	1	1	1	1	1								
0	1	1	1	1	1	1	1								
1	1	1	1	1	1	1	1								

Show your results to Laboratory Supervisor.

Items	Grade
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Quality of implementation (1 – 10)	
Completion % (0% – 100%)	
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