BUSREQ and BUSACK

The Z80 has a feature that allows an external peripheral to take over the bus. This is commonly used for DMA - direct memory access - which allows data transfers to take place directly across the bus under external control, rather than through the CPU. For instance, a block of data can be copied from an I/O device such as a disk drive directly to memory. Or a block of data can be copied from memory to an I/O device. Finally, a memory-to-memory copy can take place.

The advantage of DMA is that it can be considerably faster than requiring the CPU to read and write each byte. The Z80 family includes a Z80 DMA chip that provides this DMA functionality. This chip is described in more detail in the peripheral chapter.

The Z80 provides two pins - BUSREQ and BUSACK - that allow an external device to take over the bus. In this state, the Z80's address bus, data bus, and main control signals (MREQ, IORQ, RD, and WR) enter a high-impedance state, effectively disconnecting them.

The BUSREQ (Bus Request) pin is pulled low by a device that wishes to take over the bus. The Z80 pulls BUSACK (Bus Request Acknowledge) low when it has given up the bus.

The Z80 only gives up the bus at the end of an M cycle. The BUSREQ pin is sampled at the rising clock edge of the last T state. When the bus is released, the BUSACK pin is activated on the rising edge of what would be the first T state of the next cycle.

While the bus is inactive, the Z80 ignores all interrupts, including NMI. Also, there are no memory refreshes, which can be a problem if the bus is inactivated for a long time, as memory could start losing its data.

Like other input pins, BUSREQ is clamped with a diode. It goes through two latches that form an edge-triggered flip flop, grabbing the value when the clock goes high. This value is combined with the last_t_cycle value (and a

rest/interrupt value?) to generate the new T cycle if the bus is not requested. If the bus is requested, it looks like the T cycle latches get cleared, and the bus request circuitry suppressed the T1 state. It's unclear how the T1 state starts up when the bus is given back to the Z80. It looks like the w150 is 1 while the bus is inactivated. This control line both forces the T1 output low and forces the new T1 flag w1380 high. Thus, while the bus is inactive, the Z80 is in no T state, but will enter T1 when the bus is given back.

A latch holds the busack state. This is cleared when BUSREQ becomes inactive, delayed by the clock. It is also cleared by a reset? Should investigate what happens when reset and BUSREQ are combined.

The output circuit has a clocked pass transistor for the signal that puts the control lines into tri-state. This should force them low through the low clock, which may be half a cycle longer than the BUSACK pin. Specifically, BUSACK is inactivated (high) in T1l, while the bus doesn't become active until T1h.

These T states are the internal ones. Keep in mind that external states are half a cycle later. From the external perspective, BUSACK is released half a cycle before T1, and the bus becomes active at the start of T1 (T1h).