More pins

The HALT/ output pin is pulled low when the processor is in a halt state, triggered by a halt instruction.

While in the HALT state, the CPU executes the equivalent of NOPs until an interrupt is received, or the CPU is reset. The CPU goes through the standard M1 cycle. It fetches an instruction, but discards the instruction and performs a NOP instead. Then the memory refresh occurs. This ensures that memory is refreshed, which wouldn't happen if the CPU were totally halted.

The interrupts (NMI and INT) are sampled on the rising edge of T4, and if an interrupt occurs, the HALT state is exited at the start of T1, and an interrupt cycle starts.

The halt state is maintained by a latch near the HALT pin. Several conditions are required to enter the halt state: the PLA 95 (indicating HALT) must be triggered, along with no interrupts. Several conditions will clear the halt state: reset, interrupt, or other control lines to be examined.

As with other output pins, large transistors drive the HALT pin.

The IORQ/ pin is a tristate output pin used for IO requests. It goes low to indicate that the (lower half) of the address bus holds an I/O address from 0 to 255 for an I/O read or write.

The second use of IORQ is it is used in the interrupt acknowledge cycle. It goes low during M1 to indicate that an interrupt response vector can be placed on the data bus. In this case, IORQ takes place of the MREQ signal in M1 that normally indicates an op code fetch.

Note that a regular I/O request will not issue an I/O address during M1, since that is the fetch cycle. Thus, the two uses of IORQ will not conflict.

IORQ is put into a tristate output during BUSREQ/BUSACK, allowing other devices to control the line. The w111 control prevents a high output. The low

output doesn't occur during a BUSACK assuming the pin will be inactive at this time.
The logic to control IORQ is fairly complex, since there are multiple situations that can drive it. Its state is latched, and then the latch drives the output pin through the drive transistors.

One latch input (156) deactivates IORQ every T1l state; this is the end of an input/output address cycle.

Another input (176) deactivates IORQ in M1T3h. This ends the IORQ for an interrupt.

The IORQ latch is activated by w1338, which is associated with interrupt activation. It happens in M1.

The other IORQ latch activation is through w1340, which is triggered from T2 and the inout wait signal which indicates the M cycle associated with the I/O operation. This activates IORQ starting in T2h of the I/O operation.

MREQ

The MREQ pin indicates a memory request. Specifically, it goes low when the address bus holds a valid address, either for a read or write.

For an instruction fetch, MREQ is low from T2l through T3l. For a memory read or write, it is low half a cycle longer, from T2l through T3h.

When MREQ is low along with RFSH, it indicates the lower 7 bits of the address bus can be used as a refresh address. For this purpose, it is low through the M1T4 state.

The MREQ pin is similar to IORQ. It is a tristate output which is disabled during a BUSACK phase.

Like IORQ, it is controlled by a latch.

The latch is activated by w1384 being low, which happens in T1h/T2l or M1T3h/M1T4l, but delayed until the clock is low too, so the pin becomes active in T2l or M1T4l.

The latch will not be activated if the skip-M-cycle discussed in the address pin chapter is high. That is, if the M cycle doesn't correspond to a memory access, MREQ is deactivated for the entire M cycle.

The latch is cleared by the same M1T3 signal as deactivates IORQ. It is also cleared by the same T1 signal.

RD/
The RD/ pin goes low to indicate a read. That is, the pin goes low when the CPU requests to read data from memory or an I/O device. This is also an active-low tristate pin, that become high-impedance when the bus is taken over during BUSACK.

For an instruction fetch, the RD pin goes low from T2l through T3l, the same as MREQ. However, the RD pin remains high during the memory refresh, unlike the MREQ pin.

For a memory read, the RD pin goes low from T2l through T3h, same as MREQ. For a memory write, the RD pin remains high.

Finally, for an I/O read, the RD pin goes low from T2h through T3h, the same as IORQ.

The hardware implementation of RD resembles the other pins, with a latch driving large transistors.

The logic controlling the latch is somewhat complex.

The latch is set by w1344, which requires w154 and w1376 low.

w154 is pulled low by w157 (the MREQ activate signal), or w1338 (the same interrupt signal that activates IORQ), or w1340/clock (the signal that

activates IORQ for an I/O request).

w1376 is high in M1T3h/M1T4l, blocking RD during a refresh. It is also high during a M cycle (delayed by half a clock) performing a write. This blocks RD during a write operation.

The latch is reset, deactivating the RD pin, by the same signals 176 and 156 that reset IORQ and MREQ. This explains why these signals all end at the same time.

Thus, the RD pin has similar timing to the IORQ and MREQ, except it is not active during memory refreshes and writes. (Interrupts should be investigated, to see if it is active there.)

The WR pin

The WR pin is similar in function to RD, except it indicates a write operation, either to memory or to an I/O device.

The WR pin is not active during M1 for instruction fetch or refresh.

For a memory write, the WR pin is active during T3l and h. Note that this is a much smaller time than RD is active for a read, and less time than MREQ is active. This gives the system time for the data to be output to the external data bus before WR is pulled low. In addition, the address and data remain stable for half a clock after WR returns high, due to requirements of memory chips.

For an I/O write, the WR pin timing is the same as RD timing; the pin is low the same time as the IORQ pin.

The WR pin is latched active by the combination of signals 152 and T2. This signal gets delayed by the clock, affecting the pin in T3l. Signal 152 goes high for an M cycle (typically M4 or M5) that performs a write.

For I/O, the 152/T2 signal bypasses the clock pass transistor, so it takes effect

in T2h. Since there's also a wait state for I/O between T2 and T3, the WR pin is active much longer for I/O than for memory writes: 5 half-clocks, compared to 2.

The WR pin latch is cleared by T3 or reset, delayed by the clock so the reset doesn't take effect until T4l. This is the case for both memory writes and I/O writes.

Summary

These control pins all have many similarities. Each pin has a latch feeding a superbuffer. This superbuffer is tri-state to allow the pins to be deactivated while BUSACK is in effect. Each pin has different circuitry to set and reset the latch in the appropriate M cycles and T states. The refresh operation during M1 adds a bit of complexity, as does the different behavior for memory accesses versus I/O accesses.