High-level layout of the Z80 chip

This chapter discusses the layout of the large architectural elements in the Z80 chip.

The pads that provide access to the chip are a good place to start. The Z80 has 40 pads, corresponding to its 40 pins. These pads are arranged around the outside of the chip along all four sides. Inside the chip package, tiny wires connect these pads to the metal carrier frame that goes to the external pins.

To get oriented, consider the pinout diagram of the chip showing the external pins. Pin 1 (A11) is in the upper left of the diagram. On the die, pin 1 is in the middle of the lower edge. Going counterclockwise around the diagram, you see all 40 pins in order. Going counterclockwise around the die, you encounter the pins in the same order. (This avoids any wires needing to cross going from the die to the outside pins.)

In this book, the pictures have the chip oriented with the ground pin in the middle-left and the Vcc power pin in the middle right. The orientation of the photos is somewhat arbitrary. I have selected this orientation so the copyright logo "ZILOG '75 ©" near the middle of the chip is right side up. The die is rotated 180° from this orientation in the package diagram above.

The location of the pins constrains the organization of the chip, so it is important to see how they are arranged. The ground pin in the middle-left and power pin in the middle-right are landmarks that are easy to recognize by the wide traces leaving these pins and spreading throughout the whole chip. The 16 address pins A0 to A15 start below the ground pin, wrapping around the bottom of the chip.

On the right side of the chip, the 8 data pins D0 through D7 are arranged in an seemingly-random order, which will be explained later. In the bottom-right is the clock, which drives the whole chip. On the top of the chip and on the upper-right are the 13 control pins.

Next to each output pin is a pair of large transistors to drive the pin and

provide the necessary high current. Pins used for input only have a protective diode, which ensures that a negative signal won't latch up the chip.

The Z80 chip has some distinctive functional blocks that can be easily seen in die photos.

In the lower right is the register file with a clear rectangular organization. It is organized as 16 bits with bit 0 at the top, and bit 16 at the bottom. There are 14 registers in the register file, with each one in a column.

The register file's orientation is closely tied to the address pins. The program counter is the leftmost register, and to the left of it is the incrementer, which increments the PC for each instruction. To the left of this is a latch which feeds the address pins. The address bus flows out of here, counterclockwise around the bottom of the chip. Note that bit 0 of the register file is on top, as is address pin 0, simplifying the routing of the address bus.

To the right of the registers is the 4-bit arithmetic logic unit (ALU). Each bit is visible as a horizontal band. Again, the low-order bit is on top, and the high-order bit is on the bottom.

The data bus flows in between the register file and the ALU, across the top of the ALU, and along the right next to the data pins. As will be discussed later, the data bus has a complex partitioned structure.

The next visible block is the rectangular PLA (programmable logic array) in the upper part of the chip. The PLA performs the first step of instruction decoding, matching opcodes against bit patterns to pick out families of instructions, roughly 100 in total.

To the right of the PLA is the instruction latch. When an instruction is read from memory, it passes through the data bus to the instruction latch, where it is stored for the duration of execution. This latch provides the inputs to the PLA.

Above the PLA is the timing and control logic, conveniently located near the

control pins. This logic provides the overall control of the chip, moving it from step to step, as well as handling interrupts and other external control signals.

The control signals from the timing logic flow down and around the PLA, where the meet up with the instruction decode signals from the PLA. The instruction decode logic here determines exactly what internal operations happen at each step of the execution of an instruction. In a way, this logic is the heart of the chip, deciding what happens. From here, control signals flow down to the register file, ALU, and other parts of the chip, controlling their actions.

The last major functional block is the flag logic above the ALU. As will be explained in more detail later, flags in the Z80 have a dual existence. They are stored in the register file. But to control operation and to be modified, they are moved out of the register file to latches above the ALU. From this position, they can feed into the ALU and be modified by the ALU. At the end of the operation, the flags are copied back to the register file.

This high-level overview of the Z80's organization shows that the functional blocks are arranged so related blocks are nearby, reducing the amount of interconnection wiring in the chip. The functional blocks are also arranged to be near the pins they require.

The remainder of this book will explore these functional blocks in much more detail.