The data pins

The Z80 provides an 8-bit data bus to the outside. This is a tri-state read/write bus. It can output a byte, read a byte, or sit in a high-impedance idle state. This idle state is important because it allows other devices to use the bus, for instance the DMA controller described in the chapter on peripherals.

The schematic below shows the circuit at each data pin. The most obvious feature on the die are the large paralleled transistors driving the pin. These transistors source or sink the relatively high current required for outside circuitry connected to the pin. There is one set of driver transistors connected to ground (to pull the pin low) and another set of driver transistors connected to +5 (to pull the pin high). Note that a thick metal line for ground runs just outside the data pins (along the outside of the die), while a thick metal line for +5 runs just inside the data pins. Since the pins and transistors are between these two metal lines, they can be powered conveniently.

The large driver transistors are normally right next to the associated data pin, but there are some exceptions due to layout constraints. D4's pull-up transistors are next to the clock pin. Because the D1 pin is in the corner, its transistors ended up a distance away, between the transistors for D0 and D7.

The arrangement of the individual transistors is also modified based on the space available. D2's transistors twist and turn, while D7's transistors are mostly straight. D5's transistors have a wavy pattern.

Because these driver transistors are large and have large gates (with relatively high capacitance), they are in turn driven by superbuffers, which source and sink more current than regular gates.

Each gate has the following circuit. A simple latch holds the value at each pin. This value can be written to the data pin or read from the data pin. The latch can also be written to the data bus or read from the data bus.

The data pins are controlled by four signals that run in a bus next to the data pins:

dbus_to_dlatch (A): This control signal stores the value from the data bus into the data latch.
dpins_to_dlatch (B): This control signal stores the value from the data pin into the data latch.
dlatch_to_dpins (C): This control signal writes the value from the data latch to the data pin. It is active-low. While high, there is no output to the data pins.
dlatch_to_dbus (Z): This control signal writes the value from the data latch to the data bus.

The logic to generate these signals is fairly complex, since the data pins are used in every operation for multiple purposes.

Typical timing for these control signals:
dbus_to_dlatch: This is 0 for most instructions, since they don't write to memory. For something like LD (BC), A, the control line will be high for M4T2l. PUSH BC will also have the control line high for M5T2l. The control line will be high for M3T2l for instructions like LDD.

dpins_to_dlatch: This is high for M1T2h and M1T3l for the instruction fetch. It is also high for three half-clocks when memory reads take place, e.g. M2T2h, M2T3l, M2T3h, and similarly for M3, M4.

dlatch_to_dpins: Most instructions keep this control signal high (inactive). Only instructions that write to memory use it. For instance, LD (BC), A pulls it low for 5 half-clocks: M4T2l, M4T2h, M4T3l, M4T3h, M1T1l. It is typically low for almost the entire M cycle, starting from MxT2l through T1l of the next M cycle. Note that this first goes low the same cycle that dbus_to_dlatch is active, so the value is written directly from the dbus to the pins, and then latched for the remainder of the M cycle.

dlatch_to_dbus: This control signal is high (active) most of the time, writing the latched value to the internal data bus. It drops low for M1T2h, M1T3l while the instruction fetch takes place. It also drops low for almost a whole M cycle while writing to memory from M4T1h through the next M1T3l. For a read, it will drop low two cycles, e.g. M4T2h and M4T3l.

The logic that generates these signals is fairly complex, combining many different factors.