AVR32768: 32-Bit AVR UC3 C Series Schematic Checklist

Features

- **Power circuit**
- **Reset circuit**
- **Clocks and crystal oscillators**
- **Analog-to-digital Converter**
- **Digital-to-analog Converter**
- **USB connection**
- **Ethernet MAC interface**
- **External bus interface**
- **Quadrature decoder**
- **CAN interface**
- **USB DFU ISP Entry Point**
- **JTAG and Nexus debug ports**

1 Introduction

A good hardware design comes from a proper schematic. Because Atmel® AVR® UC3 C devices have a fair number of pins and functions, the schematic for these devices can be large and quite complex.

This application note describes a common checklist which should be used when starting and reviewing the schematics for an UC3 C design.

32-bit Atmel Microcontrollers

Application Note

Rev. 32157B-AVR-07/11

2 Abbreviations

DAC	Digital-to-analog converter
DFU	Direct Firmware Upgrade
ISP	In-System Programming
MII	Media Independent Interface
QDEC	Quadrature decoder
RMII	Reduced Media Independent Interface
S/H	Sample and Hold
WOL	Wake-on-LAN

3 References

3.1 Device datasheet

The device datasheet contains block diagrams of the peripherals and details about implementing firmware for the device. The datasheet is available on http://www.atmel.com/AVR in the *Datasheets* section.

3.2 The AVR Software Framework

http://asf.atmel.no/readme.html

All pre-loaded firmware source codes are available in the Atmel AVR Software Framework version 2.0 or higher.

3.3 The AT32UC3C-EK Getting Started

http://www.atmel.com/uc3c-ek

3.4 USB DFU boot loader

http://www.atmel.com/AVR

4 Power circuit

The UC3 C can be used in two different power supply modes.

- 3.3V single power supply mode
- 5V single power supply mode

Two internal voltage regulators, a 3.3V regulator and a 1.8V regulator, supply power to the USB pads and VDDCORE respectively.

4.1 Single 3.3V power supply

Figure 4-1. Single 3.3V power supply example schematic.

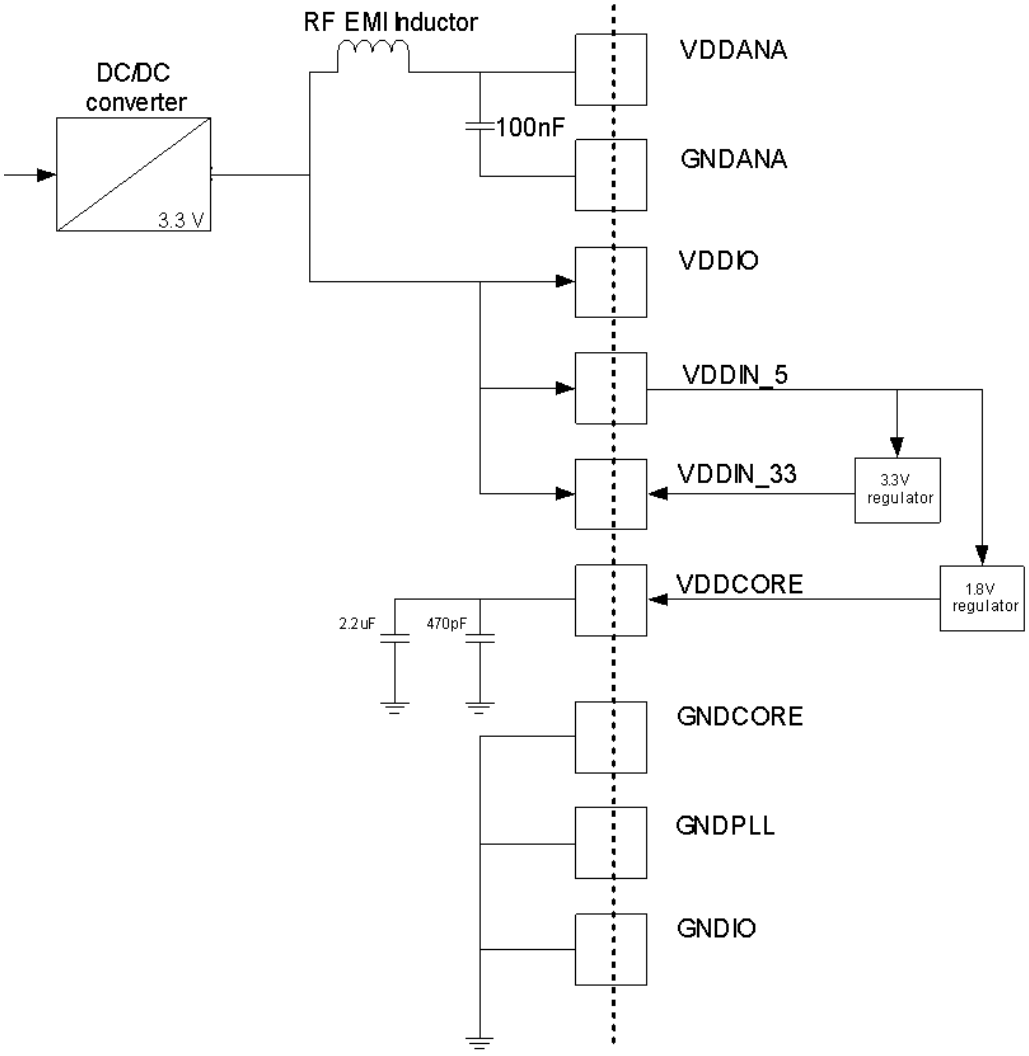

Table 4-1. Single 3.3V power supply checklist.

☑	Signal name	Recommended pin connection	Description
	VDDANA	3.0V to 3.6V RF EMI inductor Decoupling/filtering capacitor, 100nF (1) to GNDANA	Analog power supply
	GNDANA	Connect to analog ground	Analog ground
	VDDIO	3.0V to 3.6V	Powers I/O lines and the flash memory
	VDDIN_5	3.0V to 3.6V	Input voltage for the 1.8V regulator
	VDDIN_33	3.0V to 3.6V	USB I/O power supply
	VDDCORE	Decoupling/filtering capacitors, 2.2µF (1)(2) and 470pF (1)(2)	Stabilization output for the 1.8V regulator Decoupling/filtering capacitors must be added to ensure regulator stability
	GNDCORE	Connect to digital ground	
	GNDPLL	Connect to digital ground	
	GNDIO	Connect to digital ground	

Notes: 1. These values are given only as a typical example
2. Decoupling capacitor should be placed as close as possible to the pin

4.2 Single 5V power supply

Figure 4-2. Single 5V power supply example schematic.

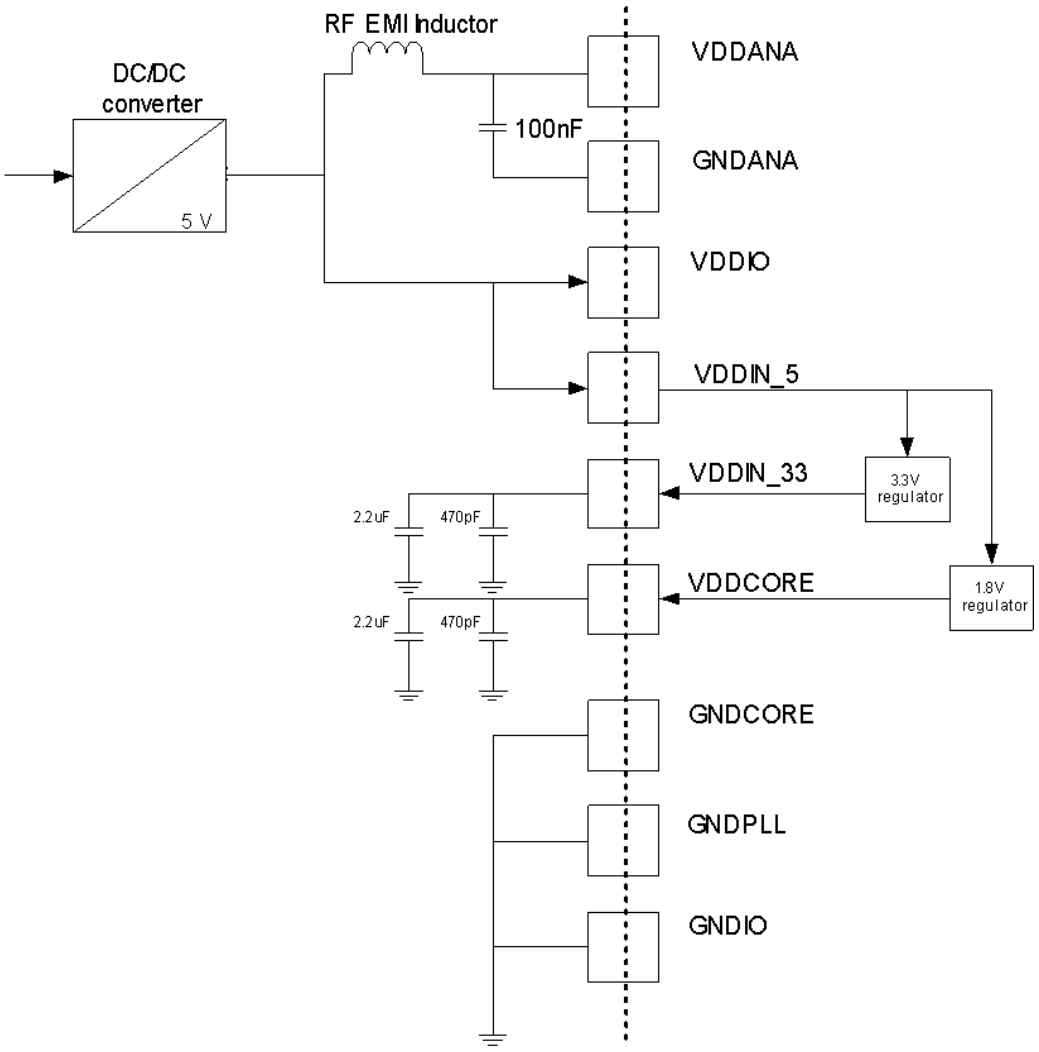

Table 4-2. Single 5V power supply checklist (UC3 C).

☑	Signal name	Recommended pin connection	Description
	VDDANA	4.5V to 5.5V RF EMI inductor Decoupling/filtering capacitor, 100nF (1) to GNDANA	Analog power supply
	GNDANA	Connect to analog ground	Analog ground
	VDDIO	4.5V to 5.5V	Powers I/O lines and the flash memory
	VDDIN_5	4.5V to 5.5V	Input voltage for the 1.8V regulator
	VDDIN_33	Decoupling/filtering capacitors, 2.2µF (1)(2) and 470pF (1)(2)	USB I/O power supply Decoupling/filtering capacitors must be added to ensure regulator stability
	VDDCORE	Decoupling/filtering capacitors, 2.2µF (1)(2) and 470pF (1)(2)	Stabilization output for the 1.8V regulator Decoupling/filtering capacitors must be added to ensure regulator stability
	GNDCORE	Connect to digital ground	
	GNDPLL	Connect to digital ground	
	GNDIO	Connect to digital ground	

Notes:
1. These values are given only as a typical example
2. Decoupling capacitor should be placed as close as possible to the pin

5 Reset circuit

The reset pin is also used for aWire (see section 14.3 for details).

Figure 5-1. Reset circuit example schematic.

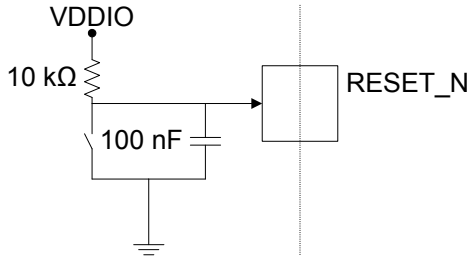

Table 5-1. Reset circuit checklist.

☑	Signal name	Recommended pin connection	Description
	RESET_N	Can be left unconnected in case no reset from the system needs to be applied to the product	The RESET_N pin is a Schmitt input and integrates a permanent pull-up resistor to VDDIO

6 Clocks and crystal oscillators

There are three clock inputs available:

- XIN0 / XOUT0
- XIN1 / XOUT1
- XIN32 / XOUT32

The recommendations below refer to XIN / XOUT, but apply to all the clock inputs.

6.1 External clock source

Figure 6-1. External clock source schematic.

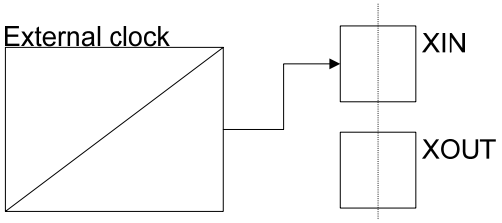

Table 6-1. External clock source checklist.

☑	Signal name	Recommended pin connection	Description
	XIN	Connected to clock output from external clock source	Up to VDDIO-volt square wave signal up to 50MHz
	XOUT	Can be left unconnected or used as GPIO	

6.2 Crystal oscillator

Figure 6-2. Crystal oscillator example schematic.

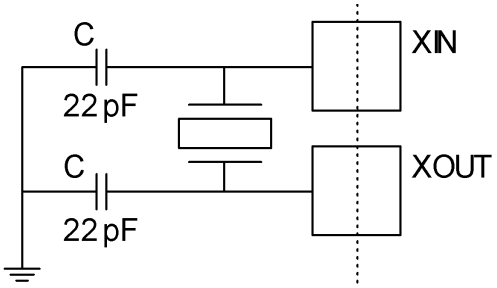

Table 6-2. Crystal oscillator checklist.

☑	Signal name	Recommended pin connection	Description
	XIN	Biasing capacitor, 22pF (1)(2)	External crystal between 450kHz and 16MHz
	XOUT	Biasing capacitor, 22pF (1)(2)	

Notes:
1. These values are given only as a typical example. The capacitance, C, of the biasing capacitors can be computed based on the crystal load capacitance, C_L, and the internal capacitance, C_i, of the MCU as follows:

   $C = 2(C_L - C_i)$

   The value of C_L can be found in the crystal datasheet and the value of C_i can be found in the MCU datasheet
2. Decoupling capacitor should be placed as close as possible to each pin in the signal group, and vias should be avoided

7 ADC Analog-to-digital converter

The UC3 C analog-to-digital converter (ADC) has a fully differential 8/10/12-bit ADC core with built-in sample and hold. It has multiple reference sources, and 1.5 mega-samples per second conversion rate for 12 bit resolution. The ADC connections require some electrical considerations, which are outlined in this section.

7.1 ADC analog Input

The ADC has 16 channels of analog input, ADCINx, which are GPIO multiplexed.

To get the best resolution, it is recommended not to use digital features of GPIO pins close to the analog inputs used.

The analog input channels require a low enough external source impedance, which depends on whether or not sample-and-hold is used (see Table 7-1).

For differential input, ADCIN[0:7] are used for positive input and ADCIN[8:15] are used for negative input. In single-ended mode, all 16 channels can be used as single-ended input. Please refer to the UC3 C datasheet for details.

Table 7-1. ADC analog inputs.

☑	Signal name	Recommended pin connection	Description
	ADCINx	Maximum input voltage: V_{VDDANA} Maximum external source impedance, • without S/H: 3kΩ • with S/H: 1kΩ	Analog input

7.2 ADC voltage reference

The internal analog-to-digital converter in the UC3 C can use different voltage references. Depending on the voltage references needed, the external voltage reference pins should be connected as advised below.

7.2.1 ADC single-ended external reference (ADCREF0/ADCREF1)

Two external, single-ended voltage references are available. The maximum voltage values depend on the power supply mode used. Refer to Table 7-2 and Table 7-3, and Figure 7-1 and Figure 7-2.

If the single-ended external voltage references are not used, the pins can be left unconnected and tied to internal pull-up through GPIO.

Figure 7-1. Single-ended external reference, 3.3V power supply mode.

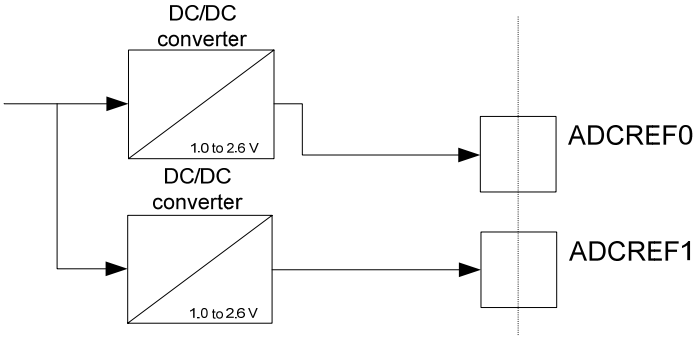

Table 7-2. ADC single-ended external voltage reference, 3.3V power supply mode.

☑	Signal name	Recommended pin connection	Description
	ADCREF0	1.0V to 2.6V	Single-ended external voltage reference
	ADCREF1	1.0V to 2.6V	Single-ended external voltage reference

Figure 7-2. Single-ended external reference, 5V power supply mode.

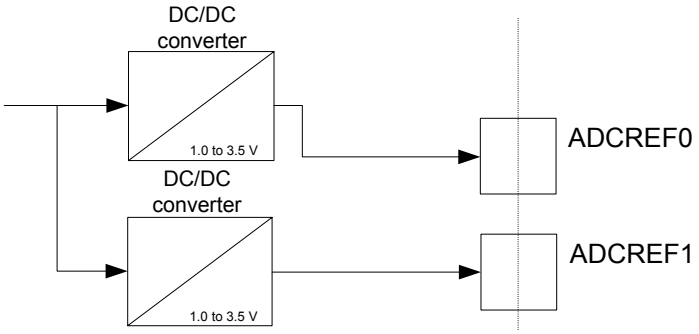

Table 7-3. ADC single-ended external voltage reference, 5V power supply mode.

☑	Signal name	Recommended pin connection	Description
	ADCREF0	1.0V to 3.5V	Single-ended external voltage reference
	ADCREF1	1.0V to 3.5V	Single-ended external voltage reference

7.2.2 ADC differential external reference pins (ADCVREFP/ADCVREFN)

In order to use the internal 1V bandgap reference, the ADCVREFP and ADCVREFN pins must be used with decoupling capacitors (see Figure 7-3 and Table 7-5 for typical values).

If the internal voltage reference is unused, ADCVREFP and ADCVREFN can be used as differential external voltage reference (see Figure 7-4 and Table 7-5).

Figure 7-3. ADCVREFP/ADCVREFN external decoupling for use of internal bandgap reference.

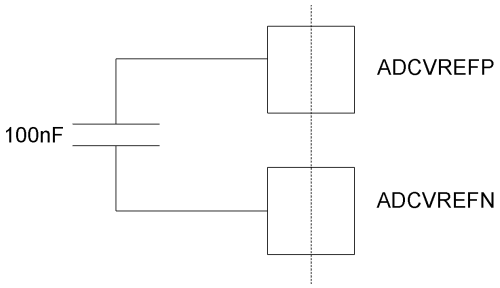

Table 7-4. ADC differential external voltage reference, internal reference used.

☑	Signal name	Recommended pin connection	Description
	ADCVREFP	Positive differential voltage	Differential external voltage reference
	ADCVREFN	Negative differential voltage	Differential external voltage reference

Figure 7-4. Differential external voltage reference.

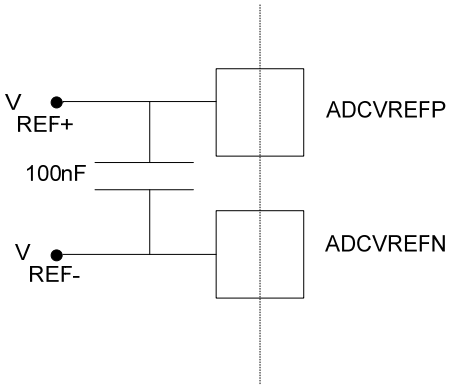

Table 7-5. ADC differential voltage inputs, internal reference not used.

☑	Signal name	Recommended pin connection	Description
	ADCVREFP	100nF decoupling capacitor	Used as decoupling for internal reference voltage
	ADCVREFN	100nF decoupling capacitor	Used as decoupling for internal reference voltage

8 Digital-to-analog converter

The digital-to-analog converter (DAC) can use either an internal or external voltage reference. When using an internal voltage reference, DACREF can be GPIO multiplexed to another function or connected to an internal pull-up.

8.1 DAC connection

Figure 8-1. DAC connection considerations.

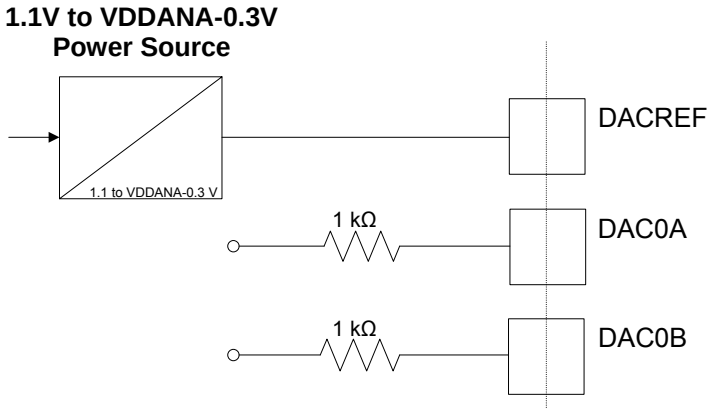

Table 8-1. Digital-to-analog converter checklist.

☑	Signal name	Recommended pin connection	Description
	DACREF	Reference voltage range: 1.1V – (VDDANA-0.3V)	External voltage reference
	DAC0A	Minimum load impedance: 1kΩ Maximum load capacitance: 100pF	Channel A analog output
	DAC0B	Minimum load impedance: 1kΩ Maximum load capacitance: 100pF	Channel B analog output

9 USB connection

9.1 Not used

When the USB interface is not used, DM, DP and VBUS should be connected to ground.

9.2 Device mode, bus-powered connection

Figure 9-1. USB in device mode, bus-powered connection example schematic.

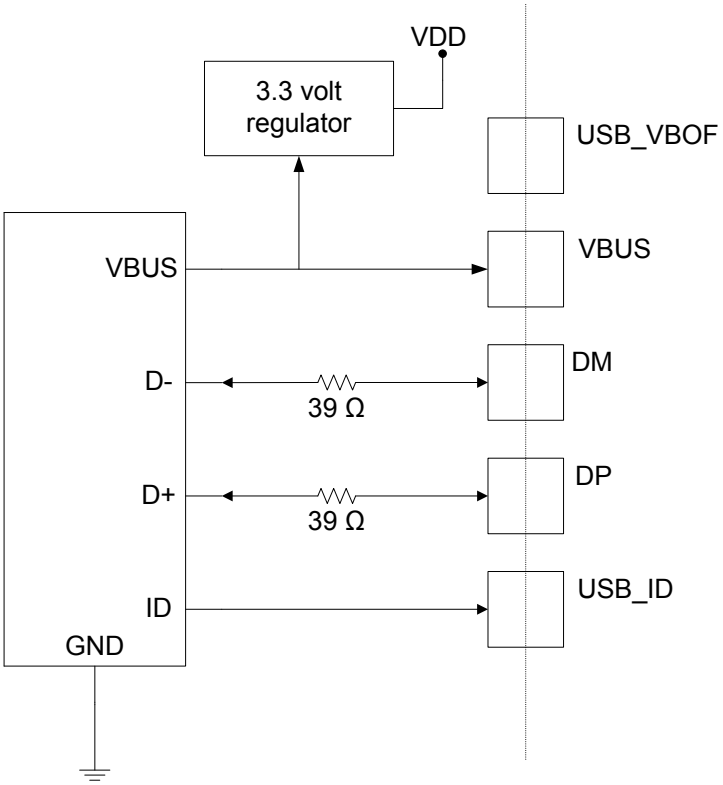

Table 9-1. USB bus-powered connection checklist.

☑	Signal name	Recommended pin connection	Description
	USB_VBOF	Can be left unconnected	USB power control pin
	VBUS	Directly to connector	USB power pin
	DM	39Ω series resistor Placed as close as possible to DM pin	Negative differential data line
	DP	39Ω series resistor Placed as close as possible to DP pin	Positive differential data line
	USB_ID	Can be used as GPIO if not used	USB connector identification pin

9.3 Device mode, self-powered connection

Figure 9-2. USB in device mode, self-powered connection example schematic.

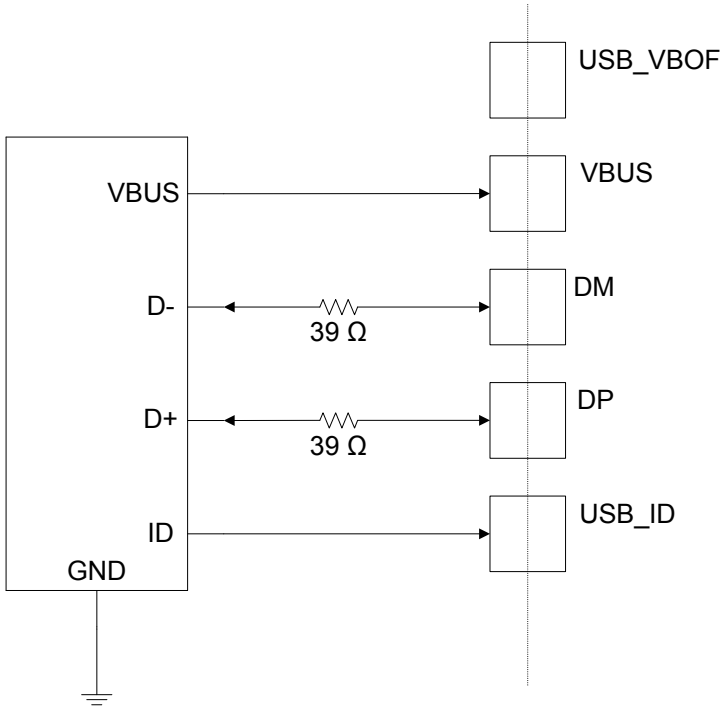

Table 9-2. USB self-powered connection checklist.

☑	Signal name	Recommended pin connection	Description
	USB_VBOF	Can be left unconnected	USB power control pin
	VBUS	Directly to connector	USB power pin
	DM	39Ω series resistor Placed as close as possible to DM pin	Negative differential data line
	DP	39Ω series resistor Placed as close as possible to DP pin	Positive differential data line
	USB_ID	Can be used as GPIO if not used	USB connector identification pin

9.4 Host mode, powered from bus connection

Figure 9-3. USB host-powering connection example schematic.

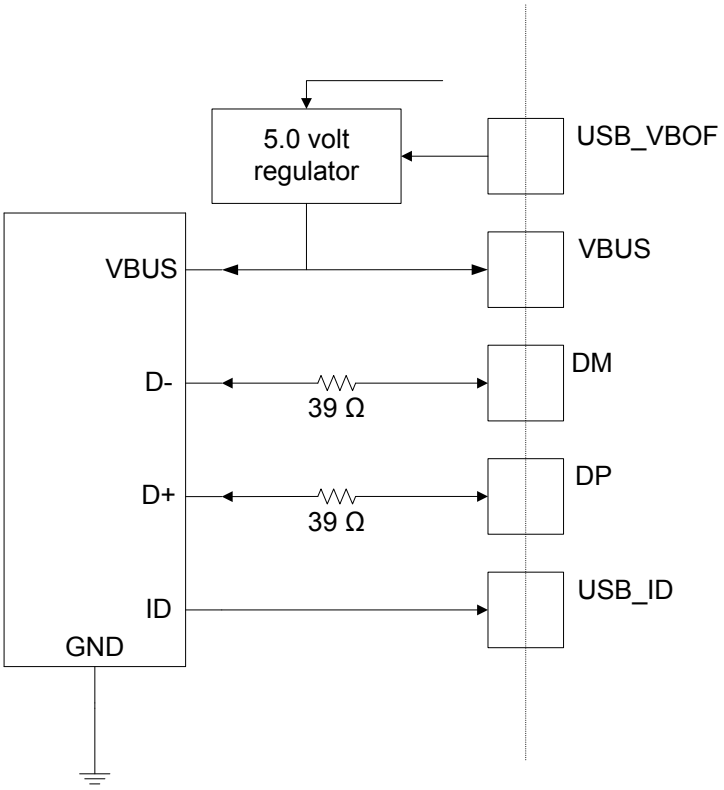

Table 9-3. USB host-powering connection checklist.

☑	Signal name	Recommended pin connection	Description
	USB_VBOF	GPIO connected to VBUS 5.0V regulator enable signal	USB power control pin
	VBUS	Directly to connector	USB power pin
	DM	39Ω series resistor Placed as close as possible to DM pin	Negative differential data line
	DP	39Ω series resistor Placed as close as possible to DP pin	Positive differential data line
	USB_ID	GPIO directly connected to connector	USB identification pin. Pull-up on GPIO pin must be enabled

9.5 USB DFU ISP entry point

The ISP is activated according to the boot process conditions described in the boot loader document (see section 3.4). By default, the hardware condition is to maintain pin PA14 of UC3 C at logical 0 while releasing the reset. Once the ISP is activated, it establishes a USB connection with the connected PC. This I/O should not be used by the application if the USB DFU boot loader is required to program the application.

10 Ethernet interface

When designing in the Ethernet physical device (PHY), the designer should refer to the datasheet for the PHY. This datasheet usually contains layout advice, connection schematics, reference design, etc.

The information in the PHY datasheet is mandatory to get optimal performance and stability.

10.1 Ethernet interface in MII mode

Figure 10-1. Ethernet interface in MII mode example schematic.

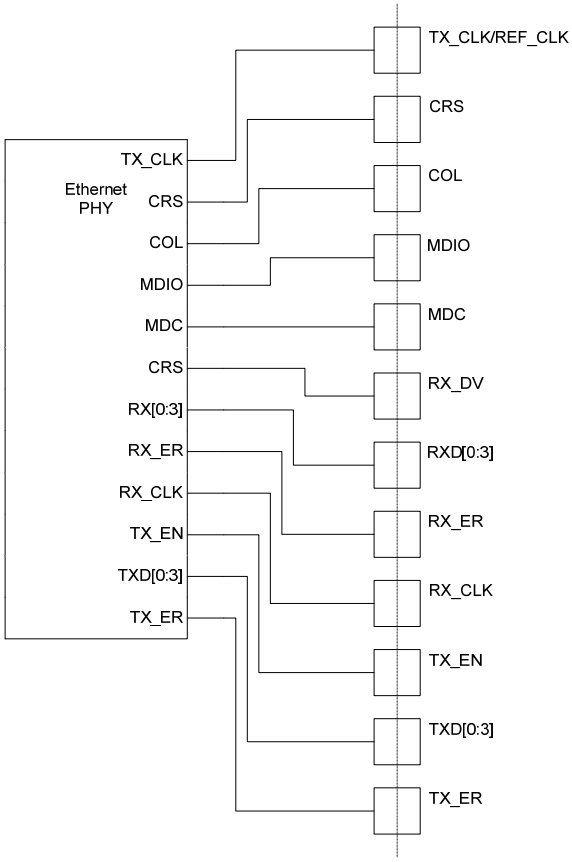

Table 10-1. Ethernet interface in MII mode checklist.

☑	Signal name	Recommended pin connection	Description
	TX_CLK/ REF_CLK		Transmit clock, 25MHz for 100Mb/s data rate
	CRS		Carrier sense
	COL		Collision detect
	MDIO		PHY maintenance data
	MDC		PHY maintenance clock
	RX_DV		Receive data valid
	RXD[0:3]		Receive data 4-bit

☑	Signal name	Recommended pin connection	Description
	RX_ER		Receive error
	RX_CLK		Receive clock, 25MHz for 100Mb/s data rate
	TX_EN		Transmit enable
	TXD[0:3]		Transmit data 4-bit
	TX_ER		Transmit error

10.2 Ethernet interface in RMII mode

Figure 10-2. Ethernet interface in RMII mode example schematic.

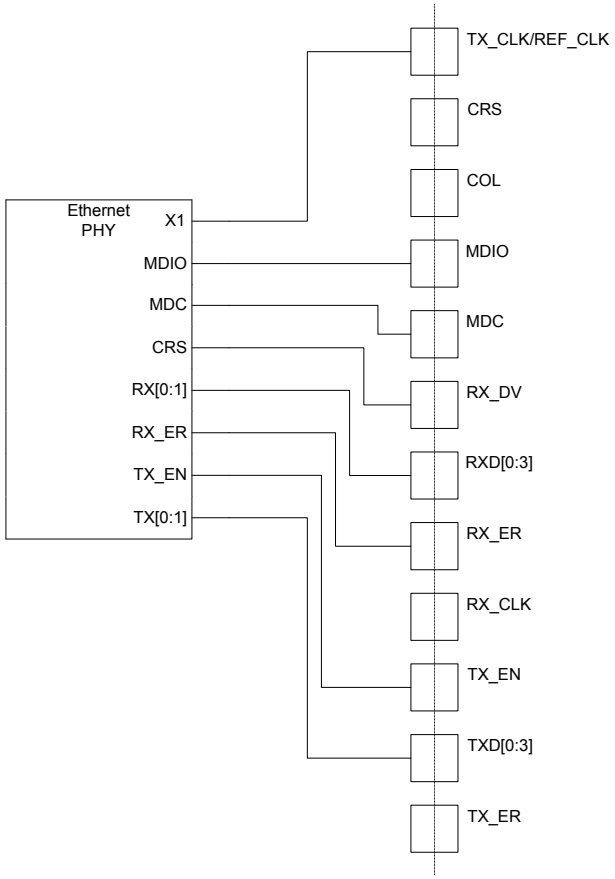

Table 10-2. Ethernet interface in RMII mode checklist.

☑	Signal name	Recommended pin connection	Description
	TX_CLK/ REF_CLK		Reference clock, 50MHz for 100Mb/s data rate
	CRS	Not used in RMII mode	
	COL	Not used in RMII mode	
	MDIO		PHY maintenance data
	MDC		PHY maintenance clock
	RX_DV		Carrier sense, data valid

☑	Signal name	Recommended pin connection	Description
	RXD[0:1]		Receive data 2-bit
	RXD[2:3]	Not used in RMII mode	
	RX_ER		Receive error
	RX_CLK	Not used in RMII mode	
	TX_EN		Transmit enable
	TXD[0:1]		Transmit data 2-bit
	TXD[2:3]	Not used in RMII mode	
	TX_ER	Not used in RMII mode	

10.3 Ethernet Wake-on-LAN

The MACB controller supports Ethernet Wake-on-LAN (WOL), which can be used to wake the UC3 C core on network activity. Figure 10-3 shows an example of how the WOL output signal can be routed to an external interrupt input.

Figure 10-3. MACB WOL to external interrupt example schematic.

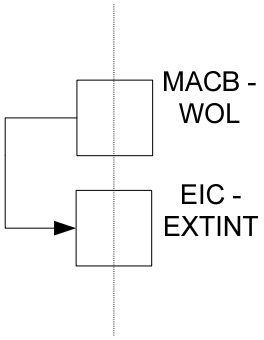

Table 10-3. MACB WOL connection checklist.

☑	Signal name	Recommended pin connection	Description
	MACB – WOL		MACB Wake-on-LAN output
	EIC - EXTINT		EIC external interrupt input

11 External bus interface

11.1 Static memory

11.1.1 16-bit static memory

Table 11-1. 16-bit static memory pin wiring.

☑	GPIO line name	16-bit static memory
	EBI-DATA[0:15]	D[0:15]
	EBI-ADDR[1:23]	A[0:22]
	EBI-ADDR[0] (NBS0)	LBE
	EBI-NWE1 (NBS1)	HBE
	EBI-NWE0	WE
	EBI-NRD	OE
	EBI-NWAIT	WAIT
	EBI-NCSx	CS

11.1.2 8-bit static memory

Table 11-2. 8-bit static memory pin wiring.

☑	GPIO line name	8-bit static memory
	EBI-D[0:7]	D[0:7]
	EBI-A[0:23]	A[0:23]
	EBI-NWE0	WE
	EBI-NRD	OE
	EBI-NWAIT	WAIT
	EBI-NCSx	CS

11.1.3 2 x 8-bit static memory

Table 11-3. 2 x 8-bit static memory pin wiring.

☑	GPIO line name	8-bit static memory	8-bit static memory
	EBI-D[0:7]	D[0:7]	
	EBI-D[8:15]		D[0:7]
	EBI-A[1:23]	A[0:22]	A[0:22]
	EBI-NWE0 (NBS0)	WE	
	EBI-NWE1 (NBS1)		WE
	EBI-NRD	OE	OE
	EBI-NWAIT	WAIT	WAIT
	EBI-NCSx	CS	CS

11.2 SDRAM

11.2.1 16-bit SDRAM

Table 11-4. 16-bit SDRAM pin wiring.

☑	GPIO line name	16-bit SDRAM
	EBI-D[0:15]	DQ[0:15]
	EBI-A[2:11]	A[0:9]
	EBI-SDA10	A[10]
	EBI-A[13:14]	A[11:12]
	EBI-A[16] (BA0)	BA0
	EBI-A[17] (BA1)	BA1
	EBI-SDCK	CLK
	EBI-SDCKE	CKE
	EBI-SDWE	WE
	EBI-RAS	RAS
	EBI-CAS	CAS
	EBI-A[0] (NBS0)	DQML
	EBI-NWE1 (NBS1)	DQMH
	EBI-NCS[1] (SDCS)	CS

11.2.2 2 x 8-bit SDRAM

Table 11-5. 2 x 8-bit SDRAM pin wiring.

☑	GPIO line name	8-bit SDRAM	8-bit SDRAM
	EBI-D[0:7]	DQ[0:7]	
	EBI-D[7:15]		DQ[0:7]
	EBI-A[2:11]	A[0:9]	A[0:9]
	EBI-SDA10	A[10]	A[10]
	EBI-A[13:14]	A[11:12]	A[11:12]
	EBI-A[16] (BA0)	BA0	BA0
	EBI-A[17] (BA1)	BA1	BA1
	EBI-SDCK	CLK	CLK
	EBI-SDCKE	CKE	CKE
	EBI-SDWE	WE	WE
	EBI-RAS	RAS	RAS
	EBI-CAS	CAS	CAS
	EBI-A[0] (NBS0)	DQM	
	EBI-NWE1 (NBS1)		DQM
	EBI-NCS[1] (SDCS)	CS	CS

11.2.3 4 x 4-bit SDRAM

Table 11-6. 4 x 4-bit SDRAM pin wiring.

☑	GPIO line name	4-bit SDRAM	4-bit SDRAM	4-bit SDRAM	4-bit SDRAM
	EBI-D[0:3]	DQ[0:3]			
	EBI-D[4:7]		DQ[0:3]		
	EBI-D[8:11]			DQ[0:3]	
	EBI-D[12:15]				DQ[0:3]
	EBI-A[2:11]	A[0:9]	A[0:9]	A[0:9]	A[0:9]
	EBI-SDA10	A[10]	A[10]	A[10]	A[10]
	EBI-A[13:14]	A[11:12]	A[11:12]	A[11:12]	A[11:12]
	EBI-A[16] (BA0)	BA0	BA0	BA0	BA0
	EBI-A[17] (BA1)	BA1	BA1	BA1	BA1
	EBI-SDCK	CLK	CLK	CLK	CLK
	EBI-SDCKE	CKE	CKE	CKE	CKE
	EBI-SDWE	WE	WE	WE	WE
	EBI-RAS	RAS	RAS	RAS	RAS
	EBI-CAS	CAS	CAS	CAS	CAS
	A[0] (NBS0)	DQM	DQM		
	EBI-NWE1 (NBS1)			DQM	DQM
	EBI-NCS[1] (SDCS)	CS	CS	CS	CS

12 Quadrature decoder

Depending on the quadrature encoder used, pull-up resistors may or may not be needed. Figure 12-1 shows an example of how the quadrature decoder (QDEC) can be connected to a quadrature encoder using pull-up on the signal wires.

Figure 12-1. Quadrature decoder example schematic.

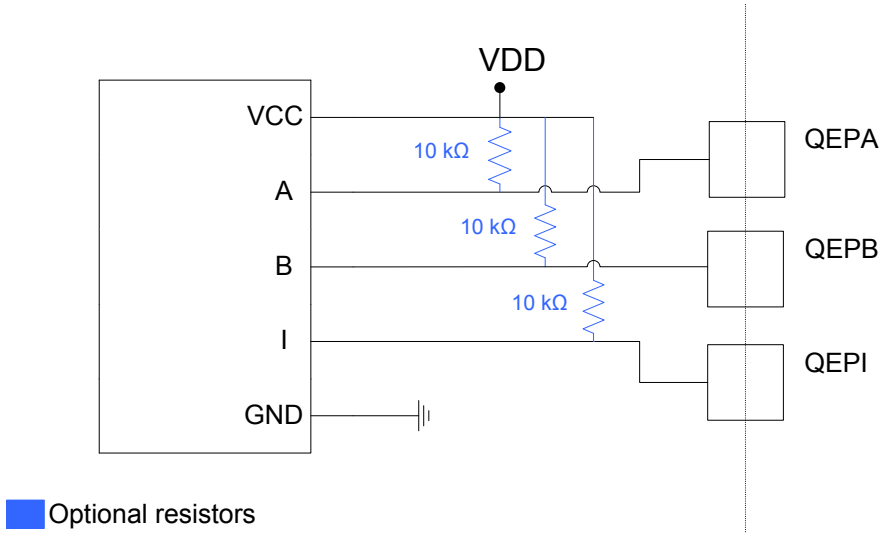

Table 12-1. Quadrature decoder connection checklist.

☑	Signal name	Recommended pin connection	Description
	QEPA	Quadrature encoder output A, 10kΩ (1) pull-up	Quadrature phase signal A digital input
	QEPB	Quadrature encoder output B, 10kΩ (1) pull-up	Quadrature phase signal B digital input
	QEPI	Quadrature encoder index output, 10kΩ (1) pull-up	Quadrature index signal digital input

Note: 1. These values are given only as a typical example

13 CAN interface

The UC3 C embeds a CAN controller, which generates and handles digital transmission and reception signals TXD and RXD. These signals can be used to interface a CAN line driver, which generates the physical differential signals on the CAN bus. Figure 13-1 shows an example schematic using the Atmel AT6660 high-speed CAN transceiver.

Usage of the CAN interface is detailed in the application note, *AVR32129: Using the 32-bit AVR UC3 CANIF*.

Figure 13-1. CAN interface to AT6660 example schematic.

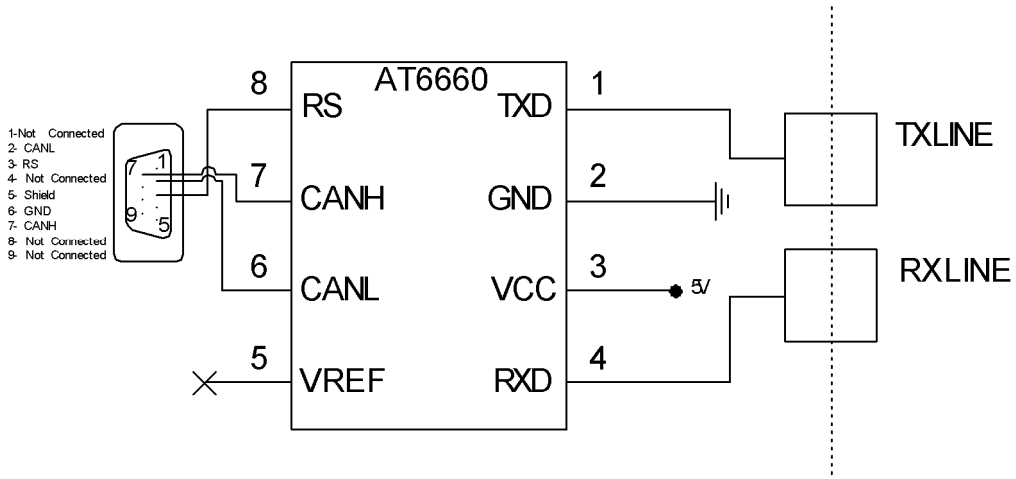

Table 13-1. CAN interface connection checklist.

☑	Signal name	Recommended pin connection	Description
	TXLINE	Directly to connector pin	Transmission line (output)
	RXLINE	Directly to connector pin	Reception line (input)

14 JTAG and Nexus debug ports

14.1 JTAG port interface

Figure 14-1. JTAG port interface example schematic.

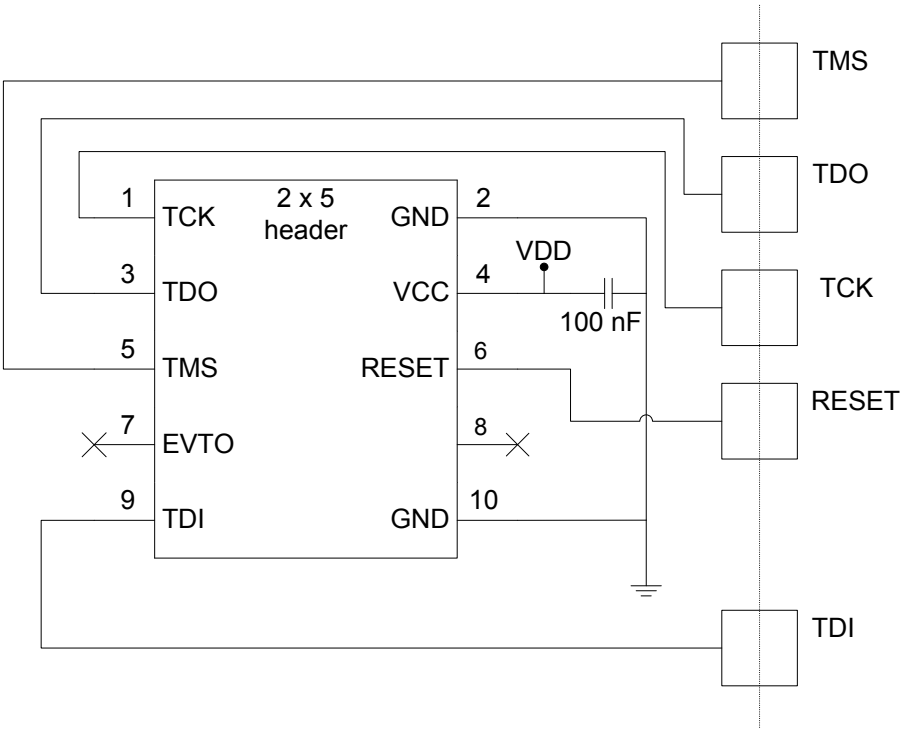

Table 14-1. JTAG port interface checklist.

☑	Signal name	Recommended pin connection	Description
	TMS		Test mode select, sampled on rising TCK
	TDO		Test data output, driven on falling TCK
	TCK		Test clock, fully asynchronous to system clock frequency
	RESET		Device external reset line
	TDI		Test data input, sampled on rising TCK
	EVTO		Event output, not used

14.2 Nexus port interface

Do not use any capacitors on NEXUS lines because they can cause a speed limitation. NEXUS uses GPIO multiplexed lines, and these should be dedicated for NEXUS when used.

Figure 14-2. Nexus port interface example schematic.

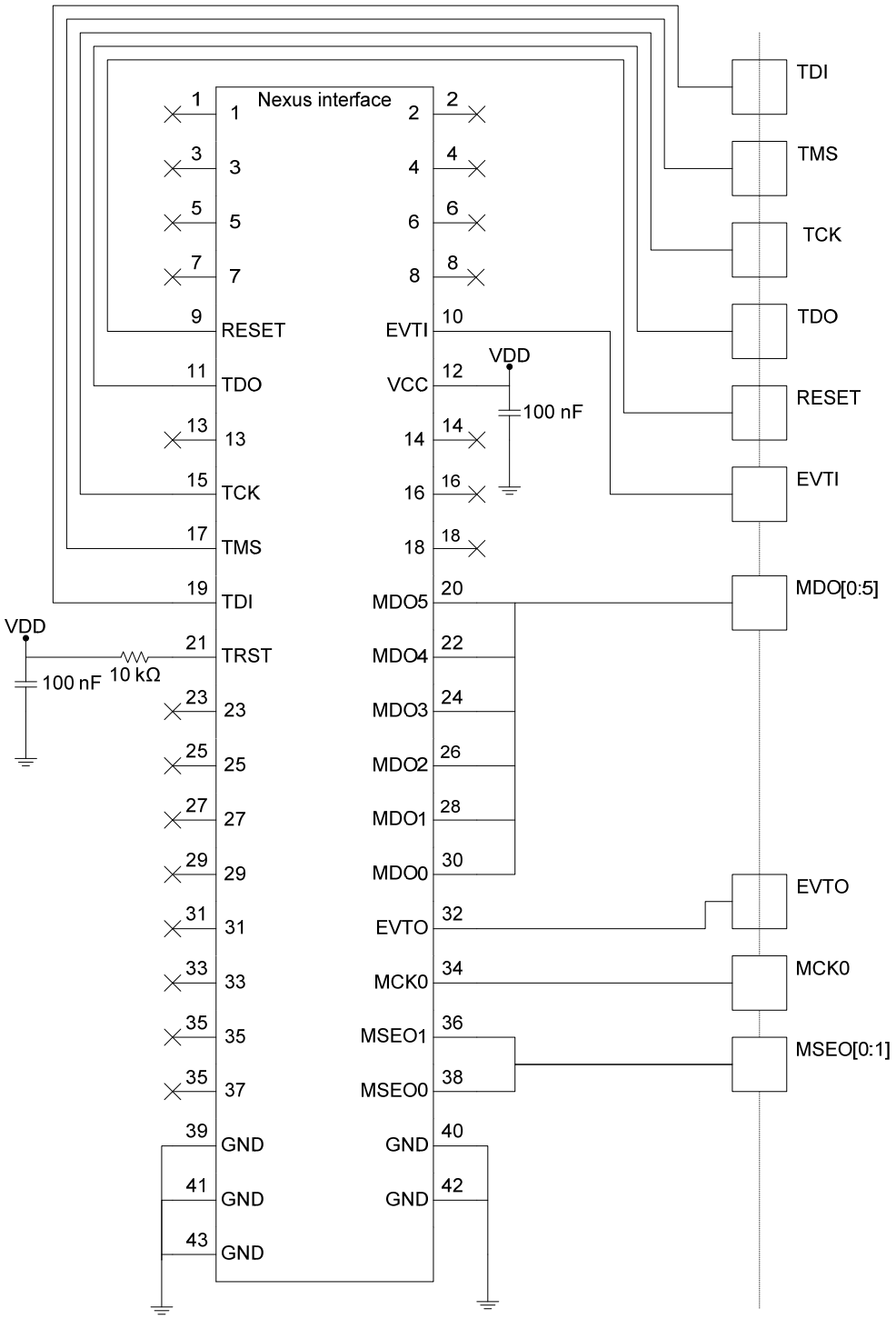

Table 14-2. Nexus port interface checklist.

☑	Signal name	Recommended pin connection	Description
	TDI		Test data input, sampled on rising TCK
	TMS		Test mode select, sampled on rising TCK
	TCK		Test clock, fully asynchronous to system clock frequency
	TDO		Test data output, driven on falling TCK
	RESET		Device external reset line
	EVTI		Event input
	MDO[0:5]		Trace data output
	EVTO		Event output
	MCK0		Trace data output clock
	MSE[0:1]		Trace frame control

14.3 aWire port interface

aWire is a single-wire debug solution that offers memory access, programming capabilities, and On-Chip Debug access. aWire can also be used as a UART when it is not used for debugging.

A full-duplex mode can be used to increase speed, in which case data is transmitted on a second pin, DATAOUT.

aWire uses the RESET_N pin for data in/data out. When using aWire, the board reset circuitry must be disconnected. Refer to Figure 14-3 which demonstrates the use of RESET_N for half-duplex mode, and Figure 14-4, where DATAOUT is added for full-duplex communication.

Figure 14-3. Disconnecting the reset circuitry to allow aWire use.

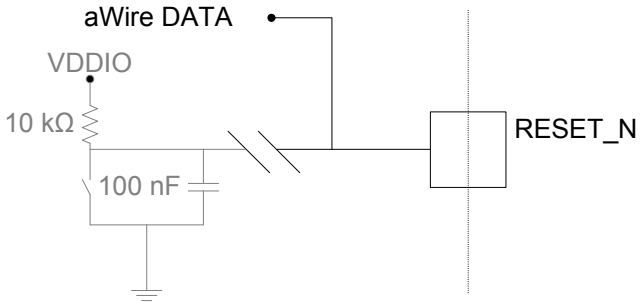

Figure 14-4. aWire with full-duplex communication.

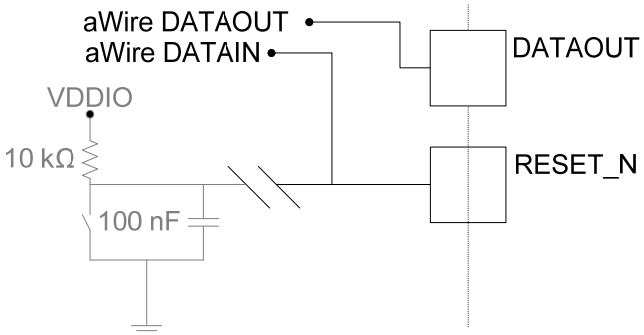

Table 14-3. aWire port interface checklist.

☑	Signal name	Recommended pin connection	Description
	RESET_N	aWire in/out (half-duplex) aWire in (full-duplex) Disconnect from reset circuitry	Input/output
	DATAOUT	aWire out (full-duplex mode only)	Output

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