Yue Fei (she / her)

Communication Systems & Digital Design & Computer Architecture

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Education

University of Toronto *Sep. 2022 – Jun. 2024*

Master of Engineering, Electrical & Computer Engineering

- **MEng Thesis: Pilot Training – Angle of Arrival and Channel Estimation in 5G Networks** [Code]
- Evaluated **LMMSE** vs. **Matrix-Pencil** methods for uplink channel estimation in **multicell MIMO-OFDM** (3GPP-compliant), showing **higher AoA accuracy** under limited-antenna regimes.
- Supervisor: Prof. Raviraj Adve

University of Toronto *Sep. 2017 – Jun. 2022*

Bachelor of Applied Science, Electrical Engineering

- **Capstone Project: CNN NPU Overlay & Compiler for Intel Stratix 10 NX**
- Collaborated to develop a custom Convolution Unit and DLS Compiler to optimize MobileNetV1 inference on Stratix 10 NX, achieving a **4.3× speedup** over baseline Microsoft Brainwave architectures.
- Supervisors: Prof. Vaughn Betz, Andrew Boutros

Publications | Peer-reviewed conferences

1. Arash Ahmadian, Louis S.P. Liu, **Yue Fei**, Konstantinos N. Plataniotis, Mahdi S. Hosseini. *Pseudo-Inverted Bottleneck Convolution for DARTS Search Space*. IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), 2023.
2. Abnash Bassi, **Yue Fei**, Gilead Posluns, Mark C. Jeffrey. *Optimized Priority Scheduling for Faster Scalable Belief Propagation*. Probabilistic Graphical Models (PGM), *[In Submission]*, 2026.

Experience

MediumAI · Software Development Engineer — Hybrid, Toronto, Canada · Freelance *Jan. 2026 – Present*

- Build API integrations for a voice LLM–powered medical scribe agent, enabling secure multilingual clinical documentation.

iQIYI.com · Data Analyst — Remote, Beijing, China · Internship *Oct. 2025 – Dec. 2025*

- Combined three-arm A/B testing with causal forests and decision-tree rules for deployable personalization, lifting renewal rates from **37%** to **54.06%.**

Qualcomm Canada · RFIC Design Verification Engineer — Onsite, Markham, Canada · Permanent Full-time *Jun. 2024 – Jul. 2025*

- Verified UWB receiver path(analog front end); Verified WLAN CP-PLL synthesizer across 500+ channels using UVM, ensuring coverage over 2G/5G bands; Developed GRU-based multi-head model for analog gain line-up optimization and an MLP for VCO capacitance prediction, replacing manual tuning across 1000+ frequency targets.

University of Toronto – WIRLab · Research Assistant — Remote, Toronto, Canada · Contract Part-time *Jul. 2021 – Sep. 2021*

- Applied **PCA-based embedding visualization** to investigate semantic clusters for **Transformer-based NLP tasks.**[Code]

Alphawave Semi · SerDes Digital Verification Engineer — Remote, Toronto, Canada · Internship *May 2020 – Jun. 2021*

- Built UVM testbenches for SerDes subsystems (clocking, datapath, SRAM), expanding coverage to 50+ scenarios; Scaled Jenkins CI/CD regression from 4 to 60+ projects, enabling **15**× throughput growth.

Selected Academic Projects

Capstone Project - NPU CNN Overlay on FPGA *Sep. 2021 – Apr. 2022*

- **NPU HLS Compiler Infrastructure** Architected a **VLIW-based Python compiler** that packs 130-bit instruction chains for parallel Loader, CONVU, and MFU execution. Implemented **tag-based dependency tracking** and **explicit NOP insertion** within the ISA to resolve RAW hazards in software.
- **RTL Logistics** Engineered a hierarchical RTL scheduler in SystemVerilog using **credit-based flow control** and pipelined reduction trees, achieving a verified **450 MHz Fmax** on Intel Stratix 10 NX.

ECE1755 Course work - Parallel Graph-Inference Scheduler *Jan. 2024 – Apr. 2024*

- **Concurrency & Scheduling:** Architected a multi-threaded asynchronous scheduler for **Ising, Potts, and LDPC** models using a Stealing Multi-Queue (SMQ) with lazy priority updates to resolve ordering bottlenecks in parallel Belief Propagation.
- **Sparse Data Optimization:** Optimized memory access for irregular graphs using **Compressed Sparse Row (CSR)** formats, minimizing cache-line contention and improving effective bandwidth on 48-thread manycore architectures.

Awards, Certificates, & Talks

- Edward S. Rogers Sr. Department Betz Entrance Scholarship ($5,000) *2017*
- Certificate in Engineering Business *Jun. 2022*
- Qualcomm Panel Discussion: *Demystifying Machine Learning* Mar. 2025

Technical Skills

Software & Tools:: C/C++, Python (NumPy/Keras), Julia, ModelSim/VCS, Git, Jenkins CI/CD, SystemVerilog, Graph IR, SIMD, ISA Simulation, MLIR/LLVM (Logic), Quartus Prime.