Quick guide to program your ZYNQ

Summary:

1. Create project:

Determine your project name and location and choose "next" for all other stages, by the way "xc7z010clg400-1" is your ZYNQ.

2. Create HDL source:

Again, select "next" for all stages, then write your Verilog HDL in the created ".v" file.

3. Add constraint file:

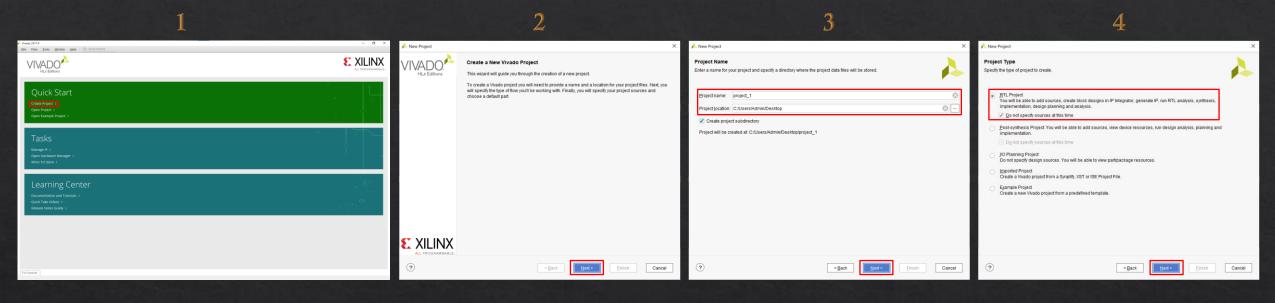
Add your ".xdc" file and click on "next" for other stages!

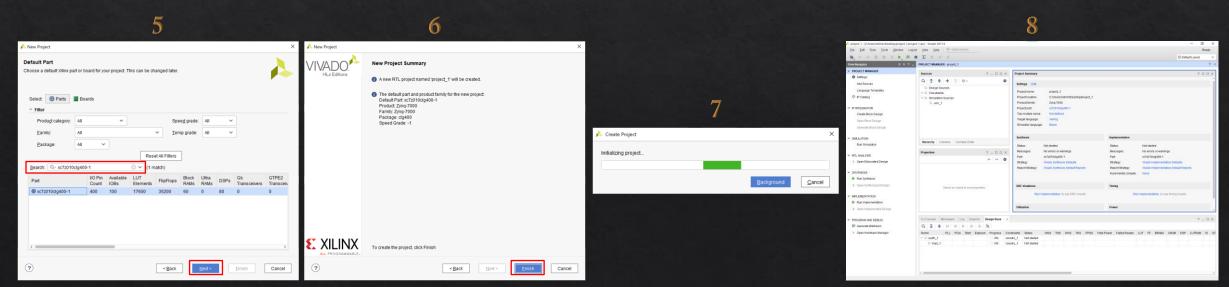
4. Program your ZYNQ

Generate bitstream, wait, open hardware manager, auto connect, and then program device. Choose "next" for other stages... . If you change your HDL, you must redo this step starting from generating bitstream.

In the following pages, you will see each of the 4 steps elaborated with screenshots...

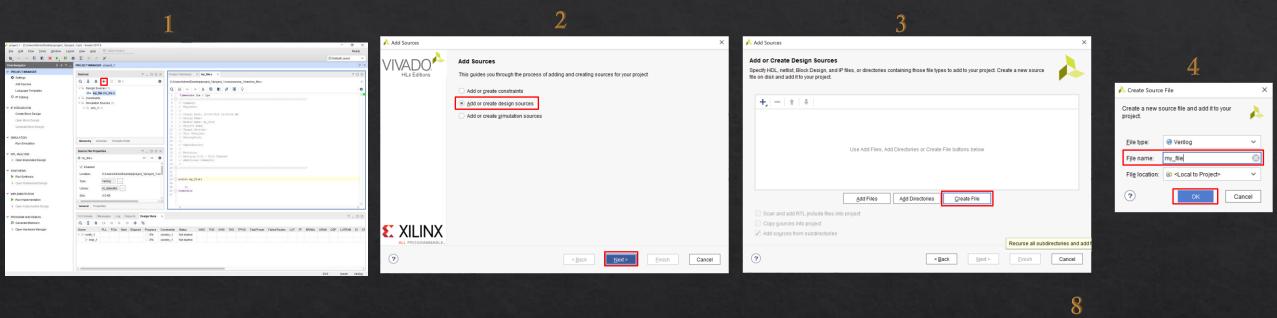
Creating a project





xc7z010clg400-1

Creating HDL source

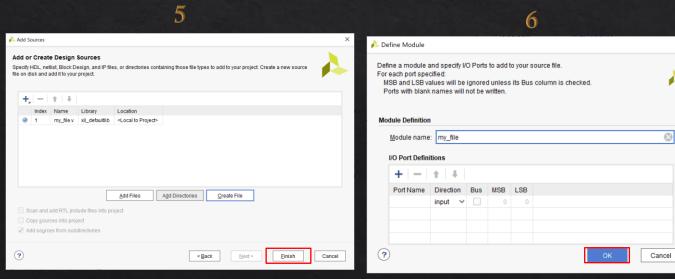


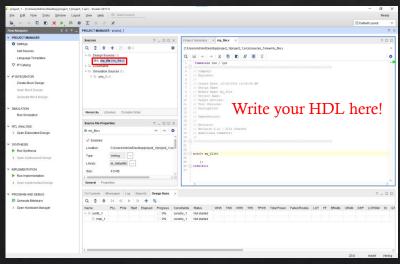
Define Module

The module definition has not been changed.

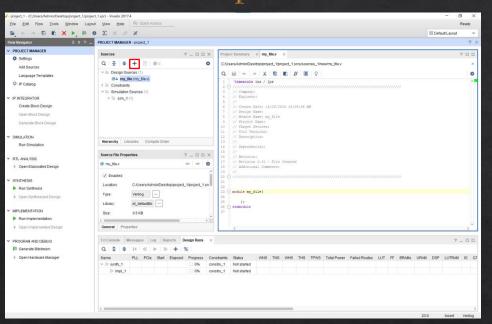
Are you sure you want to use these values?

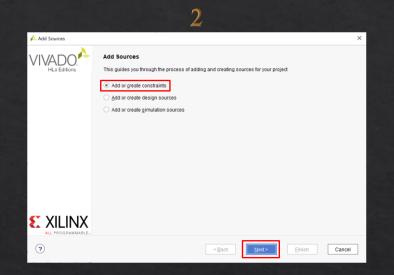
No

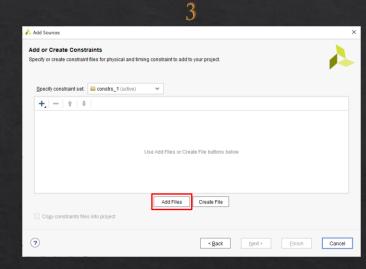


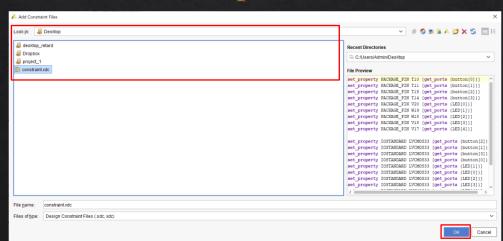


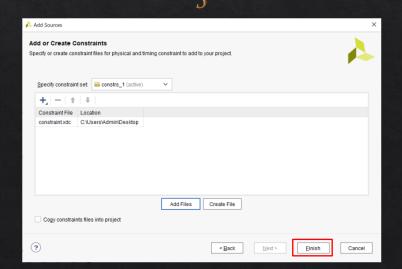
Adding constraint file





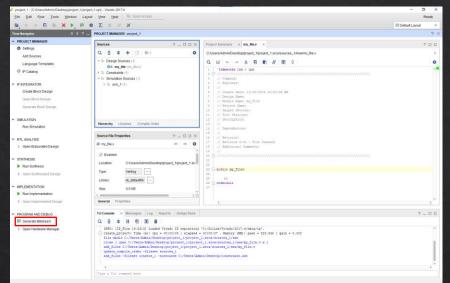




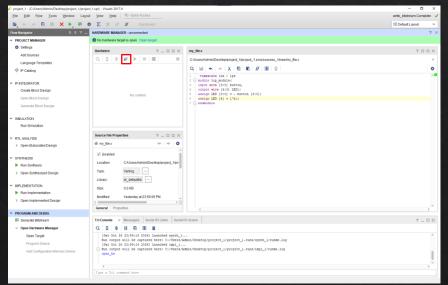


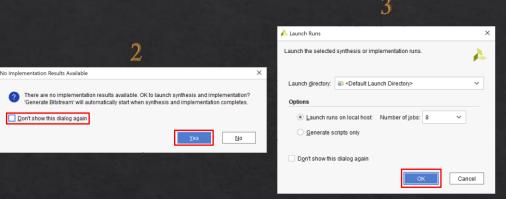
Program your ZYNQ



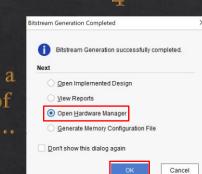


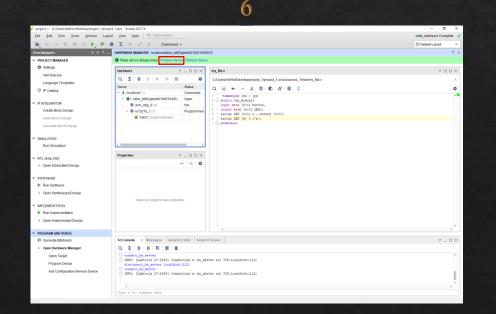






Wait for a couple of minutes...





A Program Device		×
	pramming file and download it to your hardware device. You can optionally file that corresponds to the debug cores contained in the bitstream	A
Bitstream file: Debug probes file: Enable end of s	Users/Admini/Desktop/project_1/project_1.runs/impl_1/lop_module.bit	
?	<u>Program</u> Car	ncel