Quick guide to program your ZYNQ

Summary:

1. Create project:

   Determine your project name and location and choose “next” for all other stages, by the way “xc7z010clg400-1” is your ZYNQ.

2. Create HDL source:

   Again, select “next” for all stages, then write your Verilog HDL in the created “.v” file.

3. Add constraint file:

   Add your “.xdc” file and click on “next” for other stages!

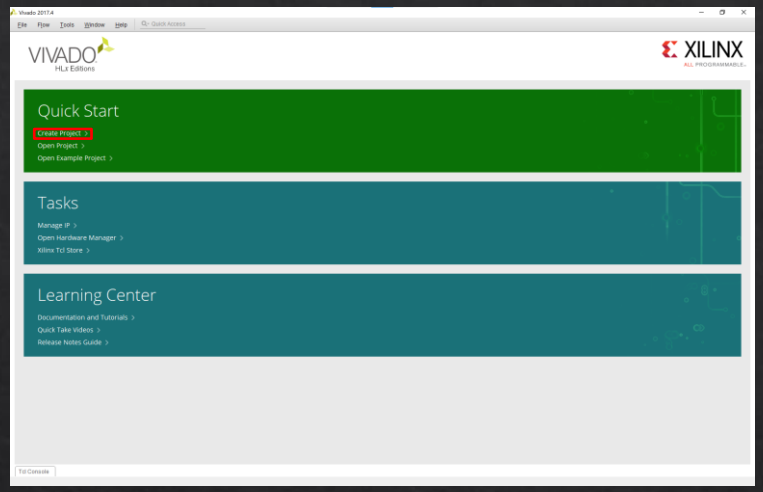
4. Program your ZYNQ

   Generate bitstream, wait, open hardware manager, auto connect, and then program device. Choose “next” for other stages… . If you change your HDL, you must redo this step starting from generating bitstream.

In the following pages, you will see each of the 4 steps elaborated with screenshots…

Creating a project

1



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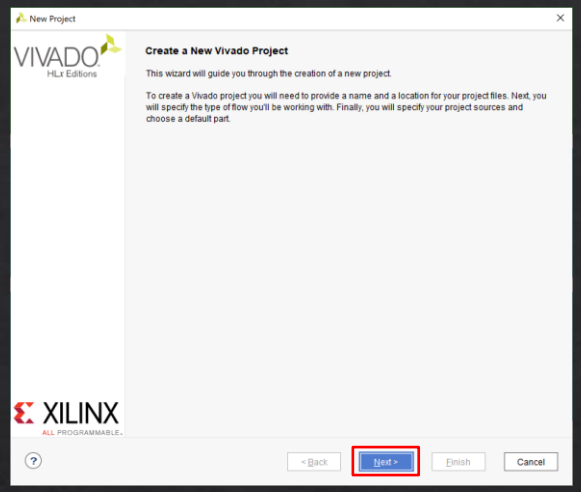

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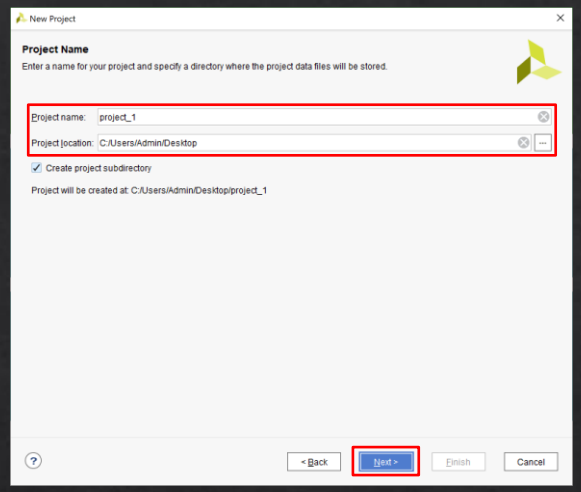

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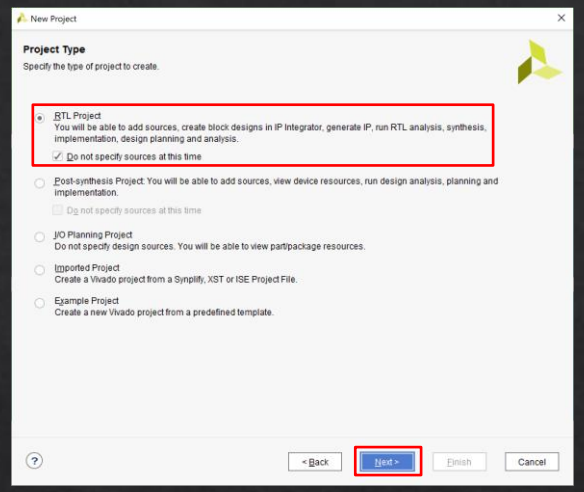

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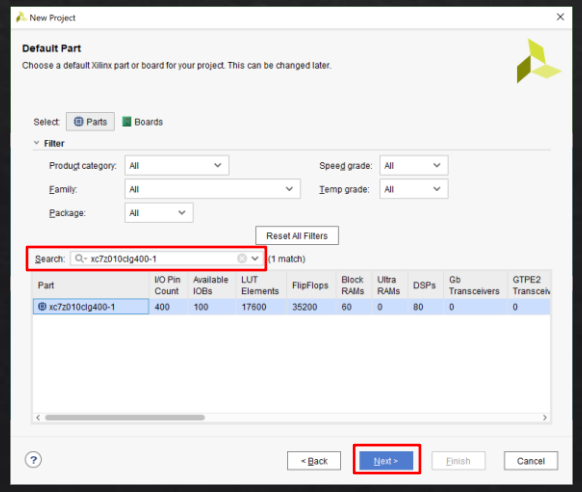

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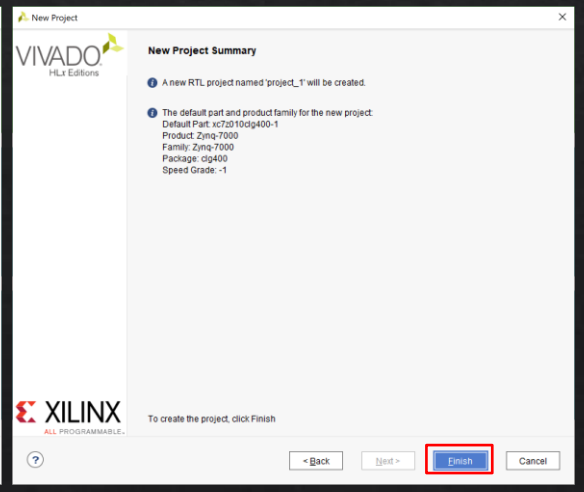

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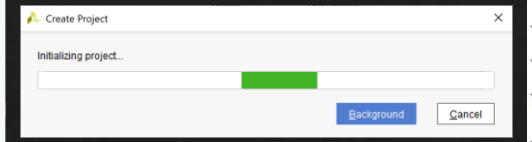

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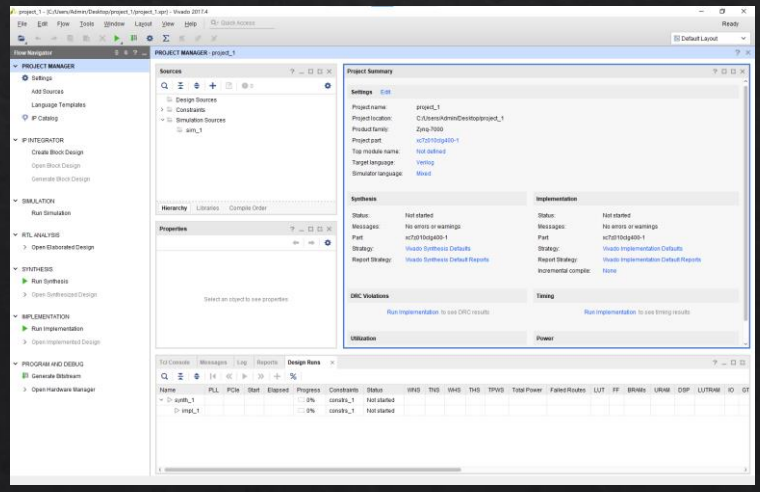
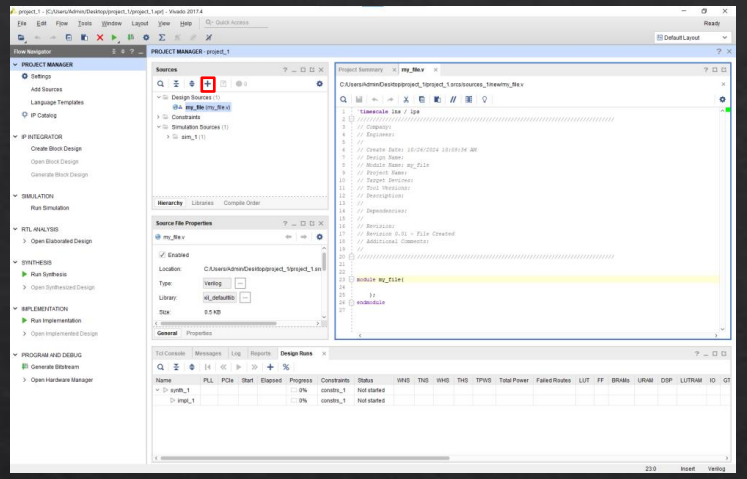


xc7z010clg400-1

Creating HDL source

1



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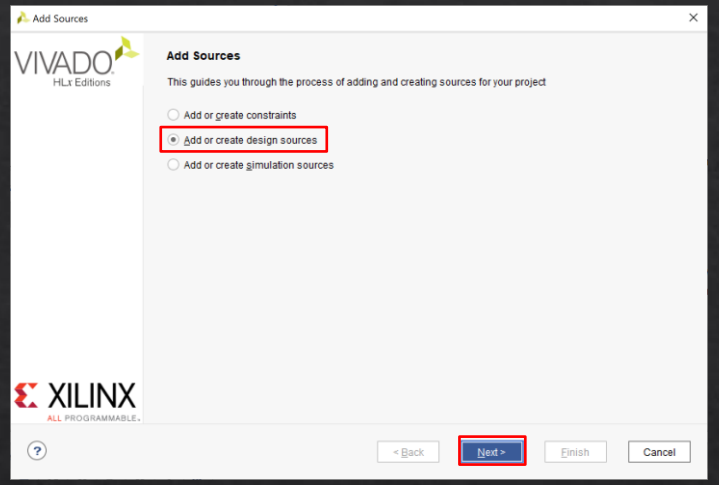

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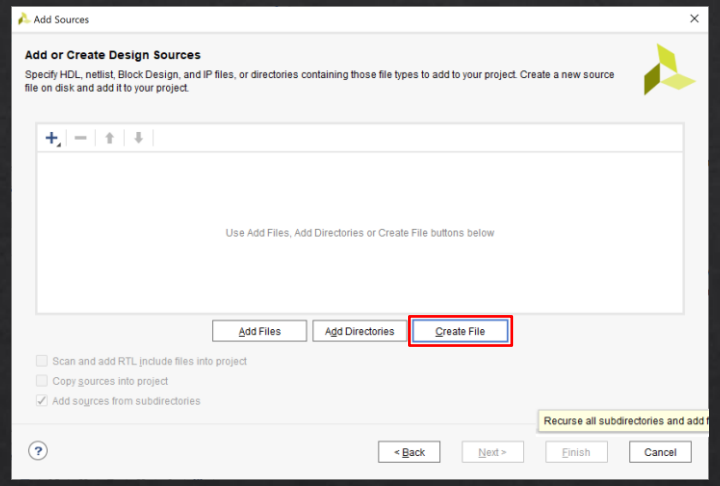

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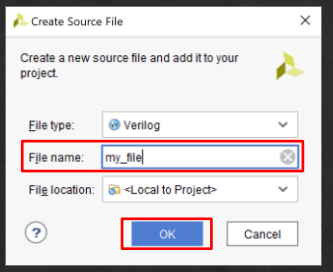

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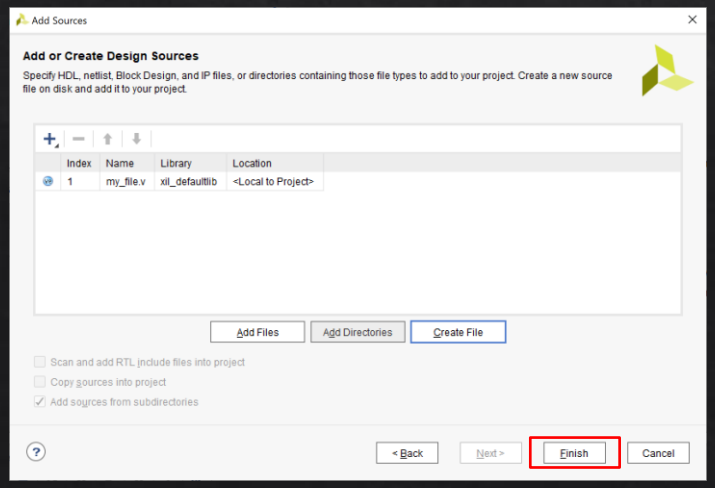

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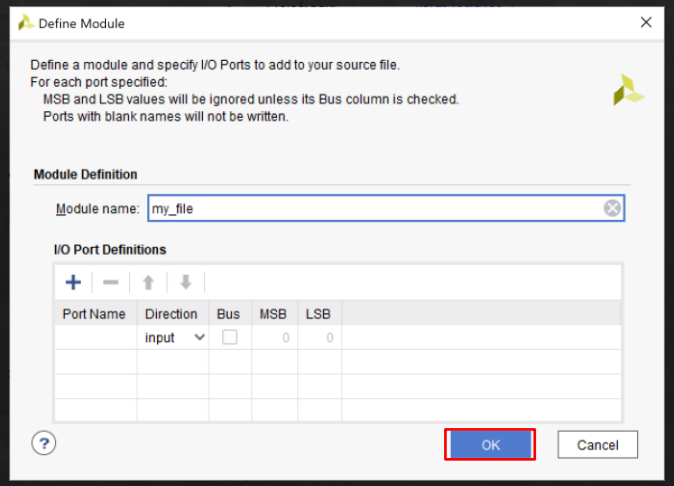

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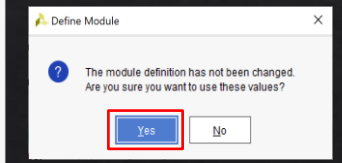

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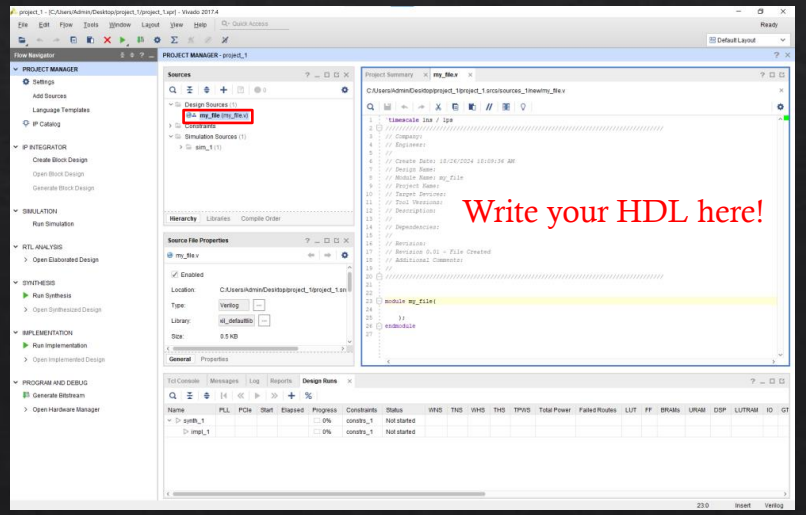

Adding constraint file

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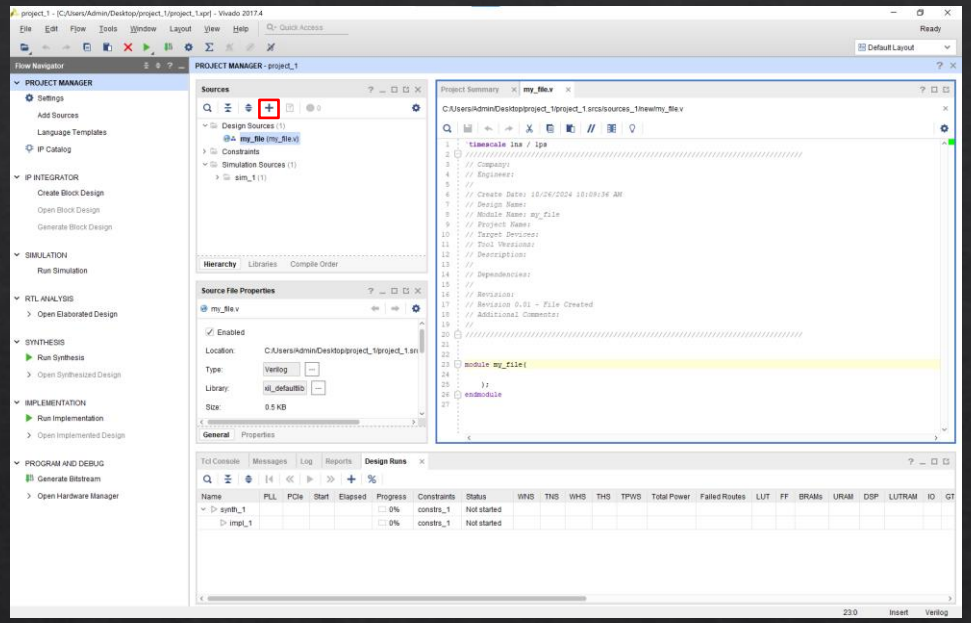

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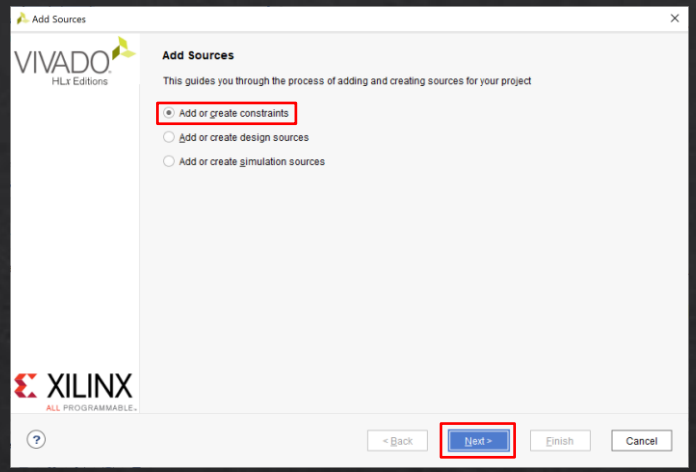

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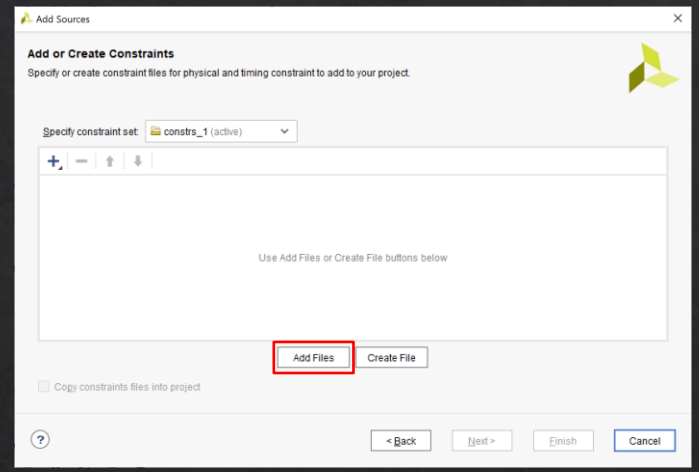

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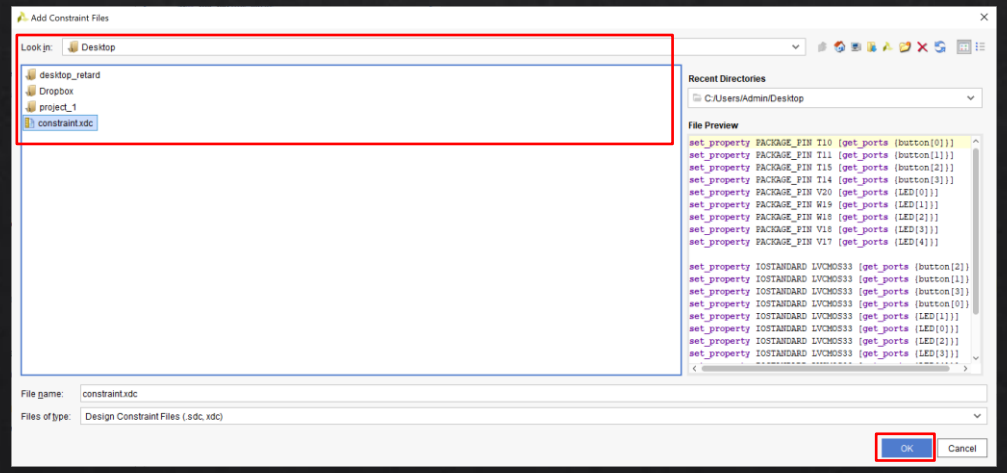

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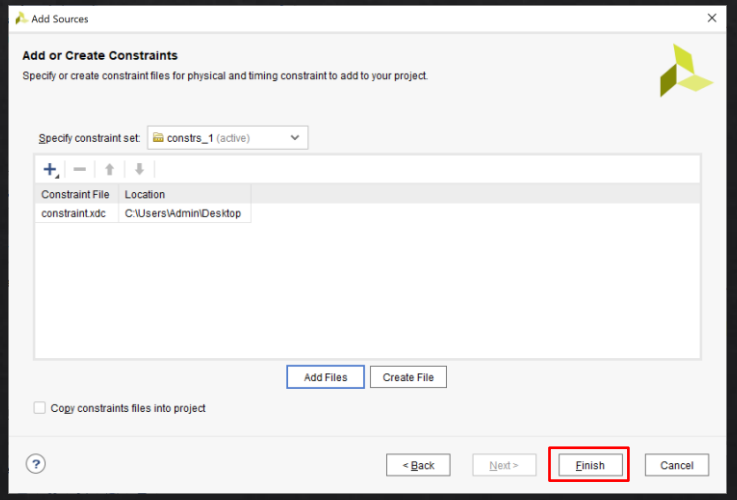
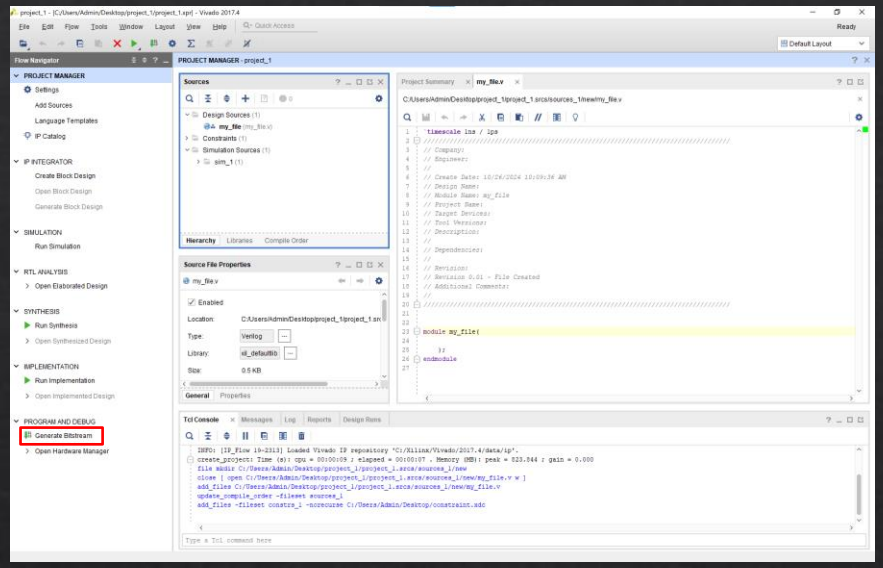


Program your ZYNQ

1



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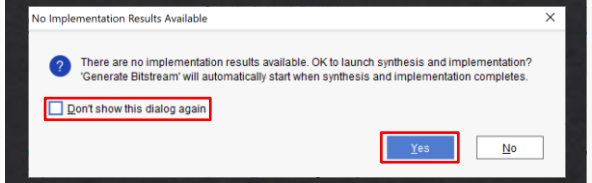

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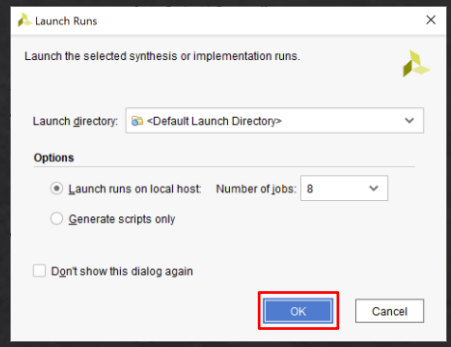

Wait for a couple of minutes…

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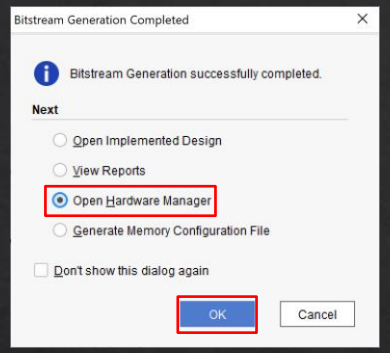

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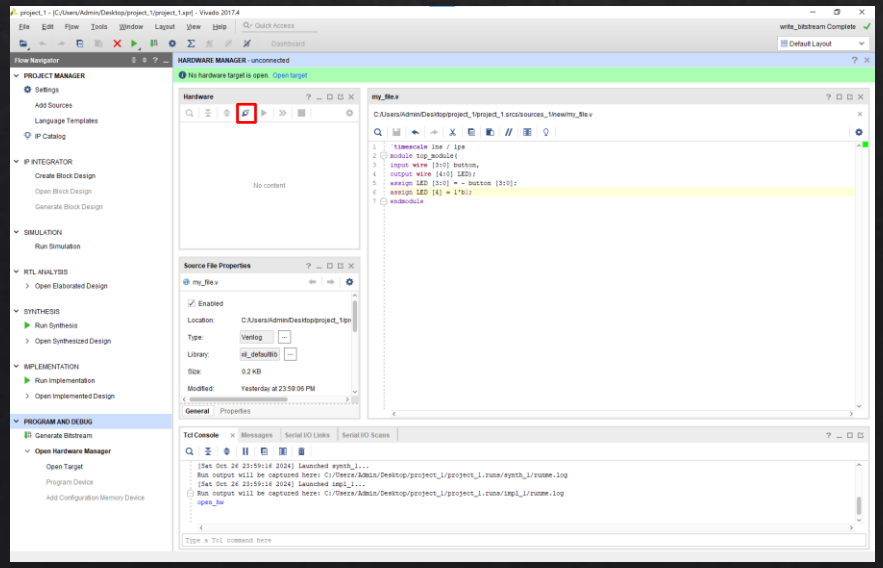

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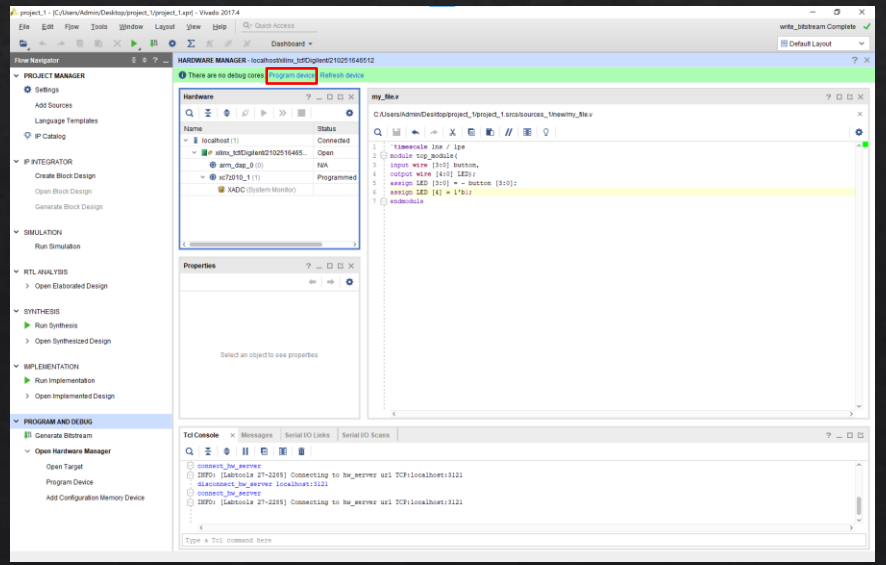

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