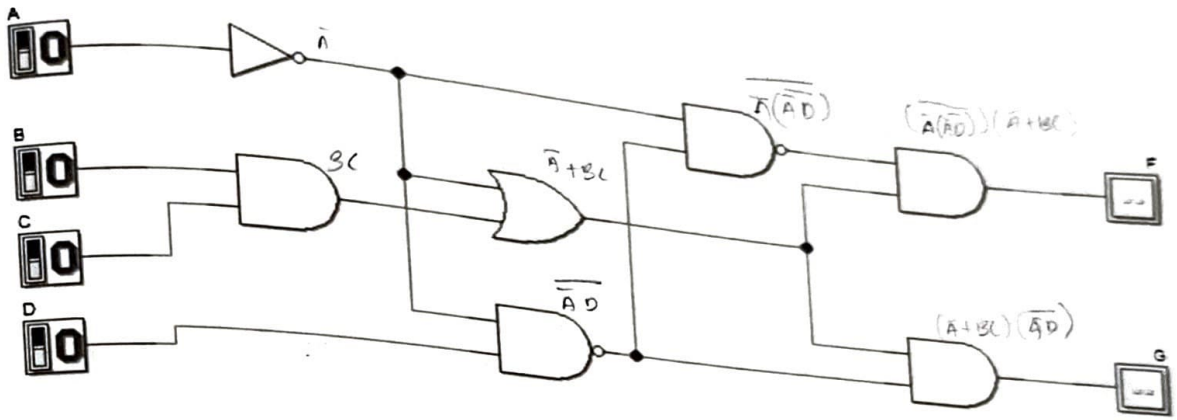
5. Experiment

5.1 Part A:

Refer to circuit in Figure 1.



a) Refer to the circuit. Derive Boolean expression for output F and G.

$$F = \overline{(\bar{A}(\overline{\bar{A}D}))}(\bar{A}+BC)$$

$$G = (\bar{A}+BC)(\overline{\bar{A}D})$$

b) Simplify equation output F using laws, rules and De Morgan Theorem, and write the equation in Sum of Product (SOP).

$$F = \overline{(\bar{A}(\overline{\bar{A}D}))}(\bar{A}+BC)$$

$$= (\bar{\bar{A}} + \overline{\overline{(\bar{A}D)}})(\bar{A}+BC)$$

$$= (A + \bar{A}D)(\bar{A}+BC)$$

$$= A\bar{A} + ABC + \bar{A}\bar{A}D + \bar{A}BCD$$

$$= ABC + \bar{A}\bar{A}D + \bar{A}BCD$$

$$= ABC + \bar{A}D + \bar{A}BCD$$

c) Simplify equation output G using laws, rules and De Morgan Theorem, and write the equation in Product of Sum (POS).

$$G = (\bar{A} + BC)(\overline{\bar{A}D})$$

$$= (\bar{A} + BC)(\bar{\bar{A}} + \bar{D})$$

$$= (\bar{A} + BC)(A + \bar{D})$$

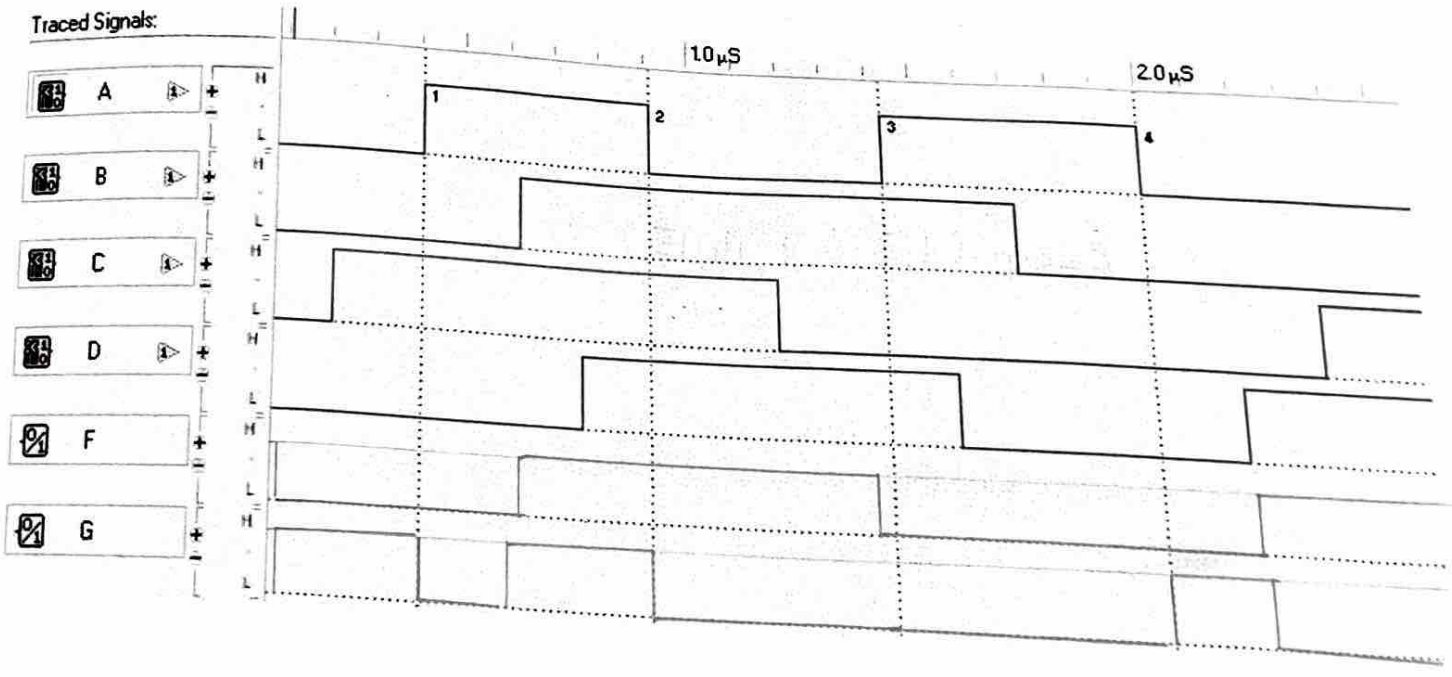
$$= (\bar{A} + B)(\bar{A} + C)(A + \bar{D})$$

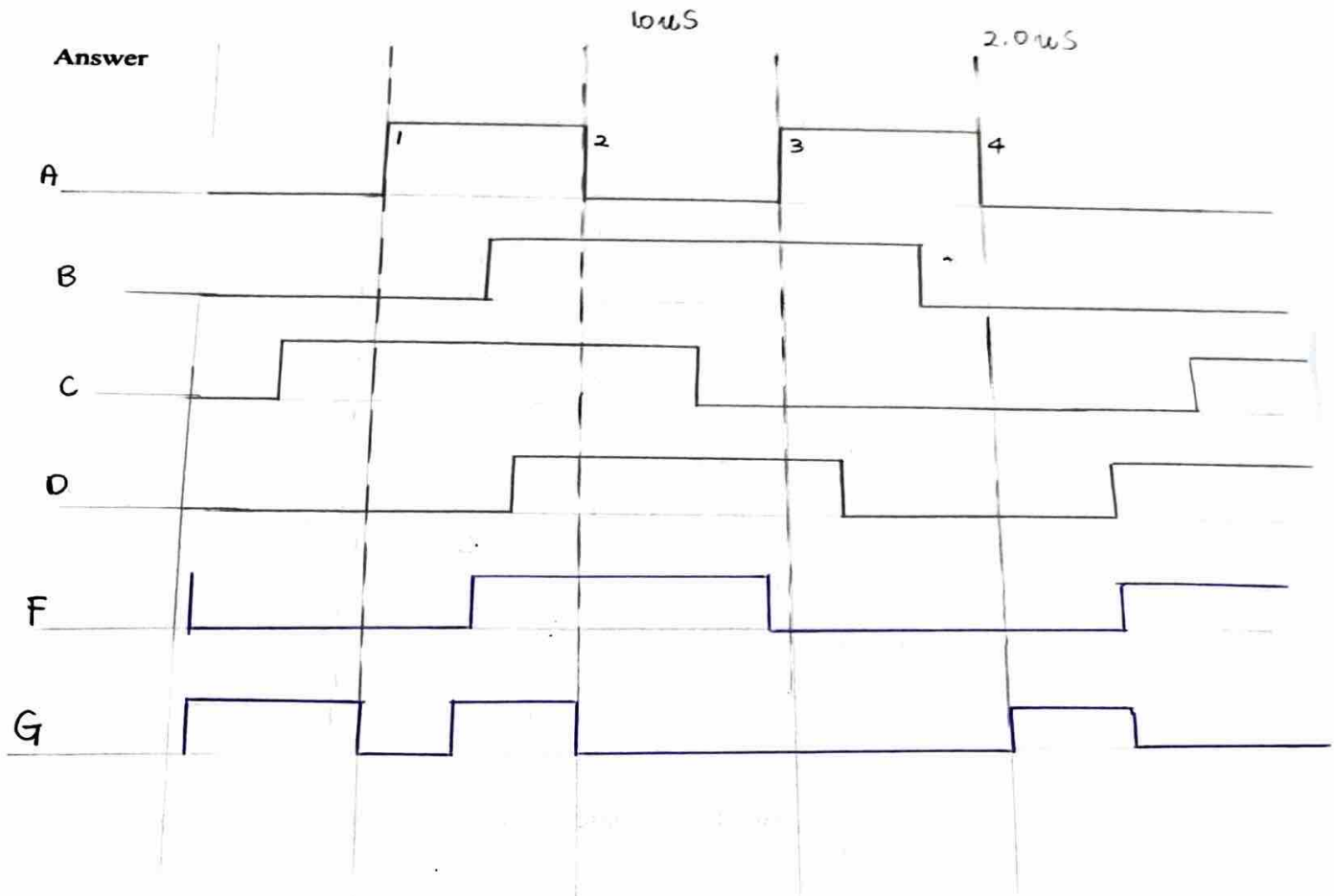
Simulate the circuit and construct the truth table and complete the following.

Truth table for output circuit F and G shown in Figure 1

Input				Output	
A	B	C	D	F	G
0	0	0	0	0	1
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	0	0
1	0	1	1	0	0
1	1	0	0	0	0
1	1	0	1	0	0
1	1	1	0	1	1
1	1	1	1	1	1

d) Using Deeds, draw circuit in Figure 1. Simulate and complete the waveform output F and G by referring the following diagram:





e) Write Boolean equation for output F using Sigma notation.

$$\Sigma_{ABCD}(1,3,5,7,14,15)$$

f) Write Boolean equation for output G using Pi notation.

$$\Pi_{ABCD}(1,3,5,7,8,9,10,11,12,13)$$

Experimental steps

i) Construct Truth Table in Table 1 for the LRT operations. Use variables *S, S1, S2,* and *S3* as INPUTS and *OPEN* and *ALARM* as OUTPUTS.

Table 1

INPUT				OUTPUT	
S	**S1**	**S2**	**S3**	**OPEN**	**ALARM**
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	0
0	1	0	0	0	1
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	0	0
1	1	0	0	1	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	0	0

ii) Use K-Map to get optimized SOP Boolean equations for the *OPEN* and *ALARM* circuits

OPEN

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	(1)	0	0	0
10	0	(1)	0	(1)

$= AB\bar{C}\bar{D} + A\bar{B}\bar{C}D + A\bar{B}C\bar{D}$

Experimental steps

i) Construct Truth Table in Table 1 for the LRT operations. Use variables *S, S1, S2,* and *S3* as INPUTS and *OPEN* and *ALARM* as OUTPUTS.

Table 1

INPUT				OUTPUT	
S	**S1**	**S2**	**S3**	**OPEN**	**ALARM**
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	0
0	1	0	0	0	1
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	0	0
1	1	0	0	1	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	0	0

ii) Use K-Map to get optimized SOP Boolean equations for the *OPEN* and *ALARM* circuit

OPEN

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	(1)	0	0	0
10	0	(1)	0	(1)

$= A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}C\bar{D}$

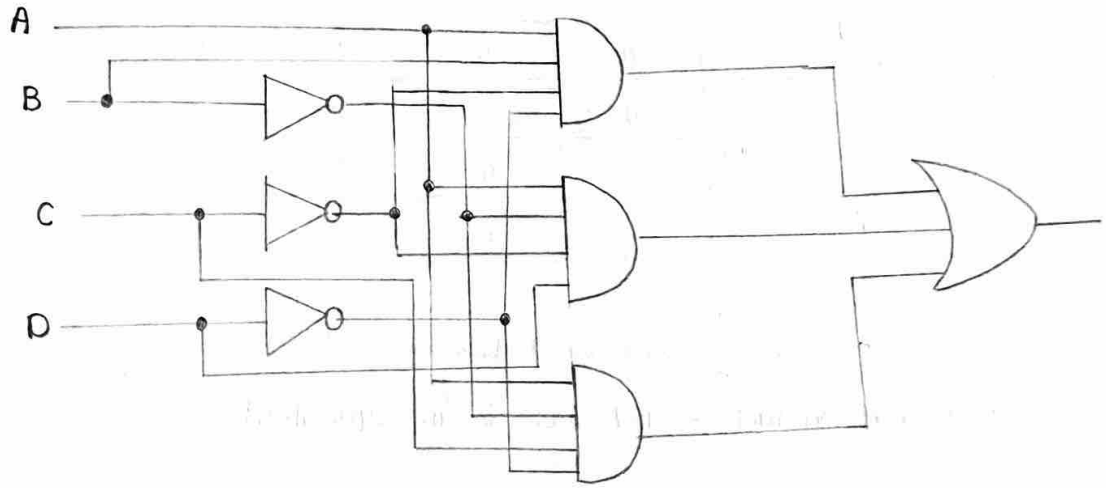
ALARM

AB \ CD	00	01	11	10
00	0	(1)	0	(1)
01	(1)	0	0	0
11	0	0	0	0
10	(1)	0	0	0

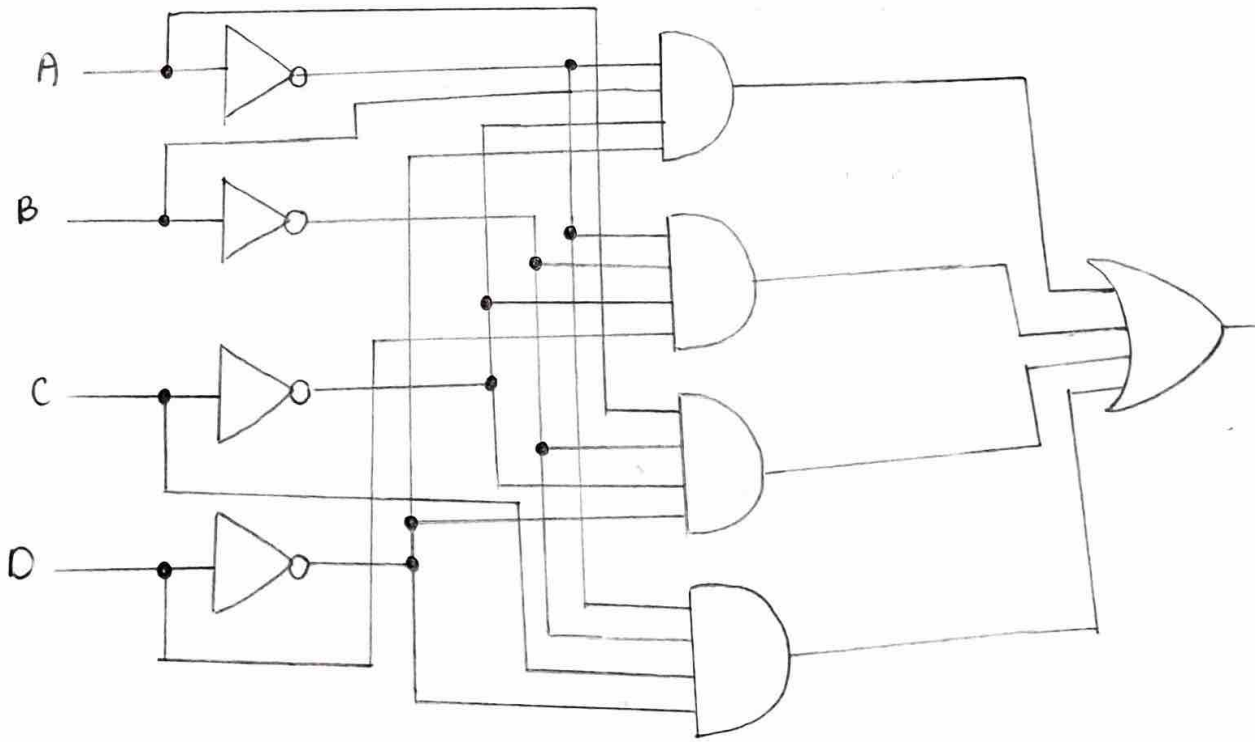
$= \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D}$

iii) From equations in (ii), draw your final *OPEN* and *ALARM* circuits using Deeds Simulator.

OPEN



ALARM



iv) Simulate the circuit design in (iii) and construct Truth Table in Table 2.

Table 2

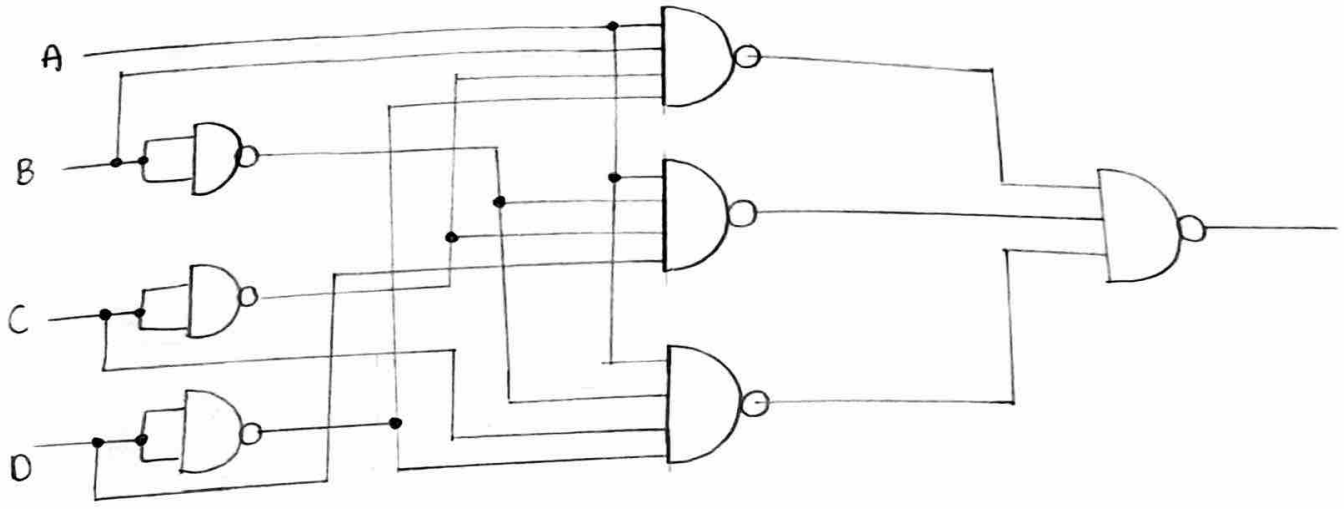
INPUT				OUTPUT	
S	S1	S2	S3	OPEN	ALARM
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	0
0	1	0	0	0	1
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	0	0
1	1	0	0	1	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	0	0

Compare the answer of Table 2 and Table 1. What is your conclusion?

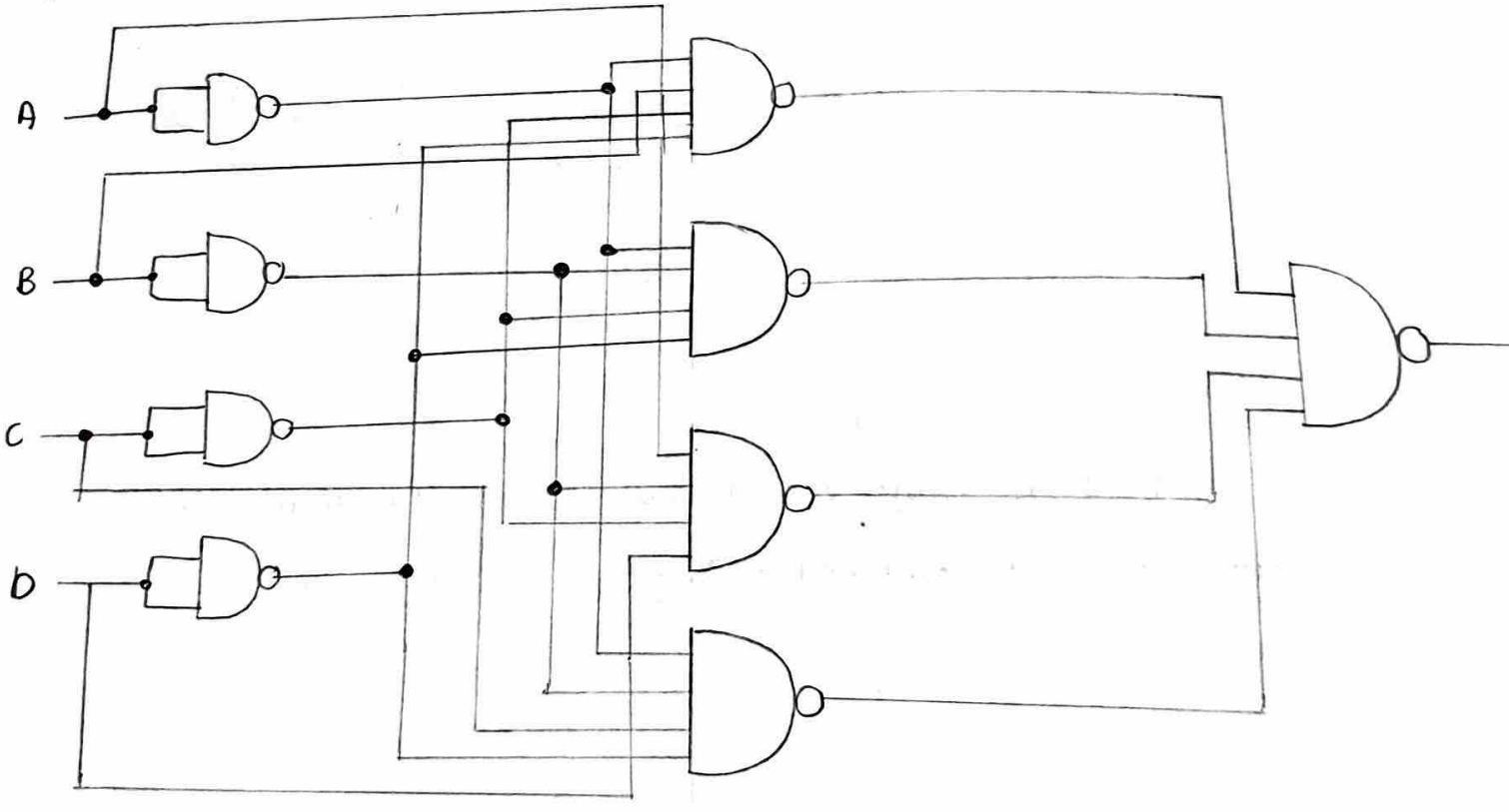
Both output on Table 2 and Table 1 are equivalent.

v) **Use dual symbol to convert, AND-OR circuit to NAND gates only. Draw the final circuit using Deeds Simulator.**

OPEN



ALARM



vi) **Simulate the final NAND gates design in (v) and construct Truth Table in Table 3.**

Table 3

INPUT				OUTPUT	
S	**S1**	**S2**	**S3**	**OPEN**	**ALARM**
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	0
0	1	0	0	0	1
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	0	0
1	1	0	0	1	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	0	0

Compare the answer of Table 2 and Table 3. What is your conclusion?

The output in Table 2 and Table 3 are equivalence. Thus, NAND gate and ~~and~~ AND-OR gate are equivalence.

Fully Completed ☐ Partially Completed ☐ Checked by: _____