6.334 Design Project

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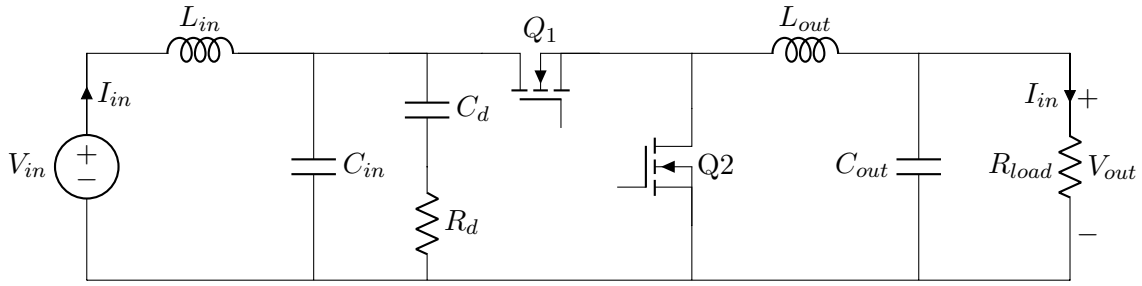
May 11, 2020

1 Summary of Completed Design

1.1 Circuit Schematic



1.2 Physical Component Selection

Component	Value	Description
Q1	NVMFS5C670NL	60V N-Channel MOSFET
Q2	NVMFS5C670NL	60V N-Channel MOSFET
L_{out}	$9\mu H$	6 turns of rectangular 8 AWG copper wire, RM14-A250 core
C_{out}	$100\mu F$	Panasonic SVF Series
L_{in}	$4\mu H$	4 turns of rectangular 4 AWG copper wire, RM14-A250 core
C_{in}	$40\mu F$	Nippon Chemi-Con NTS Series (2x $22\mu F$ in parallel)
C_d	$330\mu F$	Nichicon HD Series
R_d	0.097Ω	(after accounting for $C_{d(esr)}$, $R_d = 0.065\Omega$)

1.3 Circuit Parameters and Performance

Parameter	Value
Switching Frequency	139 kHz
Output Voltage Ripple	71mV (pk-pk, worst case, $D = 1/2$)
Inductor Current Ripple	7.99 A (pk-pk, worst case, $D = 1/2$)
Input Current Ripple	57mA (pk-pk, worst case, $D = 1/2$)
Output Voltage (static)	15V, plus ripple
Output Voltage (transient, $V_{in} : 27V \longrightarrow 40V$)	15V ± 0.7%
Output Voltage (transient, $P_{out} : 50W \longrightarrow 150W$)	15V ± 3.3 %
Maximum Efficiency	94.8 %

2 Design Process

2.1 Overview

Despite the number of required specifications, the amount of freedom within this exercise is substantial. There exist no constraints on board area, component size, or cost. As a result, multiple solutions exist that satisfy the requirements - a device with a slow switching frequency and the substantial requisite filtering would produce a high efficiency converter, while a fast-switching converter with smaller filter stages would provide lower efficiency while reducing overall size.

To overcome this, it was decided that the design process should produce a converter with the least loss possible with the components given in the assignment. This was done computationally, using a self-written Python script that optimizes the component values by trying every combination of component, and choosing the combination that minimizes loss. This process is usually quite complex as the potential solution space is incredibly large. However, the solution space can be made smaller by rewriting component losses as functions of both design specifications and as few independent variables as possible. By iterating these independent variables across reasonable ranges, the losses can be calculated and a minimum found. In the case of this buck converter, the two independent variables were the switching frequency and the capacitance of the output filter, from which all the other component specifications could be derived in the following manner:

- Transistor switching losses are proportional to the switching frequency, the turn-on and turn off times, and the series resistance of the MOSFET. The optimizer calculates the loss of every MOSFET provided in the assignment, and chooses the one with the lowest dissipation.
- The required inductance of the output filter is a product of both the switching frequency and output capacitance. A faster switching frequency and a larger output capacitance will reduce the voltage ripple on the output, which is given as a design constraint. The output voltage specification gives a constraint on the product of L_{out} and C_{out}, meaning that neither L or C can be uniquely determined. The optimizer determines a set of values of L_{out} by iterating over f_{sw} and C_{out}, and then calculates the requisite loss in the inductor.
- Once a value of L_{out} has been determined, the input filter can be designed. If L_{out} is known, then the input current ripple specification can be used to determine the attenuation required by the input filter. Both the switching frequency and the input current ripple specification can be used to put a constraint on the product of L_{in} and C_{in}. Since only losses in the inductor are being considered, the value of the inductance is desired to be minimized, but is limited by the maximum value of C_{in}. In this case, a maximum capacitor value was given to the optimizer (in this case, 100 μF was used) which was used to calculate a corresponding inductance. This was used to choose a core, wire gauge, and number of turns for an inductor. Since fractional turns are not physically possible, the number of turns was rounded up to the nearest integer, giving an inductance value larger than necessary. This oversized inductance value was used to calculate the minimum capacitance that would satisfy the input current ripple specification - which was naturally smaller than the maximum value provided to the optimizer.

- Now that values of L_{in} and C_{in} have been determined, the proper value for the input filter damping resistance R_d had to be selected. This value is uniquely determined if one defines a maximum gain that the input filter may have at resonance. In this design, optimizer was instructed to find a value of damping resistance that permitted no more than 6dB of peaking in the transfer function from filter input current to filter output current.

- Via this process, the transistor losses, output filter inductor losses, and input filter inductor losses can be found. This provides the total converter loss for a given f_{sw} and C_{out}. The optimizer iterates over both of these parameters to find the combination that provides the minimum loss, and then outputs the circuit parameters that provide said loss. Once the optimizer had finished running the efficiency was checked to ensure that it fell within specification, and the thermals were checked to determine if heatsinks were necessary.

2.2 Optimizer Output

Plots of the optimizer's results are given below:

Figure 1: Power Loss in available MOSFETs as a function of frequency. Notice that the MOSFET with the lowest loss changes as frequency rises, as switching losses begin to overcome conduction losses.

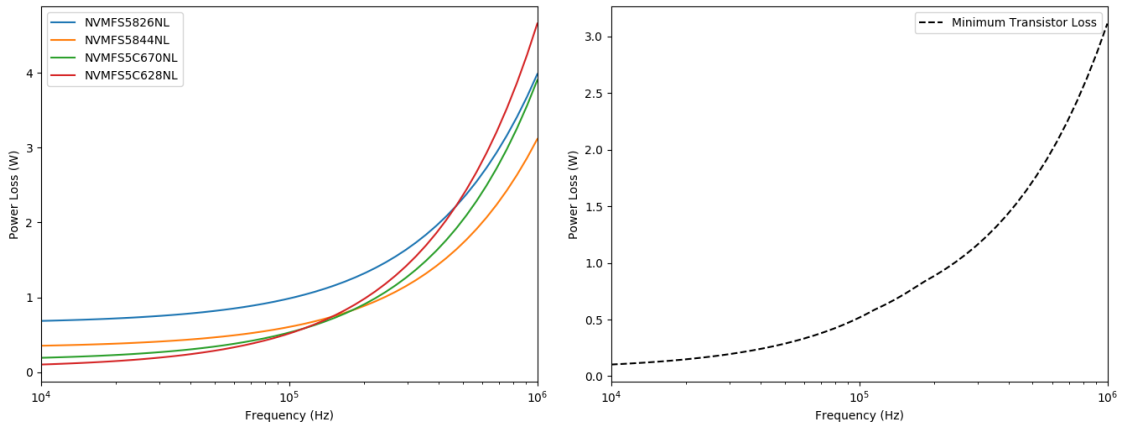
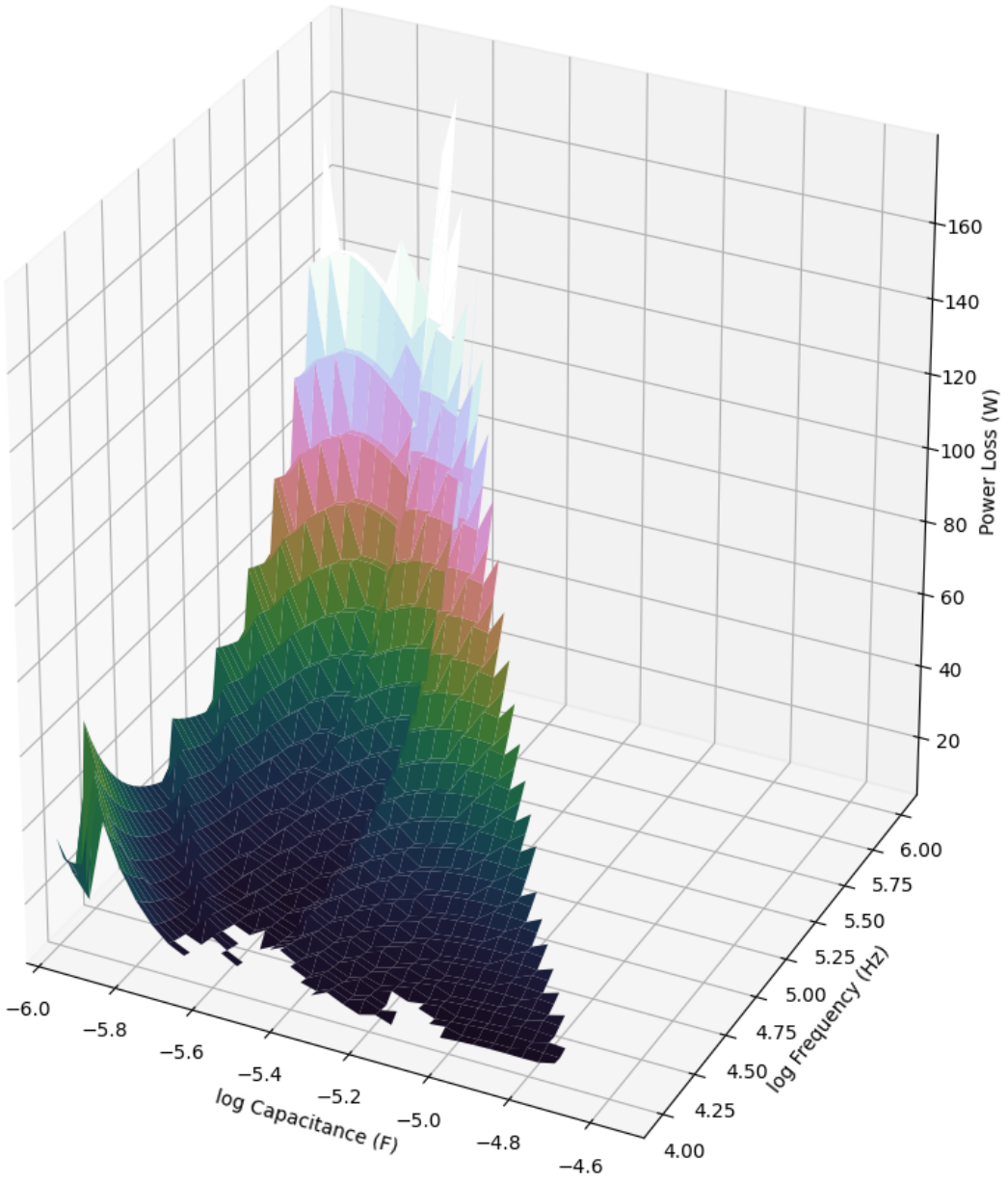


Figure 2: Total converter power loss as a function of frequency and output filter capacitance. The optimizer finds the global minimum of this graph to produce the optimal design.



3 Constraint Derivations

3.1 Controlled Switch

Losses in the switching element reduce the efficiency of the system, and include both switching and conduction losses. The switch conducts the input current D percent of the time, so conduction losses are calculated as:

$$P_{cond} = I_{rms}^2 R_{ds(on)} = I_{in}^2 R_{ds(on)} D$$

With the worst-case occurring as $D = 1$. However, the duty cycle of the converter will never exceed 55.5% as was previously mentioned. In this case, the maximum conduction losses are:

$$P_{cond} = \left(\frac{P_{max}}{V_{min}}\right)^2 R_{ds(on)} D_{max} = 16.98 \cdot R_{ds(on)}$$

Switching losses also contribute to converter inefficiency, and can be calculated as:

$$P_{switch} \approx \frac{I_L V_{in} f_{sw}}{2}(t_f + t_r) = \frac{I_L V_{in}}{2T}(t_f + t_r) = \frac{D I_{in} V_{in}}{2T}(t_f + t_r) = \frac{DP}{2T}(t_f + t_r)$$

The switch turn-on and turn-off times t_r and t_f are determined by the gate charge and the gate driver current. By approximating the turn on and turn off times as being equivalent However it is known that the maximum duty cycle of the converter is 55.5%, so the maximum switch losses may be computed with $D = 0.555$.

3.2 Complementary Switch

Since no constraint is given as to cost or circuit complexity, the decision to use either an active switch or a diode as the complementary switch is a matter of efficiency. From the selection of diodes provided, all have a maximum reverse voltage larger than the input voltage, and are therefore eligible for use in the design. Since there is no constraint of cost or board area, the diode with the lowest forward voltage is chosen to minimize losses, given by:

$$P_d = V_f I_d = V_f I_{out}(1 - D)$$

With the worst-case power loss occuring at $D = 0$. However, since the minimum duty cycle of the converter is known, it is permissible to use $D_{min} = 0.375$ instead. It is also specified that the maximum output power of the converter is 150W at 15V, giving an output current of 10A. The loss then becomes:

$$P_{d(max)} = V_f \cdot 10 \cdot (1 - 0.375) = V_f \cdot 6.25$$

The STPS3045DJF has the lowest forward voltage of the available diodes, at 460mV. The diode loss in this case is 2.9W, which is only less than an active switch for frequencies less than $\approx$ 1 MHz. Therefore, it was decided to use a MOSFET instead of a freewheeling diode for the active switch, as the optimal switching frequency was found to be far less than 1 MHz.

3.3 Output Filter

The capacitor ripple voltage is determined by assuming that the entire inductor ripple current flows through the capacitor. The inductor carries a ripple current given by:

$$\Delta I_{L(pk-pk)} = \int_0^{DT} \frac{V_L}{L} dt = \int_0^{DT} \frac{V_{in} - V_{out}}{L} = \int_0^{DT} \frac{V_{in}(1 - D)}{L} = \frac{V_{in}(1 - D)DT}{L}$$

Assuming that the switch is on for a time DT, where T is the switching period. To meet the 15V output specification across an input range of 27 - 40V, the duty cycle will have to

vary from 37.5% to 55.5%. The maximum inductor current ripple occurs at a duty cycle of 50%, which lies within this range. Therefore, the ripple at $D = 0.5$ sets a upper bound on the inductor current and capacitor voltage ripples, and the constraint equation is:

$$\Delta I_{L(pk-pk,max)} = \Delta I_{L(pk-pk)}|_{D=0.5} = \frac{V_{in}T}{4L}$$

Although the amplitude of the inductor ripple current has been calculated, this quantity varies linearly with respect to time, because of the (approximately) constant voltages the inductor is subjected to. In the calculation of worst-case output voltage ripple, it is assumed that all the ripple current flows through the capacitor. As the current flowing through the capacitor is linear, the voltage across it will be quadratic. However, only the peak capacitor voltage ripple is of interest, not the entire time series. The the total charge that flows into the capacitor while it's being charged by the inductor can be calculated:

$$q_c = \int_{t_{start}}^{t_{stop}} I_C dt = \int_{DT/2}^{(T+DT)/2} I_L dt$$

Since the current is linear, the integral evaluates to the area of the triangular region, given as $bh/2$, where b is the base of the triangular region, and h is its height:

$$q_c = \frac{1}{2}bh = \frac{1}{2}\frac{\Delta I_{L(pk-pk)}}{2}\left(\frac{T+DT}{2} - \frac{DT}{2}\right) = \frac{\Delta I_{L(pk-pk)}T}{8}$$

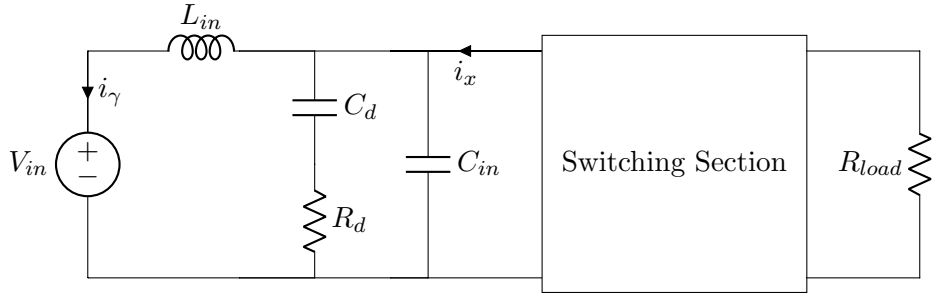
$$v_c = \frac{q_C}{C} = \frac{\Delta I_{L(pk-pk)}T}{8C} = \frac{V_{in}(1-D)DT^2}{8LC}$$

If $D = 0.5$, v_c expresses the maximum ripple voltage achievable by the converter within it's operating area:

$$v_{c(pk-pk,max)} = \frac{V_{in}T^2}{32LC}$$

3.4 Input Filter

The input filter parameters were determined by finding the transfer function between filter input and output current for the topology shown below, as was done on Problem Set 6:



$$\frac{i_\gamma(s)}{i_x(s)} = H(s) = \frac{1}{1 + L_{in}C_{in}s^2 + \frac{sL_{in}}{R_d}} \longrightarrow |H(j\omega)| = \frac{\sqrt{(R_d^2 - L_{in}C_{in}R_d^2\omega^2)^2 + \omega^2 R_d^2 L_{in}^2}}{(R_d - L_{in}C_{in}R_d\omega^2)^2 + \omega^2 L_{in}^2}$$

To meet the input current ripple requirement, $|H(jw)|$ must be less than $60\text{mA}/\Delta I_L$ at the switching frequency. This requirement implies that the resonant frequency of the

filter be below the switching frequency such that the filter attenuates. In this mode, it is permissible to ignore the damping resistance, as it does not affect the high-frequency asymptote of the filter. Doing so reduces $|H(jw)|$ to:

$$H_{simplified}(s) = \frac{1}{1 + L_{in}C_{in}s^2} \longrightarrow |H_{simplified}(jw)| = \left|\frac{1}{1 - L_{in}C_{in}\omega^2}\right| = \frac{1}{1 - L_{in}C_{in}\omega^2} = G$$

Where G is the attenuation required by the network. By solving for G a constraint is found for the product LC:

$$L_{in}C_{in} = \frac{\frac{1}{G} - 1}{\omega_{switch}^2}$$

Similarly, $|H(jw)|$ must be less than whatever the maximum allowed peaking in the transfer function is. This peaking occurs at resonance, where $\omega = 1/\sqrt{L_{in}C_{in}}$. Substituting this in yields:

$$|H(jw)|_{max} = R_d\sqrt{\frac{C_{in}}{L_{in}}} = K \longrightarrow R = K\sqrt{\frac{L_{in}}{C_{in}}}$$

Where $K = 2$ was chosen, which corresponds to a gain of 6dB. By rearranging terms, R_d is determined uniquely.

3.5 Inductor Losses

Inductor losses were taken as the sum of the winding losses and core losses. The winding losses were computed as the RMS inductor current times the winding resistance at the switching frequency, which is larger than the resistance at DC due to the skin effect.

$$P_{winding} = I_{rms}^2 R_{AC} = I_{rms}^2 R_{DC}\Delta\left[\frac{\sinh(2\Delta) + \sin(2\Delta)}{\cosh(2\Delta) - \cos(2\Delta)}\right]$$

R_{DC} was calculated as the number of turns times the circumference of the core, multiplied by the resistance per length of the wire. In the design provided, rectangular copper wire was used to maximize cross-sectional area and minimize resistance. In addition, $\Delta = w/\delta$ where δ is defined as:

$$\delta = \sqrt{\frac{\rho_{cu}}{\pi\mu_{cu}f_{sw}}}$$

Where ρ_{cu} is the resistivity of copper, μ_{cu} is the permeability of copper, and f_{sw} is the switching frequency.

In addition to winding losses, there also exist losses in the magnetic core. These losses are computed using the formula given in the assignment:

$$P_{core} = C_M \cdot f^{\alpha} \cdot (B_{ac,pk})^{\cdot} V_{core}$$

Where C_M, α and are the frequency-dependent parameters given in the assignment, and $B_{ac,pk}$ is the peak flux density in the core, and V_{core} is the volume of the magnetic core.

4 Control System

The control system was designed by modelling the circuit in LTSpice and varying the value of the commanded current $\widetilde{i_c}$ (the complementary switch was replaced with an idealized diode to help with convergence.) After much trial and error, a PI controller with a load-dependent feedforward term was selected. The commanded current is therefore given by:

$$\widetilde{i_c}(t) = K_p \cdot (V_{ref} - V_{out}(t) + K_i \cdot \int_0^t \left(V_{ref} - V_{out}(t')\right) dt' + V_{ref} \cdot \frac{V_{out}(t)}{I_{out}(t)}$$

With $K_p = 5$ and $K_i = 10000$.

4.1 Simulation Results

Figure 3: LTSpice Circuit

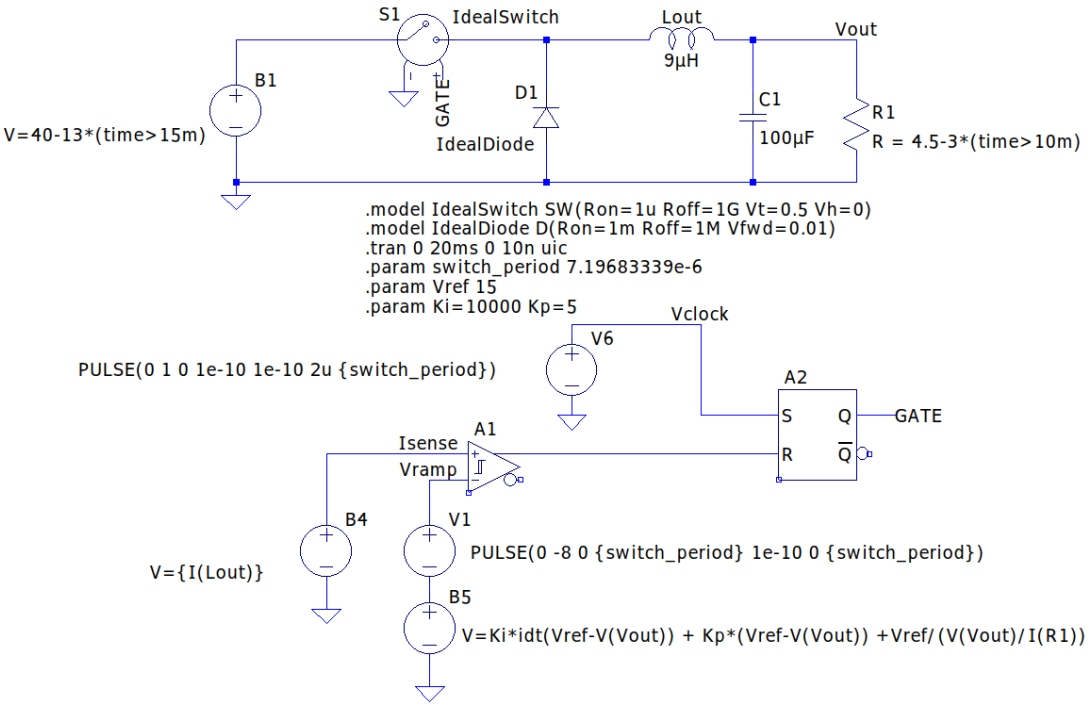
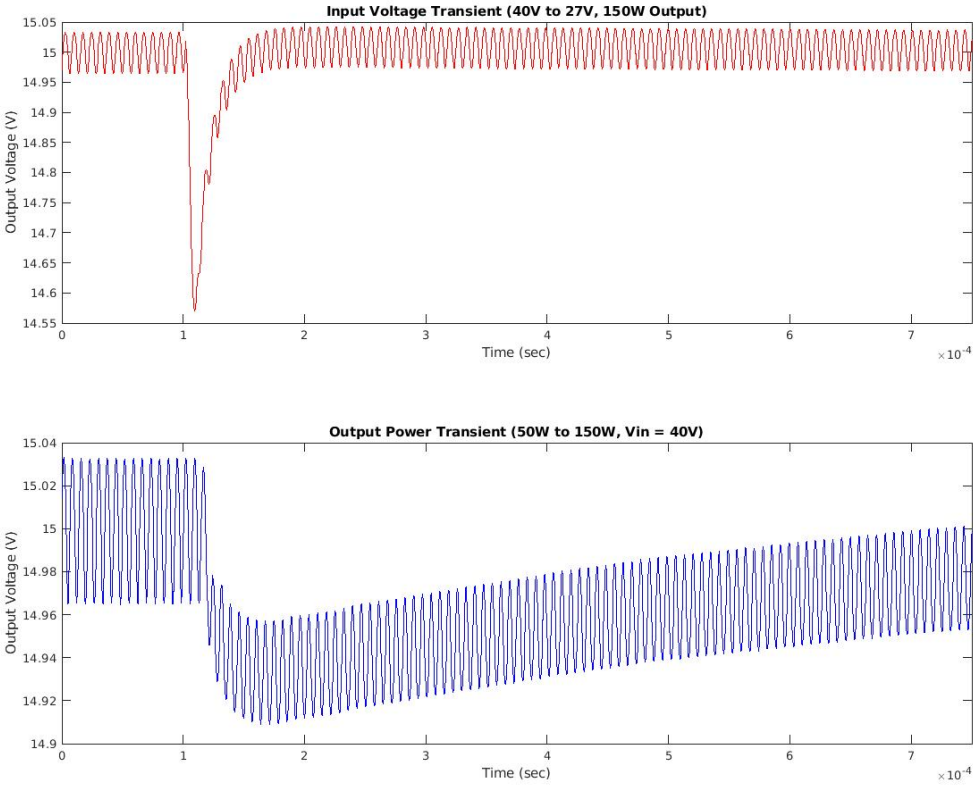


Figure 4: Output Response to Rising Input Voltage Step (27V to 40V, P_{out} = 150W)



5 Efficiency

The converter is rated for a minimum 94.5% efficiency across all input voltages and output powers (as all sources of loss are either invariant or increase with load - the inductor B field increases, the switches carry more current, etc.) The sources of loss are found to be:

Component	Loss Mechanism	Power Loss	Percentage of Total Loss
Q1	Conduction Loss	0.155 W	2.0%
Q2	Conduction Loss	0.155 W	2.0%
Q1	Switching Loss	0.520 W	6.7%
Q2	Switching Loss	0.520 W	6.7%
L_{out}	Core Loss	5.296 W	68%
L_{out}	Winding Loss	0.207 W	2.7%
L_{in}	Core Loss	0.841 W	11%
L_{in}	Winding Loss	0.094 W	1.2%
Total Loss	-	**7.788 W**	-
Efficiency (max power)	-	**94.8%**	-

6 Thermals

From these figures, a rough estimate of the converter's thermal requirements may be surmised. The switches and the inductors are the only components that dissipate power,

and their thermal resistances to ambient are 41° C/W for the switches and 19° C/W in the case of the RM14 core. With the maximum ambient temperature of 50°C and the dissipations given above, this corresponds to a temperature of 78°C at the switch junctions, 155°C at the center of L_{out}, and 68°C at the center of L_{in}. Given that this converter will likely be assembled on a PCB with some heat-sinking capacity, the slight overtemperature experienced by L_{out} under worst case conditions likely does not warrant a separate heatsink.