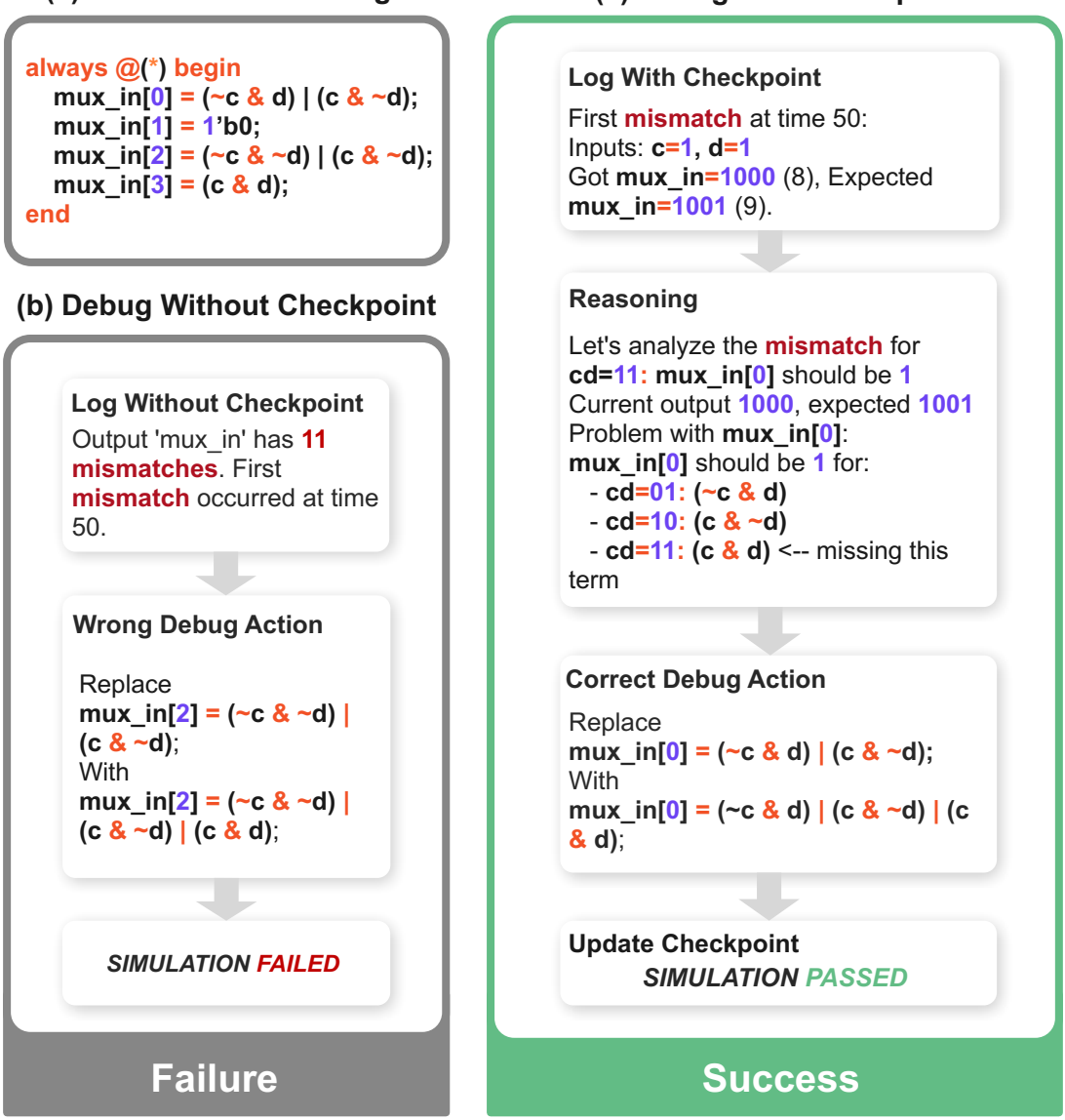
(a) RTL Module With Bugs
always @(*) begin
mux_in[0] = (~c & d) | (c & ~d);
mux_in[1] = 1'b0;
mux_in[2] = (~c & ~d) | (c & ~d);
mux_in[3] = (c & d);
end
(b) Debug Without Checkpoint
Log Without Checkpoint
Output 'mux_in' has 11 mismatches. First mismatch occurred at time 50.
Wrong Debug Action
Replace
mux_in[2] = (~c & ~d) | (c & ~d);
With
mux_in[2] = (~c & ~d) | (c & ~d) | (c & d);
SIMULATION FAILED
Failure
(c) Debug With Checkpoint
Log With Checkpoint
First mismatch at time 50:
Inputs: c=1, d=1
Got mux_in=1000 (8), Expected mux_in=1001 (9).
Reasoning
Let's analyze the mismatch for cd=11: mux_in[0] should be 1
Current output 1000, expected 1001
Problem with mux_in[0]:
mux_in[0] should be 1 for:
- cd=01: (~c & d)
- cd=10: (c & ~d)
- cd=11: (c & d) <-- missing this term
Correct Debug Action
Replace
mux_in[0] = (~c & d) | (c & ~d);
With
mux_in[0] = (~c & d) | (c & ~d) | (c & d);
Update Checkpoint
SIMULATION PASSED
Success