CVSD #hw6 Report

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1. Topic & timing/delay information

```
set cycle 10          ;#clock period defined by designer

#don't modify the following part
create_clock -period $cycle [get_ports  clk]
#new add
set_case_analysis 0 [get_ports {test_se}]

set_clock_uncertainty  0.1  [all_clocks]
set_clock_latency      0.5  [all_clocks]

#Don't touch the basic env setting as below
set_input_delay  1      -clock clk [remove_from_collection [all_inputs] [get_ports clk]]
set_output_delay 1      -clock clk [all_outputs]
set_load         1      [all_outputs]
set_drive        0.1    [all_inputs]

set_operating_conditions -max_library slow -max slow
set_wire_load_model -name tsmc13_wl10 -library slow

set_max_fanout 6 [all_inputs]
```

2. Synthesis reports & DFT-related reports (summarized)

- Area before dft

Number of ports:	45
Number of nets:	3383
Number of cells:	3228
Number of combinational cells:	2680
Number of sequential cells:	547
Number of macros/black boxes:	1
Number of buf/inv:	495
Number of references:	139
Combinational area:	29118.896981
Buf/Inv area:	4195.972800
Noncombinational area:	18019.598103
Macro/Black Box area:	69557.296875
Net Interconnect area:	352801.817993
Total cell area:	116695.791959
Total area:	469497.609952

- Timing before dft

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.50	0.50
u_sram/CLK (sram_1024x8_t13)	0.00	0.50 r
u_sram/Q[2] (sram_1024x8_t13)	1.51	2.01 f
U3896/Y (INVX20)	0.09	2.10 r
U3545/Y (NAND2X8)	0.08	2.18 f
U3897/Y (INVX20)	0.16	2.34 r
U2404/Y (NAND2X6)	0.10	2.44 f
U2405/Y (NAND4X6)	0.13	2.57 r
U2402/Y (NAND2X8)	0.09	2.65 f
U2931/Y (NAND4X8)	0.13	2.79 r
U2930/Y (XOR2X4)	0.16	2.94 r
U3546/Y (NAND3X8)	0.12	3.06 f
U2882/Y (NOR2X8)	0.15	3.21 r
U2886/Y (NOR2X8)	0.10	3.31 f
U2885/Y (INVX20)	0.08	3.39 r
U2919/Y (NAND2X8)	0.10	3.50 f
U2918/Y (INVX20)	0.09	3.58 r
U2974/Y (NAND2X8)	0.09	3.68 f
U2261/Y (NAND2X6)	0.10	3.77 r
U3456/Y (NOR2X6)	0.07	3.84 f
U2911/Y (NAND3X6)	0.09	3.93 r
R_1351/D (DFFRX4)	0.00	3.93 r
data arrival time		3.93
clock clk (rise edge)	10.00	10.00
clock network delay (ideal)	0.50	10.50
clock uncertainty	-0.10	10.40
R_1351/CK (DFFRX4)	0.00	10.40 r
library setup time	-0.17	10.23
data required time		10.23
data required time		10.23
data arrival time		-3.93
slack (MET)		6.30

- Area after dft

```
Number of ports:                   58
Number of nets:                  3794
Number of cells:                 3228
Number of combinational cells:   2680
Number of sequential cells:       547
Number of macros/black boxes:       1
Number of buf/inv:                495
Number of references:             143

Combinational area:       28738.679360
Buf/Inv area:              4195.972800
Noncombinational area:    22003.395603
Macro/Black Box area:     69557.296875
Net Interconnect area:   403948.786102

Total cell area:         120299.371838
Total area:              524248.157940
```

- Timing after dft

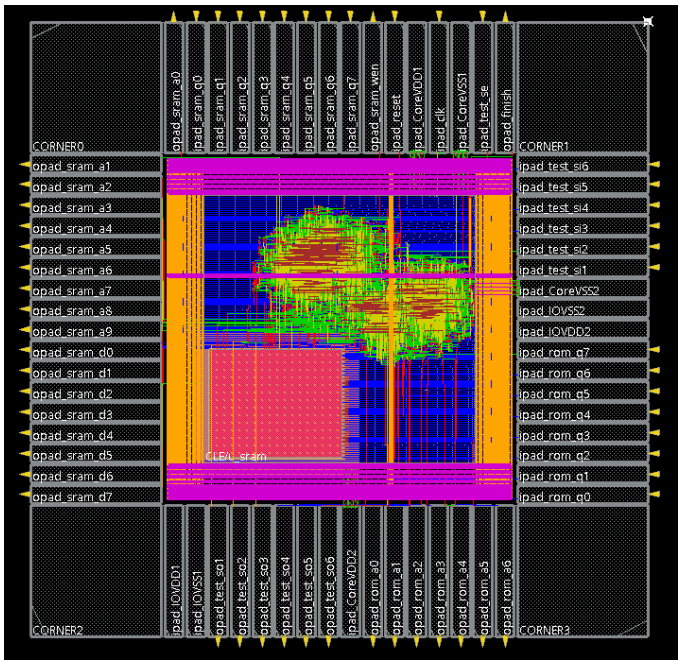
```
Point                                   Incr       Path
------------------------------------------------------------
clock clk (rise edge)                   0.00       0.00
clock network delay (ideal)             0.50       0.50
R_1486/CK (SDFFRXL)                     0.00       0.50 r
R_1486/Q (SDFFRXL)                      1.07       1.57 r
U3171/Y (NAND2X2)                       0.16       1.74 f
U71/Y (NAND3X1)                         0.54       2.28 r
U65/Y (NAND2XL)                         0.46       2.74 f
U3830/Y (NAND2X1)                       0.31       3.04 r
U3832/Y (NAND4X2)                       0.40       3.44 f
U2963/Y (NAND2X6)                       0.18       3.62 r
U1970/Y (NAND4X4)                       0.15       3.77 f
U3313/Y (NAND2X6)                       0.10       3.87 r
U2957/Y (NAND4X8)                       0.13       4.00 f
U2955/Y (XOR2X4)                        0.15       4.15 f
U2411/Y (NAND2X8)                       0.10       4.24 r
U2882/Y (NOR2X8)                        0.08       4.32 f
U2886/Y (NOR2X8)                        0.12       4.44 r
U2885/Y (INVX20)                        0.09       4.53 f
U2919/Y (NAND2X8)                       0.11       4.64 r
U2918/Y (INVX20)                        0.08       4.72 f
U2974/Y (NAND2X8)                       0.10       4.81 r
U2260/Y (INVX8)                         0.07       4.88 f
U72/Y (OAI2BB2XL)                       0.59       5.47 r
U3521/Y (NAND2X4)                       0.13       5.60 f
counter_y_r_reg[0]/D (SDFFRX1)          0.00       5.60 f
data arrival time                                  5.60

clock clk (rise edge)                  10.00      10.00
clock network delay (ideal)             0.50      10.50
clock uncertainty                      -0.10      10.40
counter_y_r_reg[0]/CK (SDFFRX1)         0.00      10.40 r
library setup time                     -0.38      10.02
data required time                                10.02
------------------------------------------------------------
data required time                                10.02
data arrival time                                 -5.60
------------------------------------------------------------
slack (MET)                                        4.42
```

從這邊可以明顯發現，插完 scan chain 後面積有變大。

3. Final chip layout figure & chip size

- Chip layout figure



- Chip Size

```
Average module density = 1.000.
Density for the design = 1.000.
       = stdcell_area 109869 sites (186492 um^2) / alloc_area 109869 sites (186492 um^2).
Pin Density = 0.08126.
            = total # of pins 12390 / total area 152481.
************************** Analyze Floorplan ***************************
    Die Area(um^2)             : 1348388.32
    Core Area(um^2)            : 258821.25
    Chip Density (Counting Std Cells and MACROs and IOs): 84.514%
    Core Density (Counting Std Cells and MACROs): 92.349%
    Average utilization        : 100.000%
    Number of instance(s)      : 11592
    Number of Macro(s)         : 1
    Number of IO Pin(s)        : 58
    Number of Power Domain(s) : 0
************************** Estimation Results **************************
************************************************************************
```

4. DRC & LVS Error

- Geometry

```
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
 *** verify geometry (CPU: 0:00:02.2  MEM: 269.1M)
```

- Connectivity

```
Begin Summary
  Found no problems or warnings.
End Summary

End Time: Mon Dec 24 22:36:46 2018
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.4  MEM: 8.812M)
```

- Antenna

```
******* START VERIFY ANTENNA ********
Report File: CHIP.antenna.rpt
LEF Macro File: CHIP.antenna.lef
Verification Complete: 0 Violations
******* DONE VERIFY ANTENNA ********
(CPU Time: 0:00:00.3  MEM: 0.461M)
```

5. Pre-layout & post-layout simulation results (summarized).

- Pre-layout (after dft)

Testfixture_a

```
----------------------------------------------------

               Simulation Summary

----------------------------------------------------

Congratulations! All data have been generated successfully!

------------------------PASS------------------------

err=   0
Simulation complete via $finish(1) at time 16489192 PS + 0
./pre_testfixture_a.v:208       #(`CYCLE/2); $finish;
ncsim> exit
```

Testfixture_b

```
----------------------------------------------------

               Simulation Summary

----------------------------------------------------

Congratulations! All data have been generated successfully!

------------------------PASS------------------------

err=   0
Simulation complete via $finish(1) at time 16617192 PS + 0
./pre_testfixture_b.v:209       #(`CYCLE/2); $finish;
ncsim> exit
```

Testfixture_c

```
----------------------------------------------------

               Simulation Summary

----------------------------------------------------

Congratulations! All data have been generated successfully!

------------------------PASS------------------------

err=   0
Simulation complete via $finish(1) at time 16089192 PS + 0
./pre_testfixture_c.v:209       #(`CYCLE/2); $finish;
ncsim> exit
```

- Post-layout (after dft)

Testfixture_a

```
----------------------------------------------------

               Simulation Summary

----------------------------------------------------

Congratulations! All data have been generated successfully!

------------------------PASS------------------------

err=   0
Simulation complete via $finish(1) at time 20614227 PS + 0
./testfixture_a.v:213       #(`CYCLE/2); $finish;
ncsim> exit
```

Testfixture_b

```
----------------------------------------------------

               Simulation Summary

----------------------------------------------------

Congratulations! All data have been generated successfully!

------------------------PASS------------------------

err=   0
Simulation complete via $finish(1) at time 20774227 PS + 0
./testfixture_b.v:212       #(`CYCLE/2); $finish;
ncsim> exit
```

Testfixture_c

```
----------------------------------------------------

               Simulation Summary

----------------------------------------------------

Congratulations! All data have been generated successfully!

------------------------PASS------------------------

err=   0
Simulation complete via $finish(1) at time 20114227 PS + 0
./testfixture_c.v:209       #(`CYCLE/2); $finish;
ncsim> exit
```

6. Complete power planning

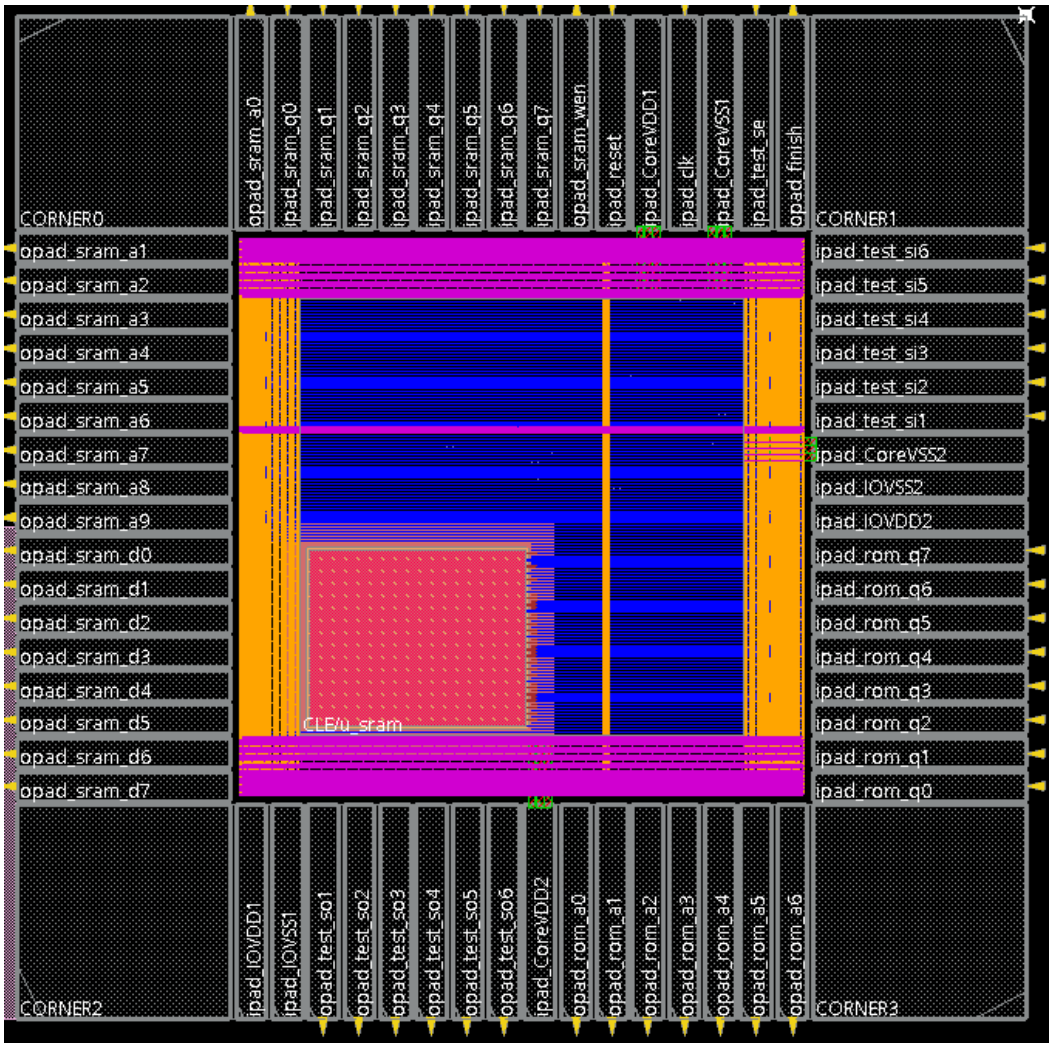
VDD/VSS/IOVDD/IOVSS 的數量沿用 LAB7 的設置：

VDD: 2, VSS: 2, IOVDD: 2, IOVSS: 2

Power ring 跟 LAB7 設置一樣：width 2, interleaving, 15 bits。

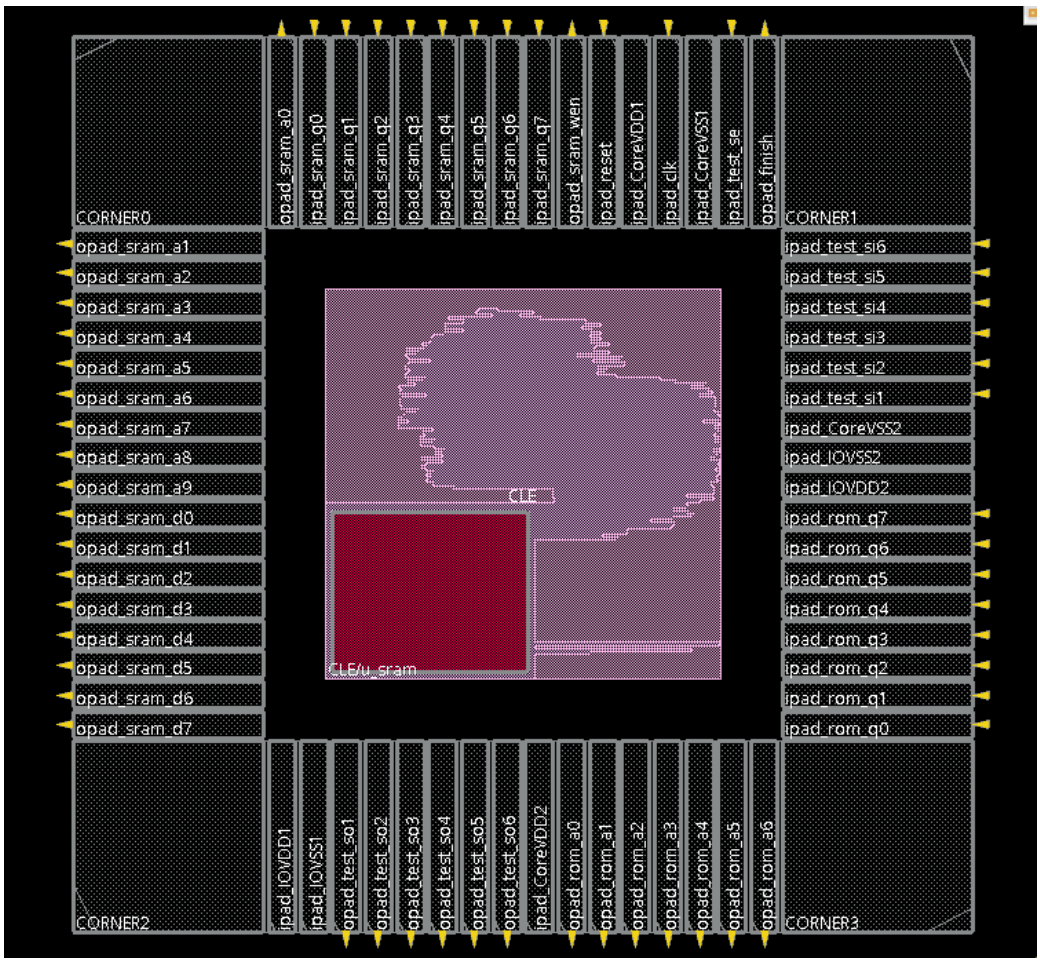
Power stripe 的部分，根據這次 sram 的位置，避開 sram 包含 Halo 的部分，讓 power stripe 不要壓到 sram，水平跟垂直的 start 都從 350 開始，stop 則是 100，distance 則是 100。

Power plan 如下圖：



7. Better I/O & modules' placement

為了讓繞線方便，在放 pad 的時候把 sram 的訊號都放在左邊，其他相近的訊號也盡量擺在一起；為了讓最後晶片的形狀維持在正方形，我把 66 個 pin 平均分在四邊，如下圖：



8. Other related discussions

a. 在設定 core utilization 的時候，可以設小一點，這樣會比較好繞。

b. Sram 擺放的位置和 pad 裡有關 sram 的出 pin 位置要盡量放在同側（如第七題所討論），不然繞線的時候很容易造成 short cut。

c. SDC 檔裡面有些合成適用的條件要記得關掉

```
#set_dont_touch_network      [all_clocks]
#set_fix_hold                [all_clocks]
#set_ideal_network           [get_ports clk]
```

然後為了讓 output 的 drive load 不要太大，我將 constraint 調寬：set_drive 設為 0.1

```
set_drive         0.1      [all_inputs]
```

d. 另外要注意的是一開始關於 library 的環境設定，我分別從 lab7 和 hw3 拿了 tsmc13fsg_8lm_cic.lef, tpz013g3_8lm_cic.lef, sram_1024x8_t13.vclef, antenna_8.lef 這些 lef 檔，接下來再把 lab7 的 mmmc 檔 include 的 sdc 改為這次作業所需，以及將 create_library_set 改成 sram 的 library。