# 1 MICROPROCESSOR AND ORGANISATION OF 8085

## INTRODUCTION

## EVOLUTION OF MICROPROCESSOR

Transistor was invented in 1948 (23 December 1947 in Bell lab). IC was invented in 1958 (Fair Child Semiconductors) By Texas Instruments J Kilby. The first microprocessor was invented by INTEL (Integrated Electronics).

**Size of the microprocessor – 4 bit**

| Name | Year of Invention | Clock speed | Number of transistors | Inst. per sec |
|---|---|---|---|---|
| INTEL 4004/4040 | 1971 by Ted Hoff and Stanley Mazor | 740 kHz | 2300 | 60,000 |

**Size of the microprocessor – 8 bit**

| Name | Year of Invention | Clock speed | Number of transistors | Inst. per sec |
|---|---|---|---|---|
| 8008 | 1972 | 500 kHz | 3500 | 50,000 |
| 8080 | 1974 | 2 MHz | 6000 | 10 times faster than 8008 |
| 8085 | 1976 (16-bit address bus) | 3 MHz | 6500 | 769230 |

**Size of the microprocessor – 16 bit**

| Name | Year of Invention | Clock speed | Number of transistors | Inst. per sec |
|---|---|---|---|---|
| 8086 | 1978 (multiply and divide instruction, 16-bit data bus and 20-bit address bus) | 4.77 MHz, 8 MHz, 10 MHz | 29000 | 2.5 Million |
| 8088 | 1979 (cheaper version of 8086 and 8-bit external bus) | | | 2.5 Million |
| 80186/80188 | 1982 (80188 cheaper version of 80186, and additional components like interrupt controller, clock generator, local bus controller, counters) | 6 MHz | | |
| 80286 | 1982 (data bus 16bit and address bus 24 bit) | 8 MHz | 134000 | 4 Million |

**Size of the microprocessor – 32 bit**

| Name | Year of Invention | Clock speed | Number of transistors | Inst. per sec |
|---|---|---|---|---|
| INTEL 80386 | 1986 (other versions 80386DX, 80386SX, 80386SL , and data bus 32-bit address bus 32 bit) | 16 MHz – 33 MHz | 275000 | |
| INTEL 80486 | 1986 (other versions 80486DX, 80486SX, 80486DX2, 80486DX4) | 16 MHz – 100 MHz | 1.2 Million transistors | 8 KB of cache memory |
| PENTIUM | 1993 | 66 MHz | | Cache memory 8 bit for instructions 8 bit for data |

**Size of the microprocessor – 64 bit**

| Name | Year of Invention | Clock speed | Number of transistors | Inst. per sec |
|---|---|---|---|---|
| INTEL core 2 | 2006 (other versions core2 duo, core2 quad, core2 extreme) | 1.2 GHz to 3 GHz | 291 Million transistors | 64 KB of L1 cache per core 4 MB of L2 cache |
| i3, i5, i7 | 2007, 2009, 2010 | 2.2GHz – 3.3GHz, 2.4GHz – 3.6GHz, 2.93GHz – 3.33GHz | | |

**Generations of microprocessors:**

1. **First-generation –**
   From 1971 to 1972 the era of the first generation came which brought microprocessors like INTEL 4004 Rockwell international PPS-4 INTEL 8008 etc.
2. **Second generation –**
   The second generation marked the development of 8-bit microprocessors from 1973 to 1978. Processors like INTEL 8085 Motorola 6800 and 6801 etc came into existence.
3. **Third generation –**
   The third generation brought forward the 16-bit processors like INTEL 8086/80186/80286 Motorola 68000 68010 etc. From 1979 to 1980 this generation used the HMOS technology.

4. **Fourth generation –**
   The fourth-generation came into existence from 1981 to 1995. The 32-bit processors using HMOS fabrication came into existence. INTEL 80386 and Motorola 68020 are some of the popular processors of this generation.

5. **Fifth-generation –**
   From 1995 till now we are in the fifth generation. 64-bit processors like PENTIUM, Celeron, dual, quad, and octa-core processors came into existence.

**What is microprocessor?**

Microprocessor is a controlling unit of a micro-computer, fabricated on a small chip capable of performing ALU (Arithmetic Logical Unit) operations and communicating with the other devices connected to it.

Microprocessor consists of an ALU, register array, and a control unit. ALU performs arithmetical and logical operations on the data received from the memory or an input device. Register array consists of registers identified by letters like B, C, D, E, H, L and accumulator. The control unit controls the flow of data and instructions within the computer.

Microprocessor is a logical multipurpose and multiprogrammable device that reads binary instruction from the memory and accepts binary data as input and processes the data as per the instruction.

**Features of a Microprocessor**

Here is a list of some of the most prominent features of any microprocessor –

- **Cost-effective** – The microprocessor chips are available at low prices and results its low cost.
- **Size** – The microprocessor is of small size chip, hence is portable.
- **Low Power Consumption** – Microprocessors are manufactured by using metaloxide semiconductor technology, which has low power consumption.
- **Versatility** – The microprocessors are versatile as we can use the same chip in a number of applications by configuring the software program.
- **Reliability** – The failure rate of an IC in microprocessors is very low, hence it is reliable.
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**GENERIC MICROPROCESSOR**

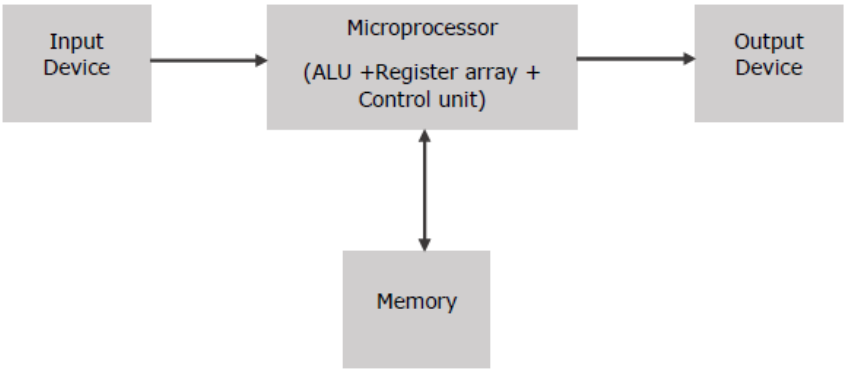



**Fig:** Generic diagram

CPU: Central processing unit

ALU: Arithmetic logic unit

REG: register

**1) CPU: Central processing unit**

CPU is the brain of your computer system. It's function is to execute the program and control the operations of all the components of the computer system.

**2) ALU: Arithmetic logic unit**

It performs all the arithmetic and logical calculations. It is used to perform mathematical operations like: addition, multiplication, subtraction, division, decrement, increment, etc.

**3) Timing and Control unit**

It generates control signals necessary for execution of instructions. It controls the entire operation of the computer system. Timing signals are provided for operations to be performed by other parts of your computer system.

**4) REG: Register**

Accumulator is used to perform input-output, arithmetic and logical operations. It is connected to ALU and internal data bus.

General purpose registers: There are 6 general purpose registers which hold 8 bit values. These 8 bit registers are B,C,D,E,H and L. These registers work as 16-bit registers when they work in pair like B-C, D-E, H-L.

**How does a Microprocessor Work?**

The microprocessor follows a sequence: Fetch, Decode, and then Execute.

Initially, the instructions are stored in the memory in a sequential order. The microprocessor fetches those instructions from the memory, then decodes it and executes those instructions till STOP instruction is reached. Later, it sends the result in binary to the output port. Between these processes, the register stores the temporarily data and ALU performs the computing functions.

**List of Terms Used in a Microprocessor**

Here is a list of some of the frequently used terms in a microprocessor –

- **Instruction Set** – It is the set of instructions that the microprocessor can understand.
- **Bandwidth** – It is the number of bits processed in a single instruction.

- **Clock Speed** – It determines the number of operations per second the processor can perform. It is expressed in megahertz (MHz) or gigahertz (GHz).It is also known as Clock Rate.
- **Word Length** – It depends upon the width of internal data bus, registers, ALU, etc. An 8-bit microprocessor can process 8-bit data at a time. The word length ranges from 4 bits to 64 bits depending upon the type of the microcomputer.
- **Data Types** – The microprocessor has multiple data type formats like binary, BCD, ASCII, signed and unsigned numbers.
-

**THE 8085 MICROPROCESSOR**

The 8085A is a NMOS chip with 40 pin package and it is an 8–bit microprocessor suitable for a wide range of applications and it is ideal microprocessor to study because its basic architecture is used in more advanced microprocessors. The Intel's microprocessor 8085 chip has selected to understand hardware of the common microprocessor and to illustrate and to illustrate the assembly language program.

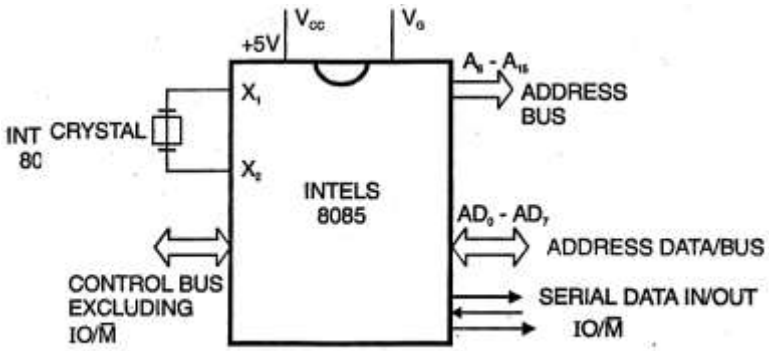



**Fig. Microprocessor 8085**

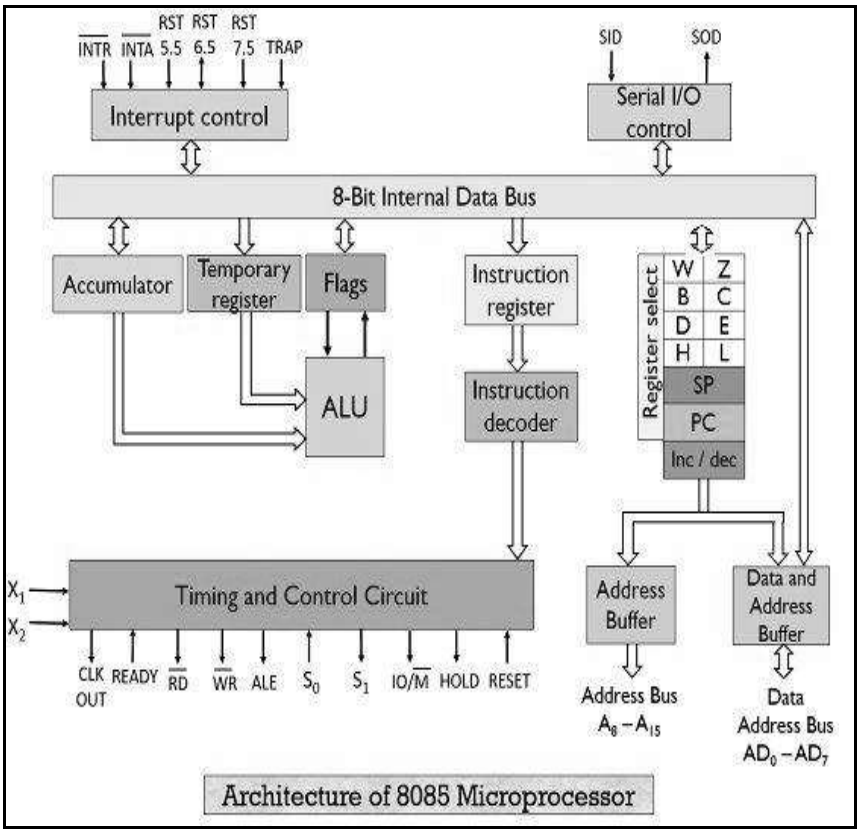
**FEATURES OF 8085**

1. The Intel microprocessor 8085 is an 8–bit microprocessor 8–bit data bus width. This indicates that 1 byte (8–bit) data can be transferred on this bus.
2. This 8085 chip is available in a 40 pin plastic ceramic (DIP) package.
3. The address bus is 16–bit that means it can address 64 K bytes. The address bus is divided into two groups as

   (a) The least significant bits of address are transmitted on the same eight lines of the data bus therefore it is called of data/address bus. This method of using common eight lines for both data and address transmission is known as "multiplexed bus", (multiplexer means many into one here it is two into one).
   The advantage of multiplexed bus is no of pins are minimised from 16 to 8.

   (b) Most significant bits of address are transmitted on address bus ($A_8$ –$A_{15}$). Since microprocessor 8085 has 16 bit = ($2^{16}$) = 64 Kbytes memory locations can be accessed. Each memory location is of 1 byte that is 8–bit wide. In 8085 to select external memory or I/O device, I/O mapped, I/O system is used.
4. The instruction set of 8085 consists of 74 instructions.

**INTERNAL BLOCK DIAGRAM OF 8085 MICROPROCESSOR**




**1) Three Bus Structure**

There are 2 I/O bus as 8-bit data bus($D_0$-$D_7$) and 16 bit address bus (A0-A15). $AD_0$-$AD_7$ bus is address/data multiplexed bus and $A_8$-$A_{15}$ are only functioning as address bus. Address bus carries address in one direction i.e from CPU to RAM(unidirectional). The main purpose of address bus is to find the address of the memory location where the data has to be written or read from. The multiplexed address and data bus carries both data as well as address from and to the CPU and various other components hence it is bidirectional.

Control bus is not labelled in the diagram but various control signals are transferred to different blocks.

**2) Registers**

There are different registers used for different purposes as

**I) 8- bit General purpose registers**

| | | |
|---|---|---|
| 1. | Accumulator | 8 bit |
| 2. | Register - B | 8 bit |
| 3. | Register - C | 8 bit |
| 4. | Register - D | 8 bit |

| | | |
|---|---|---|
| 5. | Register - E | 8 bit |
| 6. | Register - H | 8 bit |
| 7. | Register - L | 8 bit |
| 8. | Temporary Register | 8 bit |
| 9. | Flag Register | 8 bit |

Accumulator along with flag register is known as Program Status Word(PSW)

**II) 16-Bit Special Registers**

| | | |
|---|---|---|
| 1. | Program Counter | 16 bit |
| 2. | Stack Pointer | 16 bit |
| 3. | Increment-Decrement | 16 bit |

Here register B,C,D,E,H and L can be used as 16-bit registers in pairs as register pair B-C, register D-E, register pair H-L.

**Note: 16 bit register pair cannot be used as B-E or D-L.**

1) **Accumulator:** Accumulator is used to perform I/O operations , arithmetic operations like addition, subtraction etc and logical operations like AND, EX-OR etc. One of the operands is stored in accumulator. It is connected to ALU and internal data bus.
2) **General purpose registers:** There are 6 8-bit general purpose registers. These registers can hold 8 bit values. These 8-bit registers are B,C,D,E,H,L. These registers work as 16-bit registers when they work in pair like: B-C, D-E, H-L. The higher MSB 8-bits are stored in first register from the register pair i.e B,D,H and lower LSB 8-bits are stored in other register from the register pair i.e. C,E,L.
   Example: A number C050H is to be stored in D-E register pair then C0 is stored in register D and number 50 will be stored in register E.
   NUMBER: C050H

| | |
|---|---|
| C0 (MSB: MOST SIGNIFICANT BIT) | 50 (LSB: LEAST SIGNIFICANT BIT) |

REGISTER PAIR: D-E

| | |
|---|---|
| C0 (Stored in register D) | 50 (Stored in register E) |

While using these memory locations in assembly language programs they have to be written in the opcode list as 50C0 because the processor reads the LSB bit first and then the MSB bit.

3) **Temporary Register:** The temporary register is the 8-bit register that holds data values during arithmetic and logical operations.

### III) ARITHMETIC LOGIC UNIT (ALU)

It is an 8–bit unit where arithmetic and logical operations are carried out. The ALU consists of binary adder it performs only binary addition and subtraction by the 2's complement addition method. Accumulator, I/O device, memory etc, supplies data. After performing the operation it sets the flags according to the nature of resulting answer. If answer is zero then it sets zero (Z) flag. Detail explanation of flags is given below.

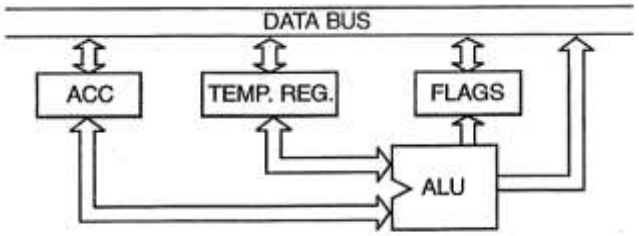



**Fig. (1.8) ALU Circuit**

### IV) FLAGS

These are single bit status registers (Flip–flops) operated by ALU. The flags are either set or reset according to the answer produced by ALU. It is important because flags are examined in conditional instructions like "JMP" and "CALL".

There are five flags:

1) Sign Flag (S), 2) Zero flag (Z), 3) Auxiliary carry Flag (AC),
4) Parity Flag (P), 5) Carry Flag (CY),

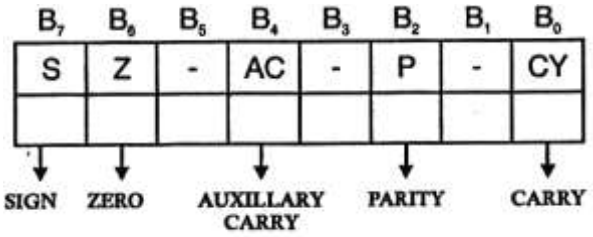



**Fig. (1.9) Flag Register**

| **Condition and Code** | | **Flag 0 = Reset, 1 = Set** |
|---|---|---|
| Not Zero | (NZ) | Z = 0 |
| Zero | (Z) | Z = 1 |
| No carry | (NC) | CY = 0 |
| Carry present | (C) | CY = 1 |
| Parity Odd | (PO) | P = 0 |
| Parity Even | (PE) | P = 1 |
| Plus | (P) | S = 0 **and when $D_7$ bit of Acc = 0** |
| Minus | (M) | S = 1 **and when $D_7$ bit of Acc = 1** |

With instruction STC carry flag is directly set. In table illustrates different conditions of ALU result and in status of flags affected.

After execution of arithmetic operation programs status word (PSW) is formed. It contains accumulator with flag.

**V) PROGRAM COUNTER (PC)**

Program Counter holds the address value of the memory to the next instruction that is to be executed. It is a 16-bit register.

**For Example:** Suppose current value of Program Counter : [PC] = 4000H

(It means that next executing instruction is at location 4000H.After fetching, program counter(PC) always increments by +1 for fetching of next instruction.) So after increment the value of program counter will be 4001H.

**VI) STACK POINTER (SP)**

It works like a stack. In stack, the content of the register is stored that is later used in the program. It is a 16-bit special register. The stack pointer is part of memory but it is part of Stack operations, unlike random memory access. Stack pointer works in a continuous and contiguous part of the memory. Whereas Program Counter(PC) works in random memory locations. This pointer is very useful in stack-related operations like **PUSH, POP, and nested CALL requests** initiated by Microprocessor. It reserves the address of the most recent stack entry.

**VII) INCREMENT-DECREMENT**

It is a 165 bit register. It is used to add or subtract 1 from the contents of the program counter or the stack pointer.

**VIII) INSTRUCTION DECODER**

It is a 8-bit register that holds the instruction code that is being decoded. The instruction is fetched from the memory.

**XI) TIMING AND CONTROL UNIT**

The timing and control unit comes under the CPU section, and it controls the flow of data from the CPU to other devices. It is also used to control the operations performed by the microprocessor and the devices connected to it. There are certain timing and control signals like Control signals, DMA Signals, RESET signals and Status signals.

**X) INTERRUPT CONTROL:**

Whenever a microprocessor is executing the main program and if suddenly an interrupt occurs, the microprocessor shifts the control from the main program to process the incoming request. After the request is completed, the control goes back to the main program. There are 5 interrupt signals in 8085 microprocessors: INTR, TRAP, RST 7.5, RST 6.5, and RST 5.5.

**Priorities of Interrupts:** TRAP > RST 7.5 > RST 6.5 > RST 5.5 > INTR

**INTERRUPTS**

Whenever a microprocessor is executing the main program and if suddenly an interrupt occurs, the microprocessor shifts the control from the main program to process the incoming request. After the request is completed, the control goes back to the main program.

There are 5 interrupt signals in 8085 microprocessors: INTR, TRAP, RST 7.5, RST 6.5, and RST 5.5.

1. **TRAP:** The TRAP interrupt is a non-maskable interrupt that is generated by an external device, such as a power failure or a hardware malfunction. The TRAP interrupt has the highest priority and cannot be disabled.
2. **RST 7.5:** The RST 7.5 interrupt is a maskable interrupt that is generated by a software instruction. It has the second highest priority.
3. **RST 6.5:** The RST 6.5 interrupt is a maskable interrupt that is generated by a software instruction. It has the third highest priority.
4. **RST 5.5:** The RST 5.5 interrupt is a maskable interrupt that is generated by a software instruction. It has the fourth highest priority.
5. **INTR:** The INTR interrupt is a maskable interrupt that is generated by an external device, such as a keyboard or a mouse. It has the lowest priority and can be disabled.

**Interrupts can be classified into various categories based on different parameters:**

**Category 1: Hardware and Software interrupts**

**1) Hardware interrupt**

When microprocessors receive interrupt signals through pins (hardware) of microprocessor, they are known as Hardware Interrupts. There are 5 Hardware Interrupts in 8085 microprocessor. They are – INTR, RST 7.5, RST 6.5, RST 5.5, TRAP.

**2) Software interrupt**

Software Interrupts are those which are inserted in between the program which means these are mnemonics of microprocessor. There are 8 software interrupts in 8085 microprocessor. They are – RST 0, RST 1, RST 2, RST 3, RST 4, RST 5, RST 6, RST 7.

**Category 2: Vectored and Non-vectored interrupts**

**1) Vectored Interrupts**

Vectored Interrupts are those which have fixed vector address (starting address of sub-routine) and after executing these, program control is transferred to that address.

| INTERRUPT | VECTOR ADDRESS |
|---|---|
| TRAP (RST 4.5) | 24 H |
| RST 5.5 | 2C H |
| RST 6.5 | 34 H |
| RST 7.5 | 3C H |

For Software interrupts vector addresses are given by:

| INTERRUPT | VECTOR ADDRESS |
|---|---|
| RST 0 | 00 H |
| RST 1 | 08 H |
| RST 2 | 10 H |
| RST 3 | 18 H |
| RST 4 | 20 H |
| RST 5 | 28 H |
| RST 6 | 30 H |
| RST 7 | 38 H |

**2) Non-vectored interrupts**

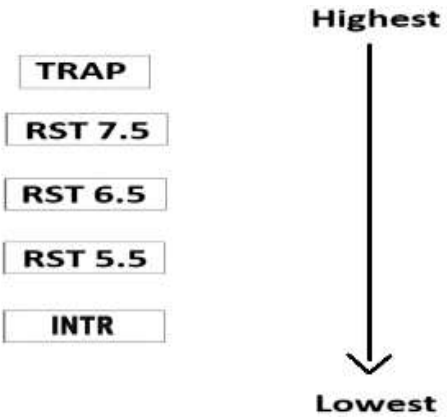
Non-Vectored Interrupts are those in which vector address is not predefined. The interrupting device gives the address of sub-routine for these interrupts. INTR is the only non-vectored interrupt in 8085 microprocessor.

**Category 3: Maskable and Non-Maskable Interrupts**

**1) Maskable Interrupts -** Maskable Interrupts are those which can be disabled or ignored by the microprocessor. These interrupts are either edge-triggered or level-triggered, so they can be disabled. INTR, RST 7.5, RST 6.5, RST 5.5 are maskable interrupts in 8085 microprocessor.

**2) Non-Maskable Interrupts- Non-Maskable Interrupts** are those which cannot be disabled or ignored by microprocessor. TRAP is a non-maskable interrupt. It consists of both level as well as edge triggering and is used in critical power failure conditions.

**Priority of Interrupts –** When microprocessor receives multiple interrupt requests simultaneously, it will execute the interrupt service request (ISR) according to the priority of the interrupts.




**FUNCTIONAL PIN DIAGRAM OF 8085 MICROPROCESSOR**

The pin diagram of 8085 is illustrated by fig. (1.4) and its brief functional description is given in table

1) $A_{D0}$–$A_{D7}$ – As shown in the pin diagram of 8085 has address/data multiplexed bus pins $A_{D0}$–$A_{D7}$ and other address bus pins are $A_8$–$A_{15}$.
2) +Vcc and Vss– Supply connections are given across pins + Vcc and Vss ground + 5V fixed.

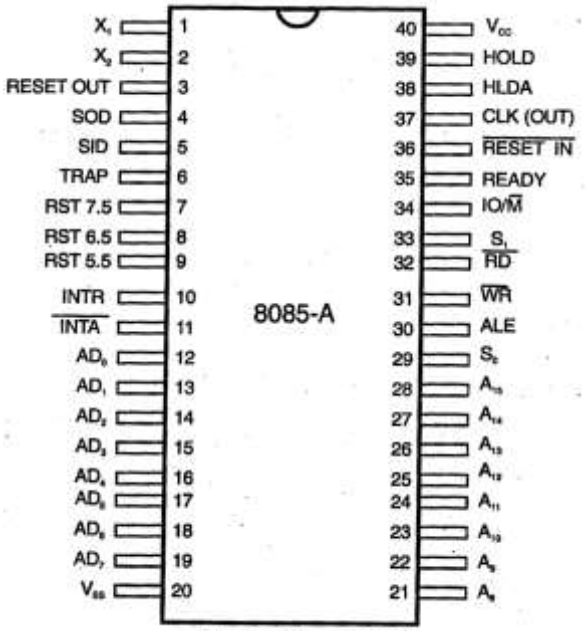



**Fig. Pin Diagram of 8085**

The pins of a 8085 microprocessor can be classified into seven groups –

**Address bus**

$A_8$-$A_{15}$ it carries the most significant 8-bits of memory/IO address.

**Data bus**

$AD_0$-$AD_7$, it carries the least significant 8-bit address and data bus.

**Control and status signals**

These signals are used to identify the nature of operation. There are 3 control signal and 3 status signals.

Three control signals are RD, WR & ALE.

- **RD** – This signal indicates that the selected IO or memory device is to be read and is ready for accepting data available on the data bus.
- **WR** – This signal indicates that the data on the data bus is to be written into a selected memory or IO location.
- **ALE** – It is a positive going pulse generated when a new operation is started by the microprocessor. When the pulse goes high, it indicates address. When the pulse goes down it indicates data.

**Three status signals are IO/M, S0 & S1.**

**IO/M**

This signal is used to differentiate between IO and Memory operations, i.e. when it is high indicates IO operation and when it is low then it indicates memory operation.

**S1 & S0**

These signals are used to identify the type of current operation.

**Power supply**

There are 2 power supply signals – VCC & VSS. VCC indicates +5v power supply and VSS indicates ground signal.

**Clock signals**

There are 3 clock signals, i.e. X1, X2, CLK OUT.

- **X1, X2** – A crystal (RC, LC N/W) is connected at these two pins and is used to set frequency of the internal clock generator. This frequency is internally divided by 2.
- **CLK OUT** – This signal is used as the system clock for devices connected with the microprocessor.

**Interrupts & externally initiated signals**

Interrupts are the signals generated by external devices to request the microprocessor to perform a task. There are 5 interrupt signals, i.e. TRAP, RST 7.5, RST 6.5, RST 5.5, and INTR. We will discuss interrupts in detail in interrupts section.

- **INTA** – It is an interrupt acknowledgment signal.
- **RESET IN** – This signal is used to reset the microprocessor by setting the program counter to zero.
- **RESET OUT** – This signal is used to reset all the connected devices when the microprocessor is reset.
- **READY** – This signal indicates that the device is ready to send or receive data. If READY is low, then the CPU has to wait for READY to go high.
- **HOLD** – This signal indicates that another master is requesting the use of the address and data buses.
- **HLDA (HOLD Acknowledge)** – It indicates that the CPU has received the HOLD request and it will relinquish the bus in the next clock cycle. HLDA is set to low after the HOLD signal is removed.

**Serial I/O signals**

There are 2 serial signals, i.e. SID and SOD and these signals are used for serial communication.

- **SOD** (Serial output data line) – The output SOD is set/reset as specified by the SIM instruction.
- **SID** (Serial input data line) – The data on this line is loaded into accumulator whenever a RIM instruction is executed.

**ADDRESSING MODES IN 8085**

The way of specifying data to be operated by an instruction is called addressing mode.

The 8085 microprocessor has several addressing modes that are used to access memory locations. Some of the most commonly used addressing modes in the 8085 microprocessor are:

**1) Immediate Addressing Mode**

In this addressing mode, the data on which the operation is to be performed is mentioned in the instruction. Instead of specifying an address, the instruction specifies an operand along with the operation that is to be performed. The instruction is 2 bytes when there is 8-bit data and 4 bytes when there is 16-bit data.

Examples of instructions that use immediate addressing mode are:

**MVI B 05 –** This instruction transfers the immediate data, that is 05, to register B.

**2) Register Addressing Mode**

In this addressing mode, the instruction mentions a register which stores some data. The operation specified by the instruction is performed in the register specified by it. The instruction can also specify two registers. The size of the instructions in register addressing mode is 1 byte. The instruction's opcode includes both the register and the operation to be performed.

Examples of instructions that use register addressing mode are:

**ADD B –** This instruction adds the data within register B with the data in the accumulator and stores the result in the accumulator.
**INR B –** This instruction increases the data stored in register B by 1.
**MOVE B, D –** This instruction moves the content of register D to register.
Therefore the operation is performed within various registers of the microprocessor.

**3) Direct addressing mode**

In this addressing mode, the instruction specifies some address which stores the data. This memory location is mentioned in the instruction as an operand. The size of an instruction in the direct addressing mode is 3 bytes. However, input/output instructions in direct addressing mode are 2 bytes.

Examples of instructions that use direct addressing mode are:

**IN 35 –** This instruction reads the data from a port. The address of the port is 35.

**LHLD address –** This instruction loads the data stored in the memory location specified by 'address' into the HL pair.

**LDA 2050 –** This instruction stores the contents of the memory location 2050H into the accumulator.

**STA 2050 –** This instruction stores the contents of the accumulator in the memory location 2050H.

**4) Register Indirect addressing mode**

In this addressing mode, the data on which the operation is to be performed is stored in some memory location. This memory location is specified in a register pair. The instruction then specifies this register pair.
Examples of instructions that use register indirect addressing mode are:

**LDAX B –** This instruction loads the contents stored in the memory location specified by the register pair BC into the accumulator.

**LXIH 9500 –** This instruction stores the address '9500' into the HL pair.

**MOV A, M –** This instruction moves the contents stored in the address specified by the HL pair into the accumulator.

**5) Implied/Implicit addressing mode**

In this addressing mode, the operand is described implicitly in the definition of the instruction. The operand is specified with the opcode of the instruction. The size of an implied addressing mode instruction is 1 byte. The instructions generally operate on data stored in the accumulator.

Examples of instructions that use implied addressing mode are as follows:

**RRC –** This instruction rotates the contents of the accumulator to the right by one bit.

**RLC –** This instruction rotates the contents of the accumulator to the left by one bit.

**CMA –** This instruction complements the content stored in the accumulator. The result is then stored in the accumulator itself.

## Exercise

**Select the correct alternative and rewrite the following.**

**1.** Microprocessor 8085 is manufactured by _____
(i) Motorola (ii) Toshiba (iii) Intel (iv) Z ilog
**1.** (iii)

**2.** 8085 uses _____V power supply
(i) +5 (ii) –5 (iii) +12 (iv) –12
**2.** (i)

**3.** There are _____ flags in 8085.
(i) 8 (ii) 2 (iii) 3 (iv) 5
**3.** (iv)

**4.** The register in the CPU that keeps track of the address of the next instruction to be fetched from program memory is called the_____
(i) Program counter (ii) Instruction register
(iii) Accumulator (iv) Stack pointer
**4.** (i)

**5.** Intel 4004 is _____ bit microprocessor.
(i) 4 (ii) 44 (iii) 8 (iv) 16
**5.** (i)

**6.** In the flag register of 8085 microprocessor _____ number of bits are kept unused.
(i) 5 (ii) 3 (iii) 4 (iv) 2
**6.** (ii)

**7.** The invalid register pair for 8085 microprocessor is _____
(i) BC (ii) HL (iii) SP (iv) DE
**7.** (iii)

**8.** The crystal frequency of 8085 is _____ and operating frequency is _____.
(i) 6MHz, 5 MHz (ii) 3 MHz, 6 MHz (iii) 6 MHz, 3MHz (iv) 5 MHz, 5 MHz
**8.** (iii)

**9.** After execution of an arithmetic instruction, the flag register of 8085 contains 04 H. This means that the result is _____.
(i) Positive (ii) Negative (iii) Floating (iv) None of these
**9.** (i)

**10.** CPU generally contains storage device called _____
(i) Registers (ii) ALU
(iii) Timing and control (iv) Counter
**10.** (i)

**11.** _____ is not a vectored interrupt.
(i) Trap (ii) INTR (iii) RST 7.5 (iv) RST 6.5
**11.** (ii)

**12.** In 8085 microprocessor, serial data from external device is received on _____pin.
(i) SID (ii) SOD (iii) HOLD (iv) READY
**12.** (i)

**13.** _____flag bit is reset, when flag resister content is D4H.
(i) S (ii) Z (iii) CY (iv) AC
**13.** (iii)

**14.** _____ register of 8085 is only used during arithmetical and logical operations and not for any other purpose.
(i) ACC (ii) B (iii) TEMP (iv) SP
**14.** (iii)

**15.** In the flag register of 8085 microprocessor _____ number of bits are kept unused.
(i) 5 (ii) 3 (iii) 4 (iv) 2
**15.** (ii)

**16.** In 8085 microprocessor, serial data from external device is received on _____ pin.
(i) SID (ii) SOD (iii) HOLD (iv) READY
**16.** (i)

**17.** _____ is not a vectored interrupt.
(i) Trap (ii) INTR (iii) RST 7.5 (iv) RST 6.5
**17.** (ii)

**18.** Usually operating frequency of 8085 is _____
(i) 3 MHZ (ii) 100 MHz (iii) 1 MHz (iv) 20 MHz
**18.** (i)

**19.** The invalid register pair for 8085 micro–processor is _____
(i) BC (ii) HL (iii) SP (iv) DE
**19.** (iii)

**20.** _____ flag bit is reset, when flag resister content is D4H.
(i) S (ii) Z (iii) CY (iv) AC
**20.** (iii)

**21.** _____ register of 8085 is only used during arithmetical and logical operations and not for any other purpose.
(i) ACC (ii) B (iii) TEMP (iv) SP
**21.** (iii)

**22.** _____ is a 32 bit microprocessor.
(i) 8086 (ii) 80386 (iii) Intel Pentium (iv) M68000
**22.** (ii)

**23.** _____ bus is one way data path from MPU to all devices.
(i) Data (ii) Address (iii) Control (iv) None of these
**23.** (ii)

**24.** TRAP is a non–maskable interrupt with _____priority.
(i) highest (ii) lowest (iii) intermediate (iv) no
**24.** (i)

**25.** In case of 8085 microprocessor, data bus between ALU and accumulator is _____.
(i) Bidirectional
(ii) Unidirectional
(iii) Either Unidirectional or Bidirectional
(iv) Neither Unidirectional nor Bidirectional
**25.** (i)

**26.** _____ is Non–maskable Interrupt.
(i) TRAP (ii) RST 7.5 (iii) RST 6.5 (iv) RST 5.5
**26.** (i)

**27.** Micro–processor 8085 belongs to _____ Company.
(i) Motorla (ii) Zilong (iii) Intel (iv) Toshiba
**27.** (iii)

**28.** In 8085 Microprocessor, serial data is outputted to the external device through ____ pin.
(i) SID (ii) SOD (iii) $S_0$ (iv) $S_1$
**28.** (iii)

**29.** In 8085 Microprocessor, _____ pin is the only output terminal interrupt control block.
(i) TRAP (ii) IN IR (iii) RST 7.5 (iv) INTA
**29.** (iv)

**30.** _____ pin of Micro–processor 8085 in never tr. Stated.
(i) SOD (ii) READY (iii) ALE (iv) HOLD
**30.** (iii)

**31.** ALU is _____ bit unit in 8085 Microprocessor.
(i) 8 (ii) 16 (iii) 32 (iv) 64
**31.** (i)

**32.** Micro–processor T 8190 is a _____ bit Micro–processor.
(i) 4 (ii) 8 (iii) 12 (iv) 16
**32.** (iii)

**33.** _____ pin of 8085 MPU is multiplexed.
(i) $IO/\overline{M}$ (ii) HOLD (iii) SID (iv) ALE
**33.** (i)

**34.** There are _____ flags in Micro–processor 8085.
(i) 8 (ii) 6 (iii) 5 (iv) 16
**34.** (iii)

**35.** Micro–processor 8085 has_____ bit wide data bus.
(i) 8 (ii) 16 (iii) 32 (iv) 64
**35.** (i)

**36.** _____ is used to store 8 bit opcode is 8085.
(i) IR (ii) PC (iii) SP (iv) Accumulator
**36.** (i)

**37.** In 8085 Microprocessor _____Pin in used for demultiplexing of address/data bus.
(i) $S_0$ (ii) ALE (iii) $IO/\overline{M}$ (iv) HOLD
**37.** (ii)

**38.** When RST 7.5 vector interrupt is activated in 8085 microprocessor the control is transferred to _____.
(i) 0024 H (ii) 002C H (iii) 0034 H (iv) 003C H
**38.** (iv)

**39.** The flag register of 8085 microprocessor contains _____ flags.
(i) 8 (ii) 3 (iii) 7 (iv) 5
**39.** (iv)

**40.** In CPU, the register which keeps the track of address of next instruction to be fetched is called _____.
(i) Instruction Register (ii) Program Counter
(ii) Stack Pointer (iv) Accumulator
**40.** (ii)

**41.** Intel 8085 is a/an _____ bit Microprocessor.
(i) 16 (ii) 4 (iii) 8 (iv) 32
**41.** (iii)

**42.** Stack pointer of 8085 holds _____
(i) 8 bit address (ii) 16 bit data (iii) 16 bit address (iv) 8 bit data
**42.** (iii)

**43.** Microprocessor 8085 is manufactured by _____.
(i) Intel (ii) Motorola (iii) Zilog (iv) Toshiba
**43.** (i)

**44.** _____ bits of flag register of 8085 Microprocessor are unused.
(i) 1 (ii) 2 (iii) 3 (iv) 4
**44.** (iii)

**45.** The register in 8085 Microprocessor that keeps the track of the address of next executable instruction is _____.
(i) Program Counter (ii) Stack Pointer
(iii) Program Status Word (iv) Instruction Register
**45.** (i)

**46.** _____ is non–maskable interrupt in 8085.
(i) RST 5.5 (ii) RST 6.5 (iii) RST 7.5 (iv) TRAP
**46.** (iv)

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