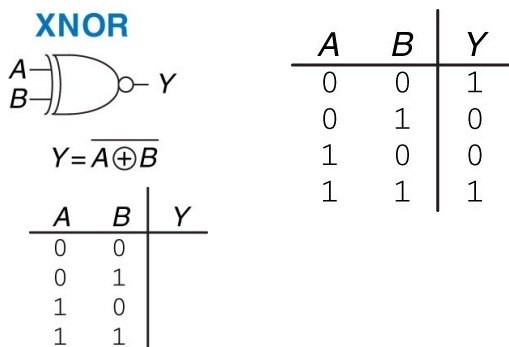
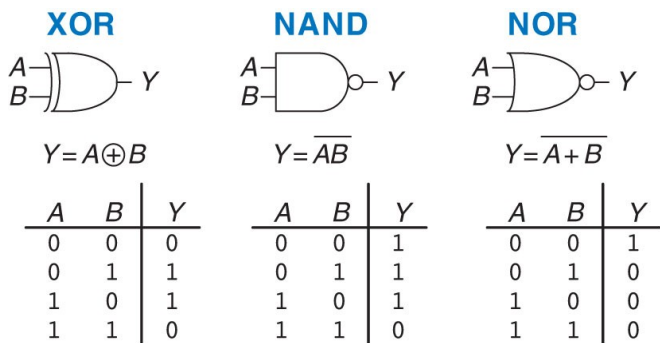
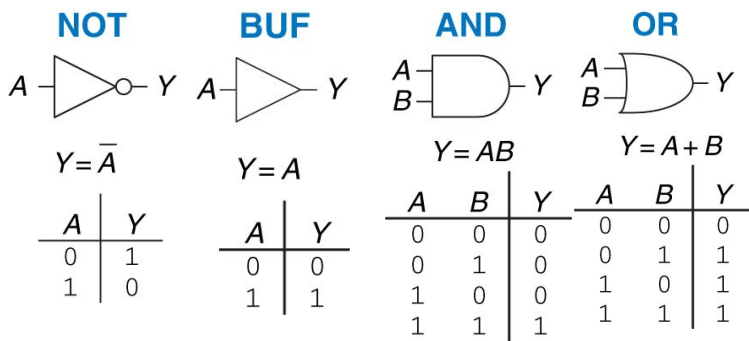
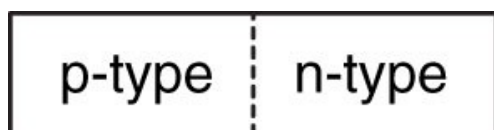


Gates



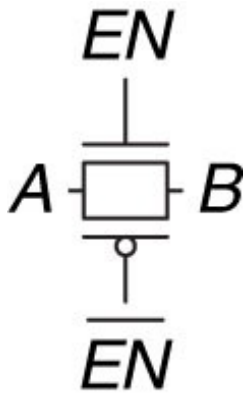
The p-n junction diode structure and symbol



anode cathode



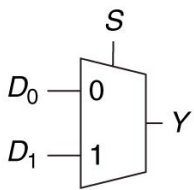
Transmission gate



Multiplexer

If $S == 0$ then $Y = D_0$

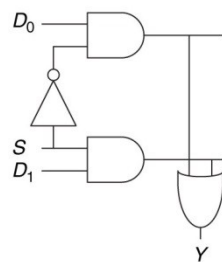
If $S == 1$ then $Y = D_1$



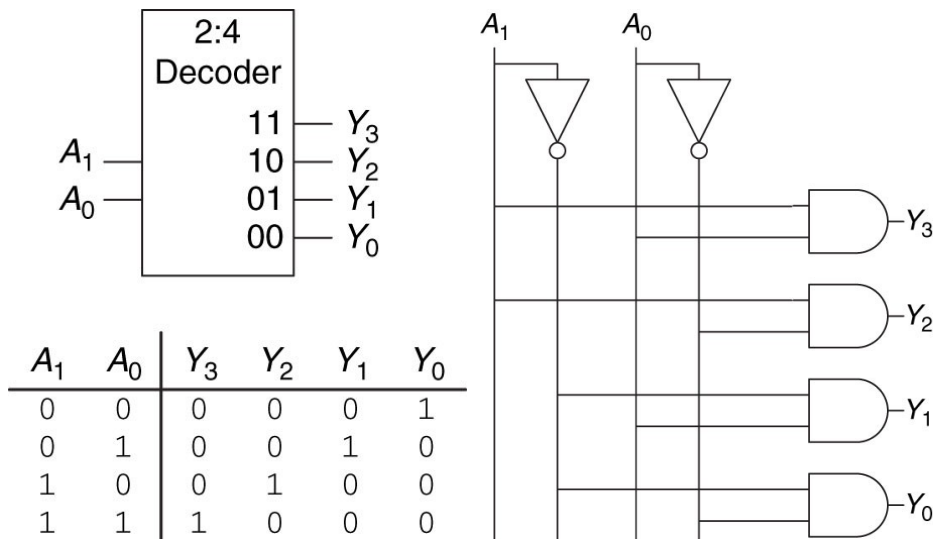
Y D _{1:0}	S				
		00	01	11	10
0	0	0	1	1	0
1	0	0	0	1	1

$$Y = D_0 \bar{S} + D_1 S$$

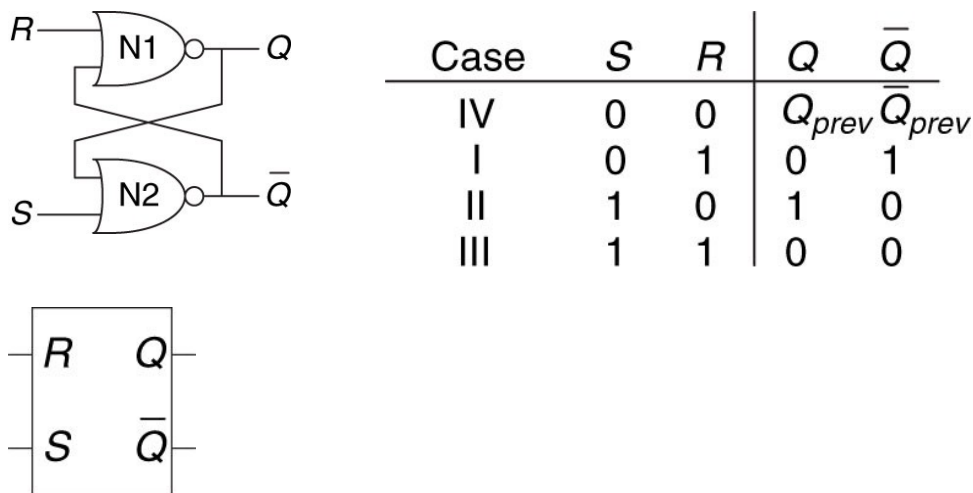
S	D ₁	D ₀	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



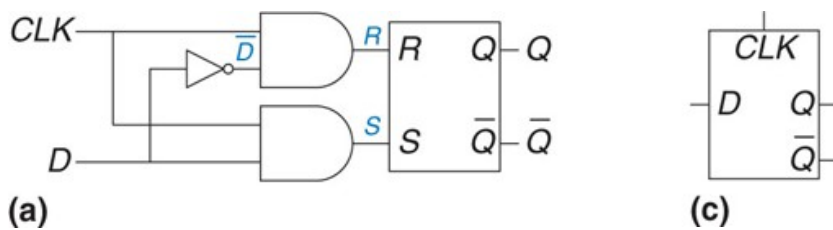
Decoder



SR latch



D latch

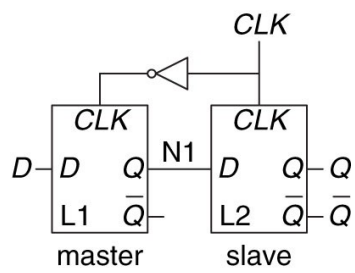


If $CLK == 1$ then set $D = X$
 If $CLK == 0$ then select Q

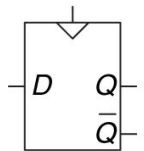
CLK	D	\bar{D}	S	R	Q	\bar{Q}
0	X	\bar{X}	0	0	Q_{prev}	\bar{Q}_{prev}
1	0	1	0	1	0	1
1	1	0	1	0	1	0

(b)

D flip-flop



(a)



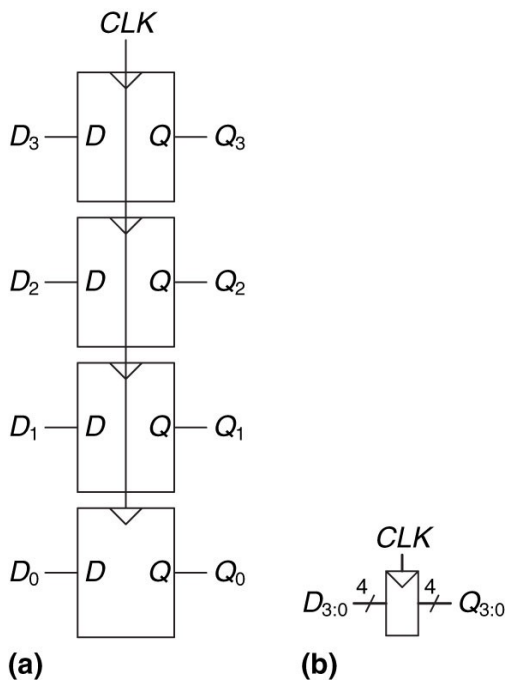
(b)



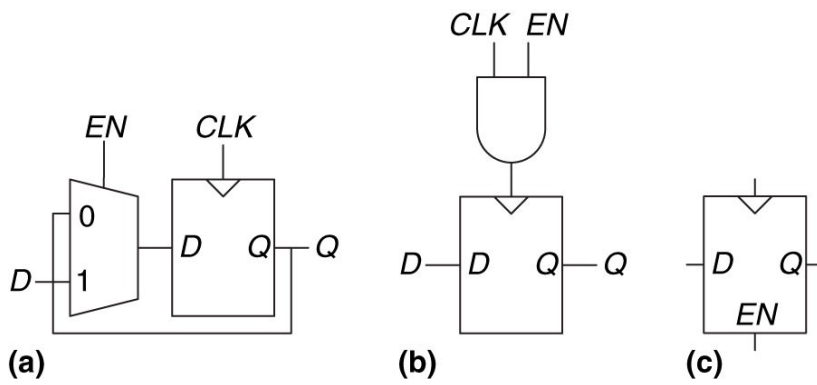
(c)

CLK	D	\bar{D}	S	R	Q	\bar{Q}
0	X	\bar{X}	0	0	Q_p	\bar{Q}_p
1	0	1	0	1	0	1
1	1	0	1	0	1	0

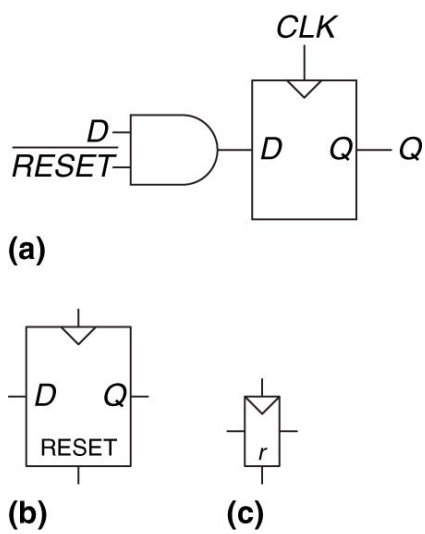
4-bit register



Enabled flip-flop



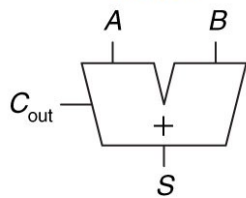
Synchronously resettable flip-flop



1-bit half adder

Carry bit	
1	
0001	
+0101	
<hr/>	
0110	

Half Adder



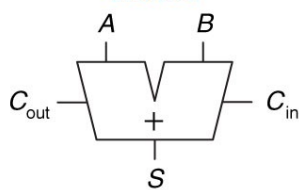
A	B	C_{out}	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$$S = A \oplus B$$

$$C_{out} = AB$$

1-bit full adder

Full Adder

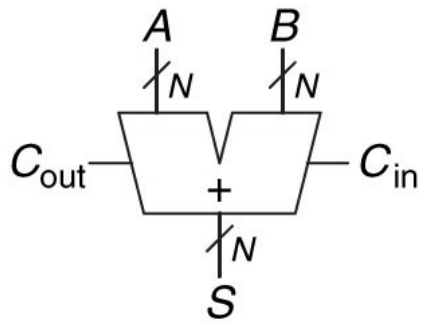


C_{in}	A	B	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

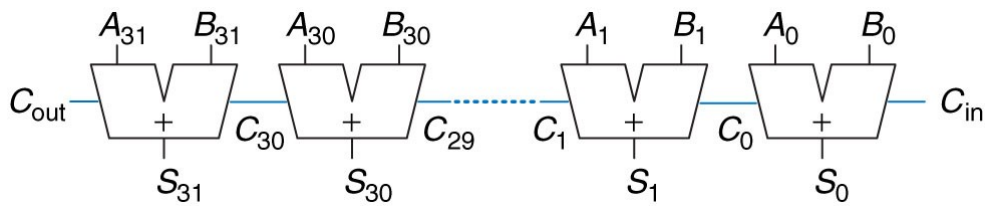
$$S = A \oplus B \oplus C_{in}$$

$$C_{out} = AB + AC_{in} + BC_{in}$$

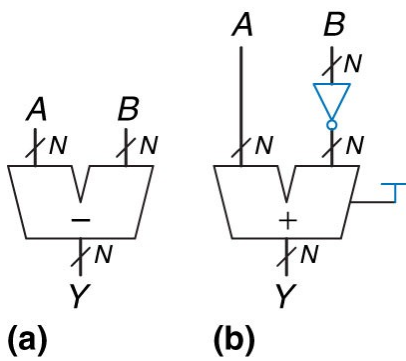
Carry propagate adder



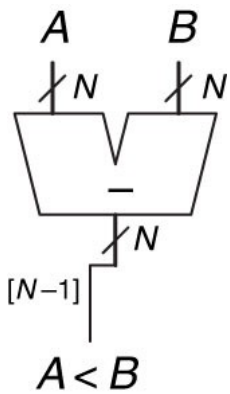
32-bit ripple-carry adder



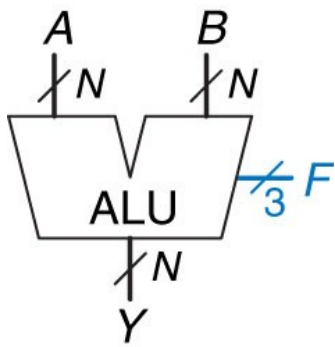
Subtractor



N -bit magnitude comparator

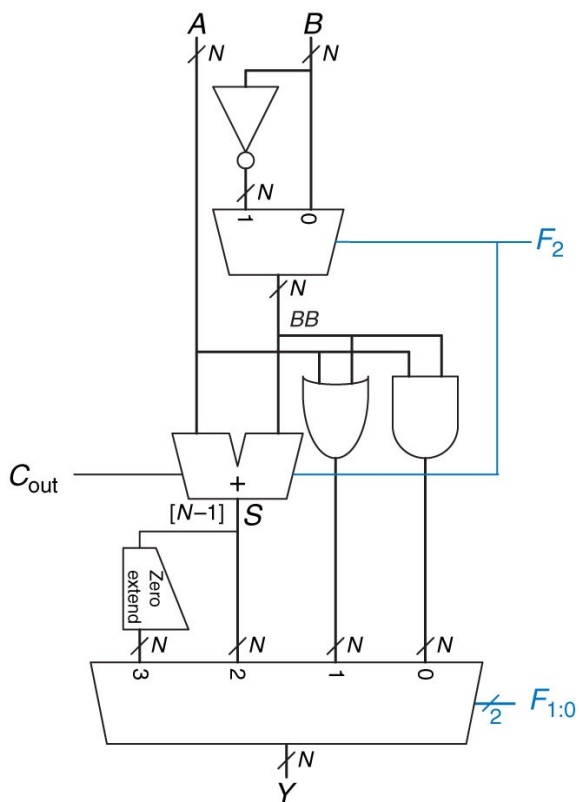


ALU

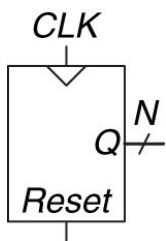
**Table 5.1** ALU operations

$F_{2:0}$	Function
000	A AND B
001	A OR B
010	A + B
011	not used
100	A AND \bar{B}
101	A OR \bar{B}
110	A – B
111	SLT

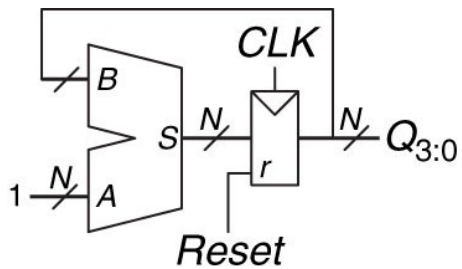
N-bit ALU



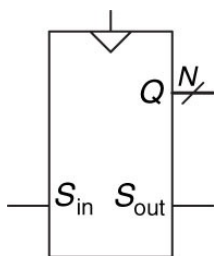
Counter



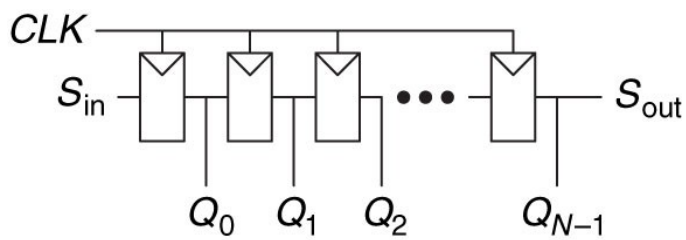
N-bit counter



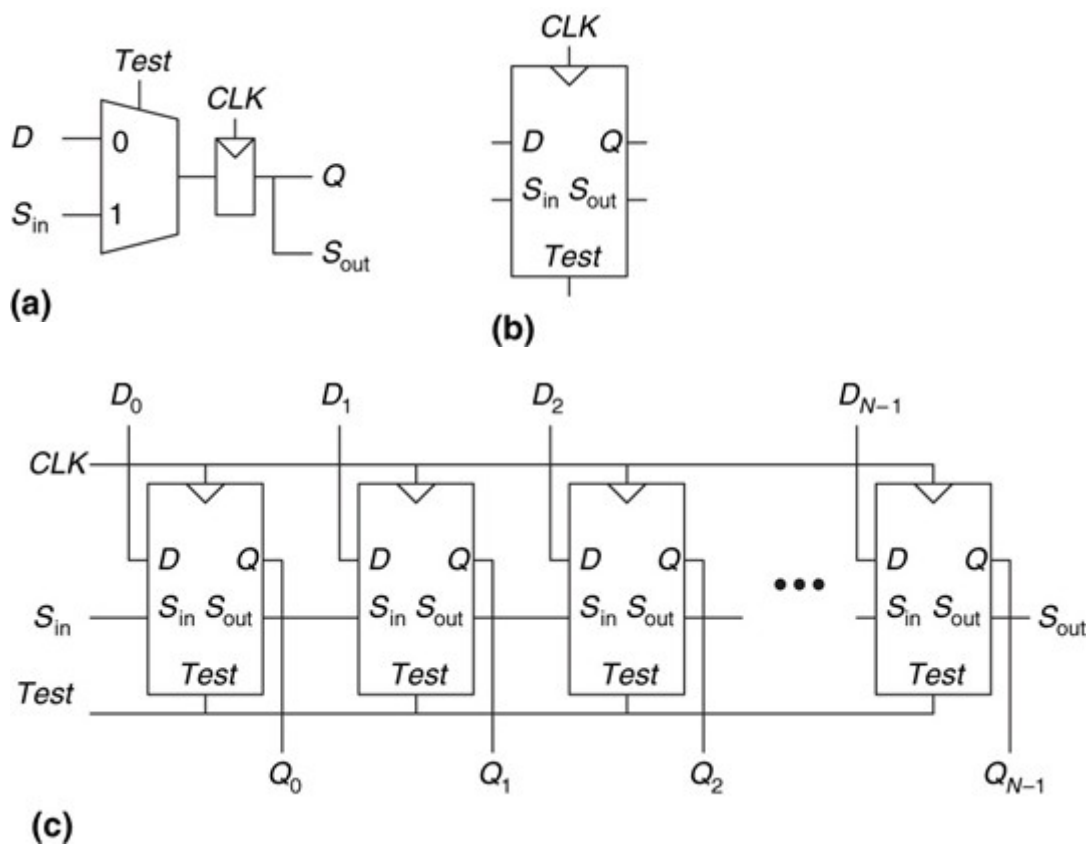
Shift register



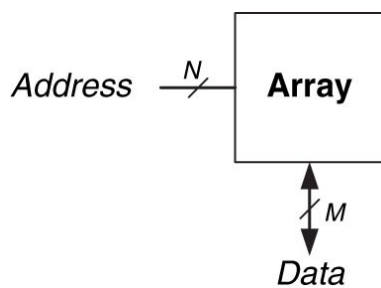
Shift register



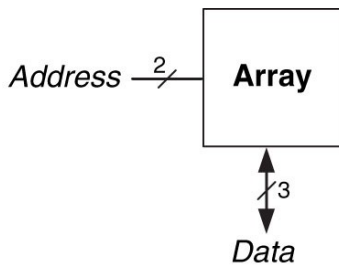
Scannable flip-flop



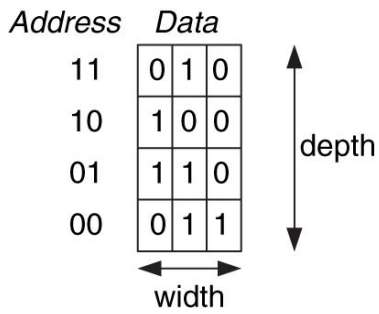
Generic memory array



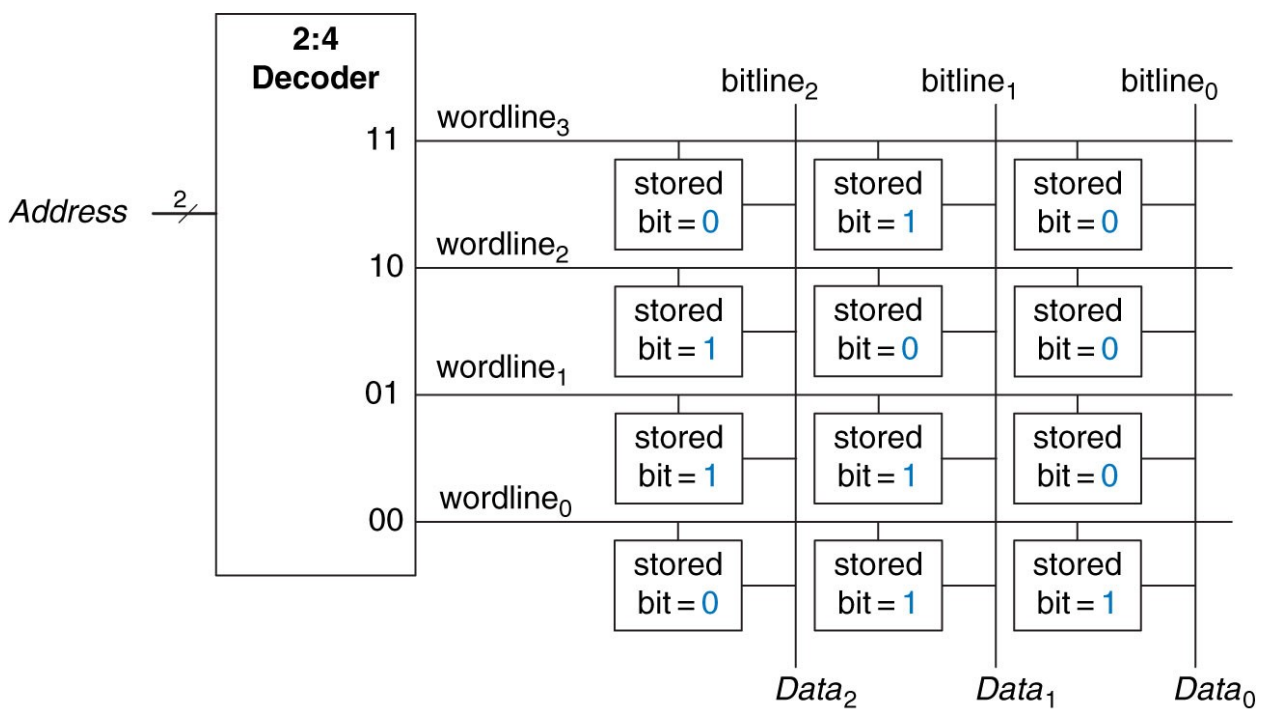
4-3 memory array



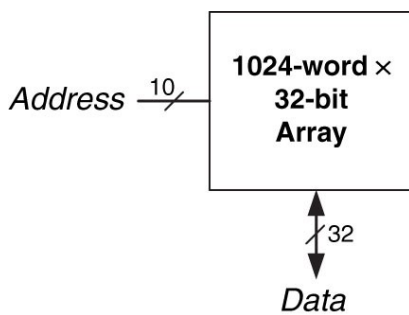
(a)



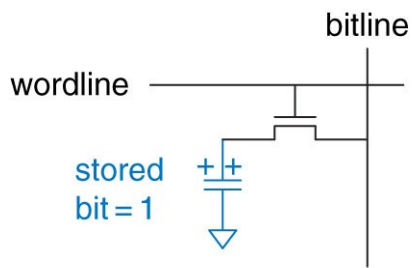
(b)



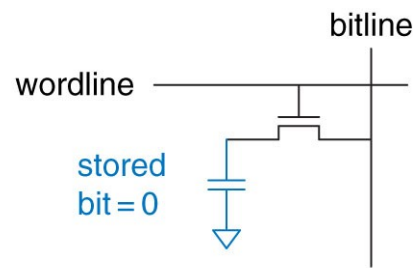
32 Kb array: depth = $2^{10} = 1024$ words, width = 32 bits



DRAM stored values

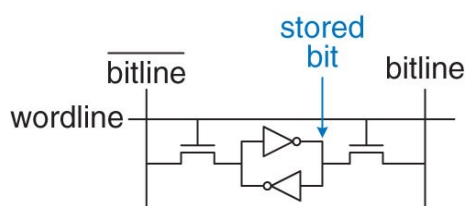


(a)

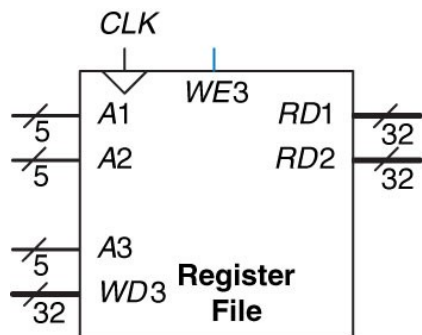


(b)

SRAM bit cell



32-32 register file with two read ports and one write port



4-word 1-bit memory array used as a lookup table

The diagram shows a 2:4 decoder with two inputs, A_1 and A_0 , and four outputs labeled 00, 01, 10, and 11. Each output line is connected to a box labeled "stored bit". The stored bit values are 0 for outputs 00, 01, and 10, and 1 for output 11. A vertical line on the right is labeled "bitline" at the top and "Y" at the bottom.

A

B

The diagram illustrates the internal architecture of a Look-Up Table (LUT) and its associated logic. The main components and their connections are as follows:

- Look-Up Table (LUT):** Receives four data inputs (data 1, data 2, data 3, data 4). Its output is fed back into the LUT via a "Register feedback" path.
- Carry Chain:** Receives "LE carry-in" and "Register chain routing from previous LE". Its output is fed back into the LUT and also serves as the "LE carry-out".
- Synchronous Load and Clear Logic:** Receives "LAB-wide synchronous load" and "LAB-wide synchronous clear". Its output is connected to the "ENA CLRn" input of the Programmable Register.
- Asynchronous Clear Logic:** Receives "labclr 1", "labclr 2", and "Chip-wide reset (DEV_CLRn)". Its output is connected to the "CLRn" input of the Programmable Register.
- Clock & Clock Enable Select:** Receives "labclk 1", "labclk 2", "labclkena 1", and "labclkena 2". Its output is connected to the "CLK" input of the Programmable Register.
- Programmable Register:** Receives "Register bypass" and "Programable register" inputs. Its output is connected to the "O" input of the LUT and also serves as the "Register chain output".
- Routing:** The output of the Programmable Register is also connected to three multiplexers that provide "Row, column, and direct link routing", "Local routing", and "Register chain output".

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