Computer Systems Design - Lab 03

Handed Out: Tues*day,* 7 Feb. *2017*
Due: Friday, 17 Feb, 2017 Demo: Feb 15-16, 2017
Submit via USF Canvas
This is a group assignment. Only one submission per group.
Late submissions will not be accepted

Objectives: To learn how to define synthesis constraints for a Verilog design, and how to synthesize a Verilog design for use on an FPGA board.

Problem: Implement the designs from labs 1 and 2 on the FPGA board.

Description: You are to synthesize the designs for Labs 1 and 2 to the FPGA board. The first task is to modify one of your Lab 1 designs (Part A, B or C - your choice) so that it can be used on the board. Only 8 input switches (bits) are available for input to this design. Two switches are used for the select lines, leaving only 6. As a result, the design must be modified to accept 3-bit inputs. How you modify it is up to you. Use the table below to map the inputs & outputs to pins on the FPGA.

Port	Width	I/O	Component	Mapping
In_A	3	I	Dip Switches	SW7 (MSB) - SW5 (LSB)
In_B	3	I	Dip Switches	SW4 (MSB) - SW2 (LSB)
SEL	2	I	Dip Switches	SW1 (MSB) - SW0 (LSB)
OUT	4+	O	GPIO LEDs	LED0 (LSB) - LED4+ (MSB)

The second task is to synthesize your design for Lab 2 to the FPGA board. No modification should be required. This design needs a clock signal. The user reference manual describes the clock available. You should use the 100MHz single-ended clock to run your design. This ought to be easy, as it's the only clock available. This is the clock you will use for all of your projects, unless specifically stated. Use the table below to map the inputs and outputs to pins on the FPGA.

Port	Width	I/O	Component	Mapping
run	1	I	Dip Switches	SW7
max_count	7	I	Dip Switches	SW6 (MSB) - SW0 (LSB)
clk	1	I	Internal Clock	USER_CLK
Digit_1	4	O	GPIO LEDs	LED3 (MSB) - LED0 (LSB)
Digit_2	4	O	GPIO LEDs	LED7 (MSB) - LED4 (LSB)

1. (50pts) **ALU:** Synthesize and test your ALU on the FPGA.
2. (50pts) **Counter:** Synthesize and test your Counter on the FPGA.

Design Constraints: The designs must properly function given the following constraints:

- The designs must both function correctly in simulation *and* on the FPGA board.

Lab Report: You must submit a written lab report. A template will be provided on Canvas. Upload this as a PDF file, DO NOT include it in your zip file.

Deliverables: Submit your report PDF and the code ZIP file separately on Canvas. The PDF should be named <netid> lab04 report.pdf. To generate the code ZIP file:

- Select **Project** → **Cleanup Project Files...** from the menu.
- Select **OK** on the pop-up box.
- Select **Project** → **Archive...** from the menu.
- On the new window, make sure **Exclude Generated Files From Archive** is *selected*.
- Choose a location for the archive, name it <netid>_lab04.zip.
- Select **OK**

Insert any images and waveforms into the report PDF. Submit the report PDF and source code ZIP separately on Canvas. If you wish, you may include copies of all images in a separate ZIP file, submitted through Canvas. Name it <netid> lab04 images.zip.

No re-grading will be done for failure to follow the guidelines. Points will be lost, never to return.