SerDes Design Considerations

Advanced Computer Systems Report

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Background

A major topic of discussion throughout this course has been the importance of data transfer bandwidth on the overall performance of computing systems. We discovered through homework assignments and lectures that our latest processors can perform more operations per second than the rest of our system can stage and handle post execution. Data transfer rates are the main bottleneck faced by high performance computing systems. In particular, there has been increased focus on improving data transfer speeds from chip to chip. As AI/ML workloads become increasingly titanic, vast compute pools need to be able to share data at extremely high speeds. As warehouses become filled with thousands and thousands of GPU's ready to train the next large language model, there becomes increasing need for high speed inter-die communication. As a result, we see solutions like NVIDIA's NVLink being touted as the fastest multi-chip link ever manufactured.

The SerDes

One important type of inter-die link is the serializer/deserializer or SerDes. In almost all cases, computer systems need to transport data that is encoded across many bits of digital information. The most natural choice for a communication channel thus is a parallel data bus with n data lines to transfer n bits. This configuration allows for high speed data transfer with low design complexity. These benefits come at a cost, however. The size of integrated circuit I/O has not decreased at the same rate as transistors. This means that our I/O interfaces are much more expensive than our transistor level infrastructure [10]. As a result, it is advantageous to utilize serial data communication protocols to reduce the per chip I/O overhead for establishing high speed links. In today's era, transistors are cheap, meaning if we can dedicate more transistor level infrastructure to achieve similar performance to a more costly parallel data bus, it could become feasible to efficiently connect thousands of chips together to tackle large scale workloads.

SerDes Transmitter Design

Leading parallel data buses can achieve extremely high speeds. Since we are concerned with the amount of I/O we spend to achieve these speeds, it is useful to describe transfer speed as a function of the length of chip perimeter that was consumed by the I/O of the link. This measurement is called the Shoreline Bandwidth Density and it is measured in Gbps / mm of chip perimeter. State of the art serial links in standard packages can achieve a shoreline bandwidth density of nearly 250 Gbps / mm. In order to achieve these massive speeds, designers must make many careful considerations and employ advanced techniques to maximize performance

[1]. Firstly, designers have to overcome limitations imposed by generating a high speed clock signal. The theoretical maximum switching speed for a modern mosfet (Intel 16nm) is around 300GHz. As the transistor starts to operate closer to its maximum operating frequency, its behavior starts to become dominated by parasitic effects. As a result it is extremely difficult to generate a stable clock signal near f_{max} of the target process transistors. In order to overcome this, designers employ multiple clock signals, each evenly phase shifted from each other. Multiphase clock generation utilizes structures such as the phase locked loop to ensure that all clock signals remain synchronized and properly phase shifted. This scheme allows us to generate a stable clock signal that is a fraction of our target operating speed, yet still have the necessary control signal timing to operate at high speed.

After we overcome the barrier of generating a high speed clock, we can start to focus our efforts on how to efficiently turn parallel data into a high speed serial data stream. We can utilize basic digital circuit building blocks to achieve this. We start by using shift registers to convert our fully parallel data into less parallel data. Consider the case where our fully parallel data is 128 bits wide, we can convert this to 16 bits of data using 8 shift registers operating at 8 times the speed at which our parallel data is being updated. These 16 streams can then be further divided into 8 streams using a 2:1 mux.

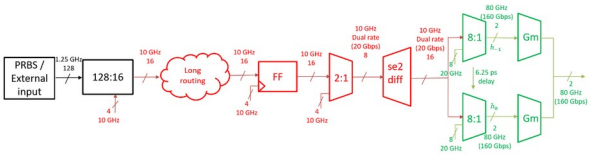

Figure 1. SerDes Transmitter Block Diagram

As seen in Figure 1., after the 2:1 mux splits the data to be transmitted into 8 streams, these lines get differentialized. This means that we now have 8 differential data streams or 16 physical data lines. Coverting the single ended data streams to differential signals makes the data transmission much more robust to PVT (process, voltage, and temperature) variations [2]. These transmissions will be especially prone to these variations since they are occurring at such high speed. After the signals are converted to differential signals, they are strobed using two high speed 8:1 muxes and amplified by a high speed amplifier with peaking structures that are used to extend the bandwidth of the amplifier. The peaking structures are passive devices that improve the speed of the transmitter by cancelling out the capacitive parastitic effects of the transistors in the circuit by adding inductance. The self resonance frequency of the transistors is lower than the target transmitting frequency for the differential lines which makes the devices behave like capacitors. A very large inductor is used to mitigate these effects.

These high speed signals then are prepared to be sent off-chip by first being routed to the edge of the die by a coplanar waveguide. A coplanar wave guide is a planar transmission line that is

carefully designed to minimize loss of the signal's power [4].

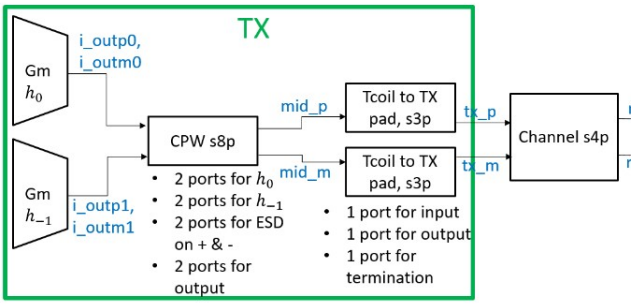

Figure 2. Physical Transmission Stage

Figure 2. shows the path of the transmitted data from the high speed amplifier, to the coplanar waveguide, and through further peaking structures to mitigate parasitic effects. The transmission then reaches a channel that connects to another die where it will be deserialized.

It is compelling to see how straightforward it can be to understand the block diagram for a high speed serializer transmitter. The overall goal of the circuit is uncomplicated. One can make use of simple digital circuit building blocks learned in the early years of one's career to implement such high performing systems that push the limits of device physics. The nuance and complexity of the design comes from the tight timing windows when synchronizing between blocks to hand off data to the next stage and in the complex parasitic effects that dominate high speed device operation. As computing systems push speeds faster and faster, it becomes impossible to ignore the fact that these systems are implemented with physical devices that follow physical laws. It is so interesting to see how careful and clever engineers have to be to compensate for these high speed effects.

IC Design Automation

In my opinion, what's even more compelling is that designers have been working on ways to automate the design of circuits like the high speed SerDes covered in the first portion of this report. Design tasks remain largely the same across years of advancement. As technology progresses and designers move from process to process, we find ourselves repeating the same steps to produce basic circuit primitives adjusting for new behaviors and effects as our devices change. These design tasks, while necessary, are repetitive and time consuming. So much manual effort is spent implementing the same circuit topologies in new process nodes. Is there anything we can do to reduce expert involvement so that we can improve productivity?

For years digital circuit design has been highly automated. Foundries provide standard cells, designers use hardware description languages to synthesize circuits using standard cells, place and route tools find optimized ways to place and connect circuit blocks on a die… yet engineers have struggled to automate the design of analog and high speed circuits. There are many more considerations and subtle nuances that must be carefully considered to automate these tasks. Regardless, there has recently been much progress in the field and thanks to relatively new techniques such as deep learning, we are at the beginning of a new era of circuit design automation [9].

Various research groups across the globe have investigated many unique methods to reduce the amount of man-hours required to design an integrated circuit from start to finish. One interesting approach is to create a surrogate model that uses deep learning to quickly approximate the results of a traditional simulation. Spice simulation can take very long to finish, especially when parametrically varying many parameters. Electromagnetic simulation is also quite slow and can destroy designer productivity. The idea is that if a deep neural network can accurately approximate a traditional simulator but with fast inference times, it can be coupled with an optimizer in an optimization loop to quickly find a potentially successful design. This strategy can be applied to any integrated circuit design task that is bottlenecked by slow simulation time. Many groups have shown promising results using this strategy to determine transistor sizing in fixed topology circuits[9].

Another interesting design automation technique is to generate random, non-intuitive structures, then predict their physical characteristics with a deep neural network [7], [8]. This technique has been successfully used in photonics and microwave circuits. One research group used this technique to quickly produce a highly optimized impedence matching network for high speed amplifiers.

The high speed SerDes discussed at the beginning of this report was designed using the Berkely Analog Generator (BAG) tool [1]. The tool uses circuit “generators” (essentially python code that describe the “bones” of an analog circuit) in conjunction with optimization techniques to automatically produce many elements of the circuit.

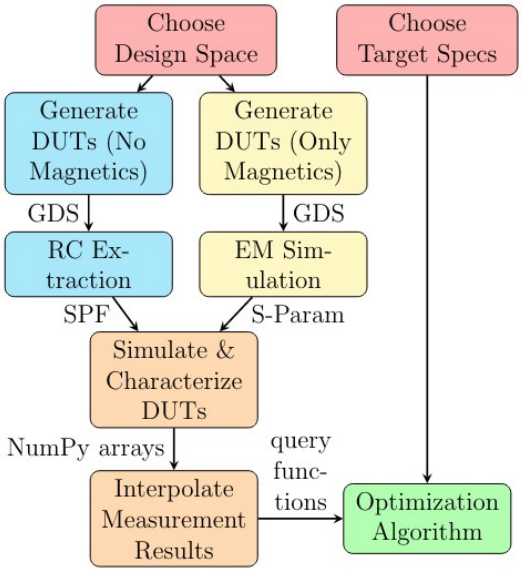

Figure 3. BAG 3++ OptDesigner Loop

As seen in Figure 3. the BAG tool is capable of searching a design space and evaluating design decisions via various modes of simulation and acting on these evaluations to converge to an optimal design. The success of the tool was proven by the impressive transfer speeds achieved by the automatically designed SerDes.

Conclusion

Analog and high speed circuit design automation has become an explosive field since deep learning has progressed in recent years. Many researchers across the globe are excited to take advantage of new developments in machine

learning to increase designer productivity and reduce the need for repetitive and time consuming efforts. Many automation techniques that have been developed show great promise and have even already successfully demonstrated that it is possible to automate these difficult design tasks. As we saw from the design of the SerDes transmitter, as automation tools continue to develop, they will only improve at capturing nuanced design decisions and details to implement high performance designs with less and less manual intervention.

References

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