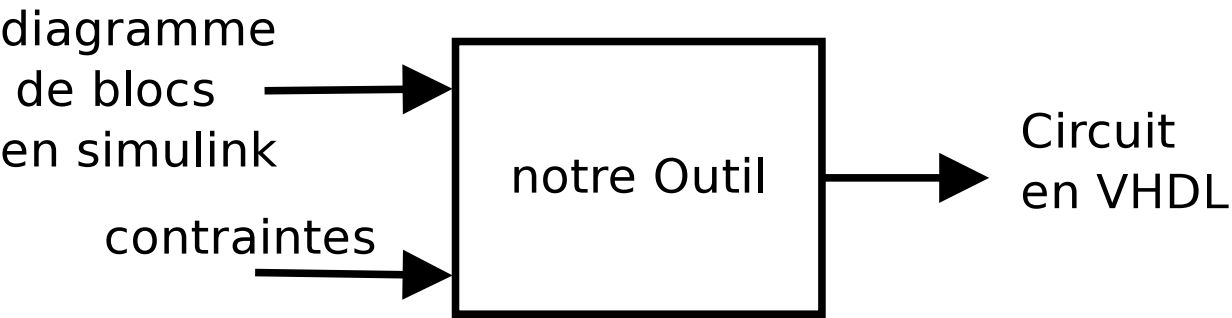
diagramme
de blocs
en simulink
contraintes
notre Outil
Circuit
en VHDL