Simulink
Blocs Diagram
(SLX)

SLX to SIF

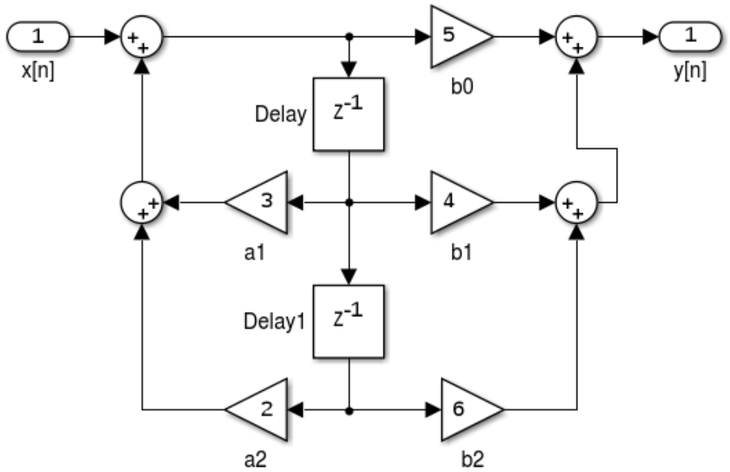
Specialized
Implicit Form
(SIF)

Fixed-Point
Generator
(FiPoGen)

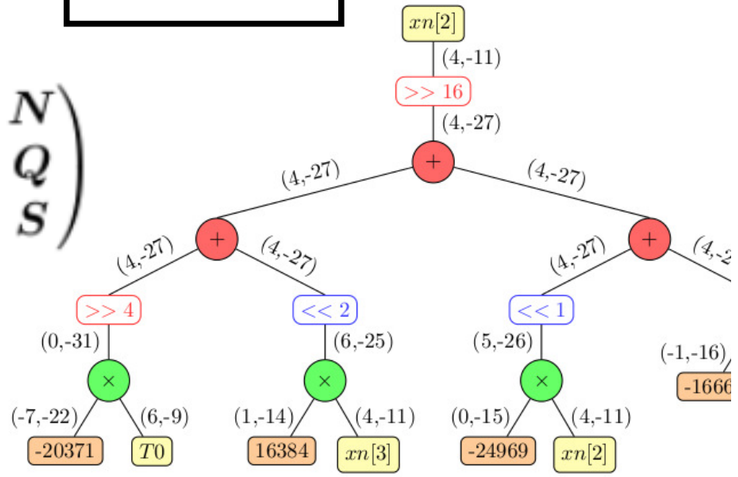
FxP ordered
Sum of Product
(oSoP)

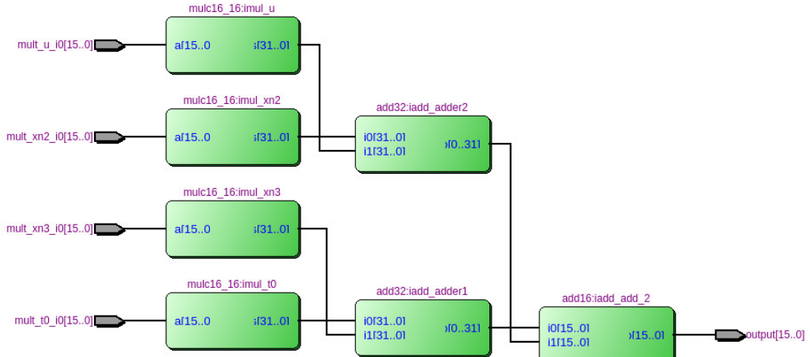
oSoP to VHDL
(& Stratus)

Circuit
(VHDL)



$$\begin{pmatrix} -J & M & N \\ K & P & Q \\ L & R & S \end{pmatrix}$$





en réel

en virgule fixe