Reg. No.:

Name :

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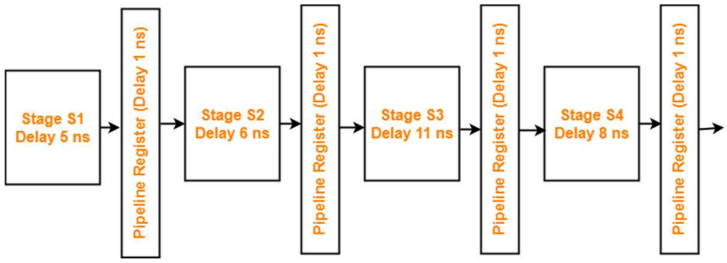
TERM END EXAMINATIONS (TEE) – November 2020

Programme	**B. Tech. – Computer Science**	**Semester**	**Fall 2020-2021**
Course Name	**Computer Architecture & Organization**	**Course Code**	**CSE2003**
Faculty Name	**Prof. Anand Motwani**	**Slot / Class No**	**A11+A12+F13/1024**
Time	**1½ hours**	**Max. Marks**	**50**

Answer ALL the Questions

Q. No.		Question Description	Marks
		PART - A – (3 x 10 = 30 Marks)	
1	(a)	A computer has 32 bit instruction and 12 bit address. If there are 250 two address instructions. Draw instruction format. How may one address instructions can be formed?	10
		OR	
	(b)	Perform Floating Point operations on decimal nos.: **i. Add:** A = 9.999 x 10^{1} and B = 1.610 x 10^{-1}. **ii. Multiply:** A = 1.110 x 10^{10} and B = 9.200 x 10^{-5}	10
2	(a)	Compare and contrast SRAM and DRAM on basis of its construction, speed, cost, capacity and application. A computer employs RAM chips of 256*8 and ROM chips of 1024*8. The computer system needs 2K bytes of RAM, 4K bytes of ROM. How many RAM and ROM chips are needed?	10
		OR	
	(b)	Compare RAID 4 and RAID 5 architectures on the basis of various parameters. Which is better and why?	10
3	(a)	Explain the hazard (with suitable diagram/example) that occurs when the pipeline makes the wrong decision on a branch prediction and therefore brings instructions into the pipeline, and as a result that are being discarded subsequently.	10
		OR	
	(b)	Consider an instruction pipeline with four stages (S1, S2, S3 and S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure-	10



What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?
Also find the clock frequency of the processor by assuming the latch delays as zero.

Part - B – (2 x 10 = 20 Marks)

4 Discuss advantages of modes of data transfer over one another. Which mode of data transfer is suitable in following scenarios: 10

a. When a small amount of data transfer is involved in the process.
b. A block of data needing to be written to a disk drive.
c. Reading a block from HDD and writing on to specific location in memory.

5 A DMA module is transferring characters to main memory from an external device transmitting at 9600 bits per second (bps). The processor can fetch instructions at the rate of 1 million instructions per second. By how much will the processor be slowed down due to the DMA activity? 10

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