Reg. No.:

Name :

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Mid-Term Examinations, April 2021

Programme	:	**B.Tech**	Semester	:	**Winter 2020-2021**
Course	:	**Digital Logic Design**	Code	:	**ECE2002**
Faculty	:	**Dr. Anirban Bhowmick**	Slot/Class No.	:	**D11+D12+D13/0377**
Time	:	**1½ hours**	Max. Marks	:	**50**

Answer all the Questions

Q. No.	Question Description	Marks
1	(i) Design a 3 bit combinational circuit which produce logic '1' when more than one input variables are at logic '1'.	**5**
	(ii) Show that **AB'C + B + BD' + ABD' + A'C = B + C.**	**5**
2	(i) A Boolean function, F is given by the minterms as f(A,B,C)=$\sum m(3,4,5,6)$. Implement this function on 4:1 MUX by considering AC as your selection lines.	**4**
	(ii) Design a multiplier which can perform the multiplication of two numbers $(5)_{10} \times (3)_{10}$.	**6**
3	(i) Minimize the following function using K-MAP: F = ∑ m(0,2,6,10,11,12,13) + d(3,4,5,14,15).	**7**
	(ii) Convert decimal 27.315 to binary.	**3**
4	(i) In a J K flip flop, we have J = Q' and K =1. Assume the flip flop was initially cleared and then clocked for 6 pulses, find the sequence at the Q after 6 pulse (Fig. 1).	**6**

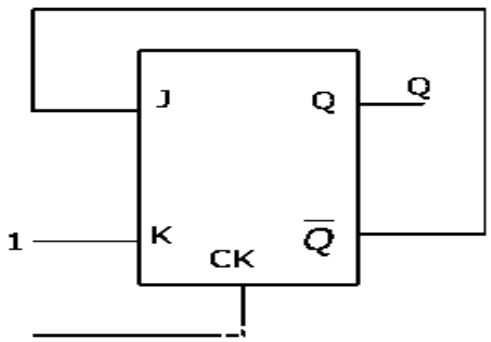

Fig.1

	(ii) Design a Half adder using 2 × 4 Decoder	**4**

5 (i) Design a J K flip flop from a S R flip flop. **5**

(ii) A sequential circuit using D flip-flop and logic gates is shown in the Fig.2, calculate the output for 4 clock cycle when you apply. X=1 and Y =1 and the clock is a negative edge trigger. Assume that initially the flip flop is cleared. **5**

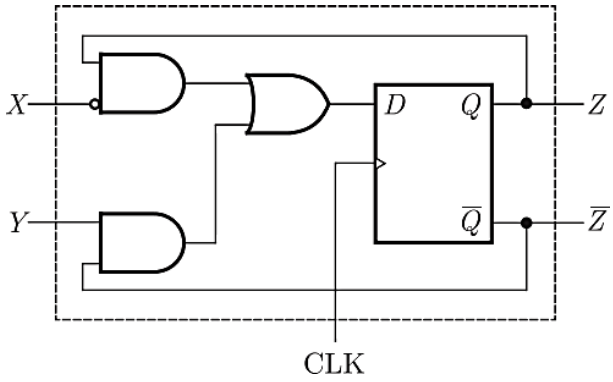

Fig.2

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