Pipelining Assignment

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4 phases → duration -> (60, 50, 90, 80) ns
latch delay = 10ns

① Pipeline cycle time :

Cycle time => Delay due to register + Max. delay due to any stage

= 10ns + Max (60, 50, 90, 80)

=> 10ns + 90ns = 100 ns

Cycle time = 100 ns

② Non-pipeline execution time –

Here we simply add up the durations

=> (60 + 50 + 90 + 80) ns

= 280ns

(3) Speed up ratio :-

→ Non-pipeline execution time / Pipeline execution time

⇒ 280 ns / 100 ns

= 2.8

Speed up ratio = 2.8

(4) Pipeline time for 1000 tasks :-

⇒ Time taken for one task + Time taken for remaing tasks.

⇒ 1 x 4 clock cycles + 999 x 1 clock cycle

⇒ 4 x cycle time + 999 x cycle time

⇒ 4 x 100 ns + 999 x 100 ns

⇒ (400 + 99900) ns

⇒ 100300 ns

Pipeline Time for 1000 tasks = 100300 ns

(5) Sequential time for 1000 tasks :-

⇒ Time taken by one task x 1000

⇒ 280 ns x 1000

⇒ 280000 ns

(6) ~~Throughout~~ Throughput

→ no. of instructions executed per unit time

⇒ 1000 tasks / 100300 ns

Throughput = 0.00997 ns^{-1}

2

frequency = 100 MHz

we know Time period = $\frac{1}{f}$ = $\frac{1}{100\,MHz}$

∴ T = $1/(100 \times 10^6)$ = 0.01 μs ⇒ 10ns

5 stages → (2.5, 1.5, 2, 1.5 & 2.5) ns

Latch delay = 0.5 ns

speed up - ?

Pipeline cycle Time ⇒ latch delay + Max delay due to any stage

⇒ 0.5 ns + Max (2.5, 1.5, 2, 1.5, 2.5)

= 0.5 + 2.5 ns

Pipeline cycle Time = 3.0 ns

Non pipeline execution time

$\Rightarrow 2.5 + 1.5 + 2.0 + 1.5 + 2.5$

$\Rightarrow 5.0 + 3.0 + 2.0$

$\Rightarrow 10ns$

speed up ratio → non pipeline executing time / Pipeline execution time

$\Rightarrow 10ns / 3ns$

speed up ratio $\Rightarrow 3.33$

Ans → option (c)

3

5 stages → FI, DI, FO, EI & WO

9 instructions.

I_3 is conditional branch instruction

target I_7

Time taken – 5ns → FI delay Buffer → 1ns

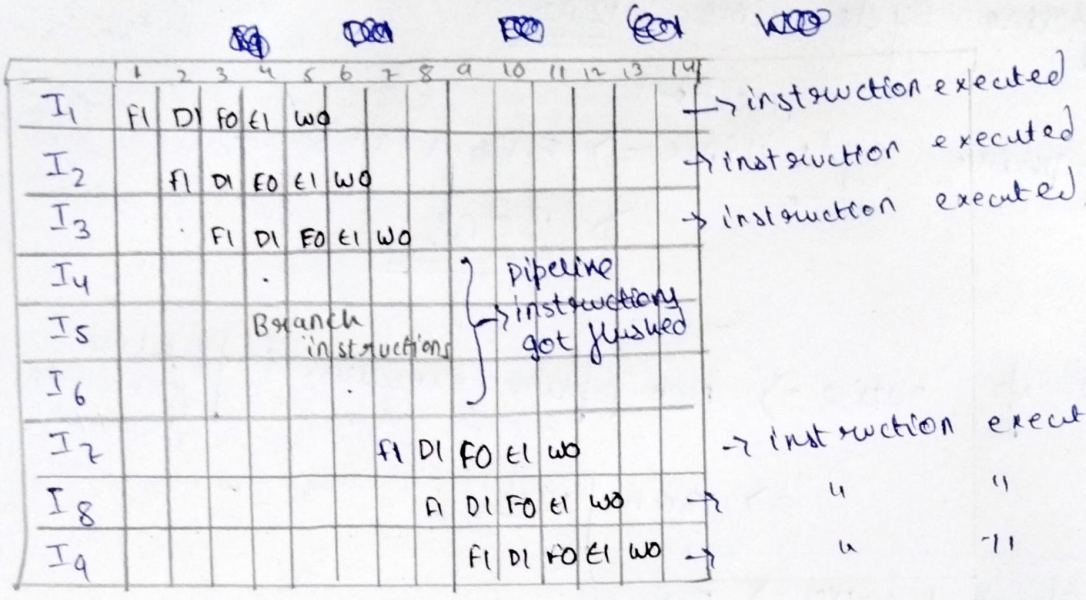
Time taken → 6ns → DI delay Buffer → 1ns

→ 11ns → FO " → 1ns

8ns → EI " → 1ns

5ns → WO

if we write it sequentially



I_4, I_5, I_6 → in pipe → got flushed

I_7 →

no instruction gets completed/executed → 8, 9, 10

it finishes in → 11, 12, 13 cycle

~~Pro~~ Instructions getting executed → $I_1 \to I_2 \to I_3 \to I_7 \to I_8 \to I_9$

we have no. of instructions = 6

no. of stages → 5

Delay : max cycle time ~~Dia~~ + Buffer delay

⇒ max (5, 6, 11, 8, 5) + 1

⇒ 11 + 1

Delay = 12 ns

Branch penalty => 4-1 => 3 cycle

→ total time to excute

=> time taken for 1st job + time taken by no. of remaining instruction

=> cycle time * no. of stages + (6-1)* time taken

=> 5*12 + 5* 12

=> 120 ns

Branch ~~of~~ penalty we know of -> 3* 12 => 36

Therefore, Total time for execution

=> 120 + 36

= 156 ns

4

no. of stages : 4 (S1, S2, S3 & S4)

Time for stage 1 → 5ns

B Pipeline Register → delay - 1ns

stge 2 → 6ns

Pipeline → 1ns

stage 3 → 11ns

Pipeline delay = 1ns

stage 4 → 8ns

~~Pipel~~ Pipline delay = 1ns

Pipeline cycle Time :

Max delay due to any stage +

Max Pipeline delay

=> Max(5, 6, 11, 8) + 1ns => 11ns + 1ns = 12ns

→ Pipeline cycle time = 12 ns

→ Non-pipelined cycle time (1 execution) => 5 + 6 + 11 + 8

=> 30 ns

→ Speed up ratio => Non pipline execution time / Pipeline execution time

=> 30 ns / 12 ns

Speed up ratio => 2.5

Speed up ratio => 3 (approx)