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TERM END EXAMINATIONS (TEE) – Jan 2022

Programme	**B. Tech. – CSE**	**Semester**	**Fall 2021-22**
Course Name	**Computer Architecture & Organization**	**Course Code**	**CSE2003**
Faculty Name	**Prof. Anand Motwani**	**Slot / Class No**	**A11+A12+A13 / 0548**
Time	**1½ hours**	**Max. Marks**	**50**

Answer ALL the Questions

Q. No.		**Question Description**	Marks
		PART - A – (3 x 10 = 30 Marks)	
1	(a)	Write the expression in two and 3 address instruction formats. $$X = \frac{A + B * C}{D - E * F + G * H}$$	10
		OR	
	(b)	Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and in the remainder the immediate operand or an operand address. a. What is the maximum directly addressable memory capacity (in bytes)? b. Discuss the impact on the system speed if the microprocessor bus has 1. A 32-bit local address bus and a 16-bit local data bus. 2. A 16-bit local address bus and a 16-bit local data bus.	10
2	(a)	Find number of chips necessary to implement a 4 MBytes memory: 1) with SRAM of 64 Kbit; 2) with DRAM of 1Mbit; 3) 64 KB using 64 Kbit SRAM & the remaining using 1Mbit DRAM.	10
		OR	
	(b)	A computer has an 8 GByte memory with 64 bit word sizes. Each block of memory stores 16 words. The computer has a direct-mapped cache of 128 blocks. The computer uses word level addressing. What is the address format? If we change the cache to a 4- way set associative cache, what is the new address format?	10

3 (a) **i.** Calculate the minimum number of times the system bus is used to DMA, as per the given description. Transfer size = 29,154 KB, DMA is using 16bit word count register. 10

ii. Is it possible to overlap CPU and DMA cycles? Justify.

OR

(b) Explain Organization and Structure of Disk with the help of suitable diagram. A hard disk with capacity 5GB has 2048 tracks/platter, 1024 sectors/track, and 512 byte sectors. Calculate the number of platters. 10

Part - B – (2 x 10 = 20 Marks)

4 Elaborate the use of following: 10
a. Translation Look-aside Buffer (TLB)
b. Paging scheme of Memory Management.

5 As per the description given in table, find out which design is better after calculating the improvement in time. Both P1 and P2 have to execute 100 instructions. Assume synchronous pipelining. 10

P1 (5 stage pipeline) (Time in ms.)	**3**	**2**	**4**	**2**	**3**
P2 (8 stage pipeline) (Time in ms.)	**3ms in each stage**				

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