Reg. No.:

Name :

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Continuous Assessment Test (CAT) – II – September 2020

Programme	:	**B. Tech.**	Semester	:	**Fall 2020-2021**
Course	:	**Computer Architecture and Organization**	Code	:	**CSE2003**
Faculty	:	**Prof. Anand Motwani**	Slot/Class No.	:	**A11+A12+TA1/1024**
Time	:	**1½ hours**	Max. Marks	:	**50**

Answer all the Questions

Q. No.	Question Description	Marks
1	**a.** How many 128 * 8 memory chips are needed to provide the memory of capacity **i.** 4096 x 16. **ii.** 2048 bytes **b.** Consider a machine with a byte addressable main memory of 2^{32} bytes divided into blocks of size 32 bytes. Assume that a direct mapped cache having 512 cache line is used with this machine. The size of the tag filed in bytes is _____.	**10**
2	Consider a direct mapped cache with 8 cache blocks (0-7). If the memory block requests are in the order- 3, 5, 2, 8, 0, 6, 3, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24 **a.** Which memory blocks will not be in the cache at the end of the sequence? **b.** Also, calculate the hit ratio and miss ratio.	**10**
3	A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each block contains 256 eight bit words. **1.** How many bits are required for addressing the main memory? **2.** How many bits are needed to represent the TAG, SET and WORD fields?	**10**
4	Elaborate the following: **a.** Translation Look-aside Buffer (TLB) **b.** Paging scheme of Memory Management	**10**
5	Explain Organization and Structure of Disk with the help of suitable diagram.	**10**

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