DIGITAL LOGIC DESIGN

ECE2002

Tutorial -1

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1. Simplify the following Boolean expressions to a minimum number of literals:

(a) $xy + xy'$ (c) $xyz + x'y + xyz'$ (e) $(a + b + c')(a'b' + c)$	(b) $(x + y)(x + y')$ (d) $(A + B)'(A' + B')'$
(f) $a'bc + abc' + abc + a'bc'$	

2. Reduce the following Boolean expressions to the indicated number of literals:

(a)	$A'C' + ABC + AC'$	to three literals
(b)	$(x'y' + z)' + z + xy + wz$	to three literals
(c)	$A'B(D' + C'D) + B(A + A'CD)$	to one literal
(d)	$(A' + C)(A' + C')(A + B + C'D)$	to four literals
(e)	$ABC'D + A'BD + ABCD$	to two literals

3. Draw logic diagrams of the circuits that implement the original and simplified expressions in Problem 2 (a).

4. Find the complement of $F = wx + yz$; then show that $FF' = 0$ and $F + F' = 1$.
5. Find the complement of the following expressions:
   a. $xy' + x'y$
   b. $(a + c)(a + b')(a' + b + c')$
   c. $z + z'(v'w + xy)$

6. Implement the Boolean function:
   $F = xy + x'y' + y'z$ with AND, OR, and inverter gates

7. The logical sum of all $minterms$ of a Boolean function of n variables is 1. Prove the previous statement for n = 3.

8. Express the following function as a sum of $minterms$ and as a product of $maxterms$:

$$F(A, B, C, D) = B'D + A'D + BD$$

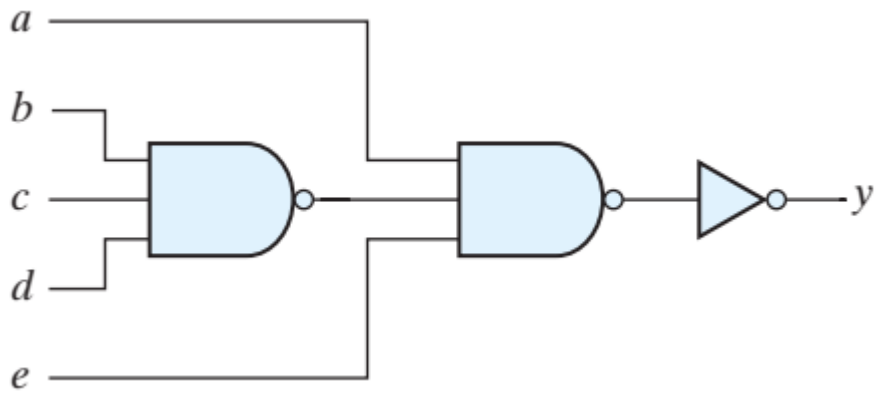
9. Express the complement of the following functions in sum-of-minterms form:
   a. $F(A, B, C, D) = \sum(2, 4, 7, 10, 12, 14)$
   b. $F(x, y, z) = \prod(3, 5, 7)$

10. Convert each of the following to the other canonical form:
   a. $F(x, y, z) = \sum(1, 3, 5)$
   b. $F(A, B, C, D) = \prod(3, 5, 8, 11)$

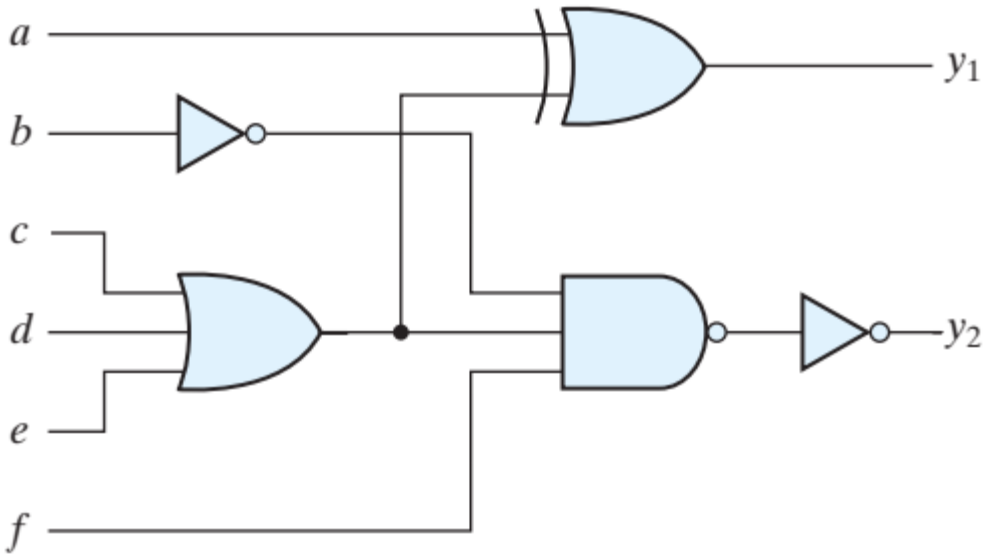
11. Convert each of the following expressions into sum of products and product of sums:
   a. $(u + xw)(x + u'v)$
   b. $x + x(x + y)(y + z')$

12. Show that the dual of the exclusive-OR is equal to its complement.

13. Write Boolean expressions and construct the truth tables describing the outputs of the circuits described by the logic diagrams as shown below:



14. Write Boolean expressions and construct the truth tables describing the outputs of the circuits described by the logic diagrams as shown below:


a
b
c
d
e
f
y_1
y_2