Reg. No.:

Name :

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Continuous Assessment Test (CAT) – I – August 2020

Programme	:	**B. Tech.**	Semester	:	**Fall 2020-2021**
Course	:	**Computer Architecture and Organization**	Code	:	**CSE2003**
Faculty	:	**Prof. Anand Motwani**	Slot/Class No.	:	**A11+A12+TA1/1024**
Time	:	**1½ hours**	Max. Marks	:	**50**

Answer all the Questions

Q. No.	Question Description	Marks
1	The following system enhancements are considered: a) faster CPU b) separate processors for different tasks (as in an airline reservation system or in a credit card processing system) Do these enhancements improve response-time, throughput or both?	**5**
2	Perform following conversions: a. $(111001)_2$ to Octal b. $(35)_{10}$ to HexaDecimal	**5**
3	Draw a Flowchart, representing the Instruction Execution Cycle.	**10**
4	An integer is stored somewhere in the memory; a pointer to this integer is at address 200. Assume the machine supports the base address (200) to be in memory and the base address is in a register. Use memory indirect addressing to increment the number and present the two address instructions for this.	**10**
5	Write the expression in one address and three address instruction format. $$A \leftarrow \left(B * \left((C + (D * E)) - \left(\frac{F}{G}\right)\right)\right)$$	**10**
6	Suppose we have two implementations of the same instruction set architecture (ISA). Machine A has a clock cycle time of 10 ns. and a CPI of 2.0; Machine B has a clock cycle time of 20 ns. and a CPI of 1.2. Show using calculations, which machine is faster for a program size having 10^9 instructions and by how much.	**10**

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