Reg. No.:

Name :

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TERM END EXAMINATIONS (TEE) – May 2021

Programme	:	**B.Tech.**	**Semester**	:	**Winter 2020-21**
Course Name	:	**Digital Logic Design**	**Course Code**	:	**ECE2002**
Faculty Name	:	**Dr.Anirban Bhowmick**	**Slot / Class No**	:	**D11+D12+D13/0377**
Time	:	**1½ hours**	**Max. Marks**	:	**50**

Answer ALL the Questions

Q. No.		Question Description	Marks
		PART - A (30 Marks)	
1	(a)	(i) Perform signed addition of -32.75 to -54.625 using 2's complement in a 12-bit register (4 bit for decimal). Verify the answer.	7
		(ii) Prove the following: **A ⊕ B = A' ⊕ B'**	3
		OR	
	(b)	Design a 4 bit parallel adder using carry look ahead logic	10
2	(a)	(i) Design an S-R flipflop using T flipflop?	6
		(ii) Write the excitation table of the following flip flop: SR flip flop and JK flip flop	4
		OR	
	(b)	State diagram of this synchronous sequential circuit is shown in the figure 1, you have to design the circuit with D Flip Flop.	10

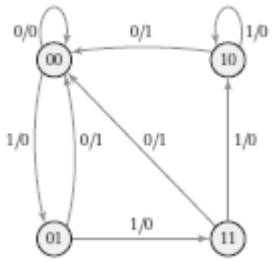

Figure 1

3 (a) Design a synchronous J K counter that goes through states 3, 4, 6, 7, 3. 10

OR

(b) Design a overlapping sequence detector which can detect '101' sequence using JK flip-flop 10

PART - B (20 Marks)

4 (i) Design a Full adder circuit using two 4:1 Multiplexer, one multiplexer output will be sum and another for carry out. 7

(ii) Reduce the following Boolean expressions: 3
F=AB+A(B+C)+B'(B+D)

5 What is HDL? Write a Verilog code to design positive edge trigger J-K flip-flop. 10

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