Logic Circuit Design

Dr. Hajar Falahati
98-99-1

Logic Circuit Design (LCD)!

"A New Golden Age for Computer Architecture: Domain-Specific Hardware/Software Co-Design, Enhanced Security, Open Instruction Sets, and Agile Chip Development"
By John L. Hennessy and David A. Patterson

Logic circuit design course aims to make you familiar with the digital system concepts, digital storages, digital system modeling, and digital system design. This course is one of the **main courses** in bachelor program in top universities around the world, such as MIT, Berkley, Stanford, ETH Zurich, USC, Caltech, British Columbia, EPFL, and etc.

Instructure and TAs

Hajar Falahati, assistant professor at Iran University of Science and Technology (IUST), is the course lecturer.
The teaching assistant teams:

- Mr. Sepehr Babapour BSs. candidate at IUST
- Ms. Sana Shoeibi, BSs. candidate at IUST
- Ms. Zahra Hoseini, BSs. candidate at IUST
- Mr. Mahsa Meimari, BSs. student at IUST
- Mr. Mirhossein Seyednasiri, BSs. student at IUST

Class information

Saturday and Monday 15:00-17:00 at Class 113.
TA class: Tuesday at 12:00 – 13:00.

Grading Policies

- **Final Exam**: 30%
- **Midterm Exam**: 20%
- **Quiz**: 10%
  - Four *scheduled* quizzes
  - TA class quizzes
- **Class attendance and class activity:** 5% - 5%
  - Lecture Class
  - TA class
- **Assignments & Projects**: 30%
  - Bonus points for outstanding projects

Assignment Policies

- Deadlines are **tight**.
- You have **3-day extra time** for submitting assignments/projects in the whole semester.
- **20% penalty** for your late assignment/project submissions after 3-day extra time!
- **Zero score** for the late assignment/project submissions after uploading the solution in the course website!
- **Zero score** for **copied** assignments/projects and **academic misconduct**.

Class Schedule

Please check the class schedule for more information about the quizzes (Q), assignments (A), and Projects (P) deadlines.

Week	Day	Date	Topic	Events & Deadlines
1	Sun.	1398/06/31	Administrative Lecture	A. 1 Fri. 1398/07/05
	Tue.	1398/07/02	Basic Concepts	
2	Sun.	1398/07/07	Number Systems	A. 2 Fri. 1398/07/12
	Tue.	1398/07/09	Arithmetic	
3	Sun.	1398/07/14	Signed – unsigned	A. 3 Fri. 1398/07/19
	Tue.	1398/07/16	1's complement	
4	Sun.	1398/07/21	Computer Codes	A. 4 Fri. 1398/07/26
	Tue.	1398/07/23	Error Detection Codes && Floating Point	
5	Sun.	1398/07/28	Boolean Algebra	A. 5 Fri. 1398/08/03
	Tue.	1398/07/30	Boolean Algebra	
6	Sun.	1398/08/05		A. 6 Fri. 1398/08/10
	Tue.	1398/08/07		
7	Sun.	1398/08/12	Logic Gates - Transistors	A. 7 Fri. 1398/08/17
	Tue.	1398/08/14	Logic Gates	
8	Sun.	1398/08/19	Logic Gates – active Low	A. 8 Fri. 1398/08/24
	Mon.	1398/08/20	Analysis & Synthesis	
	Tue.	1398/08/21	Analysis & Synthesis - Sample	
9	Sun.	1398/08/26	Optimization – K-map	A. 9 & P. 1st phase Fri. 1398/09/01
	Mon.	1398/08/27	Optimization – Q-McCluskey	
	Tue.	1398/08/28	Timing Hazards & Combinational (Comb.) Blocks	
10	Sun.	1398/09/03	Comb. Blocks 2: Decoder – Encoder / Selection Logic	A. 10 Fri. 1398/09/08
	Tue.	1398/09/05	Comb. Circuits 1 / Comb. Circuits 2	
	Wed.		Sequential Circuits (Seq. Circuits)	
11	Sun.	1398/09/10	Seq. Circuits 2: Flip Flops	A. 11 & P. 2nd phase Fri. 1398/09/15
	Tue.	1398/09/12	Analysis of Seq. Circuits: Mealy & Moore FSM	
	Wed.	1398/09/14	Midterm (W. 1-8)	
12	Sun.	1398/09/17	ASM	A. 12 Fri. 1398/09/22
	Tue.	1398/09/19	Application of Seq. Circuits	
13	Sun.	1398/09/24	Q.3 [W. 9- 11] & Application of Seq. Circuits 2	A. 13 Fri. 1398/09/29
	Tue.	1398/09/26	Synthesis of Seq. Circuits	
14	Sun.	1398/10/01	Simplification of Seq. Circuits	A. 14 & P. 3rd phase Fri. 1398/10/06
	Tue.	1398/10/03	Simplification of Seq. Circuits	
15	Sat.	1398/10/08	Programmable Logic Device	
	Tue.	1398/10/10	Q.4 [W.12 – 14] & Review, Samples	

More References:

1. "Digital Logic Circuit Analysis and Design," by Nelson, Nagle, Carroll and Irwin.
2. "Digital Design," fifth edition by Moris Mano.