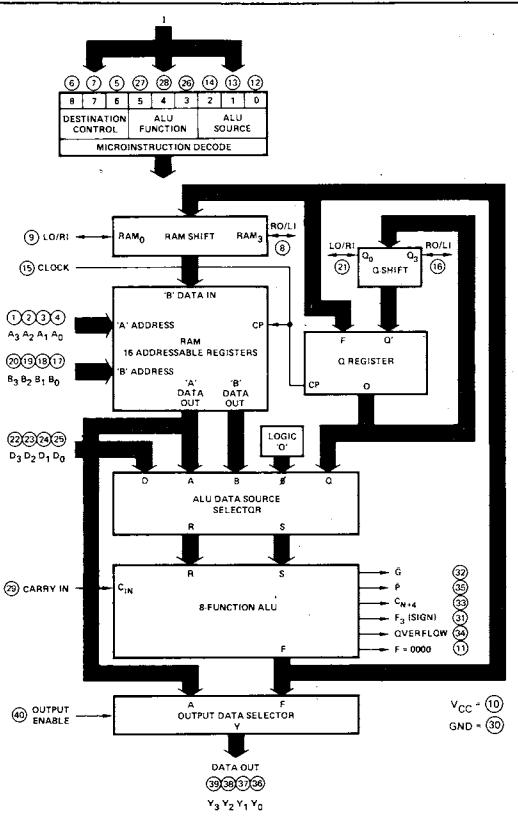


Am2901A

BLOCK DIAGRAM



Am2901A

INSTRUCTIONS

Destination

I ₈₇₆	Mnemonic	Load	Y =
0	LQ	F → Q	F
1	NOP	-	
2	LRA	F → B	A
3	LRF	F → B	F
4	LROD	F/2 → B, Q/2 → Q	F
5	LRD	F/2 → B	F
6	LRQU	2F → B, 2Q → Q	F
7	LRU	2F → B	F

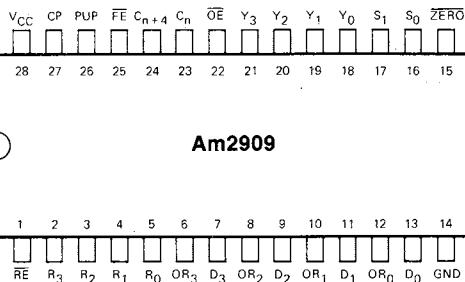
Function

I ₅₄₃	Mnemonic	Function
0	ADD	R + S
1	SUBR	S - R
2	SUBS	S - R
3	OR	R ∨ S
4	AND	R ∧ S
5	NOTRS	R ∼ S
6	EXOR	R ∨ S
7	EXNOR	R ∼ S

Source

I ₂₁₀	Mnemonic	Source R S
0	AQ	A Q
1	AB	B Q
2	ZQ	O B
3	ZB	O B
4	ZA	O A
5	DA	D A
6	DQ	D A
7	DZ	D Q

Am2909 PIN CONNECTIONS



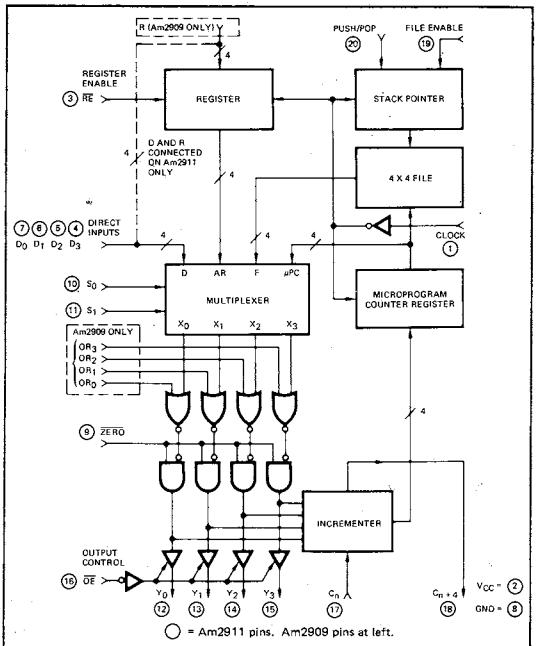
Am2909

NEW ARITHMETIC CIRCUITS COMING

Am2903 Four-Bit Slice with Expandable Register File

Am2904 Status and Shift Control

BLOCK DIAGRAM



INSTRUCTIONS

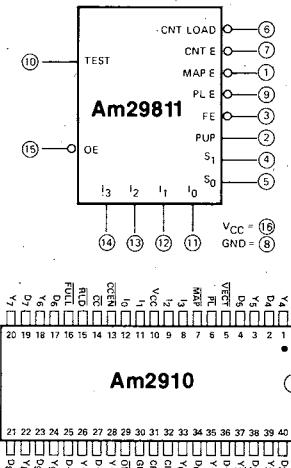
Address Selection

OCTAL	S ₁	S ₀	SOURCE FOR Y OUTPUTS	SYMBOL
0	L	L	Microprogram Counter	μPC
1	L	H	Register	REG
2	H	L	Push-Pop Stack	STK0
3	H	H	Direct Inputs	D _i

Synchronous Stack Control

FE	PUP	PUSH-POP STACK CHANGE
H	X	No Change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

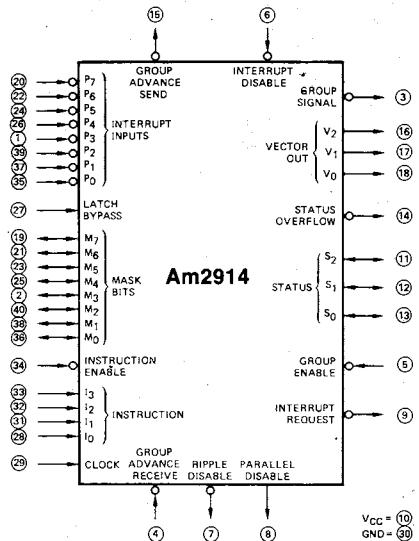
PIN CONNECTIONS



INSTRUCTIONS

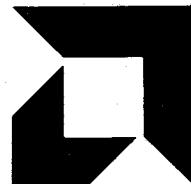
MNEMONIC	I ₃	I ₂	I ₁	I ₀	INSTRUCTION
JZ	L	L	L		Jump to Address Zero
CJS	L	L	L	H	Conditional Jump-to-Subroutine with Jump Address in Pipeline Register.
JMAP	L	L	H		Jump to Address at Mapping PROM Output.
CJP	L	L	H		Conditional Jump to Address in Pipeline Register
PUSH	L	H	L		Push Stack and Conditionally Load Counter
JSRP	L	H	L		Jump-to-Subroutine with Starting Address Conditionally Selected from Am2911 R-Register or Pipeline Register.
CJV	L	H	L		Conditional Jump to Vector Address.
JRP	L	H	H		Jump to Address Conditionally Selected from Am2911 R-Register or Pipeline Register.
RFCT	H	L	L		Repeat Loop if Counter is not Equal to Zero.
RPCT	H	L	L	H	Repeat Pipeline Address if Counter is not Equal to Zero.
CRTN	H	L	H		Conditional Return-from-Subroutine.
CJPP	H	L	H		Conditional Jump to Pipeline Address and Pop Stack.
LDCT	H	H	L		Load Counter and Continue.
LOOP	H	H	L		Load Counter and Continue.
CONT	H	H	H	L	Test End of Loop.
					Continue to Next Address.
JP	H	H	H		Jump to Pipeline Register Address.
TWB	H	H	H		Three Way Branch — To PC if Pass Test, to Loop if Fail Test and CNT ≠ 0, to Pipeline if Fail Test and CNT = 0
					29811 Only
					2910 Only

LOGIC SYMBOL



INSTRUCTIONS

Decimal	$I_3I_2I_1I_0$
0	MCLR
1	CLRIN
2	CLRMB
3	CLRMR
4	CLRVC
5	RDVC
6	RDSTA
7	RDM
8	SETM
9	LDSTA
10	BCLRM
11	BSETM
12	CLRM
13	DISIN
14	LDM
15	ENIN

BIPOLAR
MICROPROCESSOR
FAMILYMICRO
PROGRAMMING
CARD

ADVANCED MICRO DEVICES

AMDASM

COMMAND SUMMARY

Δ = required space

{ } = optional

DEFINITION PHASE	
TITLE Δ	maximum 60 characters
WORD Δ n	$n \leq 128$
EQUA	name: EQU Δ constant/expression
SUB Δ	name: SUB Δ field,..10 fields max
DEFA Δ	name: DEF Δ field,..30 fields max
NOLIST	do not print following stmts
LIST	print following statements
END	end of definition source file
ASSEMBLY PHASE	
TITLE Δ	maximum 60 characters
EQUA	name: EQU constant/expression
NOLIST	do not print following stmts
LIST	print following statements
f.n. Δ	format name Δ VFS,..(from DEF)
FF Δ	free format FF Δ field,..max 30
SPACE Δ n	spaces n blank lines
EJECT	ejects page
ORG Δ n	resets program counter (forward)
RES Δ n	reserves n words of code
*ALIGN Δ n	sets PC to next even multiple of n
**DATA Δ n	constant, right just. in word
**DUP Δ n	duplicates next word n times
LABEL:	precedes f.n. or FF, value = PC
*LABEL::	entry point for mapping PROM
:	comment statement
*not available on AMDASM/TS	
**not available on AMDASM/80	
names = 8 characters, no blanks	
char 1 = A-Z, or .. char 2-8 = A-Z,1-9, or ..	

AMDASM

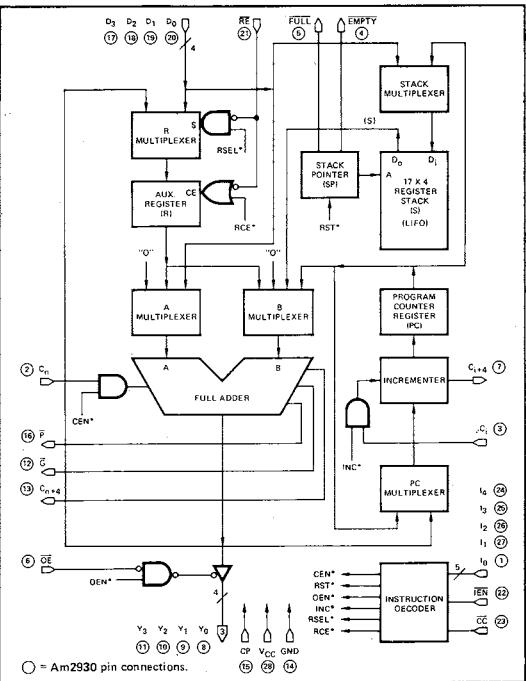
FIELD & OPERATOR INFORMATION

CONSTANTS, EXPRESSIONS, CONSTANT FIELDS	
{n} des digits {mod}	
VARIABLE FIELDS	
n V {attr} {des} {digits} {mod} (digits are default value)	
n V {attr} X (defaults to X)	
max n = 16 (AMDASM/80), = 32 (AMDASM/TS)	
DON'T CARE FIELDS	
n V {attr} X max n = word size	
MODIFIERS (mod) and ATTRIBUTES (attr)	
*	inversion
-	negation
%	right justify or field has expression
:	truncation
\$	paging (relative addressing) ATTRIBUTE only, sets % and :
EXPRESSION OPERATORS	
+	add
-	subtract
*	multiply
/	divide
	} evaluated left to right
DESIGNATORS (des)	VARIABLE FIELD SUBSTITUTE (VFS)
B# binary	label
D# decimal	label\$
Q# octal	expression
H# hexadecimal	digits des digits {mod} constant name

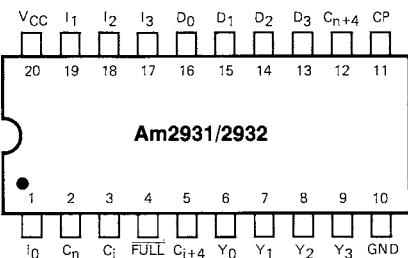
{ } = optional
 des = designator
 attr = attribute

mod = modifier
 digits = numbers

BLOCK DIAGRAM



Am2931/32 PIN CONNECTIONS



Am2931/2932

INSTRUCTIONS

Am2930 I ₄ I ₃ I ₂ I ₁ CC	IEN	Am2931 I ₃ I ₂ I ₁ CC	Am2932 I ₃ I ₂ I ₁ CC	Mnemonic	Instruction	Y ₀₋₃	PC
all	X	H	-	-	Disable	Notes 1, 3	NC
0	X	L	0	0	PRST	0	PC
1	X	L	1	4	FPC		
2	X	L	-	8	FR	R	
3	X	L	2	-	FD	D	
4	X	L	4	-	FRD	Fetch R + D	R+D+C _n
5	X	L	3	-	FPD	Fetch PC+D	PC+C _n +C _n
6	X	L	-	9	FPR	Fetch PC+R	PC+R+C _n
7	X	X	-	-	FSD	Fetch S+D	S+D+C _n
8	X	L	-	10	FPLR	Fetch PC→R	PC
9	X	X	5	-	FRDR	Fetch R→D-R	R+D+C _n
10	X	X	12	15	PLDR	Load R	
11	X	X	-	6	PSHP	Push PC	PC
12	X	X	-	2	PSHD	Push D	PC
13	X	X	13	3	POPS	Pop S	S
14	X	X	-	-	POPP	Pop PC	PC
15	X	X	-	-	PHLD	Hold	PC (Note 3)
16-31	H	L	-	-	Fail Condition (do FPC)	PC	
16	L	L	-	11	JMPR	Jump R	R
17	L	L	6	5	JMPD	Jump D	D
18	L	L	-	-	JMPZ	Jump zero	0
19	L	L	8	-	JPRD	Jump R+D	R+D+C _n
20	L	L	-	12	JPPD	Jump PC+D	PC+D+C _n
21	L	L	7	-	JPPR	Jump PC+R	PC+C _n +C _n
22	L	L	-	13	JSBR	JSB R	R
23	L	L	9	-	JSBD	JSB D	D
24	L	L	-	-	JSBZ	JSB zero	0
25	L	L	11	-	JSRD	JSB R+D	R+D+C _n
26	L	L	-	10	JSPD	JSB PC+D	PC+D+C _n
27	L	L	-	14	JSPR	JSB PC+R	PC+C _n +C _n
28	L	L	14	7	RTS	Return S	S
29	L	L	-	-	RTSD	Return S+D	S+D+C _n
30	L	L	-	-	CHLD	Hold	PC (Note 3)
31	L	L	15	1	PSUS	Suspend	Z (Note 2, 3)
						NC	NC

Notes:

- When IEN is HIGH, the Y outputs contain the same data as when IEN is LOW, as determined by CC and I_0-4 .
- Z = High impedance state (OFF).
- Clock is disabled internally.

NEW CIRCUITS COMING

Am2934 Program Control Unit

Am2940 DMA Address and Word Count Generator