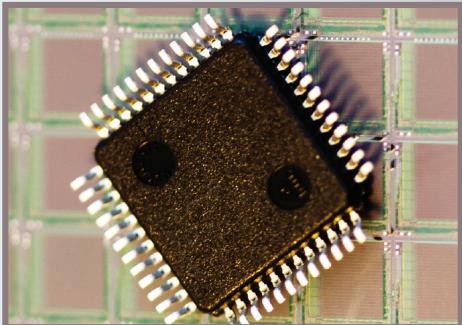
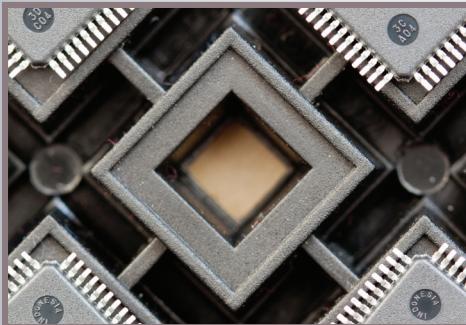
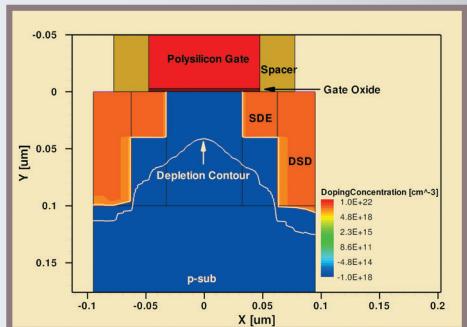
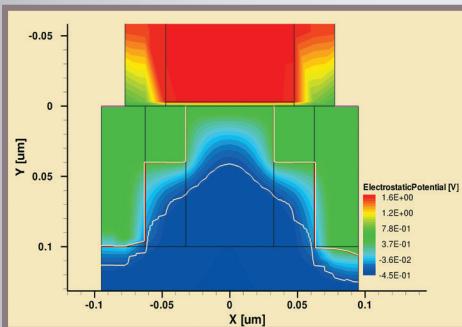


# TECHNOLOGY COMPUTER AIDED DESIGN

## Simulation for VLSI MOSFET



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**Edited by**  
**Chandan Kumar Sarkar**



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*To our family members*



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# *Contents*

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Preface.....	.ix
The Editor.....	xiii
Contributors.....	xv
<b>1 Introduction to Technology Computer Aided Design .....</b>	<b>1</b>
<i>Samar K. Saha</i>	
<b>2 Basic Semiconductor and Metal-Oxide-Semiconductor (MOS) Physics.....</b>	<b>45</b>
<i>Swapnadip De</i>	
<b>3 Review of Numerical Methods for Technology Computer Aided Design (TCAD) .....</b>	<b>145</b>
<i>Kalyan Koley</i>	
<b>4 Device Simulation Using ISE-TCAD .....</b>	<b>155</b>
<i>N. Mohankumar</i>	
<b>5 Device Simulation Using Silvaco ATLAS Tool .....</b>	<b>187</b>
<i>Angsuman Sarkar</i>	
<b>6 Study of Deep Sub-Micron VLSI MOSFETs through TCAD .....</b>	<b>237</b>
<i>Srabanti Pandit</i>	
<b>7 MOSFET Characterization for VLSI Circuit Simulation .....</b>	<b>267</b>
<i>Soumya Pandit</i>	
<b>8 Process Simulation of a MOSFET Using TSUPREM-4 and Medici....</b>	<b>363</b>
<i>Atanu Kundu</i>	
<b>Index .....</b>	<b>411</b>



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## *Preface*

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In the era of System-on-Chip (SoC) fabricated with ultra-deep sub-micron complementary metal-oxide-semiconductor (CMOS) technology, the semiconductor industry has to keep pace with the increased performance-capacity demands from consumers. The current sub-90 nm CMOS technology poses several critical challenges to very large scale integrated (VLSI) circuit and device designers regarding the characteristic behavior and performance of MOS transistors. In addition, there is huge pressure on the designers for reduction of the design time for economic reasons. To cope with issues like design productivity gap and yield drop and also to ensure correct behavior of each device, there is a need to involve computer aided design (CAD) methodologies and design automation tools. Technology computer aided design (TCAD) is an electronic design automation (EDA) tool that models the semiconductor device operation and fabrication based on fundamental physics through the computer aided simulations for design and optimization of semiconductor processing technologies and devices. Research and development (R&D) cost and time for electronic product development can be reduced by taking advantage of TCAD tools, thus making TCAD indispensable for modern VLSI devices and process technologies. TCAD simulation is gaining importance because it is prohibitively expensive for academia as well as for the several fab-less design industries to use silicon prototype for design verification.

The motivation for editing this volume on TCAD simulation of VLSI MOSFET came about when I was looking for student-level reference materials on TCAD simulation tools while teaching courses for postgraduate and senior undergraduate students. However, I could not find an appropriate book and was thus compelled to teach the course by consulting various user guides and manuals supplied with TCAD software and some semiconductor device textbooks. However, none of these caters to the intended purpose of introducing the physics of TCAD simulations to the students. Therefore, I found that there is a need for a book to provide the most up-to-date and comprehensive source of TCAD simulation of VLSI MOSFETs with an emphasis on the fundamental theory and the underlying physics.

This book is intended for senior undergraduate and postgraduate students of electrical and electronics engineering disciplines and for researchers and professionals working in the area of electronic devices. The purpose of the present edited volume is to rapidly disseminate to them the fundamental concepts and underlying physics of TCAD simulation of MOSFETs. The objectives of this book are to introduce the advantages of TCAD simulations for device and process technology characterization, to introduce the fundamental physics and mathematics involved with TCAD tools, to expose readers

to two of the most popular commercial TCAD simulation tools, Silvaco and Sentaurus, to characterize performances of VLSI MOSFETs through TCAD tools, and to familiarize readers with compact modeling for VLSI circuit simulation. This volume provides the reader with comprehensive information and a systematic approach to the design, characterization, fabrication, and computation of VLSI MOS transistors through TCAD tools.

The chapters contain different levels of difficulty. Several example programs are supplied for illustration of the software tools and related physics. The book therefore provides a desirable balance between the basic concepts, equations, physics, and recent technologies of MOS transistors through TCAD simulation. The book is organized into eight chapters that encompass the field of TCAD simulation for VLSI MOSFET.

Chapter 1 provides an overview of the role, need, and advantages of TCAD tools in design, characterization, and fabrication of VLSI MOS transistors. The evolution of modern TCAD and its challenges are also provided. Chapter 2 reviews and analyzes the basic concepts and physics involved with nanoscale MOS transistors. The physical approach to the tools is described by basics of band theory, Poisson's equation, continuity equation, drift diffusion (DD), and hydrodynamic models. The physics of the scattering mechanisms and different mobility models used in TCAD simulations are discussed. Chapter 3 describes the basics and importance of numerical solution techniques applicable to TCAD. The numerical solution of the DD equations coupled with Poisson's equation and its application to semiconductor device modeling is described. Chapter 4 provides a detailed overview of the two-dimensional/three-dimensional (2D/3D) device simulator Synopsys Sentaurus TCAD. The various tools involved are introduced in a comprehensive manner. The different software-related aspects of this tool for device simulations are described. Complete design examples explaining step by step the construction, simulation, and performance extraction of MOS transistors are provided. Chapter 5 attempts to present the MOSFET simulation using Silvaco TCAD tools. From basic syntax to choice of a complex model is presented in this chapter with emphasis on the usage of the SILVACO simulation software. An overview of the software developed by Silvaco to meet simulation needs of researching conventional and advanced MOSFET structures is also presented. The discussion is presented with examples to perform simulations of different types of MOSFETs. Chapter 6 discusses in detail the physics of nanoscale MOS transistors through TCAD simulations. The various short channel effects involved with nanoscale MOS transistors are demonstrated through actual TCAD simulation results. Different technology aspects and engineering techniques for future MOSFETs are also introduced. Chapter 7 presents a comprehensive overview of compact modeling of MOS transistors for use in VLSI circuit simulation. The mathematical models for characterizing various ultra-deep sub-micron effects of sub-65 nm MOS transistors are introduced. The effects are demonstrated through actual simulation program with integrated circuit emphasis (SPICE)

simulation results using industry standard compact models. The various circuit performances of MOS transistors are discussed. Chapter 8 addresses process simulation of MOSFET using TSUPREM-4. The chapter is devoted to bringing the key fabrication issues and their implementation in TCAD process simulation tool TSUPREM-4. It also considers how the output of process simulator TSUPREM-4 can be linked to device simulator MEDICI in order to analyze the performance of the fabricated device. An extensive list of references is provided at the end of each chapter for more elaborate discussion of the issues and to motivate readers to engage in further research.

I wish to congratulate all contributors and their peers. Their convictions and efforts were key to the success of this enterprise. The compilation of this book would not have been possible without the dedication and efforts of all the contributing authors. Special thanks go to Gagandeep Singh and Laurie Schlags and staff members of CRC Press for their responsiveness and immense patience demonstrated throughout the publishing process of this book.

**C.K. Sarkar**



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## *The Editor*

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In 1980, Sarkar received the British Royal Commission Fellowship to work at Oxford University. He worked as a visiting scientist at the Max Planck Laboratory in Stuttgart, Germany, as well as at Linko Pink University in Sweden. Sarkar also taught in the Department of Physics at Oxford University, and was a distinguished lecturer of the IEEE EDS.

Sarkar has served as a senior member of IEEE and was chair of the IEEE EDS chapter, Calcutta Section, India. He served as Fellow of IETE, Fellow of IE, Fellow of WBAST, and member of the Institute of Physics, United Kingdom.

His research interests include semiconductor materials and devices, VLSI devices, and nanotechnology. Sarkar has published and presented more than 300 research papers in international journals and conferences and also mentored 21 Ph.D.s.



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# 1

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## *Introduction to Technology Computer Aided Design*

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Samar K. Saha

### CONTENTS

1.1	Technology Computer Aided Design (TCAD) .....	1
1.1.1	Process CAD.....	3
1.1.2	Device CAD .....	4
1.2	A Brief History of TCAD .....	5
1.2.1	History of Device CAD .....	5
1.2.2	History of Process CAD.....	9
1.3	Motivation for TCAD .....	10
1.3.1	Motivation for Device CAD.....	10
1.3.2	Motivation for Process CAD .....	12
1.4	TCAD Flow for IC Process and Device Simulation .....	15
1.4.1	Generation of Simulation Structure .....	15
1.4.2	Verification of the Robustness of Simulation Structure .....	16
1.4.3	Calibration of Physical Models .....	18
1.4.4	Coupled Process and Device Simulation Flow .....	22
1.5	TCAD Application .....	23
1.5.1	TCAD in Device Research .....	23
1.5.1.1	Double-Halo MOSFET Devices.....	24
1.5.1.2	Sub-90 nm Split-Gate Flash Memory Cells.....	27
1.5.2	TCAD in Fabrication Technology Development (TD) .....	32
1.6	Benefit of TCAD in TD Projects .....	35
1.7	Summary.....	36
	References.....	37

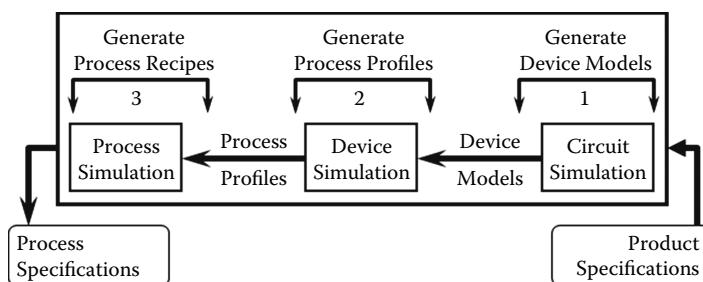
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### **1.1 Technology Computer Aided Design (TCAD)**

Technology computer aided design (CAD), commonly known as *technology CAD* or *TCAD*, is the electronic design automation that models integrated circuit (IC) fabrication and device operation. TCAD is the art of abstracting IC electrical behavior by critical analysis and detailed understanding

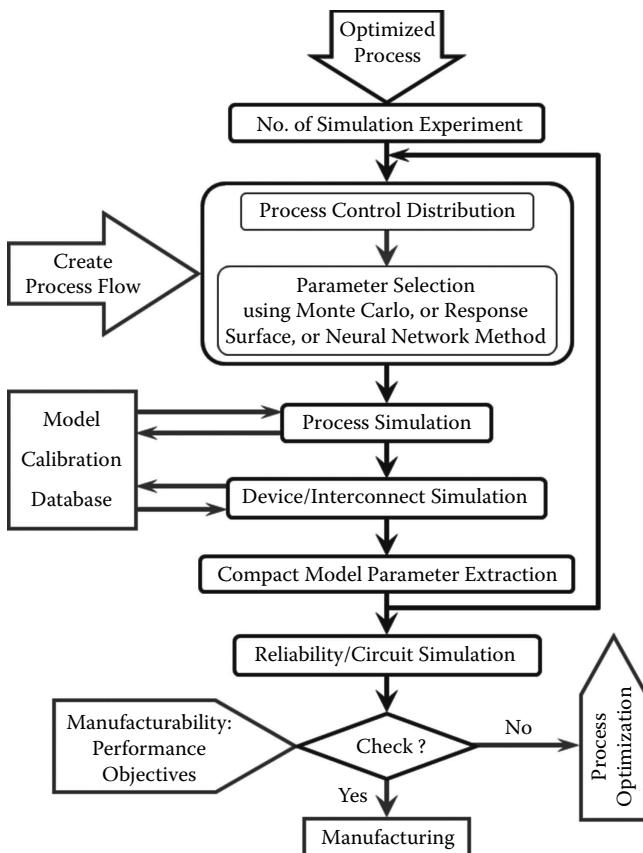
of process, device, and circuit simulation data. In general, TCAD includes *lithography modeling* to simulate the imaging of the mask by the lithography equipment, photoresist characteristics, and processing; *front end process modeling* for simulating the physical effects of manufacturing steps used to build transistors up to metallization; *device modeling* using hierarchy of physically based models for the operational description of active devices; *compact modeling* for active, passive, and parasitic circuit components; *interconnect modeling* to analyze the operational response of back-end architectures; *reliability modeling* for simulating the reliability and related effects on process, device, and circuit levels; *equipment modeling* for simulating the local influence of the equipment on each point of the wafer, especially in deposition, etching, and chemical-mechanical polishing (CMP) processes; *package simulation* for electrical, mechanical, and thermal modeling of chip packages; *materials modeling* to predict the physical and electrical properties of materials; *modeling for design robustness, manufacturing, and yield* to simulate the impact of process variability and dopant fluctuations on IC performance and determine design specifications for manufacturability and yield of ICs; and *numerical techniques* including grid generators, surface-advancement techniques, solvers for systems of partial differential equations (PDEs), and optimization routines [1,2].

TCAD offers capabilities to analyze how structural factors such as the geometry and processes conditions influence the electrical behavior of devices and circuits. Simulation data help in quantifying the details of the behavioral models for ICs at the transistor and circuit levels and show physical limitations at the processing and manufacturing levels [3,4]. By reverse modeling, the extended TCAD tools can be used to develop IC fabrication technology from product concept (i.e., from the product specification to IC fabrication technology as shown in Figure 1.1) [1]. The extended TCAD tools can also be used to assess the manufacturability of IC fabrication processes as shown in Figure 1.2 [1,5].



**FIGURE 1.1**

Extended TCAD use to generate product-specific IC process recipe by reverse modeling; in this approach, the sequential steps 1, 2, and 3 represent use of circuit, device, and process CAD, respectively. (From S.K. Saha, Managing technology CAD for competitive advantage: An efficient approach for integrated circuit fabrication technology development, *IEEE Trans. Eng. Manage.*, vol. 46, no. 2, pp. 221–229, May 1999. With permission.)

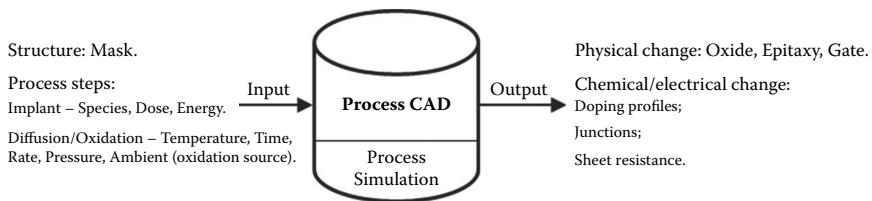
**FIGURE 1.2**

Flowchart showing the use of extended TCAD to evaluate the manufacturability of IC fabrication technology with respect to the target specifications. (From S.K. Saha, Managing technology CAD for competitive advantage: An efficient approach for integrated circuit fabrication technology development, *IEEE Trans. Eng. Manage.*, vol. 46, no. 2, pp. 221–229, May 1999. With permission.)

In the microelectronics industry, TCAD is widely referred to as *front-end process modeling* or *process CAD* and *device modeling* or *device CAD*. Therefore, unless otherwise specified, hereafter in this chapter TCAD refers to IC front-end process CAD and device CAD only.

### 1.1.1 Process CAD

Process CAD refers to front-end process modeling that includes the numerical simulation of the physical effects of IC processing steps used to fabricate transistors up to metallization. The process CAD is used to simulate the semiconductor processing steps such as oxidation and diffusion, deposition

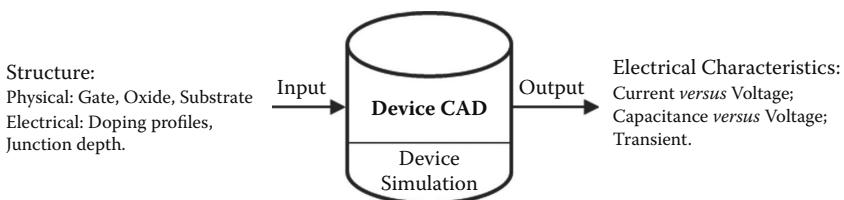
**FIGURE 1.3**

IC fabrication process simulation using process CAD to generate input file for device simulation; the “physical change” refers to the structural change of the device such as the oxide growth, whereas the “chemical change” refers to impurity diffusion; process CAD includes physical process models to perform numerical process simulation.

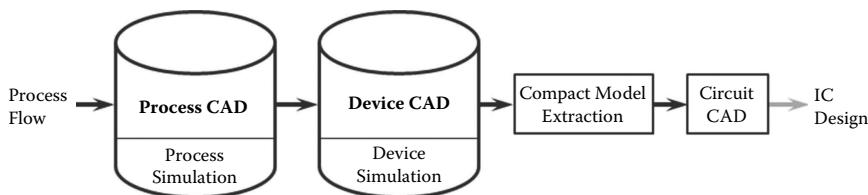
and etching, ion implantation, and annealing, and generate input data files for the device simulator as realistically as possible based on the microscopic information as shown in Figure 1.3 [1–5]. In the area of process simulation, physical models for process technology were rather limited in the 1960s and 1970s, and the sophisticated process simulators with multidimensional models were not necessary for the large device geometry used during that time. In recent years, the physical understanding of IC processes has advanced significantly. Moreover, the current evolution of IC devices into the nanoscale regime necessitates accurate multidimensional process models.

### 1.1.2 Device CAD

Device CAD refers to numerical simulation of IC device operation as shown in Figure 1.4. In general, the device CAD includes a suite of physical models describing carrier transport in materials. Device models range from the simple drift diffusion, which solves Poisson and continuity equations, to more complex and computationally challenging models such as the energy balance, which solves some higher moment simplification of the Boltzmann transport equation (BTE). In addition, the complex physics of today’s nanoscale devices mandates the use of Monte Carlo (MC) codes, which stochastically solves BTE, and the use of Schrödinger solvers that account for quantum

**FIGURE 1.4**

IC device simulation using device CAD to generate electrical characteristics of IC devices for circuit analysis; device CAD includes physical device models to perform numerical device simulation.

**FIGURE 1.5**

Process and device CAD are synergistically linked to predict the influence of various IC processing steps on device and circuit performance; here circuit CAD represents a modeling tool to analyze circuit performance.

mechanical (QM) effects in metal-oxide-semiconductor field-effect transistor (MOSFET) devices. The choice of the appropriate model depends on the problem and the level of detail required. Despite the significant advances of both numerics and physics, continuous development is required to meet the increasingly challenging industry needs for device exploration, scaling, and optimization. Therefore, the ability of device CAD to accurately model today's device performance and predict tomorrow's device limitations is of utmost importance [3,4].

Though the process CAD and device CAD refer to numerical simulation of different areas of computational electronics, they are synergistically linked. An understanding of the various IC processing steps is crucial to predicting device and circuit performance as shown in Figure 1.5.

## 1.2 A Brief History of TCAD

During the last four decades, technology CAD has evolved from one-dimensional (1D) Direct current (DC) or steady-state simulation only during the 1970s to full two-dimensional (2D) and three-dimensional (3D) simulation of today's complex very large scale integrated (VLSI) circuit fabrication processes and devices. This evolution of process and device CAD has been possible due to advancements in the computer technology and mathematical models, thus providing cost-effective and efficient multidimensional numerical analysis of IC fabrication processes and devices. A large number of researchers have contributed to the evolution of TCAD. In this section, we present only a brief history of the major development in the device and process CAD leading to commercial TCAD tools.

### 1.2.1 History of Device CAD

The seminal work of Gummel in 1964 led to the foundation of device CAD. For the first time, Gummel reported 1D simulation results of bipolar junction transistors (BJTs) by sequentially solving the three PDEs in the drift-diffusion

system using an iterative method [6]. Gummel's numerical approach was further developed and applied to simulate p-n junction by De Mari in 1968 [7,8] and Read diode oscillator by Scharfetter and Gummel [9] in 1969. In the 1969 publication, Scharfetter and Gummel reported a methodology for stable upwind discretization of the transport equations [9]. This method is still almost universally used and is responsible for making device simulation a computationally feasible design activity.

In 1968, the first 2D numerical solution of Poisson's equation for a MOSFET was reported by Loeb et al. [10] and, in parallel, by Schroeder and Muller [11]. In 1969, the 2D simulation results on planar devices were published by Barron on MOSFETs [12] and Kennedy and O'Brien on junction field-effect transistors (JFETs) [13] by solving the Poisson equation and one continuity equation. In the same year, Slotboom reported the 2D simulation results on BJTs using the full two-carrier system [14], and in 1971 Reiser reported the first 2D transient simulation results of metal-semiconductor field-effect transistors (MESFETs) [15].

During the 1970s, the major numerical techniques for 2D device simulation [16,17], including the first finite element analysis of the semiconductor equations [18,19], were reported. The finite element method can be considered a precursor to the development of the more general-purpose tools commonly used in the 1980s. In the late 1970s, some of the first publicly available device CAD tools were released including the first version of the CADDET<sup>H</sup> programs from Hitachi [20] to simulate single carrier field-effect transistor (FET) structures, the SEDAN program from Stanford University [21] to simulate 1D bipolar device phenomena, and a special-purpose MOSFETs simulation program MINIMOS from Vienna [22].

Though the work on a general-purpose, non-planar multidimensional device CAD program began in the mid-1970s, the first device simulation program successfully used for bipolar device analysis was FIELDAY [23] from IBM. Besides FIELDAY, the other first generation non-planar codes include the GEMINI program in 1980 [24] which solved only Poisson's equation and PISCES-I in 1982 [25] which solved Poisson and a single continuity equation in the steady-state, both from Stanford University.

The real impact of a general-purpose device CAD tool came in the mid-1980s with the development of programs like PISCES-II at Stanford University [26,27], DEVICE at AT&T Bell Laboratories [28,29], BAMBI at Vienna [30], and HFIELDS [31] at the University of Bologna. Each of these programs worked for two carriers, allowed arbitrary device non-planarities, and included a more comprehensive set of materials, physical models, and simulation capabilities than the prior state-of-the-art. However, the primary advantages of these tools were improved computational methods such as the discretization and grid generation, non-linear and linear solution techniques that made device simulation practical for device designers. It is worth noting that PISCES-II has been commercialized by Technology Modeling Associates (TMA), now Synopsys [32], and Silvaco [33] and is the source of widely used device simulators MEDICI and ATLAS, respectively.

Major advances in the numerical solution of BTE [34] also began in the late 1970s. In 1979, the initial 2D MC device simulation results were reported by Warriner [35]; in 1982, the PDE for energy transport was first treated numerically in 2D by Cook and Frey [36]; in 1984, Fukuma and Uebbing used the energy balance model to predict velocity overshoot in silicon MOSFETs [37] and the hot carrier post-processors with lucky electron based approach were first implemented by Siemens [38]; in 1985, the first realistic 2D simulations of hetero-structure devices were reported from the University of Illinois [39]; in 1986, Laux and Warren reported the coupled 2D Schrödinger-Poisson solver and directly introduced quantum mechanics in device CAD [40]; in 1988, an MC post-processor for silicon MOSFETs was developed at Bologna [41]; and the first general-purpose code incorporating hydrodynamic solutions was implemented in HFIELDS [42].

With the increasing complexities of IC devices due to continuous downscaling of feature size, the 3D numerical analysis became critical. The first paper using 3D device simulation of MOSFET narrow channel effects was published in 1980 [43]. The FIELDAY was the first of many programs extended into 3D in 1981 [44] by extending the grid uniformly in the depth plane. Also, in 1981 and 1982, the 3D device simulation results of narrow channel effects were published using the simulator WATMOS [45,46] which used a finite difference scheme numerical solution of Poisson's equation. Following the approach of FIELDAY, almost every 2D simulation program has been extended to 3D by extending the grid uniformly in the depth plane [47–52]. The FIELDAY program solved Poisson's equation and both carrier continuity equations. The program was later enhanced to include the hydrodynamic energy-balance equations, Fermi-Dirac carrier statistics, lattice energy equation, and incomplete ionization [53]. Thus, both drift diffusion and hydrodynamic simulations were possible using FIELDAY.

In 1985, Hitachi announced CADDET as a 3D device simulator designed to run on a supercomputer [49]. CADDET solves both Poisson's equation and two current continuity equations using conjugate gradient-based methods for non-symmetric linear systems; distinguishes between three different materials, namely semiconductors, insulators, and metals; and implemented advanced physical models [49]. Another 3D simulator was developed by Toshiba in 1985, called TOPMOST [54,55]. TOPMOST was designed to analyze MOS structures and solve the semiconductor equations for the drift-diffusion case. Both 1D and 2D simulations could be performed by pseudo-1D and pseudo-2D device models by reducing the number of points in the omitted directions. TOPMOST was used to study the effect of the gate structure on the output characteristics [54] and subthreshold swing in 3D MOSFETs [55].

In 1987 Vienna announced 3D device simulator, MINIMOS Version 5 [56]. MINIMOS-5 is one of the first 3D device simulators [56–59] for MOSFET structures, SOI transistors, and gallium arsenide MESFETs. MINIMOS-6, released in 1994 [60], supports transient analysis and MC modeling to replace

the drift diffusion approximation in critical device areas. The fundamental semiconductor equations, consisting of Poisson's equation and two carrier continuity equations, are solved numerically in 2D or 3D space. MINIMOS is able to simulate planar and non-planar device structures along with AC small signal analysis and transient simulations.

The reported 3D device CAD tools from the industry include SMART [61] from Matsushita in 1987, PADRE [62] from Bell Laboratories, SITAR [63] from Siemens in 1988, MAGENTA [64] from Microelectronics and Computer Technology Corporation in 1989, and SIERRA [51] from Texas Instruments in 1989. SIERRA solves Poisson's equation and the carrier continuity equations for static, AC small signal, and transient cases. Based on SIERRA, TMA developed their first 3D device simulator known as DAVINCI in 1991 [32]. DAVINCI has been used to investigate the effects of radiation on DRAM cells and narrow channel effects in MOS structures. In January 1998, TMA merged with Avant!, and in 2001 Avant! merged with Synopsys, and DAVINCI has been the starting basis of the TAURUS 3D DEVICE program from Synopsys [32].

Some of the other reported 3D device CAD tools include HFIELDS-3D [65–67] from the University of Bologna in 1989, SECOND [68–70] from ETH Zürich and STRIDE [71] from Stanford University in 1991, FLOODS [72] from the University of Florida in 1994, and DESSIS [73] in 1996. The development of DESSIS began in 1992 in collaboration with Bologna, ETH Zürich, Bosch, and ST Microelectronics [73]. DESSIS is created by merging the device simulators HFIELDS from Bologna and SIMUL from ETH and circuit simulator BONSIM from Bosch to enable efficient mixed-mode IC circuit/device analysis [73]. In 1993, Integrated Systems Engineering (ISE) was founded and took over the simulator. In 2004 ISE merged with Synopsys which took over DESSIS and is the basis of commercial Sentaurus device simulator from Synopsys [32].

With the evolution of IC technology and devices, TCAD is continuously evolving. Another notable device CAD tool includes MINIMOS-NT [74] reported in 1997. MINIMOS-NT is a generic 2D device simulator that allows the modeling of high electron mobility transistors. A new method is used which divides the device region into several sub-domains, referred to as segments, each segment with its specific physical models. The segmentation of device region allows appropriate physical models to be used where required, such as a hydrodynamic model in the channel region and drift diffusion solution for the non-critical region of the device. This increases the overall efficiency of device simulation with the desired accuracy. Also, with the ongoing reduction of feature sizes, atomistic simulations become reasonable to study the effects of random discrete doping in the channel region [75–77].

The device CAD tools are continuously evolving, and mathematical models describing the performance of advanced devices are continuously implemented, especially in the commercial TCAD tools to model today's complex IC devices.

### 1.2.2 History of Process CAD

After the invention of ICs in 1958, the IC industry was dominated by BJT technology through the 1960s. However, in the 1970s MOSFET technology began to overtake BJT technology in terms of the functional complexity and level of integration. Since the 1980s, complementary MOS (CMOS) technology with its cost-effective technology solution has become the pervasive technology for ICs. With aggressive scaling of MOSFETs in the mid-1970s, transistor dimensions soon reached the point at which first-order assumptions about the physical effects and dopant distributions began to break down. For the MOSFETs, the intrinsic device problem such as output conductance, velocity saturation, and subthreshold behavior all received substantial interest and effort. TCAD became critical to understand the many interrelated process and device effects in MOSFETs.

By the mid-1970s, the critical role of processing technology in establishing device characteristics was evident. Many important interrelated process and device effects were identified by means of computer coupled analysis tools. Industry leaders such as IBM and Texas Instruments had aggressive efforts to model process physics and relate these models to device characteristics and circuit statistics. A unified process and device simulator, the SITCAP program was developed at Katholieke University, Leuven, Belgium [78]. This program inputs process specifications such as processing times and temperatures along with simple mask geometries to output  $I-V$  and  $C-V$  curves, along with selected SPICE model parameters. And, a process analysis program CASPER was jointly developed at Lehigh University (Bethlehem, Pennsylvania) and AT&T Bell Laboratories (Allentown, Pennsylvania) [79].

In 1977, the first version of 1D process simulator, SUPREM, was developed and released by Stanford [80]. Since then, the process models in SUPREM have developed substantially and evolved due to ongoing efforts at Stanford and at industrial and other research laboratories worldwide. Versions II and III of SUPREM were released in 1978 and 1983, respectively [81,82]. The release of a process simulator had a tremendous impact on the accuracy to which device simulations could be performed. Process simulation has continued to improve dramatically since the release of SUPREM. And the notable events in the evolution of process CAD include the development of the full 2D simulators such as SUPRA from Stanford [83] in 1982 and BICEPS from AT&T Bell Laboratories [84] in 1983. In 1986, the most advanced 2D process simulation program SUPREM-IV was developed at Stanford [85]. The SUPREM-IV included more physically based models including point defect calculations and stress dependent oxidation required for modeling ultra-small device structures. A 2D SUPREM-IV process simulation program has been commercialized by Crosslight [86], Sillvaco [33], and TMA [32] as CSUPREM, ATHENA, and TSUPREM4, respectively.

In 1992, ISE (now Synopsys [32]) developed 1D and 2D process simulators TESIM and DIOS, respectively. DIOS was a widely accepted tool prior to the introduction of the Sentaurus process by Synopsys in 2005.

The development of 3D process CAD tools began in the mid-1980s for accurate modeling of ultra-small geometry device technology [87,88]. In 1993, FLOOPS was released from the University of Florida [89] and became the source of Synopsys 3D process simulator, Sentaurus process that was released in 2005 [32]. Other 3D process simulators include PROPHET from AT&T Bell Laboratories [90] released in 1994 and Taurus 3D process from TMA released by Avant! in 1998 [32].

The history of commercial TCAD began with the foundation of TMA in 1979. TMA was the first commercial supplier of TCAD software that was the result of the TCAD research program at Stanford University under the supervision of Professor Dutton and Professor Plummer. Currently, the major sources of commercial TCAD tools are Silvaco [33] and Synopsys [32]. Synopsys TCAD tools include Taurus process/device TSUPREM4/MEDICI for 2D TCAD and Sentaurus process/device for both 2D and 3D TCAD. Silvaco TCAD tools include ATHENA for 2D process simulation, ATLAS for 2D device simulation, and Victory process/device for 3D simulation.

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## 1.3 Motivation for TCAD

The major motivation for the use of TCAD in the semiconductor industry is the cost-effective and efficient development of IC fabrication technology using device CAD to analyze device performance and process CAD to input realistic structural information from process flow to device CAD [1,5].

### 1.3.1 Motivation for Device CAD

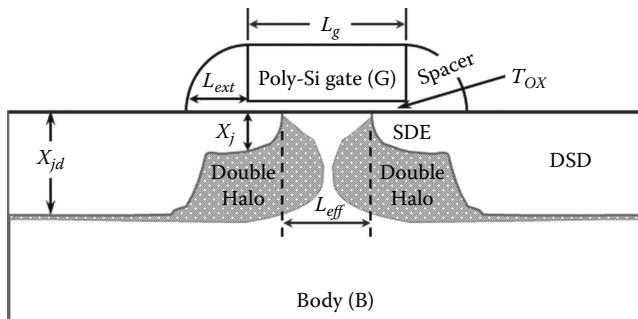
The motivation for the use of device CAD in IC device analysis is the optimization of device performance for specific applications. This optimization is a complex task due to the complexities of the equations describing semiconductor device performance. For semiconductor devices, particle conservation is modeled by several cross-coupled non-linear PDEs: the interaction of charged particles due to electric fields is modeled by Poisson's equation, and the particle concentrations relating to particle fluxes and generation and recombination are modeled by continuity equations. Also, electron and hole concentrations are exponentially related to potentials through Boltzmann, Fermi-Dirac, or other exponentially determined probability distribution functions. These equations are difficult to solve by hand, making computer aided analysis a desirable alternative. Again, by the introduction of the SPICE program from Berkeley in 1975, the circuit simulator became a useful design

tool, essentially replacing the bread-boarding of prototypes [91]. However, for accurate circuit analysis, compact device models, commonly known as SPICE models, are required. For the generation of SPICE models the device CAD became a necessity. Thus, the widespread use of circuit simulation also motivated the development and use of device CAD for IC device analysis.

Figure 1.5 illustrates the use of device CAD to generate compact models for circuit analysis. Compact models such as BSIM4 [92] provide an excellent framework to analyze different modes of MOSFET circuit behavior. However, in order for the BSIM4 model to be useful in practice, reliable values for the model parameters must be generated. Device CAD tools are useful for linking fabrication conditions to BSIM4 parameters. For example, the device simulator uses inputs such as device geometry, doping profiles, and bias conditions to generate data files for device characteristics such as capacitance ( $C$ ) and current ( $I$ ) versus voltage. The simulated data files are then used to extract BSIM4 model parameters for circuit analysis.

Another major motivation for using device CAD is to study the feasibility of realizing concept devices in manufacturing. As the MOSFET devices are scaled down, device performance is severely degraded by short channel effect (SCE), drain-induced barrier lowering (DIBL), quantum-mechanical (QM) effects, and so on. The use of device CAD is critical to minimize these physical effects and improve the device performance by optimizing the device structure. Figure 1.6 shows a nanoscale “double-halo” MOSFET device structure designed to suppress SCE, reduce DIBL and QM effects, and improve device performance [93–97].

The double-halo MOSFET structure as shown in Figure 1.6 includes a poly-silicon gate, a gate oxide ( $T_{OX}$ ), vertically and laterally non-uniform channel doping profiles, shallow source-drain extensions (SDEs), deep source-drain (DSD) regions, and two halo profiles: first around SDE and the second around DSD regions to control DIBL from SDE and DSD junctions, respectively. A



**FIGURE 1.6**

An idealized double-halo MOSFET device structure showing the basic technology elements:  $L_g$  and  $L_{eff}$  are the drawn and effective channel lengths, respectively,  $T_{OX}$  is the gate oxide thickness,  $L_{ext}$  is the spacer width, and  $X_j$  and  $X_{jd}$  are the junction depths of the source-drain extension (SDE) and deep source-drain (DSD) regions, respectively.

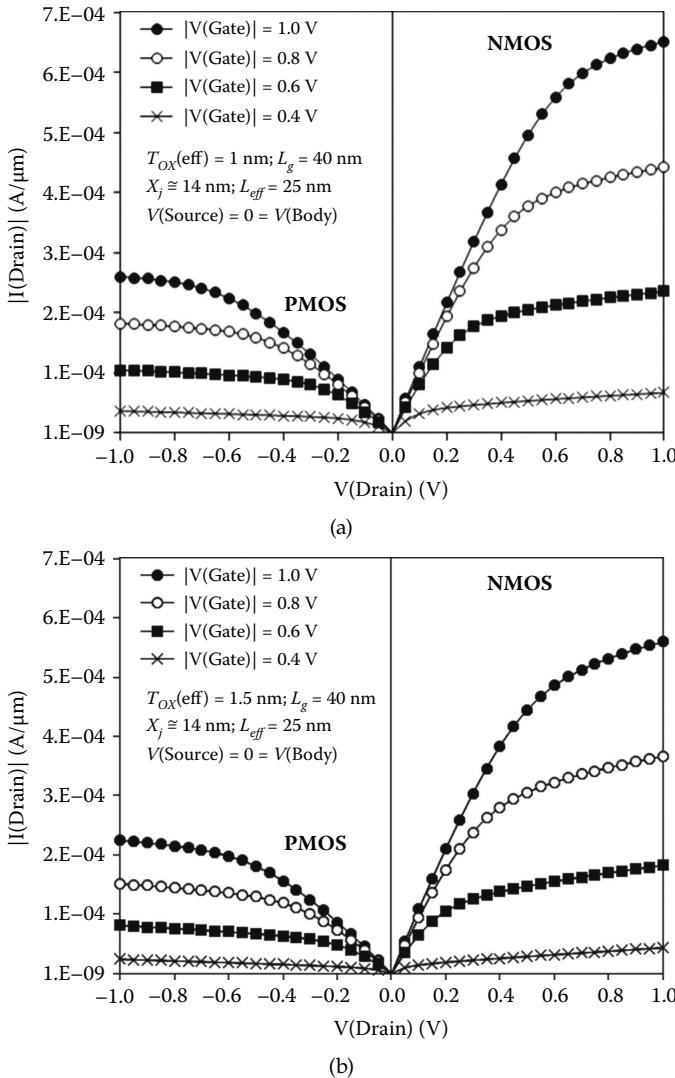
super-steep retrograde (SSR) or “low-high” channel doping profile with a low impurity concentration at the silicon/silicon-dioxide ( $\text{Si}/\text{SiO}_2$ ) interface and a higher peak concentration at a finite depth below the interface is used to provide the non-uniform vertical channel profile [98]. The SSR profile is optimized to achieve the target threshold voltage ( $V_{th}$ ) for the long and wide devices. The SSR profile also provides superior  $V_{th}$  control. The halo doping profiles are optimized to achieve the target leakage current for the nominal devices. In reality, the low-high channel doping profiles are achieved using multiple buried layers under an undoped epitaxial layer of appropriate thickness [99]. Because, in reality, the ion-implanted profiles are non-linear, more sophisticated 2D/3D device analysis tools are required for device optimization. Thus, the device CAD use is critical to optimize the halo doping profiles in conjunction with other key technology parameters such as  $T_{\text{Ox}}$  and SDE junction depth ( $X_j$ ) to realize the nanoscale double-halo MOSFETs in manufacturing.

In optimizing the double-halo device performance, it is critical to analyze the effect of scaling key technology parameters such as  $X_j$  and  $T_{\text{Ox}}$  on device performance. Figure 1.7 shows 2D device simulation results of drain current ( $I_{ds}$ ) versus source-drain voltage ( $V_{ds}$ ) with a given gate-to-source voltage ( $V_{gs}$ ). Two similar technologies are compared: one optimized for  $T_{\text{Ox}} = 1.5 \text{ nm}$ , and the other with  $T_{\text{Ox}} = 1.0 \text{ nm}$ . For both cases, the devices are optimized to achieve the same off-state leakage current,  $I_{off} \geq 10 \text{ nA}/\mu\text{m}$ . From Figure 1.7, we find that for small values of  $V_{ds}$ , the curves show almost identical values of  $I_{ds}$ . At higher  $V_{ds}$ , the device with the lower  $T_{\text{Ox}}$  shows substantially more current handling capability. Thus, both the technologist and the circuit designers are anxious to understand and control the dependencies of key technology parameters to realize the optimum circuit performance of double-halo CMOS technology. Therefore, the motivation to use device CAD is to understand the dependence of key building blocks of device structure on device and circuit performance.

### **1.3.2 Motivation for Process CAD**

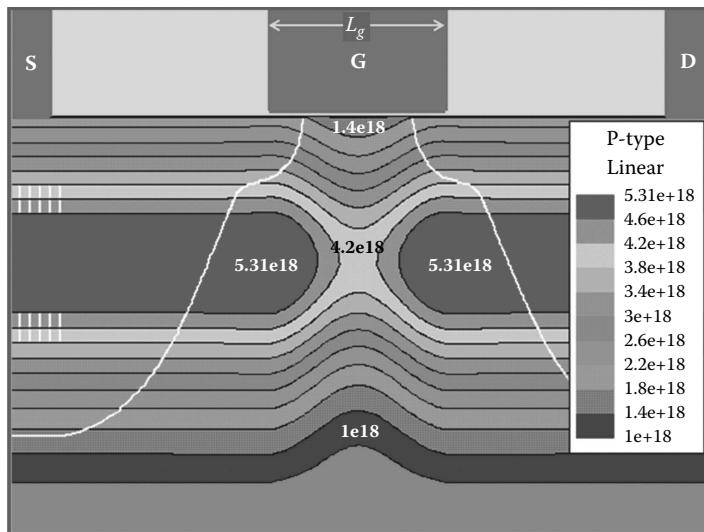
In the previous section, we have established the motivation for device CAD in determining circuit design parameters with reference to MOSFET devices. Now, let us discuss certain critical parameters in MOSFETs that depend directly on the quantitative features of the doping profiles within the device. Because doping profiles are determined by process variables such as ion implantation energy, total implanted dose, and drive-in time/temperature cycles, the dependence of device parameters on process variables provides motivation for process simulation.

For MOSFET devices,  $V_{th}$  and other device parameters are directly related to the distribution of the channel doping profile within the device structure. In order to produce accurate compact model parameters such as  $V_{TH0}$ ,

**FIGURE 1.7**

$I-V$  characteristics of double-halo MOSFETs for (a)  $T_{\text{OX}}(\text{eff}) = 1 \text{ nm}$  and (b)  $T_{\text{OX}}(\text{eff}) = 1.5 \text{ nm}$ ; the simulation data are obtained for 40 nm devices with  $L_{\text{eff}} = 25 \text{ nm}$  and optimized for  $|I_{\text{off}}| = 10 \text{ nA}/\mu\text{m}$  at  $|V(\text{Drain})| = 1 \text{ V}$ ;  $V(\text{Gate}) = V(\text{Source}) = V(\text{Body}) = 0$ . (From S. Saha, Scaling considerations for high performance 25 nm metal-oxide-semiconductor field-effect transistors, *J. Vac. Sci. Tech. B*, vol. 19, no. 6, pp. 2240–2246, November 2001. With permission.)

modeling  $V_{th}$  for large devices,  $K1$  and  $K2$  describing body effect,  $U0$  describing inversion layer carrier mobility,  $PDIBL1$  and  $PDIBL2$  describing DIBL, and so on, the device simulator must have an exact description of the channel doping profile in all dimensions. This accurate description of channel doping profile can be generated using process CAD.

**FIGURE 1.8**

Simulated 2D-doping contours of a typical double-halo nMOSFET device with laterally and vertically non-uniform p-type channel doping generated using device CAD MEDICI; 2D cross-section shows S, G, and D are the source, gate, and drain terminals, respectively, and the outline of SDE and DSD junctions. (From S. Saha, Device characteristics of sub-20-nm silicon nanotransistors, in *Proc. SPIE Conf. on Design and Process Integration for Microelectronic Manufacturing*, vol. 5042, pp. 172–179, July 2003. With permission.)

Figure 1.8 shows the 2D doping profile of the 25 nm double-halo MOSFET structure shown in Figure 1.6. A number of details of the technology are apparent from the cross sections shown. First, the 2D halo doping contours from the source and drain regions approach a peak at a certain depth from the Si/SiO<sub>2</sub> interface under the gate. The halo diffusion from the source and the drain regions has enhanced the p-type doping concentration at the center of the device under the gate region. With scaling  $T_{OX}$ , the doping distribution within the device changes both laterally and vertically. Calibrated process, especially, diffusion models are essential for accurate generation of a 2D doping profile within the active region of the simulation structure. Therefore, process simulation is critical to reproduce the doping distributions within the structure for accurate device simulation and compact model parameter extraction for circuit analysis.

Thus, the motivation to use process CAD is to couple the relevant fabrication information into the device CAD. The process CAD captures the critical aspects of the target fabrication process to accurately determine device models for circuit analysis and predict the limitations in device performance. For most device parameters, the exact description of doping profile is needed to obtain agreement between the simulated and measured data.

## 1.4 TCAD Flow for IC Process and Device Simulation

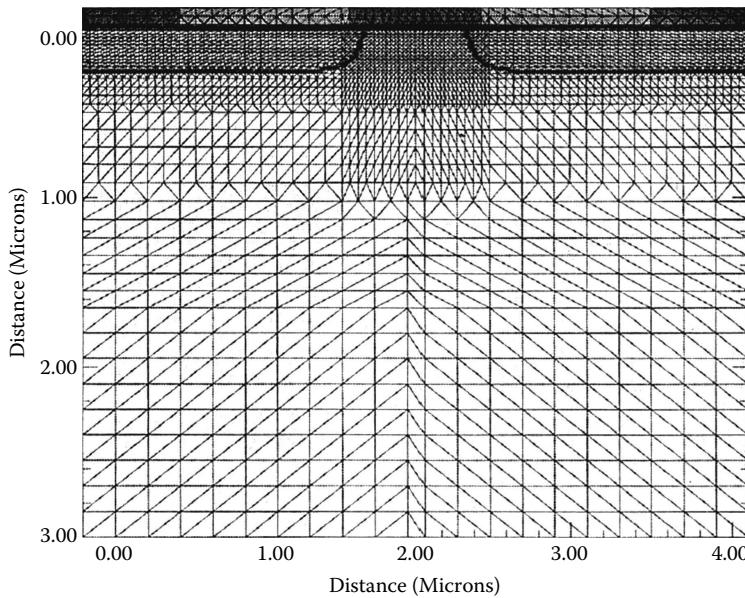
TCAD flow for IC process and device analysis includes the (1) generation of simulation structure to numerically solve the PDEs that model IC processing and device performance, (2) verification of the robustness of the simulation structure and sensitivity of simulation results on grid space, (3) calibration of physical models for accuracy and predictability, and (4) coupled process and device simulation.

### 1.4.1 Generation of Simulation Structure

The first step in the numerical approach is the discretization of the simulation domain in time and space. In this step, the device cross section is partitioned into sub-domains or small cells, each of which is evaluated at discrete time intervals. Then in each of these cells, the PDEs are approximated by algebraic equations that include only the values of the continuous dependent variables at discrete points in the domain and the knowledge of the structure of the functions approximating the dependent variables within each cell. In case of process modeling, the time and space must be partitioned in such a way so that the concentrations of the various impurities present are constant over each individual cell during each time increment along with the diffusivity and other physical parameters. Finally, the solution is computed at each discrete point, known as the mesh or grid, within the domain. The grid spacing must be sufficiently dense so that all the relevant features of the doping profile are accurately represented. The increments of time must be short enough to model important physical effects. On the other hand, it is important not to use excessively small intervals to avoid time-consuming and expensive numerical solutions. The detailed discretization technique is discussed in the literature [100].

The layout of a mesh or grid in a simulation structure is a very important aspect of the numerical solution of PDEs, as it directly determines how well the discrete model represents the actual problem. There are a number of considerations regarding grid selection. First, the points must be allocated to accurately approximate any physical quantities of interest including potentials, concentrations, fields, and currents, as well as any irregularities in the geometry of the domain. Second, because the overall computation time depends on the total number of grid points, grid points must be optimized for computational efficiency. Finally, the finer grid must be allocated in the active regions of device operation under the biasing conditions [3,101].

Solution variables such as potentials, doping, charge, and recombination appear in the PDEs. Therefore, high grid densities must be allocated in regions where any of these quantities undergo rapid changes (e.g., p-n junctions). Conversely, the spacing between points could be relaxed in areas where values remain relatively constant without adding any significant



**FIGURE 1.9**

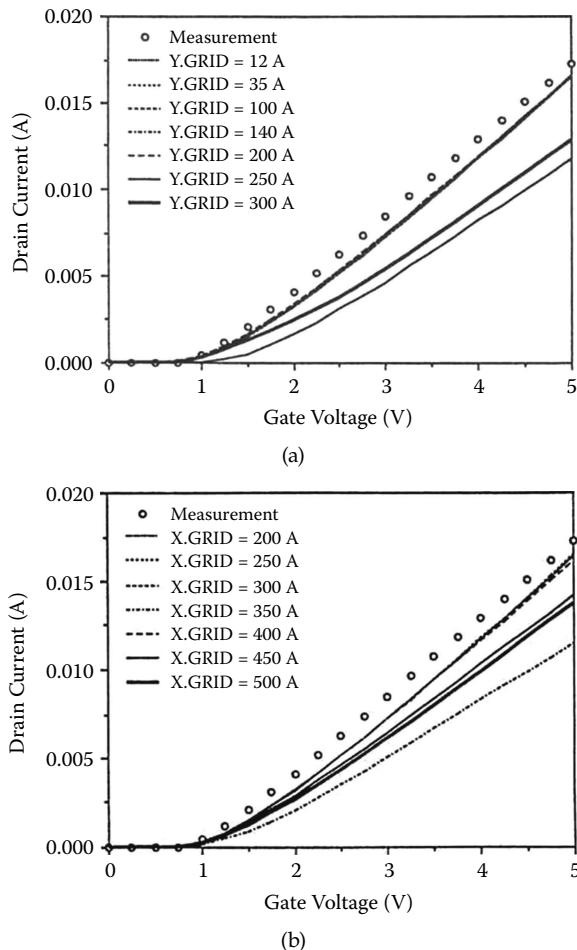
A typical optimized mesh of an LDD MOSFET simulation structure; grid is denser in the gate oxide and channel region as well as at the source-drain junction. (From S. Saha, MOSFET test structures for two-dimensional device simulation, *Solid-State Electron.*, vol. 38, no. 1, pp. 69–73, January 1995. With permission.)

contribution to the overall error (e.g., quasi-neutral regions deep inside the device). In addition, the simulation structure must be robust so that the simulated device performance is independent of grid density, and the robustness of the simulation domain; that is, sensitivity of simulation results on grid must be checked [101] after the structure generation. Figure 1.9 shows a typical robust mesh of a MOSFET simulation structure.

#### 1.4.2 Verification of the Robustness of Simulation Structure

In the previous subsection we discussed that an appropriate simulation domain is required to emulate the impurity distribution within the device as accurately as possible. Inaccurate mesh may cause fluctuation in the simulation results. Therefore, it is critical to check the robustness of the simulation structure by varying the grid space to generate grid-independent simulation results [101].

Figure 1.10 shows the sensitivity of simulated  $I$ - $V$  characteristics of nMOSFETs on grid allocation. Figure 1.10(a) shows the sensitivity of  $I$ - $V$  data on vertical grid space, Y.GRID in the channel at the  $\text{SiO}_2/\text{Si}$  interface. It is seen from Figure 1.10(a) that for  $\text{Y.GRID} \leq 200 \text{ \AA}$ , the magnitude of  $I_{ds}$  attains a maximum value and the electrical characteristics become insensitive to the

**FIGURE 1.10**

Sensitivity of grid density on MOSFET device performance; (a) sensitivity of vertical grid, Y.GRID on  $I_{ds}$  and (b) sensitivity of lateral grid, X.GRID on  $I_{ds}$ ; here  $L_g = 0.8 \mu m$ ,  $W = 40 \mu m$ , and  $T_{ox} = 15 \text{ nm}$ ; all data are obtained at  $V(\text{Drain}) = 5 \text{ V}$  and  $V(\text{Body}) = 0 = V(\text{Source})$ . (From S. Saha, MOSFET test structures for two-dimensional device simulation, *Solid-State Electron.*, vol. 38, no. 1, pp. 69–73, January 1995. With permission.)

values of Y.GRID at the surface. Figure 1.10(a) also shows that the magnitudes of the measured and simulated data are closer for  $\text{Y.GRID} \leq 200 \text{ \AA}$ . Thus, Y.GRID = 12 Å at the surface near the Si/SiO<sub>2</sub> interface generates robust test structures for device simulation and accurately models critical physical effects such as inversion layer quantization in the MOSFET channel [98].

Figure 1.10(b) shows the sensitivity of  $I$ - $V$  data on the lateral grid space, X.GRID in the channel region. It is also seen from Figure 1.10(b) that for

$X.\text{GRID} \leq 300 \text{ \AA}$ , the magnitude of  $I_{ds}$  attains a maximum value, and the device characteristics are independent of  $X.\text{GRID}$ . It is obvious from Figure 1.10(b) that the simulated and measured data are in close agreement for  $X.\text{GRID} \leq 300 \text{ \AA}$ . Thus,  $X.\text{GRID} \leq 200 \text{ \AA}$  can be used to reduce the uncertainty in the simulated electrical characteristics due to incorrect grid allocations and generate robust test structures for device simulation.

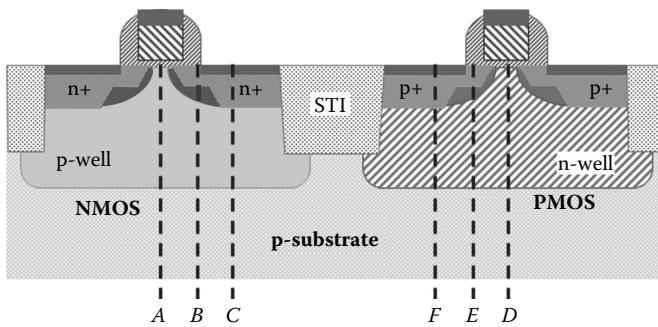
For simulation accuracy and computational efficiency, fine grid is allocated only in the regions of most physical importance as shown in Figure 1.9. The procedure to verify the robustness of the generated mesh by studying the electrical behavior as a function of grid space minimizes the probable errors in the simulation data due to incorrect grid allocation and therefore provides accurate calibration of the fundamental material parameters for device simulation.

### 1.4.3 Calibration of Physical Models

The accuracy of simulation results relates to the underlying physics, numerical discretization issues, and the proper characterization of the models implemented in the process and device CAD tools. Over the years, the capabilities of TCAD point tools have significantly improved. However, due to the deficiencies in physical models, the simulation results are not 100% predictable and reliable. Although the development and implementation of advanced physical models have been moving ahead with a steady-state growth pattern, the characterization of the existing models is critical to make TCAD accurate. Therefore, the predictability issue must be addressed by proper calibration of the process and device models implemented in TCAD point tools. The calibration is a complex and time-consuming task. In the following section, a brief overview of physical model calibration is presented.

The physical process models implemented in the process CAD tool must be calibrated for the target technology under development. The calibration methodology includes designing short loop wafer fabrication experiments to calibrate all critical as-implanted as well as final doping profiles of all relevant impurities in the simulation structures. For a typical CMOS technology this includes 1D doping profiles for (1) channel, (2) SDE, and (3) DSD regions along the cutlines shown in Figure 1.11.

In order to calibrate the physical device models implemented in device CAD tools, a set of appropriate device characteristics are measured from the fabricated wafers of the target technology. For a typical CMOS technology this includes  $I_{ds}$  versus  $V_{gs}$ ,  $I_{ds}$  versus  $V_{ds}$ , substrate current,  $I_{sub}$  versus  $V_{gs}$ , and so on to characterize the physical device models [102,103]. Figures 1.12(a) and 1.12(b) show a basic flow for process and device model calibration of a typical CMOS technology. As shown in Figure 1.12(a) coupled process and device CAD is used to calibrate 2D doping profiles.



2D-CMOS cross-section to obtain 1D doping profiles along the cut lines:

$A/D \Rightarrow$  NMOS / PMOS channel;

$B/E \Rightarrow$  NMOS / PMOS SDE;

$C/F \Rightarrow$  NMOS / PMOS DSD.

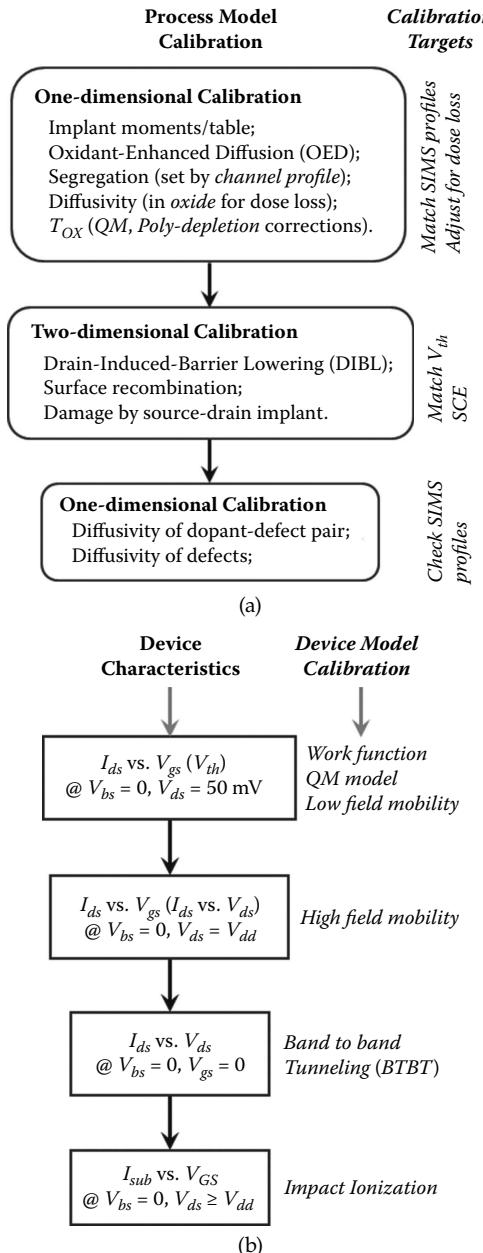
**FIGURE 1.11**

A typical 2D-CMOS cross-section showing the cutlines along the depth of the simulation structure to obtain 1D doping profiles for process model calibration. (STI represents the shallow trench isolation.)

For greater accuracy and predictability of simulation results, two levels of calibration are performed, namely (1) local calibration and (2) global calibration [1]. A brief outline of the calibration levels is presented below:

*Local calibration:* The physical models implemented in the process and device CAD tools can be characterized with the measured data of the target technology for predictive process and device simulation. During the IC fabrication process development cycle, a large number of measured data are generated. This experimental database of the target technology can be used to calibrate the process and device models and correlate simulation data with the measured data of the target technology. The calibrated TCAD models and simulation files are transferred to manufacturing at the end of the technology development (TD) cycle. These models can be used with a higher degree of accuracy (1) to evaluate the effects of process control variables on device and product performance and (2) for manufacturing process control [104–107]. Therefore, the calibrated TCAD models of a particular process technology can be used for the predictive simulation of that technology.

*Global calibration:* In order to develop a new IC fabrication technology, the TCAD point tools must be accurate and must accurately predict new physical phenomena, as may emerge during the development phase. Unfortunately, due to the lack of accurate physical models, effective calibration methodologies must be developed for the successful application of TCAD in designing a new technology. For the

**FIGURE 1.12**

A simplified process and device model calibration flow for a typical CMOS technology: (a) process model calibration using coupled process and device CAD; (b) device model calibration using device CAD with measured device characteristics. In (a), SIMS represents secondary ion mass spectrometry.

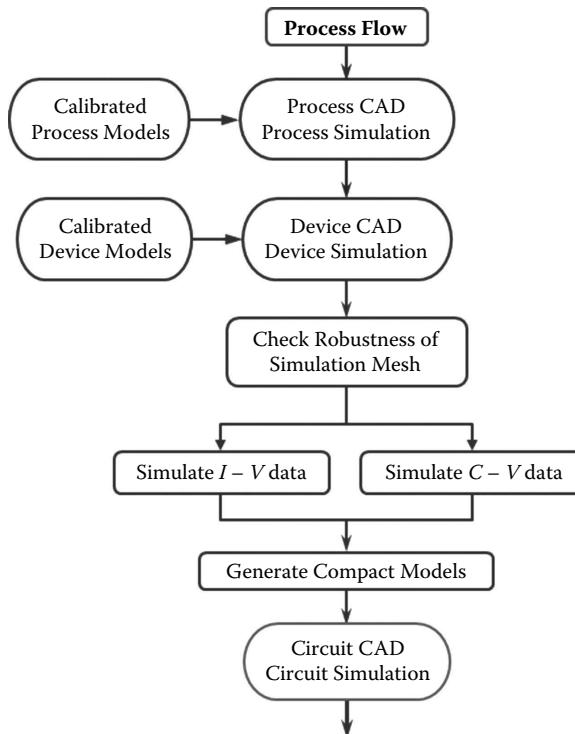
predictive application of TCAD, the numerical models must be initially characterized with a known previous generation of technology. These models can be applied to several similar technologies with the available experimental database. An iterative method of model updates to correlate the simulation and the measurement data must be continued up to an acceptable limit of tolerance of the simulation data with respect to the measurement data. This iterative method of model characterization with different known technologies and constant updating of the models provides a global calibration of the numerical models, which can be applied for next-generation IC fabrication process development with a higher degree of confidence. In addition, the calibration database must include the data from a wider range of anticipated process conditions for the next-generation process technology and device characteristics. Finally, a limited number of wafers of the target new technology should be processed concurrently for a local update of the globally calibrated models. These calibrated physical models and the model parameters will provide a higher degree of accuracy for simulation results and can be applied successfully in developing next-generation IC fabrication technology.

*Calibration database:* The calibration database used in simulation must include the measured doping profiles and device characteristics. The doping profiles must be obtained under a wide range of processing conditions covering the anticipated process variations of the target technology. The device characteristics must be obtained under various biasing conditions of circuit operations. The database must also be updated to include any new physical phenomena observed in the fabrication facility. In order to develop the next-generation IC fabrication technology, the database must also include the measured data of the anticipated doping materials under the anticipated processing conditions of the target technology. In reality, the individual process module for a new technology is developed prior to the start of the cycle for TD. Therefore, working with the unit process or the module development group, the calibration database can be prepared to include the data for the development of a target technology. In addition, the measurement data for an advanced technology with respect to the newer fabrication equipment can be obtained in collaboration with the equipment vendors. Thus, the calibration database must have experimental data for all the possible effects of the existing and the target next-generation technology.

#### 1.4.4 Coupled Process and Device Simulation

Process CAD is used for unit process development such as time and temperature required for growing the MOSFET gate oxide, shallow trench isolation (STI) module for CMOS technology, and so on. Similarly, the device CAD is used to analyze the effect of process variables on device operation. However, the coupled process and device simulation allows IC designers to directly investigate the effect of process specifications on electrical variations in devices and circuits. The key task of process CAD is to capture the features that accurately reflect the performance limitations of a given fabrication technology.

Figure 1.13 presents an overview of the simulation flow that is used to link process specifications to circuit performance. For the most part, the user input is simply a description of how the actual fabrication sequence progresses. The process simulation generates a set of data with the structural information like device geometry, doping distribution, and so on. The output of process simulation is then used as the input of device CAD to perform device simulation to obtain  $I-V$ ,  $C-V$  data. These simulation data are used to generate SPICE models by well-established parameter extraction techniques, and



**FIGURE 1.13**

Link IC process flow to circuit performance using coupled process and device CAD.

the SPICE models are used for circuit simulation. At each step, the emphasis is on focusing a broad spectrum of inputs into a coherent set of outputs that will be of maximum utility in the next step. Thus, the coupled process and device CAD can be considered as a “virtual factory” simulating ICs from the process flow analogous to wafer fabrication facility manufacturing ICs from the target process flow as shown in Figure 1.13 [104].

Through well-defined data exchange formats, the various levels of CAD are linked quite efficiently with or without simulation framework. The linkage of process to device CAD occurs through the exchange of both topographic information and arrays of data representing dopant distributions.

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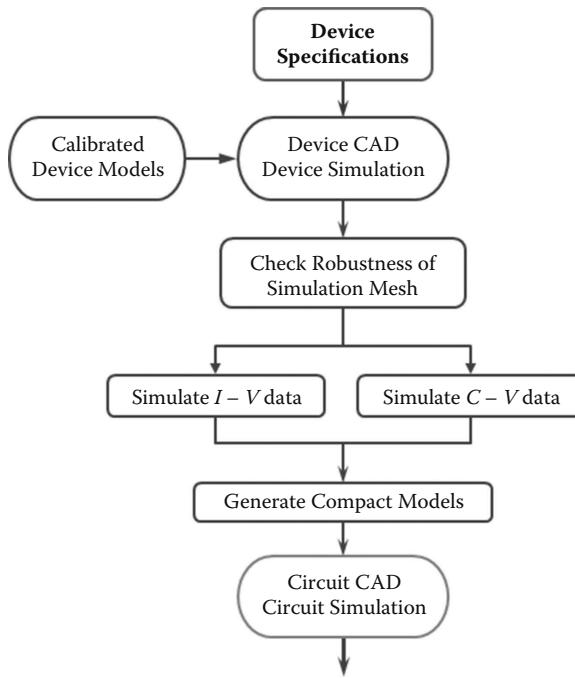
## 1.5 TCAD Application

In the semiconductor industry the major use of TCAD is in advanced device research to study new device concepts, TD, and technology transfer process [1,105–107]. In the following subsections we discuss some examples of these TCAD usages.

### 1.5.1 TCAD in Device Research

TCAD is used to study the feasibility of new device concepts or exploratory devices for the next-generation IC fabrication TD. For exploratory devices, the fabrication process is yet to be determined. Therefore, only device CAD is used to design and optimize the device structure and device performance. In this case, the device structure is generated using analytical doping profiles. Figure 1.14 shows a typical flow to use device CAD in the feasibility study of new concept devices.

In Figure 1.14, the basic simulation flow includes device architecture by analytical doping profile, use of device CAD to simulate device characteristics, verification of the robustness of the simulation structure, and optimization of the device structure to achieve the target performance objectives. After device optimization, perform device simulation to generate  $I-V$  and  $C-V$  data, format device simulation data, and generate compact models for circuit analysis. In Figure 1.14, note that calibrated device models are required for accurate prediction of device performance. After achieving the target device performance by iterative device simulation, appropriate fabrication process is designed for technology optimization using coupled process and device CAD flow. To illustrate the use of device CAD in device development for the next-generation fabrication technology, let us discuss the architecture and performance of nanoscale double-halo MOSFETs and split-gate (SG) flash memory cells.

**FIGURE 1.14**

A typical device CAD-based simulation flow to study new device concepts and generate electrical device characteristics for circuit analysis.

### 1.5.1.1 Double-Halo MOSFET Devices

It is well known that the conventional scaling of MOSFET devices in the nanoscale regime requires a reduction of the gate oxide thickness ( $T_{OX}$ ) and an increase in the channel doping concentration (NCH) to control SCE, DIBL, and leakage. However, the combination of such high NCH and ultra-thin  $Tox$  is likely to cause severe performance degradation due to higher  $V_{th}$ . In order to suppress SCE and control DIBL, typically, a single halo profile is used around SDE. However, as the MOSFET devices approach their ultimate dimension near the 10 nm regime, both SDE and DSD regions near the source-end of the channel contribute to DIBL, resulting in higher  $I_{off}$  and degradation in the subthreshold swing. In order to control DIBL from both SDE and DSD, we can use two halo doping profiles, one around SDE and other around DSD. Then use device CAD to optimize these halo doping profiles to control  $V_{th}$ , SCE, DIBL, and  $I_{off}$  in the nanoscale MOSFETs. Therefore, our objective is to design high performance nanoscale MOSFETs with low leakage, fast switching, controlled SCE, and reduced DIBL and QM effects [93–97]. In order to achieve our objective an ideal structure shown in Figure 1.6 is used to optimize the device performance.

In device architecture, the n/p MOS device structure shown in Figure 1.6 includes an n+/p+ polysilicon gate, a gate oxide, vertically and laterally non-uniform channel doping profile, shallow n+/p+ SDE, deep n+/p+ DSD, and two halo doping profiles: the first around SDE and the second around DSD regions. An SSR doping profile with a low impurity concentration at the Si/SiO<sub>2</sub> interface and a higher peak concentration at a finite depth below the interface is used to provide the non-uniform vertical channel profile [97, 98]. The SSR profile is optimized to achieve a target  $V_{th}$  for the long channel devices. The SSR profile also provides superior  $V_{th}$  control caused by dopant fluctuations [108].

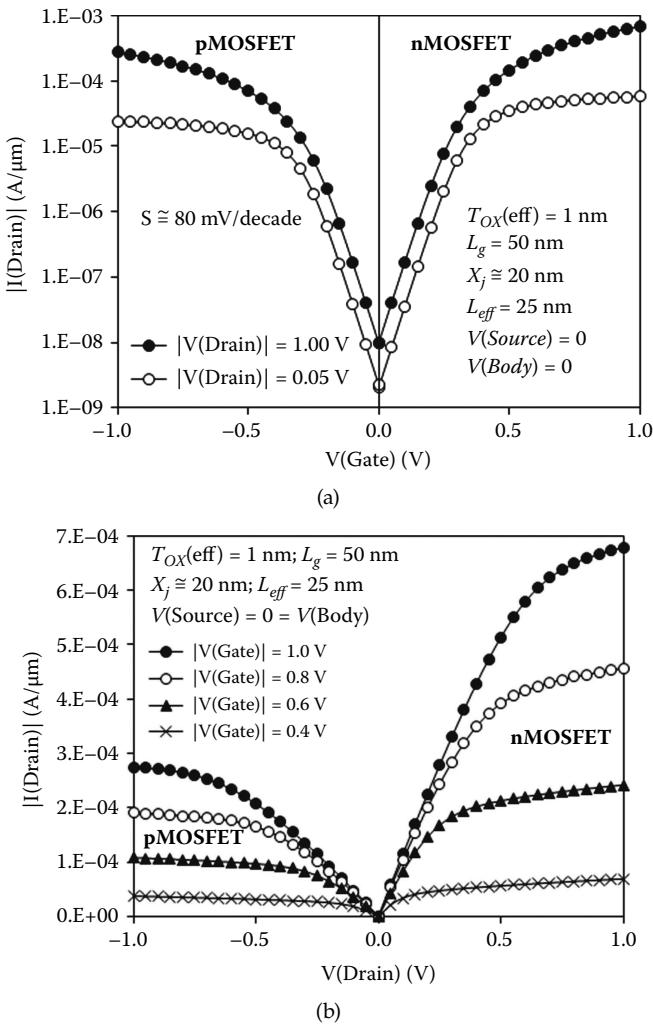
The non-uniform analytical lateral channel doping profile is achieved using two Gaussian halo profiles during drain-profile engineering [109]. The first halo doping profile is a heavily doped shallow profile defined on both sides of the gate region aligning at the gate edge. The peak concentration of the shallow halo profile is defined immediately below the SDE junction ( $X_j$ ) to reduce DIBL due to SDE. The second halo profile is a lightly doped deep profile defined on both sides of the gate region by an offset distance from the gate edge. The peak concentration of the second halo doping is placed immediately below the DSD junction ( $X_{ja}$ ) to control DIBL due to DSD. The detailed fabrication procedure is described in [95]. After device architecture, device CAD is used to study the device performance of the double-halo MOSFETs.

A hydrodynamic model for semiconductors with full energy balance solution along with an analytical QM model [110] is used for device simulation [111]. The halo profiles along with the SSR channel doping profile are optimized to the target  $I_{off} = 10 \text{ nA}/\mu\text{m}$ . The 2D doping distribution of an optimized double-halo nMOSFET device is shown in Figure 1.8. And, Figures 1.15(a) and 1.15(b) show the simulated device performance of double-halo nMOSFET and pMOSFET devices with effective channel length,  $L_{eff} = 25 \text{ nm}$ .

Device simulation results in Figure 1.15 show excellent device performance, thus achieving the target objective of this study. Thus, device CAD can be used to optimize exploratory devices and assess the feasibility of these devices for next-generation IC fabrication technology.

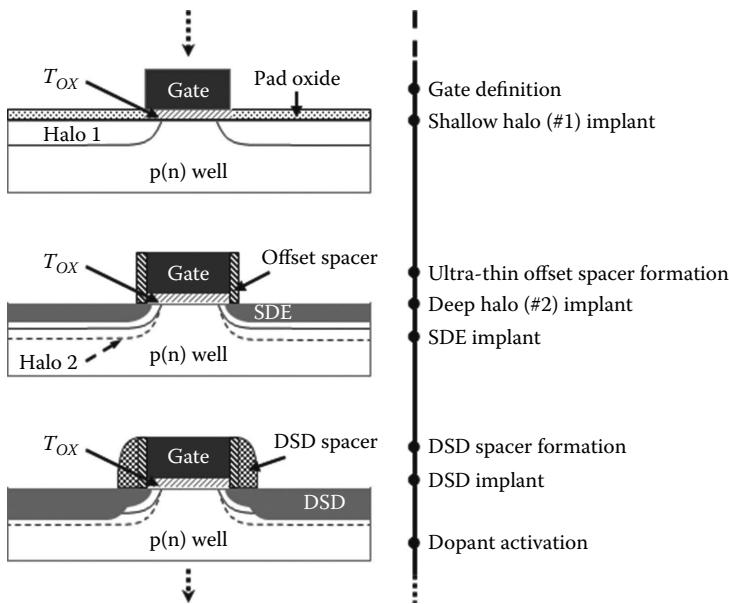
After device optimization using device CAD, an initial guess process flow is created to reproduce the analytical doping profiles used in device simulation. Then the process CAD is used to perform process simulation and optimize the process flow. Figure 1.16 shows only the section of process flow used to integrate the double-halo MOSFETs in advanced CMOS technology. The detailed process flow is described in [95].

In Figure 1.16, the shallow halo doping profile is implanted after the gate definition with peak concentration immediately below  $X_j$ . Then about a 2-nm wide offset spacer is used to implant the deep halo and SDE profiles. Because the depth of the shallow halo is  $\sim X_j$ , SDE regions are encroached by about 2 nm with the halo doping near the Si/SiO<sub>2</sub> interface within the channel. Thus, the shallow doping profiles only enhance the channel doping by about 4 nm of  $L_{eff} \approx 25 \text{ nm}$  near the Si/SiO<sub>2</sub> interface. On the other hand, the deep halo

**FIGURE 1.15**

Device characteristics of double-halo MOSFETs obtained by device CAD: (a)  $I_{ds}$  versus  $V_{gs}$  and (b)  $I_{ds}$  versus  $V_{ds}$ ; the simulation data are obtained for 50 nm devices with  $L_{\text{eff}} = 25 \text{ nm}$  and optimized for  $|I_{off}| = 10 \text{ nA}/\mu\text{m}$  at  $|V(\text{Drain})| = 1 \text{ V}$ ;  $V(\text{Gate}) = V(\text{Source}) = V(\text{Body}) = 0$ . (From S. Saha, Design considerations for 25 nm MOSFET devices, *Solid-State Electron.*, vol. 45, no. 10, pp. 1851–1857, October 2001. With permission.)

doping profiles with depth  $\sim$  DSD junction depth diffuse laterally into the channel region to enhance the channel doping at a finite depth below the Si/SiO<sub>2</sub> interface. Thus, the combination of double-halo profiles provides the non-uniform lateral channel doping while maintaining a lower channel doping concentration near the surface due to the SSR channel doping profile. The halo implant dose and energy are optimized to achieve the target value of  $I_{off}$

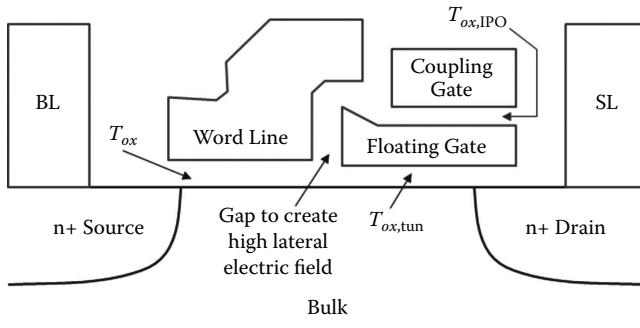
**FIGURE 1.16**

Part of the process flow showing the integration of two halo profiles in CMOS technology to fabricate nanoscale double-halo MOSFET devices. (From S. Saha, Device characteristics of sub-20-nm silicon nanotransistors, in *Proc. SPIE Conf. on Design and Process Integration for Microelectronic Manufacturing*, vol. 5042, pp. 172–179, July 2003. With permission.)

for the nominal devices of the target technology. The source-drain regions are optimized to achieve an improved device behavior, and the peak impurity concentrations for SDE and DSD profiles used are  $2.5 \times 10^{20} \text{ cm}^{-3}$  and  $3.7 \times 10^{20} \text{ cm}^{-3}$ , respectively [93,94].

### 1.5.1.2 Sub-90 nm Split-Gate Flash Memory Cells

Our second example of device CAD use in advanced device research and development is to study the feasibility of scaling split-gate (SG) NOR-type flash memory cells below 90 nm. A typical SG cell with top coupling gate (CG), called SG-TCG cell [112], is shown in Figure 1.17. The structure includes a select gate or word-line (WL) with gate oxide ( $T_{ox}$ ), a floating gate (FG) with tunneling oxide ( $T_{ox,tun}$ ), a CG with inter-poly oxide ( $T_{ox,IPo}$ ), an n+ source as the “Bitline” (BL), and an n+ drain as the “Sourceline” (SL). The FG is completely isolated within the gate dielectric and acts as a potential well to store charge by programming the cell using source-side injection (SSI) of hot carriers. The erase operation is performed by poly to poly Fowler-Nordheim tunneling of carriers from the FG to WL. The sharp FG-tip near the WL edge in Figure 1.17 improves the erasing efficiency of the programmed cells. Because the cell structure in Figure 1.17 consists of two MOSFET devices in series, it is difficult to scale these cells in the sub-90 nm regime due to several constraints [113,114].

**FIGURE 1.17**

An idealized SG-TCG flash memory cell structure used for scaling in the sub-90 nm regime: here, BL = bitline,  $T_{ox}$  = WL-transistor gate oxide thickness,  $T_{ox,tun}$  = tunneling oxide thickness,  $T_{ox,IPO}$  = inter-poly oxide thickness and SL = Sourceline. (From S.K. Saha, Non-linear coupling voltage of split-gate flash memory cells with additional top coupling gate, *IET Circuits, Devices & Systems*, vol. 6, no. 3, pp. 204–210, May 2012. With permission.)

The major scaling constraints of NOR-type SG-TCG cells are (1) the high value of SL programming voltage,  $V_{SL} \equiv V_{sp} \gg 3.2$  V required for an efficient hot-electron programming [113] and  $V_{sp} >$  floating gate (FG) transistor saturation voltage ( $V_{SL,sat}$ ) required to mitigate the risk of supply voltage fluctuations [112]; (2) excessive program-inhibit leakage current,  $I_{off(BLI)}$  causing inhibited cells susceptible to soft-write error [113,114]; (3) high program cell leakage current,  $I_{r0}$  causing ineffective sensing of the write and erase states by the sense amplifiers [113,114]; and (4) degradation of program/erase (P/E) coupling ratio causing degradation in P/E efficiency [113,114].

Our objective is to design high performance sub-90 nm NOR-type SG-TCG cells within the above described scaling constraints. First, the requirement for  $V_{sp} \gg 3.2$  V makes the scaled SG-TCG cells susceptible to punchthrough at the operating conditions, causing degradation in the cell reliability. Therefore, in order to improve the punchthrough voltage, the channel doping concentration must be increased which in turn decreases the SL p-n junction breakdown voltage,  $BV_j$ . Thus, we need to optimize the channel doping profile and use graded SL/BL p-n junctions to improve the overall cell breakdown voltage ( $BV$ ) to achieve the target  $V_{sp}$  for the scaled SG-TCG cells. In this case, three channel doping profiles are used to optimize cell performance for the target  $V_{sp}$  value.

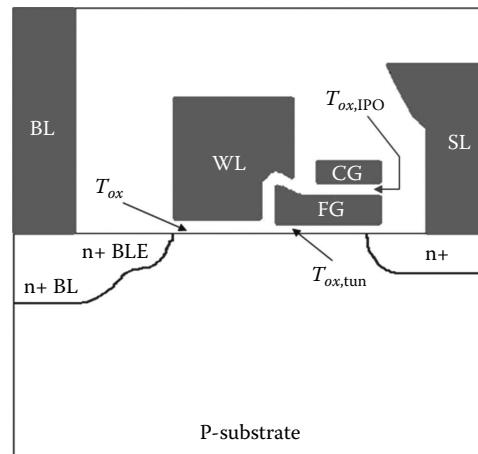
The next requirements are tolerable leakage currents  $I_{off(BLI)}$  and  $I_{r0}$  at the target SL voltage ( $V_{SL}$ ) for the sub-90 nm SG-TCG cells.  $I_{off(BLI)}$  is the off-state leakage current of WL-MOSFETs, whereas  $I_{r0}$  is the off-state leakage current of FG MOSFETs. Thus,  $I_{off(BLI)}$  can be optimized to the target value required for the target  $V_{sp}$  using shallow BL-extension (BLE) and optimizing BL-halo to reduce SCE and DIBL. Similarly, to achieve the target  $I_{r0}$  shallow SL junction along with a lightly doped FG-channel profile is used as shown in Figure 1.17. The target values of leakage currents at the required  $V_{SL} = V_{sp}$  are

obtained using device CAD. In this case, we can use device CAD to determine the maximum tolerable parasitic leakage current for  $BV > V_{sp}$ . In this example, the device simulation data show that  $I_{r0} \sim 200$  pA/cell at  $V(BL) = 0.8$  V and  $V(FG) = 0$  with WL device on and  $I_{off(BLI)} \sim 200$  nA/kbit at  $V(BL) = 1.8$  V and  $V(WL) = 0$  with FG device on are required to maintain  $V_{sp} = 6.5$  V  $< BV$ . The detailed optimization technique is reported in the references [113,114].

The final requirement to design sub-90 nm SG-TCG cells is to account for the degradation of the coupling ratio in the scaled devices. The addition of top CG improves the programming coupling ratio, whereas the shallow BLE without overlap under the WL transistor improves the erase coupling ratio.

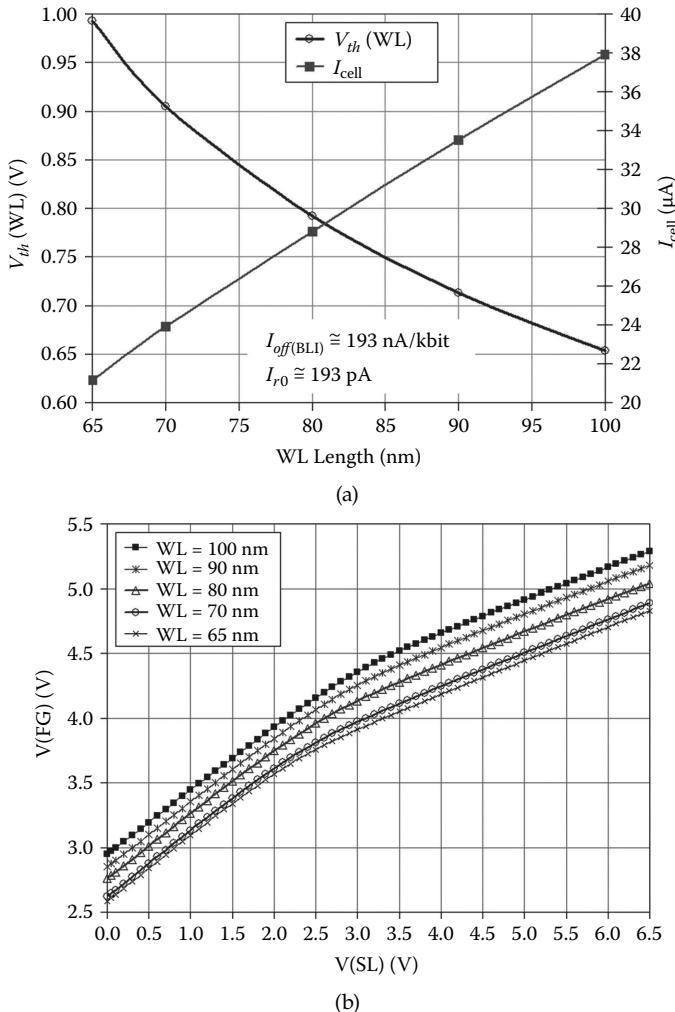
Thus, the use of shallow SL junction will control SCE and DIBL and improve scalability of SG-TCG cells. In addition, a shallow BL-junction will control DIBL and improve scalability of the cells. In this example, a shallow BLE and deep BL regions along with BL-halo are used to optimize the cell to the desired performance objective [112–114]. The final simulation structure of the optimized SG-TCG cell is shown in Figure 1.18.

Figure 1.19 shows device simulation results of the optimized SG-TCG cells. Figure 1.19 shows that  $V_{th}(WL)$  and cell read current ( $I_{r1}$ ) as function of WL transistor channel length. In Figure 1.19(a),  $V_{th}(WL)$  is extracted from the extrapolated  $I_{ds} - V_{gs}$  plots of WL-devices at  $V_{ds} = 50$  mV with overdrive  $V(FG) = 2.5$  V. And  $I_{r1} = I_{cell}$  is obtained at the read condition,  $V(WL) = 2.5$  V,  $V(BL) = 0.8$  V,  $V(FG) = 1.8$  V =  $V(CG)$ , and  $V(SL) = 0$ . The device simulation data show acceptable read current  $I_{r1} \approx 22.2$   $\mu$ A for 65 nm cells optimized for  $V_{sp} = 6.5$  V. Figure 1.19(b) shows the



**FIGURE 1.18**

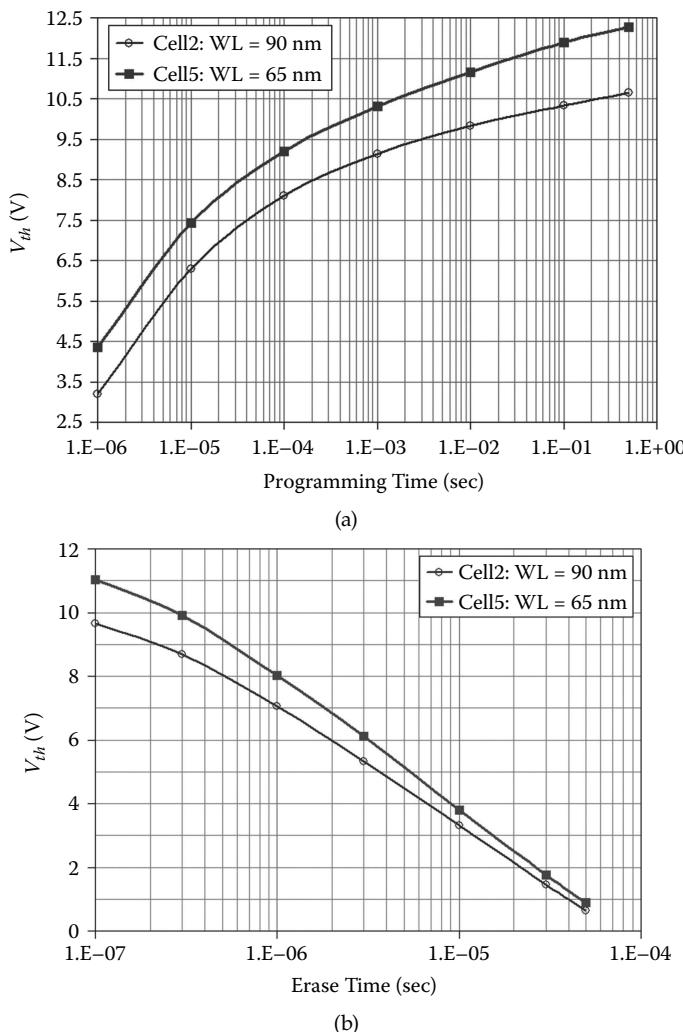
The final sub-90 nm SG-TCG flash memory cells structure generated using device CAD tool MEDICI: here, BL = bitline, WL = word line, FG = floating gate, CG = coupling gate,  $T_{ox}$  = WL-transistor gate oxide thickness,  $T_{ox,tun}$  = tunneling oxide thickness,  $T_{ox,IPO}$  = inter-poly oxide thickness, SL = sourceline, and BLE = shallow BL extension. (From S.K. Saha, Non-linear coupling voltage of split-gate flash memory cells with additional top coupling gate, *IET Circuit, Devices & Systems*, vol. 6, no. 3, pp. 204–210, May 2012.)

**FIGURE 1.19**

Simulated device performance of SG-TCG cells: (a)  $V_{th}$  and  $I_{cell}$  versus WL-transistor channel length and (b) programming coupling voltage  $V(FG)$  as a function of programming voltage  $V(SL)$  obtained at function of programming voltage  $V(CG) = 10 \text{ V}$ . (From S.K. Saha, Design considerations for sub-90 nm split-gate Flash memory cells, *IEEE Trans. Electron. Devices*, vol. 54, no. 11, pp. 3049–3055, November 2007. With permission.)

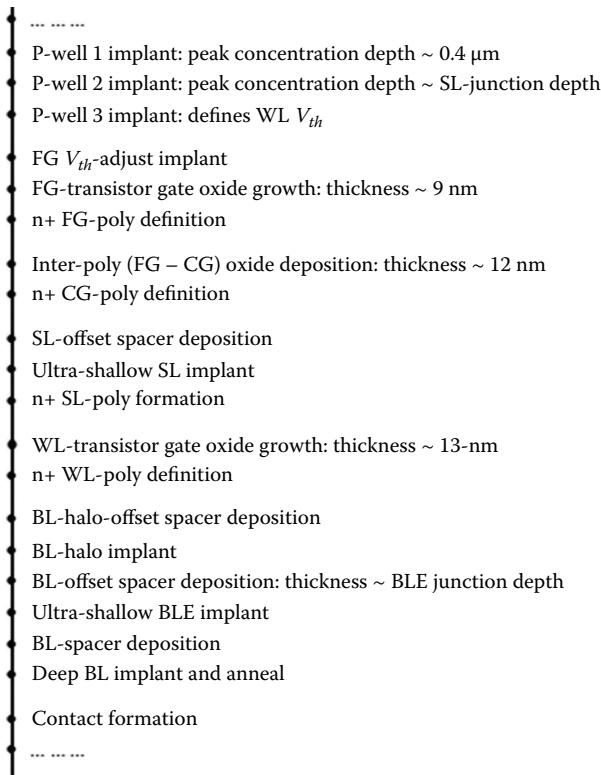
simulated  $V(FG)$  versus  $V(SL)$  plots of the SG-TCG cells at  $V(CG) = 10 \text{ V}$ . Similarly, Figure 1.20 shows an improvement in both programming coupling ratio due to CG and the new device architecture with shallow SL and BLE junctions.

The device simulation study clearly shows the feasibility of SG-TCG cell scaling near the 65-nm regime. After the device optimization, an initial guess process flow is created as shown in Figure 1.21 for complete technology optimization using coupled process and device CAD as shown in Figure 1.13.

**FIGURE 1.20**

Programming/erase characteristics of SG-TCG cells: (a) programming at  $V(WL) = 1.2$  V,  $V(SL) = 6.5$  V,  $V(BL) = 0.3$  V, and  $V(CG) = 10$  V; and (b) erase; at  $V(WL) = 10$  V and  $V(SL) = 0 = V(BL)$ ; from simulation data the time to program,  $T2P \approx 30 \mu\text{s}$  and time to erase,  $T2E \approx 40 \mu\text{s}$ . (From S.K. Saha, Design considerations for sub-90 nm split-gate Flash memory cells, *IEEE Trans. Electron. Devices*, vol. 54, no. 11, pp. 3049–3055, November 2007. With permission.)

The device-simulation results show that the sub-90-nm SG-TCG flash-memory cells can be achieved with tolerable  $I_{r0} < 200$  pA,  $I_{OFF(BL)} < 200$  nA/kb, acceptable  $I_{rl}$ , and excellent  $T2P \approx 30 \mu\text{s}$  and  $T2E \approx 40 \mu\text{s}$ . Thus, the present design methodology demonstrates the feasibility of high performance sub-90-nm split-gate flash-memory cells down to 65 nm with  $I_{rl} \approx 235 \mu\text{A}/\mu\text{m}$  along with efficient P/E characteristics. From the results of device CAD, a process flow is developed for coupled process and device simulation.

**FIGURE 1.21**

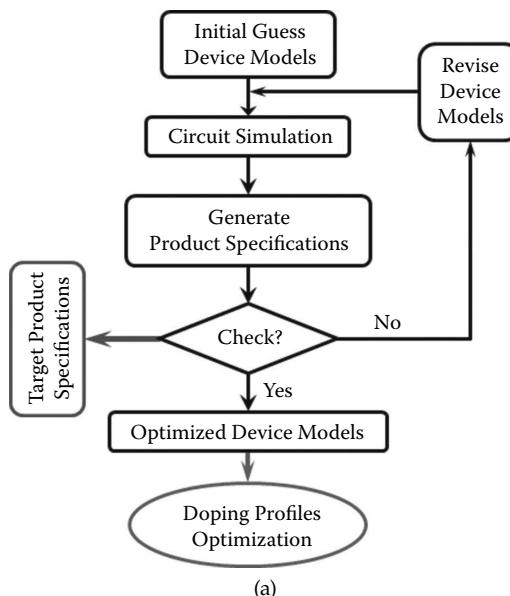
The major technology steps to integrate sub-90 nm split-gate NOR-flash memory cells in a standard CMOS technology. (From S.K. Saha, Design considerations for sub-90 nm split-gate Flash memory cells, *IEEE Trans. Electron. Devices*, vol. 54, no. 11, pp. 3049–3055, November 2007. With permission.)

### 1.5.2 TCAD in Fabrication Technology Development (TD)

The coupled process and device CAD flow as shown in Figure 1.13 is used in IC fabrication TD. Typically, in the semiconductor industry, the next-generation IC fabrication technology is derived by scaling the current technology. In this case, the current generation fabrication process flow with appropriate modifications is used as the initial guess to optimize the process recipe of the next-generation technology. As shown in Figure 1.13, the initial guess process recipe is iteratively optimized using coupled process and device CAD to the target achievable device specifications; then the compact model parameters are extracted from the simulated device characteristics; and finally, circuit CAD is used to analyze the circuit performance. Figure 1.13 also shows that for accurate prediction of device and circuit performance, calibrated physical models are essential. Also, the calibration database with experimental doping profiles under various processing conditions and device characteristics

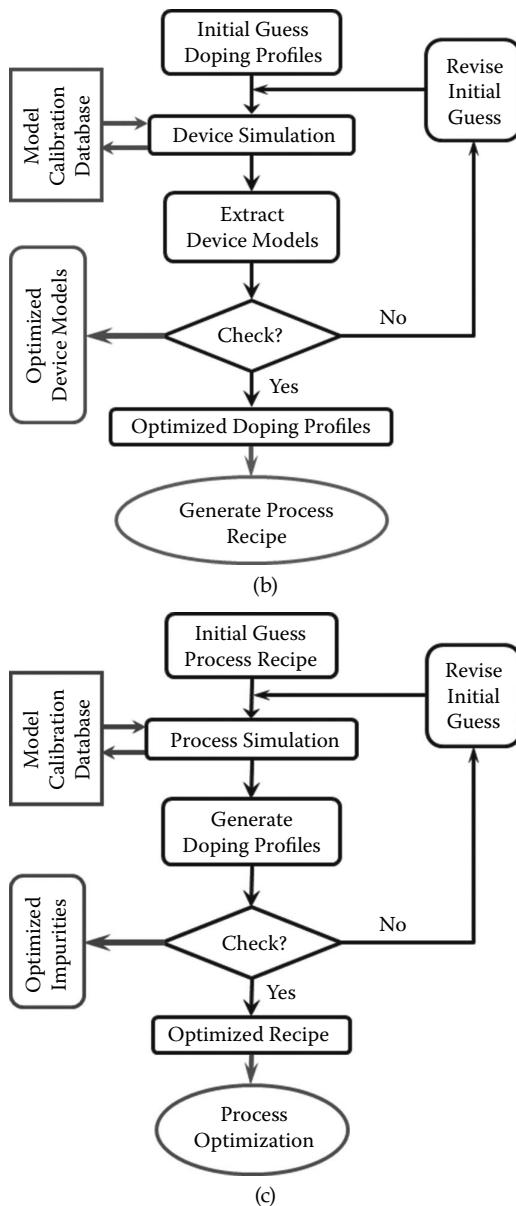
are essential to validate the simulation results in each step of the optimization process.

Besides the conventional TD approach described above, the initial guess process recipe can be efficiently obtained by “reverse modeling” as shown in Figure 1.1. As we discussed in Section 1.3, the ultimate motivation for TCAD is to extract circuit design parameters to enable designers to predict circuit performance of the target technology. In the TCAD flow in Figure 1.13, the circuit design parameters are generated by optimizing the initial guess process recipe of the current generation technology using coupled process and device CAD. However, for exploratory devices, the current generation technology does not exist; therefore, the initial process flow and recipe are obtained by reverse simulation flow (e.g., circuit CAD to process CAD), as shown in Figure 1.1. Because the ultimate goal of the new technology generation is to predict circuit performance, circuit/product specific process recipe will ensure the target circuit performance. The basic simulation flow for the product-specific IC process design is shown in Figure 1.22. The initial guess process recipe is generated by reverse engineering from the target product specifications in three sequential steps: (1) generation of device models using circuit simulation as shown in Figure 1.22(a); (2) generation of doping profiles



**FIGURE 1.22**

Flowchart for the generation of initial guess process recipe using three-step approach: (a) optimization of device models to the target product specifications; (b) optimization of process profiles to the target device models; (c) optimization of process recipe to the target process profiles. (From S. Saha, Technology CAD for integrated circuit fabrication technology development and technology transfer, *Proc. SPIE*, vol. 5042, pp. 63–74, July 2003. With permission.) (continued)

**FIGURE 1.22**

(continued) Flowchart for the generation of initial guess process recipe using three-step approach: (a) optimization of device models to the target product specifications; (b) optimization of process profiles from the target device models; (c) optimization of process recipe to the target process profiles. (From S. Saha, Technology CAD for integrated circuit fabrication technology development and technology transfer, *Proc. SPIE*, vol. 5042, pp. 63–74, July 2003. With permission.)

within the device using device CAD as shown in Figure 1.22(b); and (3) generation of process recipe using process CAD as shown in Figure 1.22(c). This initial guess product-specific process recipe can then be further optimized using coupled process and device CAD as shown in Figure 1.13 to generate the final process flow and device specifications.

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## 1.6 Benefit of TCAD in TD Projects

TCAD is widely used in advanced IC fabrication TD to optimize IC devices and fabrication processes through critical analysis and detailed understanding of process, device, and circuit simulation data. The TCAD tools that accurately predict the process and device characteristics of the anticipated wafer fabrication technology have shown great promise in nanoscale device and advanced IC manufacturing TD. Therefore, TCAD has become indispensable to reduce the development cycle time and cost of advance IC fabrication technology and products [1–5]. TCAD tools offer manufacturing and development engineers vast improvements in flexibility, innovation, efficiency, and customer responsiveness [1].

In Section 1.3, we established the motivation and importance of TCAD in IC device and process architecture. It is obvious that the knowledge gained by TCAD is impossible to quantify. However, for industrial applications it is essential to quantify the benefit of TCAD in reducing TD cycle time and cost [1,5]. By conducting a survey of TCAD users, International Technology Roadmap for Semiconductors (ITRS) reported about 32% reduction in development time and about 30% in development cost by the appropriate use of TCAD [2]. Though this demonstrates high relevance and potential for the industrial use of TCAD, a survey-based benefit assessment is not adequate to undertake a TCAD-based development project in the industry. Therefore, a quantitative model to assess the benefit of TCAD use in a development project is crucial for project managers.

In 1999, the basic formulations of a quantitative model to compute the benefit of TCAD use in IC development were reported [1] and the detailed analytical model to compute the benefit of TCAD was reported in 2010 [5]. In these reports, a set of realistic assumptions is used to derive a set of mathematical expressions to compute the cycle time and cost benefit of a TCAD-based project compared to that of the trial-and-error experimentation or “conventional” approach. The key assumption of this model is that the TCAD tools accurately predict the process and device characteristics of the target wafer fabrication technology. In order to develop a realistic analytical model to compute the benefit of TCAD over the conventional approach, a typical IC fabrication TD project is divided into three phases ( $\phi$ ): phase 1, generation of initial guess process recipe; phase 2, process optimization to generate process and device specifications; and phase 3, evaluation of process

manufacturability. According to this model, the reduction in the development cycle time,  $\Delta t$ , and cost,  $\Delta C$ , on a project by TCAD use compared to the conventional approach is described by

$$\Delta t \equiv Ft_{conv} \quad (1.1)$$

$$\Delta C \geq C_{wfr} \left( \frac{F}{1-\rho} + (1+ROI) \right) \Delta n - C_{tcad} \quad (1.2)$$

$$\Delta C \geq C_{wfr} [F + (1+ROI)(1-\rho)]A \cdot m \cdot n_p - C_{tcad} \quad (1.3)$$

where the model parameters in Equations (1.1)–(1.3) are as follows:  $F$  is the development cycle time reduction factor by a TCAD-based project compared to a conventional project;  $t_{conv}$  is the conventional TD time without using TCAD;  $C_{wfr}$  is the cost of processing a single wafer-lot in the fab;  $\rho$  is the fraction of the conventional TD wafers used in a TCAD-based project; ROI is the return on investment from IC sale;  $\Delta n$  is the reduction in the number of wafer-lots in the fab by using TCAD;  $C_{tcad}$  is the total cost of implementation of CAD infrastructure;  $m$  is the total number of iterations required to optimize a technology in each phase of a TD project and is assumed to be the same for both conventional and TCAD-based processes;  $n_p$  is the number of process-control variables  $p$  (e.g., ion implant) and defines the complexity of an IC fabrication technology; and  $A = n_x n_y \phi / w_n$  is the model parameter that depends on the number of project phases  $\phi$ , the split conditions of implants (e.g., energy  $n_x$  and dose  $n_y$ ), and the number of wafers in a wafer-lot  $w_n$ .

By using the appropriate values of the parameters in Equations (1.1) and (1.2) or (1.1) and (1.3) for the TCAD tools that accurately predict the process and device characteristics of the target wafer fabrication technology, the above analytical model provides a reduction in the TD cycle time of about 67% with multimillion dollar cost savings compared to the conventional approach [1,5].

## 1.7 Summary

This chapter presents the mission and scope of extended technology CAD in IC process modeling and device performance analysis. A brief history of the evaluation of device and process CAD during the past four decades leading to the commercialization of TCAD software is described. The motivation for TCAD use is outlined with a few typical examples. A brief outline of TCAD flow including generation of robust simulation structure and physical model calibration for accurate IC process and device simulation is presented. A few

examples of typical TCAD application, especially, in studying the feasibility of exploratory devices for the next-generation fabrication technology are discussed. Finally, an analytical cost model to compute the benefit of TCAD use in saving IC TD cycle time and cost over the conventional trial-and-error-experimentation based TD project is discussed.

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