1

Triggering and Gate Characteristics of Thyristors

Gate Trigger Characteristics, Ratings, and Methods

The key factor in the widespread utility of the triode thyristor (SCR or triac) for control of power is its ability to switch from nonconducting to conducting state in response to a small control signal. Proper triggering of the thyristor requires that the source of the trigger signal should supply adequate gate current and voltage, without exceeding the thyristor gate ratings, in accordance with the characteristics of the thyristor and the nature of its load and supply. Other important design factors include the trigger source impedance, time of occurrence and duration of the trigger signal, and off-state conditions. This chapter covers the fundamentals of the gate triggering process, gate characteristics and ratings, interaction with the load circuit, characteristics of active trigger-circuit components, and basic examples of trigger circuits since all application of thyristors require some form of triggering. This chapter covers mostly SCRs.

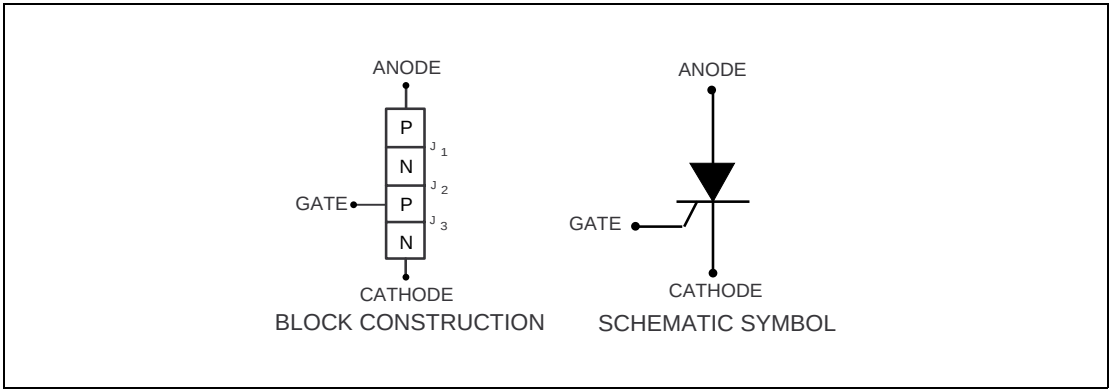


Figure 1.1 SCR Simple Block Construction

The operation of a PNPN device can best be visualized as a specially coupled pair of transistors as shown in Figure 1.2.

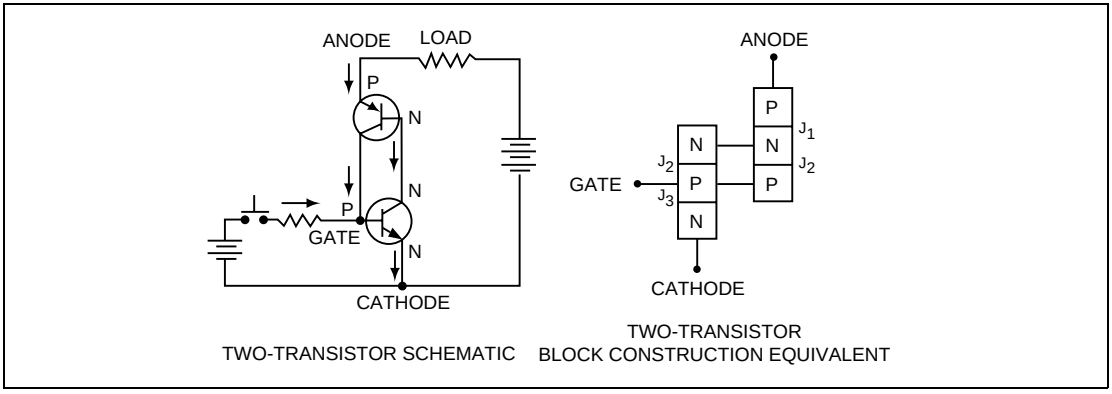


Figure 1.2 Coupled Pair of Transistors

The connections between the two transistors enable regenerative action when a proper gate signal is applied to the base of the NPN transistor. Normal leakage current is so low that the combined h_{FE} of the specially coupled two-transistor feedback amplifier is less than unity, keeping the circuit in an off-state condition. A momentary positive pulse applied to the gate biases the NPN transistor into conduction which, in turn, biases the PNP transistor into conduction. The effective h_{FE} momentarily becomes greater than unity so that the specially coupled transistors saturate. Once saturated, current through the transistors is enough to keep the combined h_{FE} greater than unity. The circuit will remain "on" until it is "turned off" by reducing the anode-to-cathode current (I_T) so that the combined h_{FE} is less than unity and regeneration ceases. This threshold anode current is the holding current of the SCR.

Triggering Process

Subsequent sections will present the two-transistor analogy of the SCR, the junction gate and remote gate operation of the triac, and the remote-base transistor action of the SCR. That discussion will indicate that internal transistor-like action determines the transition of a thyristor from the non-conducting to the conducting state.

Symmetrical transistor action in which anode current increases proportionally to gate current precedes the switching action, with slowly increasing DC gate current. The anode current is relatively independent of anode voltage with a positive anode voltage and of anode voltage up to a point where a form of avalanche multiplication causes the current to increase. (See Figure 1.3.) The small-signal (or instantaneous) impedance (dv/di) of the thyristor changes rapidly, but smoothly, at this point from a high positive resistance to zero resistance, increasing values of negative resistance as increasing current is accompanied by decreasing voltage. Until the "transistors" approach saturation, the negative resistance region continues, with the impedance smoothly reverting from negative to zero to positive resistance.

The criteria for triggering depends upon the nature of the external anode circuit impedance and the supply voltage, as well as the gate current. Note this by constructing the load line of the curves in Figure 1.1, connecting between the open-circuit supply voltage V_L and the short-circuit load current I_A. The thyristor characteristic curve intersects the load line at a stable point (1) with zero-gate current. At a gate current of I_{G1}, the characteristic curve becomes tangential to the load line at a point where the negative resistance of the thyristor is equal in magnitude to the external load resistance. The thyristor switches to the low-impedance state at stable operating (3) since this condition is unstable. Removing the gate current at this point maintains conduction at point (3). If the supply voltage is reduced to V_{L2}, the load line shifts and the operating point (3) moves toward the origin. The condition is again unstable, and the thyristor reverts back to the high-impedance "off state" when the load line becomes tangential to the characteristic curve at point (4).

The anode current at point (4) is the "holding" current for this set of conditions. If the load resistance increases instead of reduces supply voltage to reach point (4), the point (5) at which the characteristic curve becomes tangential to the load line occurs at a lower current, which is the holding current for that set of conditions. Turn-off occurs at point (6), a lower anode current, if the gate current I_{G1} remains constant while supply voltage reduces to V_{L3}. Triggering the SCR at a higher gate current requires I_{G2}, but reduction of this gate signal below I_{G1} allows it to switch off, and so the SCR does not truly latch in the on-state. The latching current is at least as high as the holding current (at $I_G = 0$) and is higher in some SCRs because of non-uniform areas of conduction at low currents. The triggering criterion is not

only meeting a negative-resistance intercept condition such as point (2), but also is reaching a certain minimum anode current at point (3) in those cases.

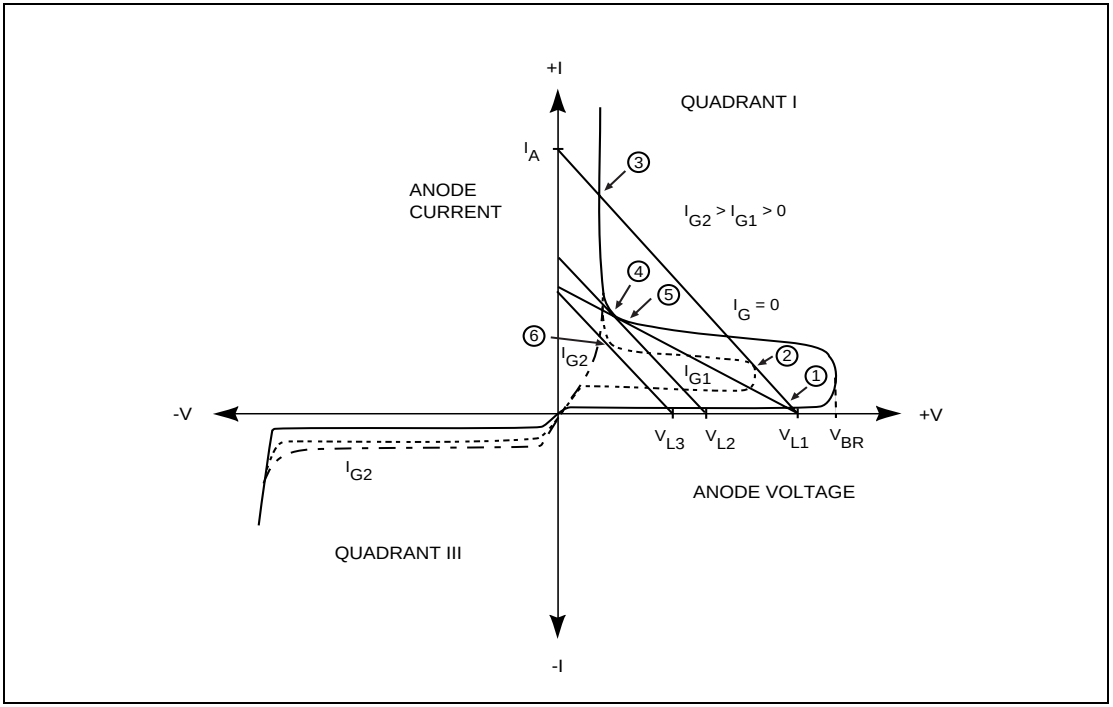


Figure 1.3 SCR Anode-Cathode Characteristics with Gate Current

The triac gate characteristics in Quadrant I (QI) and Quadrant III (QIII) appear similar to those of the SCR in QI. The turn-on process is not perfectly symmetrical for all possible biasing and triggering conditions, but either a positive or negative gate signal can trigger the triac.

Thyristor triggering requirements are dependent on both anode and gate conditions. Therefore, specifications on a given thyristor's requirements for gate voltage and gate current to trigger (V_{GT} and I_{GT}) also define the anode circuit voltage and load resistance conditions.

SCR Gate–Cathode Characteristics

Trigger circuits must be designed to produce proper current flow between the gate and cathode terminals of the SCR. The nature of the impedance that these two terminals present to the trigger circuit is a determining factor in circuit design.

Therefore, the electrical characteristics presented between the gate and cathode terminals, from basic construction and theory of operation, are basically those of a p-n junction—a diode. (See Figures 1.1 and 1.2.)

Characteristics Prior to Triggering

Figures 1.4 and 1.5 show the low-frequency full and simplified equivalent circuits of the gate-to-cathode junction with no anode current flowing (open anode circuit) for both conventional and amplifying gate SCRs. The series resistance R_L represents the lateral resistance of the p-type layer to which the gate terminal is connected. The shunt resistance R_S represents any "emitter short" that may exist in the structure. The magnitudes of R_L and R_S are variables resulting both from structure design and manufacturing process. For example, R_S is extremely high in the sensitive-type SCR and quite low in the standard type which features emitter "shorts" to increase its V_{DRM} rating and dv/dt characteristic. Because the reverse avalanche voltages of SCR gate junctions are typically in the range from 5 to 20 volts, the illustration shows the diodes as avalanche ("zener") diodes, a condition easily encountered in trigger circuits.

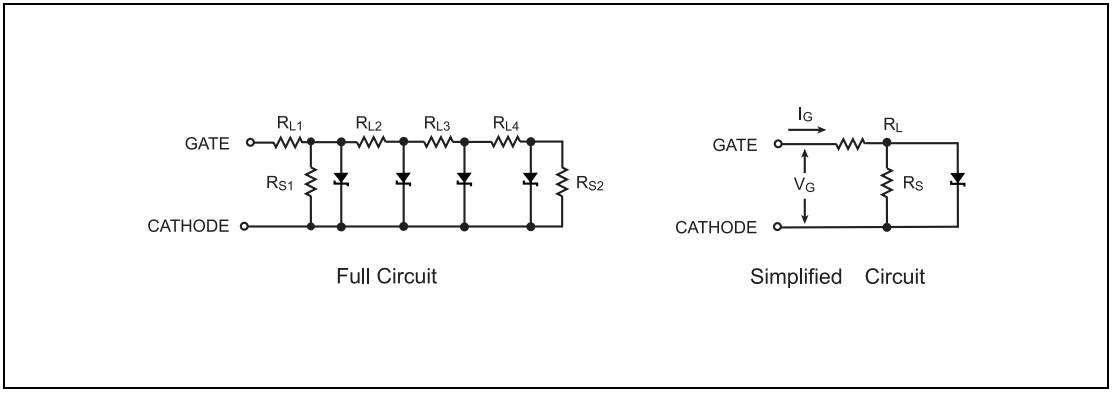


Figure 1.4 Gate-Cathode Equivalent Circuit for the Conventional SCR

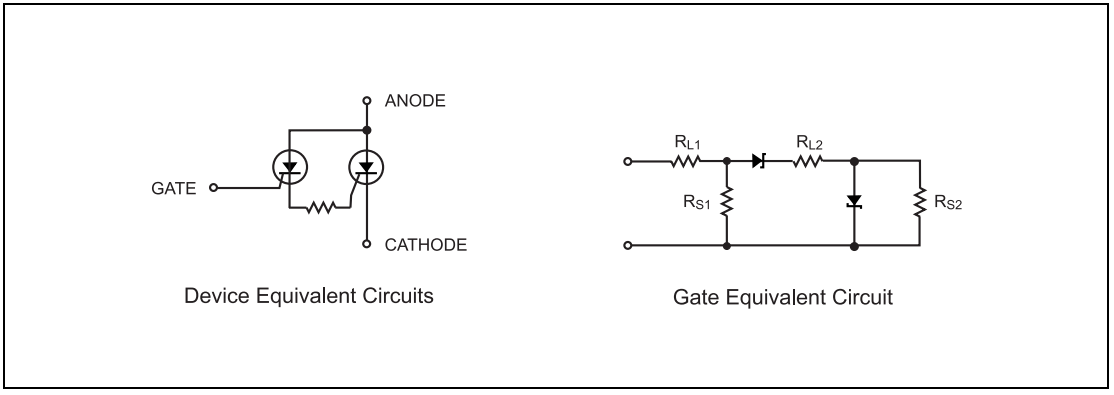


Figure 1.5 Gate-Cathode Equivalent Circuit for the Amplifying Gate SCR

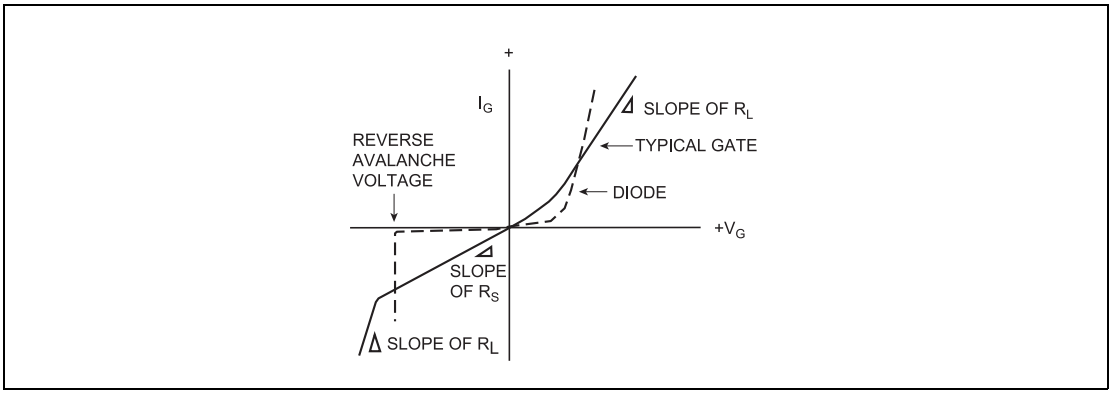


Figure 1.6 Gate-Cathode Characteristic Curve (I_A = 0)

Figure 1.6 shows the difference between a typical gate characteristic and an ordinary diode junction. The relative effects of R_L and R_S are apparent in different regions of the curve.

Compared with gate current, the equivalent circuit and characteristics in Figure 1.6 are valid only when anode current is zero or small. This information is useful for reverse gate bias, for very low forward gate current, and for examination of trigger circuits with the anode disconnected.

Characteristics at Triggering Point

The equivalent gate circuit must be modified to include the anode current flow across the gate junction with the anode supply connected. (See Figure 1.7.) The total current through the junction and the voltage drop across the junction increases more rapidly than with gate drive alone since anode current is a function of gate current. The small-signal impedance between the gate and cathode terminals changes smoothly from positive to zero to negative resistance as anode current increases. (See Figure 1.8.) When the characteristic curve becomes tangential with the load line of the gate signal source impedance at point (1), the anode current becomes regenerative and the SCR can then trigger. For specification purposes, "I_{GT}" is the maximum gate supply current required to trigger, measured at the peak of the curve.

It is apparent that the impedance of the gate signal source is another factor in the criteria for thyristor triggering.

Characteristics After Triggering

The gate impedance changes after the thyristor triggers and the anode current flow across the gate-cathode junction is sufficient to maintain conduction. Figure 1.7 shows that it behaves like a source, with a voltage equal to the gate-cathode junction drop (at the existing anode current) and an internal impedance R_L. This voltage is very nearly equal to the voltage drop between anode and cathode. Figure 1.9 shows characteristics under this condition. The curvature in Quadrant IV (QIV) is effectively the result of an increasing R_L as more current is withdrawn from the gate, a result of the distributed nature of the gate junction shown in Figures 1.4 and 1.5. The current flow through the lateral resistance of the p-type layer causes current to cease flowing through that portion of the p-n junction nearest the gate terminal as withdrawing current reduces the gate-to-cathode terminal voltage. This causes an

increase in current density in areas remote from the gate terminal. The higher current density and power dissipation in the lateral resistance can cause thermal damage to the thyristor.

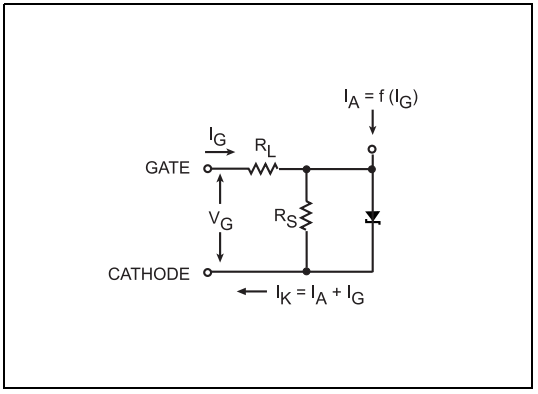


Figure 1.7 Gate-Cathode Equivalent Circuit [$I_A = f(I_G)$]

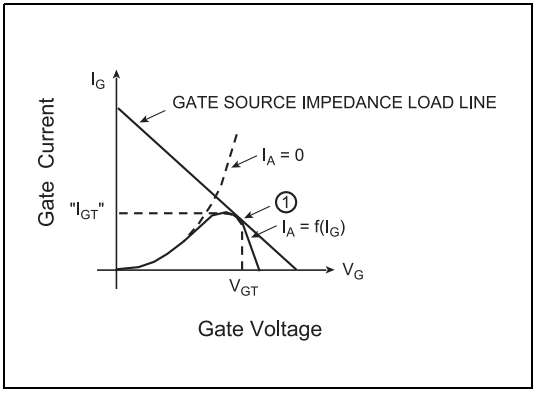


Figure 1.8 Gate Characteristics, Anode Connected

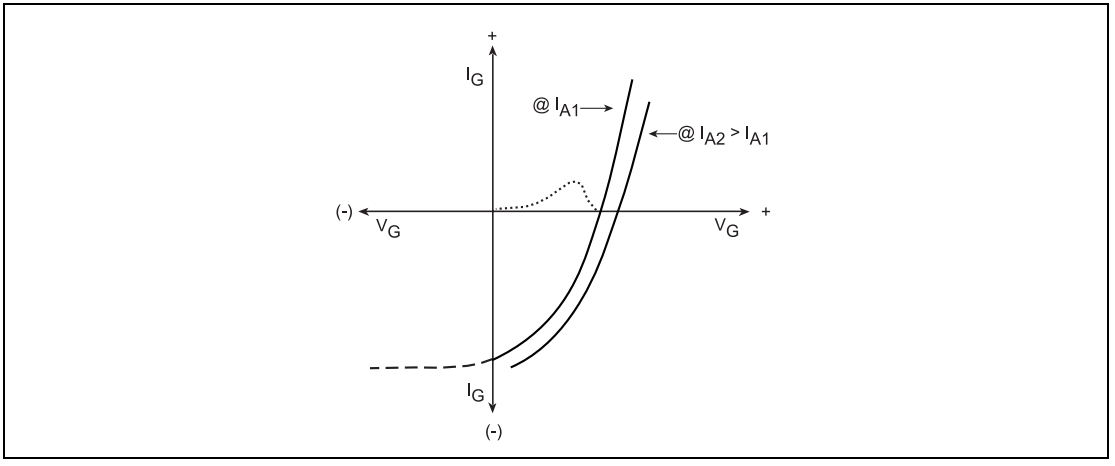


Figure 1.9 Gate Characteristics After Triggering

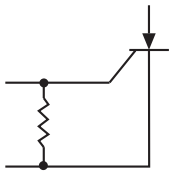
In some cases, the gate voltage produced by conduction of one SCR can produce adequate triggering current in the gate of the other SCR if two SCRs are connected with common gates and cathodes. Turning on both SCRs simultaneously may be the desired effect in many instances. In other cases, such as when the anode supply voltages of the two are 180 degrees out of phase, the existence of gate current in the reverse-biased SCR can cause triggering at the instant it becomes forward-biased because of stored charge in the p-type layer. It can also cause excessive reverse current by the remote-base transistor action.

Effects of Gate-Cathode Impedance and Bias

The preceding section described the criteria for triggering, involving the gate current, gate signal source impedance, and anode supply (load) impedance. The interaction between gate and anode circuits demands examination in some depth.

Gate-Cathode Resistance

The two-transistor analogy shows that a low external resistance between gate and cathode bypasses some current around the gate junction, requiring a higher anode current to initiate and maintain conduction. (See Figure 1.10.) Low-current, high-sensitivity SCRs are triggered by such a low current through the gate junction that a specified external gate-cathode resistance is required in order to prevent triggering by thermally-generated leakage current. This resistance bypasses also some of the internal anode current caused by rapid rate-of-change of anode voltage (dv/dt). It raises the forward breakover voltage by reducing the efficiency of the n-p-n "transistor" region, thus requiring a somewhat higher avalanche multiplication effect to initiate triggering. The current which bypasses the gate junction also affects the latching and holding anode currents.



Primary Purpose:
(1) Increase dv/dt capability
(2) Keep gate clamped to assure V_{DRM} capability
(3) Lowers t_q time

Related Effects:
Raises the device latching and holding current

Figure 1.10 Gate-Cathode Resistance

The relative effect of the external resistance is dependent upon the magnitudes of the internal resistances, R_L and R_S shown in Figures 1.4 and 1.5. For low-current thyristors, the type of construction used generally leads to high values of R_S (virtually no emitter shorting) and low values of R_L because the die/chip size is small. Figure 1.11 shows the effect of external gate-to-cathode resistance upon holding currents for the T106 low-current SCR. For low-current SCRs, the spread between maximum and minimum values represents production variations of the internal resistances and variations in current-gain of the equivalent "transistor" regions.

External gate shunt resistance also slightly reduces the turn-off time (t_q) of the SCR by assisting in recovering stored charge, by raising the anode holding current, and by requiring higher anode current to initiate re-triggering.

Sensitive SCRs benefit most from gate shunting because they are "sensitive."

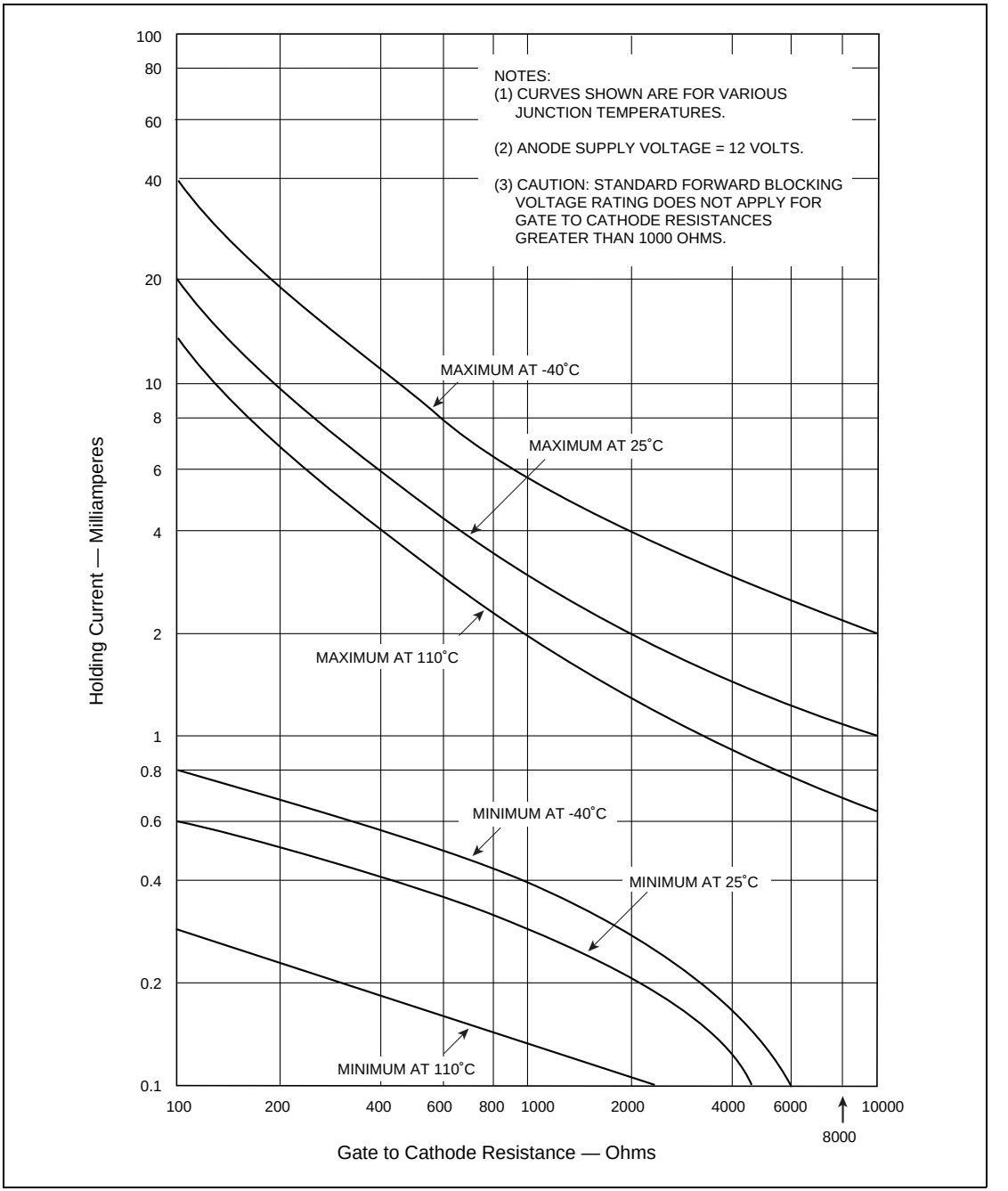
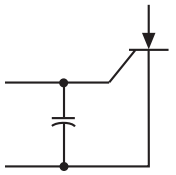


Figure 1.11 Maximum and Minimum Holding Current Variation with External Gate-to-Cathode Resistance for T106 SCR

Gate-Cathode Capacitance

A low-shunt capacitive reactance at high frequencies can reduce the sensitivity of a thyristor to dv/dt effects, in much the same manner as a resistor, while maintaining higher sensitivity to DC and low-frequency gate signals. The integrating effect is useful particularly when high-frequency “noise” is present in either the anode or gate circuits. (See Figure 1.12.)



Primary Purpose:
(1) Increase dv/dt capability
(2) Remove high frequency noise

Related Effects:
(1) Increases delay time
(2) Increases turn-on interval
(3) Lowers gate signal rise time
(4) Lowers di/dt capability
(5) Increases t_q time

Figure 1.12 Gate-Cathode Capacitance

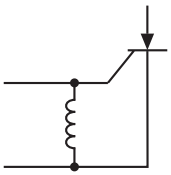
The gate voltage must increase as anode current increases at the point of triggering. Therefore, a capacitor connected between gate and cathode tends to retard the triggering process, yielding longer delay-time and rest-time of anode current. This action can be detrimental when a high di/dt of anode current is required.

The gate acts as a voltage source after turning on the SCR, charging the capacitor to the voltage drop across the gate junction. Since this voltage is generally higher than the gate voltage required to trigger the SCR (V_{GT}), the energy stored in the capacitor can supply triggering current for a period of time after removal of anode current. It is possible for this to cause the SCR to fail to commutate. A capacitor of approximately 10 microfarads can maintain gate current for over 10 milliseconds in low-current SCRs, preventing commutation in half-wave, 50- or 60-Hz circuits.

If the gate triggering signal is a low-impedance pulse generator in series with a capacitor, the gate current can charge the capacitor during the pulse, and because of the polarity at the end of the pulse, the SCR gate will be driven negative. At this instant the negative drive may raise the holding current requirement above the anode current and turn off the SCR for low values of anode current.

Gate-Cathode Inductance

Inductive reactance between gate and cathode reduces sensitivity to slowly changing anode current or gate source current while maintaining sensitivity to rapid changes. (See Figure 1.13.) This differentiating effect is useful in improving thermal stability since changes in thermal leakage current are slow. It provides sensitivity to a flash of light with insensitivity to steady-state ambient light when used with a light-activated SCR.



Primary Purpose:
(1) Decrease DC gate sensitivity
(2) Decrease t_q time

Related Effects:
(1) Negative gate current increases holding current and causes gate area to drop out of conduction
(2) In pulse gating the gate signal tail may cause the device to drop out of conduction

Figure 1.13 Gate-Cathode Inductance

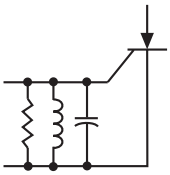
With anode current flowing, the gate voltage causes current to flow out of the gate through the inductance. The rate at which this current builds up after triggering is a function of the L/R ratio of the inductance to both internal and external resistance. As this negative gate current rises, the holding current of the thyristor also rises. The thyristor may drop out of conduction if anode current is low or is increasing more slowly than negative gate current.

Negative gate current will continue for a period of time after the SCR anode current ceases, decaying according to the L/R time-constant. This negative gate current during the turn-off condition can reduce turn-off time (by nearly 10:1 in small SCRs) and can permit a faster rate of re-applied off-state voltage (higher dv/dt).

The pulse can produce a current flow through the inductor if a triggering current pulse is applied in parallel with an inductor and the gate. The inductor current continues to flow as a negative gate current at the termination of the pulse, thereby raising holding current and possibly causing turn-off of the SCR.

Gate-Cathode LC Resonant Circuit

A parallel LC resonant circuit connected between gate and cathode can provide a frequency-selective response and can also produce a condition of oscillation. (See Figure 1.14.)



Primary Purpose:
Frequency selection

Related Effects:
Unless circuit is "damped" the positive and negative gate current may inhibit conduction or bring about sporadic anode current

Figure 1.14 Gate-Cathode LC Resonant Circuit

Obtain the oscillating condition by making the anode current value intermediate between the normal holding current ($I_G = 0$) and the holding current with maximum negative gate current flowing through the inductor. After initial SCR turn-on the negative gate current can increase until the SCR turns off. After turn-off, inductor current charges the capacitor to a negative voltage; then, the capacitor discharges into the inductor in a resonant manner. The capacitor voltage can re-trigger the SCR when it swings positive again and the process repeats indefinitely. Avoiding such oscillation requires damping.

Positive Gate Bias

The presence of positive current in the gate when applying reverse voltage to the anode may increase substantially reverse blocking (leakage) current through the device. As a result the SCR must dissipate additional power. Therefore, it is necessary either to make provision for this additional loss or to take steps to limit it to a negligible value.

Figure 1.15 gives the temperature derating for different SCR lines at various gate drive duty cycle (percent of full cycle or 360 electrical degrees) for values of peak positive gate voltage. For proper application, include this loss in the total device dissipation. It is necessary to subtract the temperature derating, ΔT, (in Figure 1.15) from the maximum allowable case temperature (found from the device rating curve) for the proper cell type and conduction angle. Subtract from the ambient temperature curve for lead mounted device. Derating becomes negligible if the gate voltage is less than 0.25 volt or the temperature derating turns out to be 1°C or less.

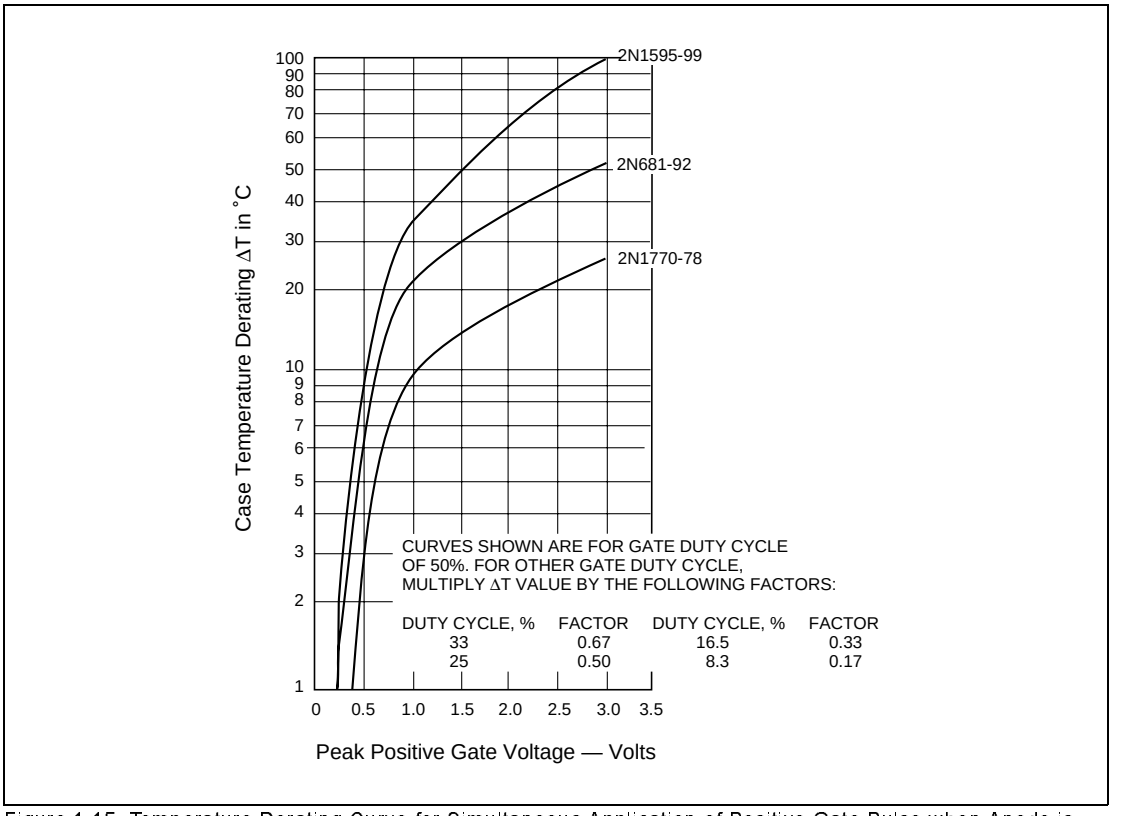


Figure 1.15 Temperature Derating Curve for Simultaneous Application of Positive Gate Pulse when Anode is Negative

A gate-clamping circuit (as shown in Figure 1.16) provides one means of limiting the additional reverse dissipation to a negligible value for low- and medium-current SCRs. When the anode is negative, connect resistor R_A and a diode from gate to attenuate positive gate signals. For a given peak value of open circuit gate source voltage, Figure 1.16 gives the maximum ratio of the value of R_A to R_G that safely clamps the gate for all values of reverse voltage within the reverse voltage rating of the SCR.

An alternate way to limit additional reverse leakage dissipation due to positive gate voltage is to insert in series with the SCR a rectifier diode that has a lower reverse blocking current. In this manner the diode assumes the greater share of the reverse voltage applied to the series string, significantly reducing reverse dissipation in the SCR.

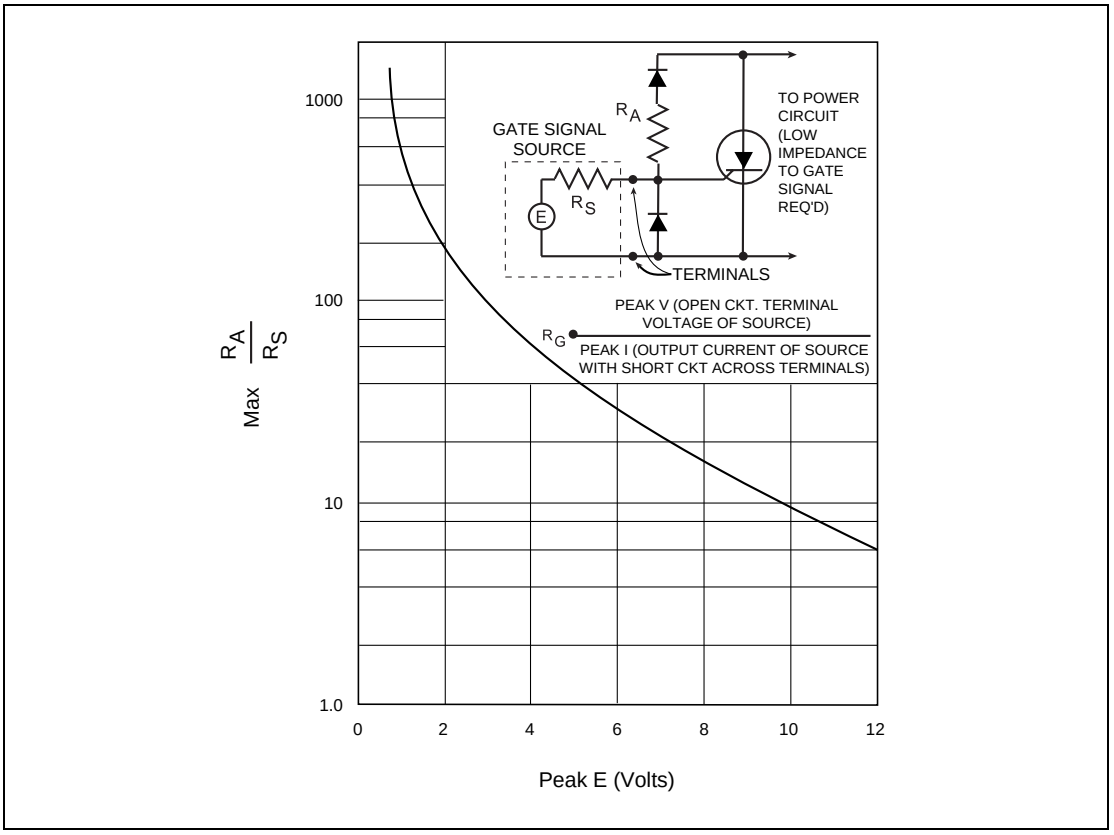


Figure 1.16 Gate Clamp Circuit for Controlled Rectifier

Negative Gate Bias

Never allow the gate to become more negative with respect to the cathode than is indicated on the sensitive gate SCR data sheet. For example, the gate of the 2N5064 has a rated peak reverse voltage (V_{GRM}) of 5 volts. If it is possible for the gate to swing more negative than the rated value, connect a diode either in series with the gate or from cathode to gate to limit the reverse gate voltage.
A considerable negative gate current (conventional current flow out of the gate) can be caused to flow if the cathode is disconnected with the gate connected to common while the SCR is conducting forward load current (conventional current flow from anode to cathode). Initially only the impedance of the gate circuit would limit this current and could cause an excess of allowable gate dissipation, leading to possible failure of the SCR.

Negative gate bias tends to increase the forward breakover voltage V_{BO} and the dv/dt withstand capability at a given junction temperature for small SCRs without internal emitter shorting when the anode is positive. For example, the T106 has V_{DRM} specified for a certain value of gate-to-cathode resistance (R_{GK} = 1000 ohms) and at a specified junction temperature.

Figure 1.17 shows a voltage bias arrangement. Resistor R_b goes to a negative supply instead of merely returning to the cathode. The voltage source E_b establishes the following current:

$$I_b \cong \frac{E_b - D}{R}$$ where D is the voltage drop across diode CR_1 (typical value 0.7 volt)

The diode provides a fixed negative bias voltage gate-to-cathode for the SCR. A disadvantage of this approach is the loss of input sensitivity due to resistor R_b.

Figure 1.18 shows a current bias scheme useful for smaller junction diameter SCRs. Selecting resistor R_b and the bias source establishes a bias current $I_b \approx I_{FXM}$ through resistor R_b in the direction indicated; I_{RXM} is the maximum forward-blocking (leakage) current of the SCR under the prevailing junction temperature and anode voltage. Selection of I_b in this manner yields a "worst case" design on the assumption that most, if not all, I_{DRM} diverts from the SCR emitter (gate-cathode junction). Limit this approach to SCRs with sufficient reverse gate power ratings to handle reverse current I_b at its associated reverse gate voltage.

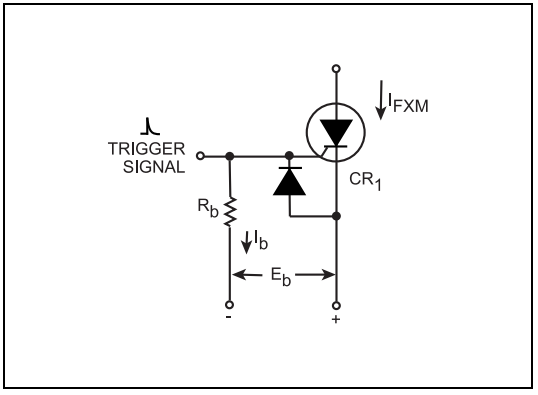


Figure 1.17 Negative Gate Voltage Bias Arrangements

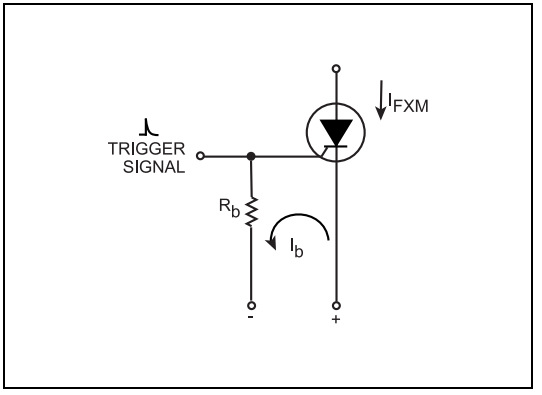


Figure 1.18 Negative Gate Current Bias Arrangements

Figure 1.19 shows the improvement achieved in dv/dt withstand capability by negative gate biasing for a typical SCR. It shows the effect of gate bias on the allowable time constant of application of forward blocking voltage without having the SCR switch on. For the open gate condition, the zero gate voltage curve corresponds to the time constant values given on specification sheets. Figure 1.19 extends the usefulness of this information for different values of gate bias.

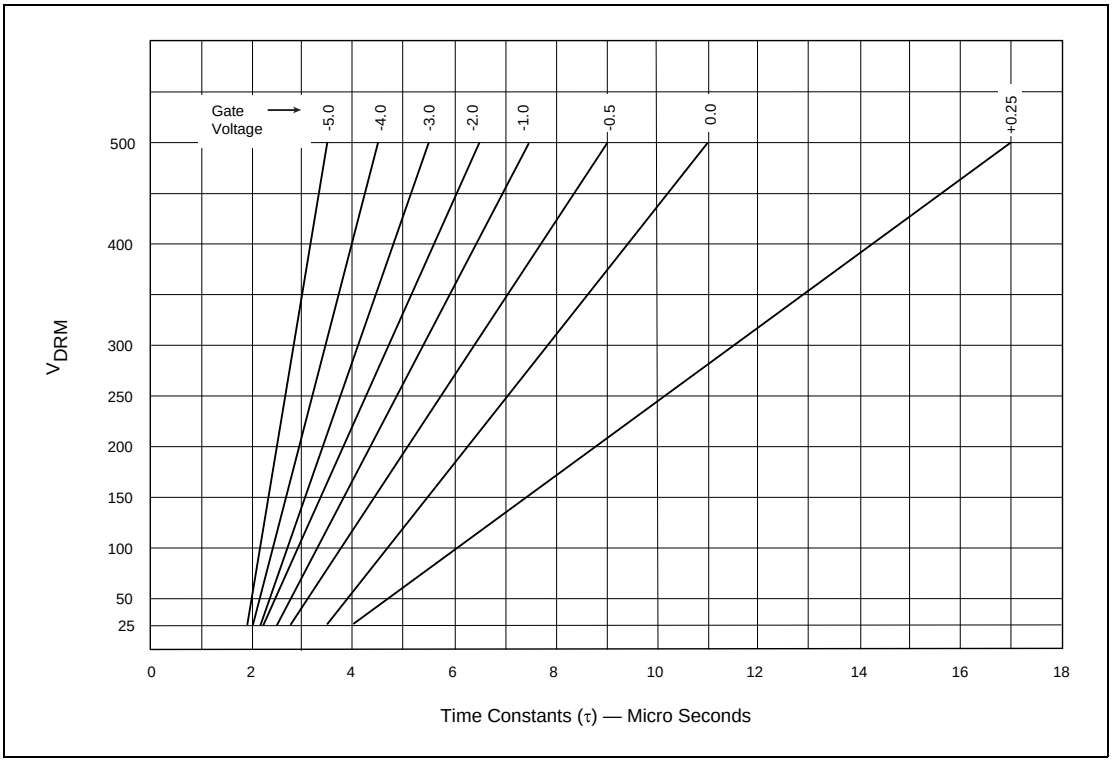


Figure 1.19 Effect of Gate Bias on Allowable Time Constant of Application of Forward Blocking Voltage (dv/dt)

It is possible to design circuits which apply a negative gate bias or short the gate to the cathode only while dv/dt is being applied. These circuits do not degrade the gate signal as much as those shown in Figure 1.17 but are expensive for most applications.

The basic idea is to differentiate the dv/dt applied to the anode, invert the polarity, and apply it to the gate. Figure 1.20 shows a transistorized dynamic snubber. R_1C supplies base current to Q_1, turning it on when anode voltage is rising. Gate triggering would be lost during the time of rising dv/dt since the gate is being shunted. However, the insertion of Q_2 avoids this problem since now the gate signal not only triggers the SCR but first shunts the base drive to Q_1. Both Q_1 and Q_2 are epitaxial transistors with low saturation voltages.

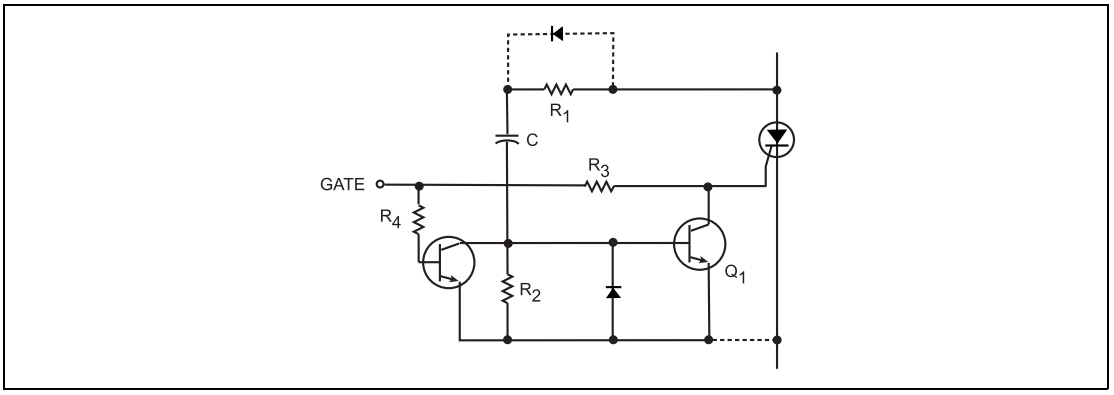


Figure 1.20 Transistor Snubber to Improve dv/dt

Because of the shunting effects of R_S, gate shorting has little influence on large area devices and devices with emitter shortings. (See Figure 1.7.) Conservative circuit design practice is not dependent upon increasing V_{BO} by negative gate biasing unless V_{BO} is specified with bias resistor.

Because it is mainly a function of carrier lifetime in an area not accessible by the gate, the influence of turn-off time by different gate bias techniques appears very limited.

Effects of Anode Circuit upon Gate Circuit

Discussions in previous sections presented the anode circuit voltage and impedance as determining factors in triggering and presented the effect of anode current. Note two other effects: junction capacitance in the SCR can couple high-frequency signals from the anode to the gate circuit, which may interfere with normal operation of the trigger circuit although not causing triggering.

A voltage appears at the gate terminal when the anode voltage of the SCR reaches either the forward breakover or reverse avalanche voltage. In the case of forward breakover voltage, a forward anode current starts flowing which produces a positive gate voltage, as in normal conduction. The gate junction becomes reverse biased when the reverse avalanche voltage is reached. Depending on the magnitude of R_S the negative voltage appearing at the gate terminal may rise to the avalanche voltage of the gate junction. If a reverse voltage transient on the anode exceeds reverse avalanche, the reverse-blocking junction of the SCR no longer blocks, thereby applying the transient energy to the gate junction in reverse. The gate junction and any external circuit connected to the gate may then receive excessive voltage and current from this process.

The gate is essentially at the same potential as the anode when an SCR is conducting. When the SCR is non-conducting, the gate potential is not related to anode potential within the normal operating range. However, the gate goes through an intermediate phase during the commutating transition from conduction to non-conduction which can result in a large negative voltage appearing at the gate terminal. If an SCR is commutated (as in a DC chopper or flip-flop circuit) by the step application of a reverse bias, the gate voltage is initially the normal forward gate-cathode junction drop until that junction recovers, whereupon both anode and the gate go negative. The gate voltage then follows anode voltage until the main reverse-blocking (p-n) junction recovers, at which time the gate reverts to its normal characteristics.

Small SCRs in particular readily reflect these transitions. Lower values of internal shunt resistance R_S somewhat mask the effects on larger SCRs. The negative transient at the gate can cause malfunction or damage in the external gate circuit.

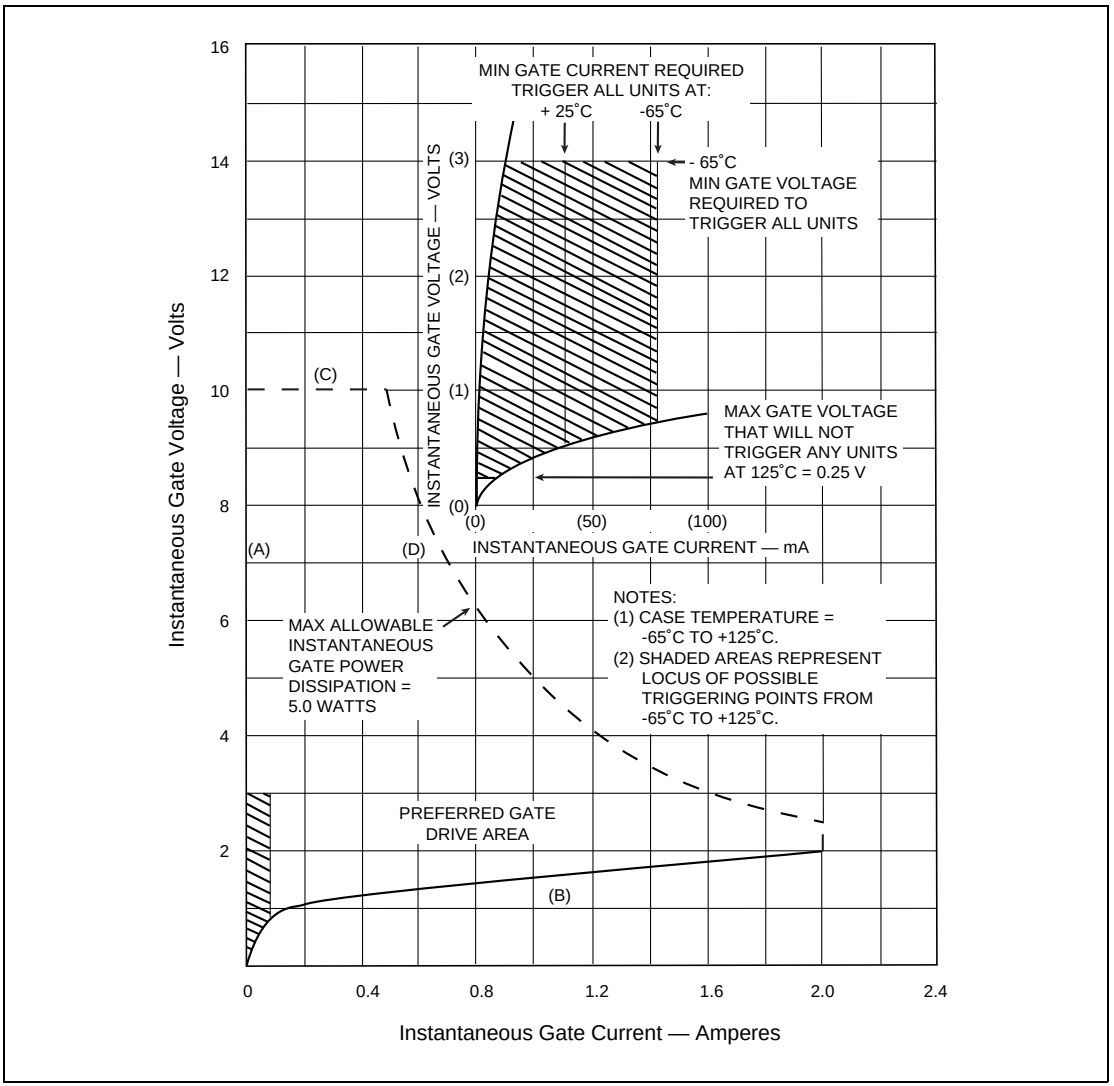


Figure 1.21 DC Gate Triggering Characteristics (for 2N681 SCR)

The DC gate trigger characteristics of an SCR are similar to the graph in Figure 1.21 which applies to the 2N681 SCR. The graph shows gate-to-cathode voltage as a function of positive gate current (flow from gate to cathode) between limit lines (A) and (B) for all indicated SCRs. These data apply to a zero-anode-current condition (anode open).

The basic function of the trigger circuit is to simultaneously supply the gate current to trigger I_{GT} and its associated gate voltage to trigger V_{GT}. The shaded area in Figure 1.21 contains all the possible trigger points (I_{GT}, V_{GT}) of all SCRs conforming to this specification. Therefore, the trigger circuit must provide a signal (I_G, V_G) outside the shaded area in order to reliably trigger all SCRs of that specification.

The shaded area in Figure 1.21 bounds the "preferred gate drive area" of SCR gate operation. This shaded area represents the locus of all specified triggering points (I_{GT}, V_{GT}), the limit lines (A) and (B), line (C) representing rated peak allowable forward gate voltage V_{GF}, and line (D) representing rated peak power dissipation P_{GM}. Some SCRs may also have a rated peak gate current I_{GRM} which would appear as a vertical line joining curves (B) and (D).

The upper right-hand portion shows the detail of the locus of all specified trigger points, and the temperature dependence of the minimum gate current to trigger I_{GTMIN}. The lower the junction temperature, the more gate drive triggering requires. (Some specifications may also show the effect of forward anode voltage on trigger sensitivity. Increased anode voltage tends to reduce the gate drive requirement, particularly with small SCRs.) Figure 1.21 also shows the small positive value of gate voltage below which no SCR of the particular type will trigger.

Load Lines

The trigger circuit load line must intersect the individual SCR gate characteristic in the "preferred gate drive area" region in Figure 1.21. Furthermore, locate the intersection, or maximum operating point, as closely to the maximum applicable (peak, average, and so on) gate power dissipation curve as possible. Gate current rise times of several amperes per microsecond minimize anode turn-on time, particularly when switching high currents. The result is minimum turn-on anode switching dissipation and minimum jitter.

Construction of a "load line" is a convenient means of placing the maximum operating point of the trigger circuit/SCR gate combination into the preferred triggering area. Figure 1.22 illustrates a basic trigger circuit of source voltage e_S and internal resistance R_S driving an SCR gate. It also shows the placement of the maximum operating point well into the "preferred trigger" area close to the rated dissipation curve. Construct the load line by connecting a straight line between the trigger circuit open circuit voltage E_{OC} (entered on the ordinate) and the trigger circuit short circuit current (entered on the abscissa):

$$I_{sc} = \frac{E_{oc}}{R_s}$$

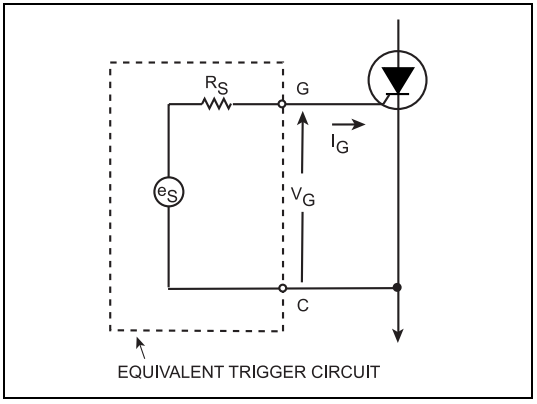


Figure 1.22 Gate Circuit

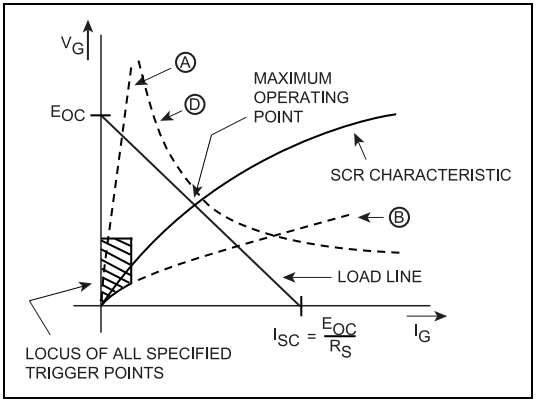


Figure 1.23 Load Line Superimposed on Gate Trigger Characteristic

The load line sweeps across the graph, starting as a point at the origin and reaching its maximum position, the load line, at the peak trigger circuit output voltage if the trigger circuit source voltage is a function of time $e_S(t)$.

Base the applicable gate power curve selection on whether average or peak allowable gate power dissipation is limiting. For example, do not exceed the average maximum allowable gate dissipation (0.5 watt for 2N681 if using a DC trigger. If using a trigger pulse, apply the peak gate power curve (for the 2N681)—the 5-watt peak power curve (D) in Figure 1.21). The duty cycle of the trigger signal determines the limiting allowable gate power dissipation curve according to the following equation:

peak gate drive power X pulse width X pulse repetition rate ≤
allowable average gate power for intermediate gate trigger waveforms

Inverter SCRs that require a stiff gate signal because of high di/dt and high-frequency operation often have peak pulse gate power curves. (See Figure 1.24). These pulse curves take advantage of the transient thermal resistance of the gate in order to achieve higher power pulses. Again, do not exceed the average gate power dissipation.

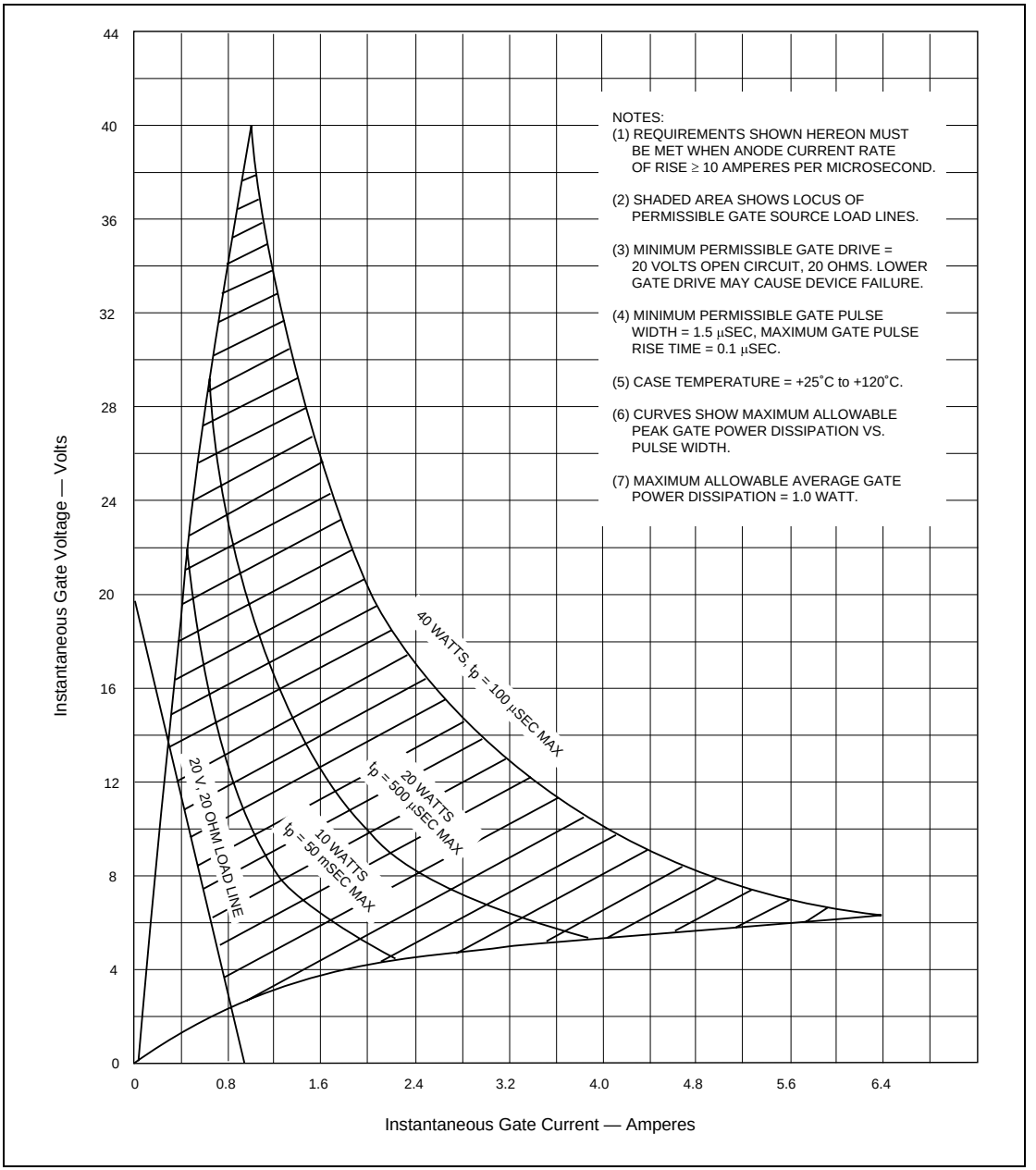


Figure 1.24 Gate Trigger Requirements for High Frequency and High di/dt Operation

Positive Gate Voltage That Will Not Trigger SCR

Figure 1.21 also indicates the maximum gate voltage that will not trigger the SCR. For example, in the illustration this value is 0.25 volt for the 2N681 at 125°C junction temperature. This limit is important when designing a trigger circuit which has a standby leakage current when no trigger signal is present, such as saturable reactors and directly-coupled unijunction transistor trigger circuits. Connect a resistor across the output of the trigger circuit to prevent false triggering under these circumstances. Its value of resistance in ohms must be less than the maximum gate voltage that will not trigger divided by the maximum trigger circuit standby current.

Pulse Triggering

Thyristor specification is commonly in terms of the continuous DC gate voltage and current required to trigger. The DC data apply for trigger pulse widths down to 100 µsec. V_{GT} and I_{GT} increase for shorter pulse widths.

Like transistors, thyristors are generally charge controlled on a short-time basis. The free charge stored within the gate p-type layer of an SCR may be the difference between the incoming charge flow rate ($dq/dt = I_G$) and the internal recombination rate. The free charge is directly a function of gate current under DC conditions and for a given recombination rate. When the free charge reaches a certain level, the device triggers. Charging into the gate in less than the recombination time requires higher current (and higher voltage).

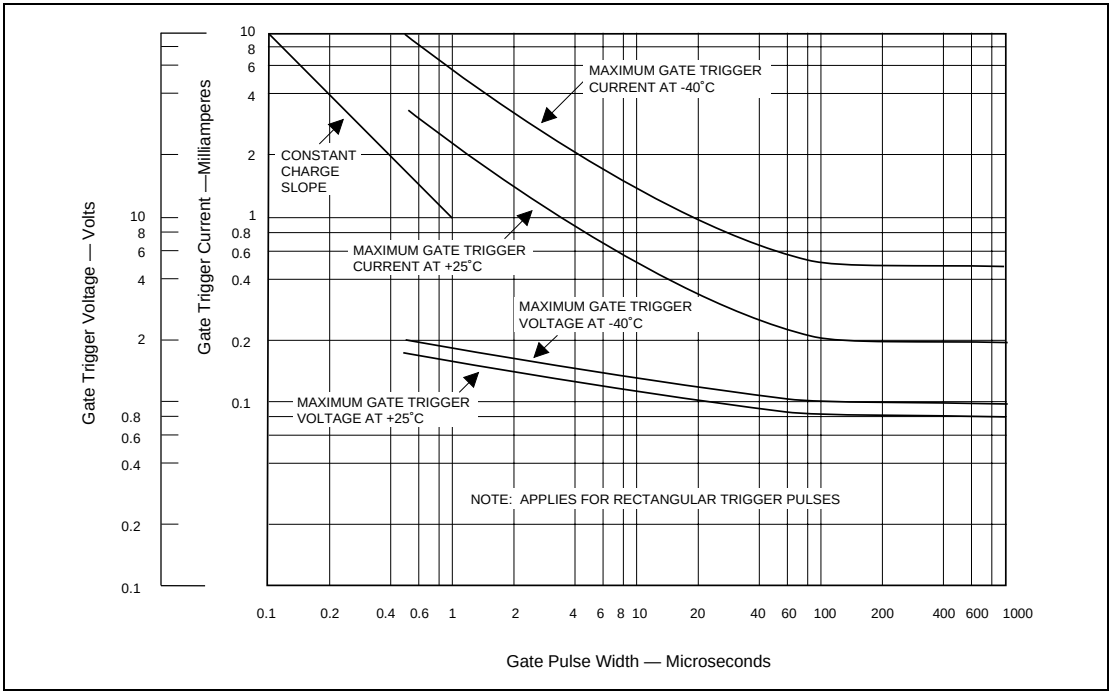


Figure 1.25 Effect of Trigger Pulse Width (T106 SCR) — Current and Voltage Requirements

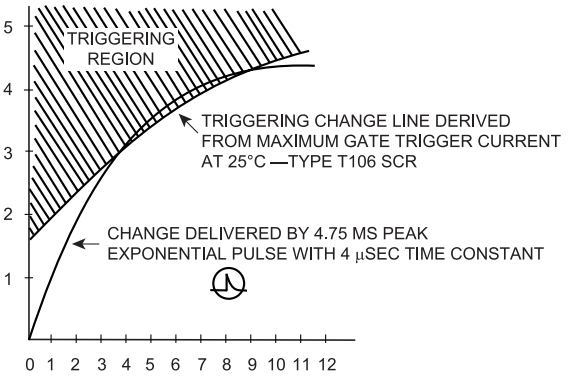


Figure 1.26 Effect of Trigger Pulse Width (T106 SCR) — Charge versus Time

Figure 1.25 shows the relationship between pulse width and peak current for a rectangular pulse to trigger the T106 SCR. Note that the current curves approach a constant-charge slope at the smaller pulse-widths. The point at which the pulse current curve departs from the DC current level is about 200 μsec for this small thyristor. Pulse current equal to the DC level down to about 20 μsec can trigger other SCR types with shorter recombination times.

The illustration in Figure 1.25 does not infer that only rectangular pulses are acceptable. Use any unidirectional waveshape which does not exceed gate current, voltage, and power ratings if the total charge is adequate. Plotting the integral of the actual current wave and the integral of the rectangular pulse current can determine proper charge criteria. (See Figure 1.26.) The triggering charge is adequate if the two curves cross.

Figure 1.27 shows the increase in gate drive required for triggering four types of SCRs with trigger signals of short pulse duration. Allow the anode current to build up rapidly enough for the SCR to trigger and reach the latching current before terminating the pulse. (Assume the latching current is three times the value of the holding current given on the specification sheet.) Use a maintained type of trigger signal for highly inductive anode circuits to ensure gate drive until latching current is attained.

Figure 1.28 shows a common on-state current when the discharge of a capacitor provides a latching current pulse in a highly inductive circuit.

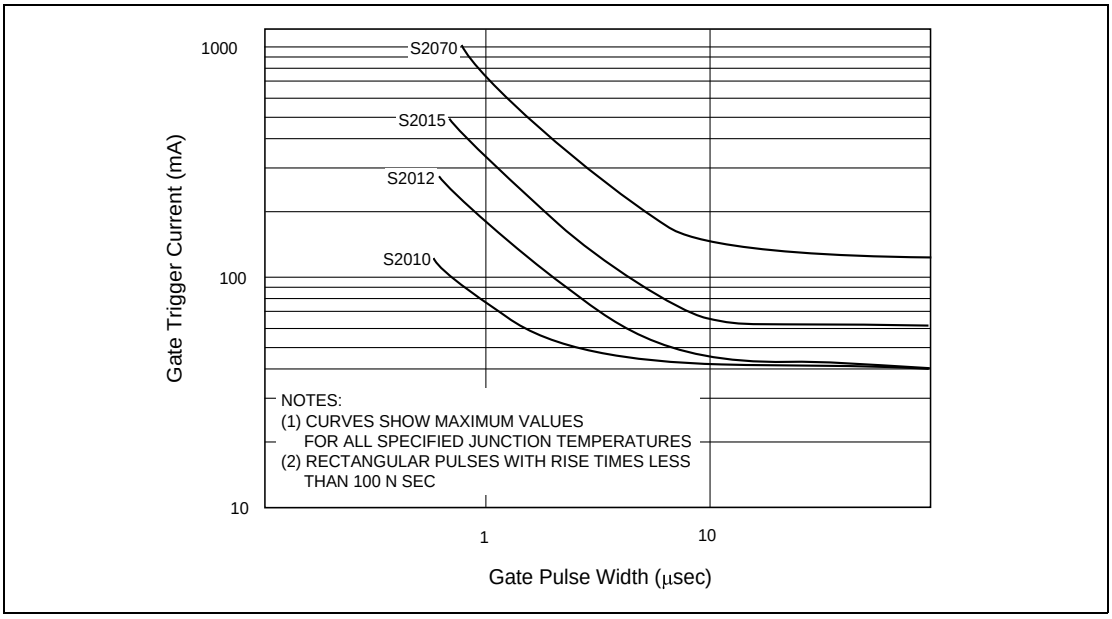


Figure 1.27 Gate Drive Required for Short Trigger Pulse Duration

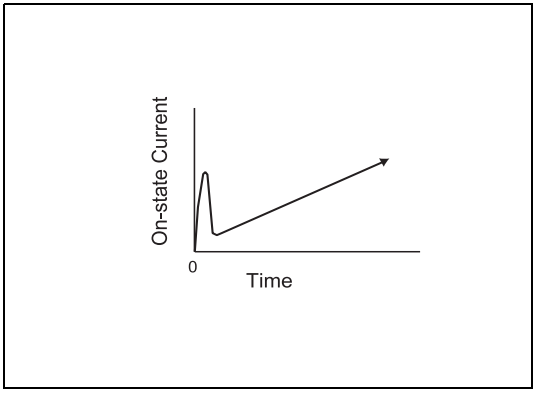


Figure 1.28 Current Waveform for Capacitive and Inductive Load

A slowly-rising anode current determined primarily by inductance in the circuit follows the latching pulse from the capacitor discharge. Very often, confusion exists regarding holding current and latching current in such cases. The device must remain in the on-state at the valley point where the main circuit takes over if the gate trigger pulse ends before the end of the initial current pulse.

The device goes out of conduction and the circuit will not latch if the device has a holding current higher than the valley current level provided. This is, however, a result of high device holding current rather than

latching current. It is a latching current problem rather than a holding current problem if the gate trigger signal lasts beyond the valley point before it is ended and the device still fails to latch.

The DC gate trigger characteristics are measured on a 100% basis in production for all SCRs, but the pulse trigger characteristics are based on a sampling only. Request special specification to ensure satisfactory pulse triggering for applications where the pulse trigger characteristics are critical.

Anode Turn-On Interval Characteristics

Figure 1.29 shows the turn-on, or switching, characteristics of a typical 2N1770 SCR. It is also representative of other SCR types. In this illustration percent anode voltage is a function of time, following application of the trigger signal at zero time, for switching from 500 volts and from 100 volts for two different circuit current levels.

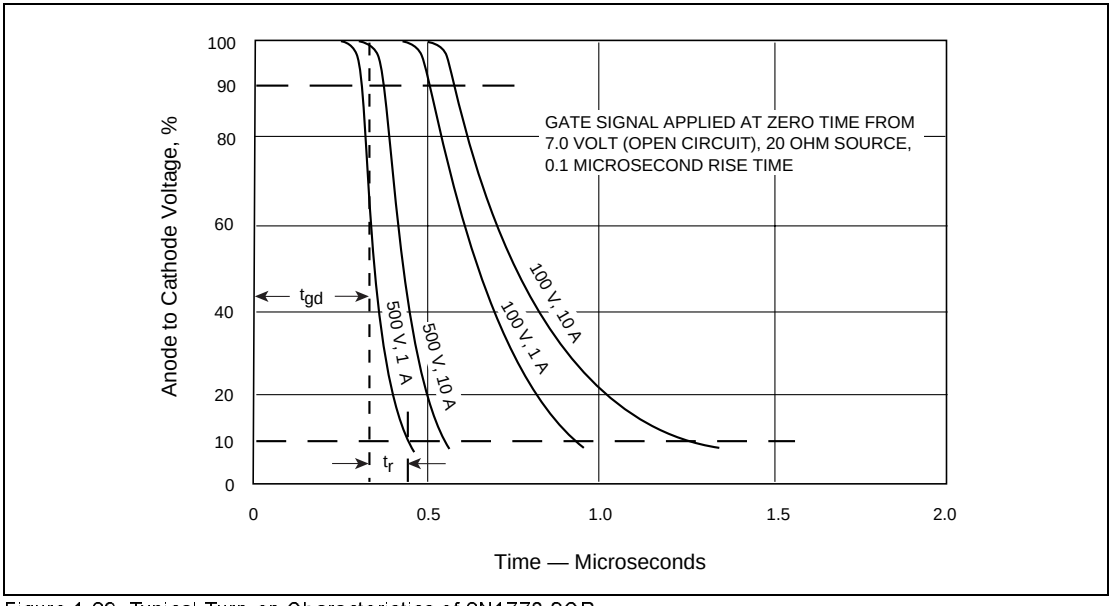


Figure 1.29 Typical Turn-on Characteristics of 2N1770 SCR

Delay time t_{gd} shown for the 500 volt ampere switching characteristic is the time between the 10% point of the leading edge of the gate current pulse and the 10% point of the anode voltage waveform. The delay time decreases as the amplitude of the gate current pulse increases but approaches a minimum value of 0.2 to 0.5 μsec for gate current pulses of 500mA or more.

Rise time t_r is the time required for the anode voltage to drop from 90% of its initial value to 10%, as indicated for the 500 volt ampere curve in Figure 1.29. In large part the circuit determines the rise of current as the voltage across the SCR falls. In a purely resistive circuit the current rises in the same manner as the voltage falls, thus the term rise time. It is important that the instantaneous voltage-current product during the turn-on interval not exceed the dissipation capability of the SCR. For this reason, it is necessary to limit the rate of rise of anode current (di/dt). A large gate drive within the allowable gate dissipation ratings of the SCR tends to reduce rise time and delay time. Drive the gate in the area of

"preferred triggering" close to the allowable gate power dissipation curve in order to minimize turn-on switching dissipation. (See Figure 1.21.) Amplifying gate SCRs do not require as strong a gate source as conventional thyristors and, therefore, allow the designer greater latitude in selection of a gate drive circuit.

Total turn-on time is $t_{on} = t_{gd} + t_r$. It is important to note that, as defined above, large turn-on switching dissipation can still occur after the termination of the turn-on time, particularly when switching from a high voltage into a large current.

If the gate is driven at two to three times the minimum amplitude required for triggering, the jitter, or variation of switching time from one cycle to the next, is usually less than 2 μsec at constant temperature.

Simple Resistor and RC Trigger Circuits

Repeatability over a temperature range sometimes requires finding the simplest and most economical means for triggering an SCR when some performance compromise can be made.

Figures 1.31 and 1.33 show a simple method of obtaining gate current for triggering the SCR (Figures 1.30 and 1.32 for triacs) from the main AC supply whenever the anode is positive with respect to the cathode. The anode voltage drops to the conduction value and the gate current decreases to zero as soon as the SCR triggers. Resistor R limits the peak gate current. Provide the diode in the gate circuit to prevent reverse voltage between cathode and gate during the reverse part of the cycle. It is possible to connect the diode between gate and cathode rather than in series with R. Initiate conduction by closing contact S_1 in Figure 1.30 or by opening contact S_2 (Figure 1.31). Interruption of load current occurs within one-half cycle after opening S_1 or closing S_2 due to line voltage reversal.

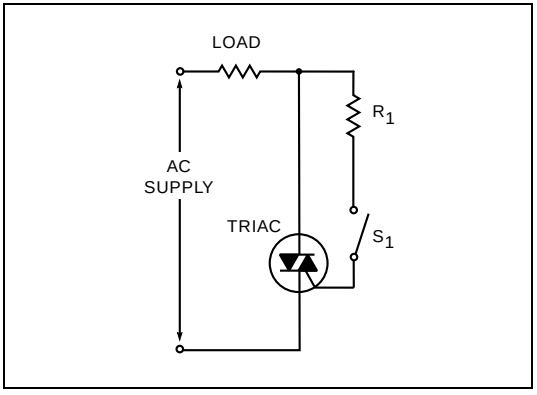


Figure 1.30 Static Switches — Full-wave TRIAC, Series Gate Switch

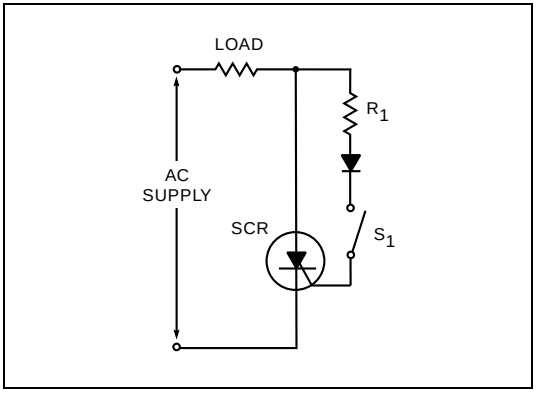


Figure 1.31 Static Switches — Half-wave SCR, Series Gate Switch

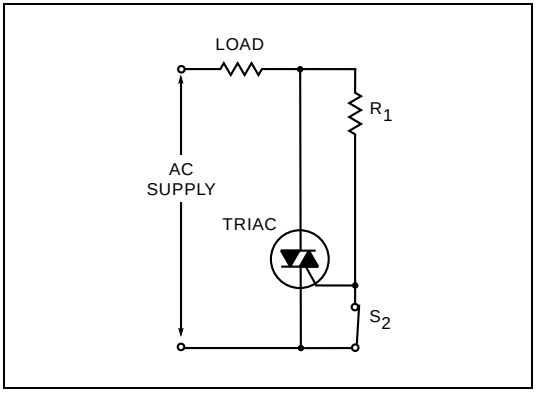


Figure 1.32 Static Switches — Full-wave Triac, Gate Shunt Switch

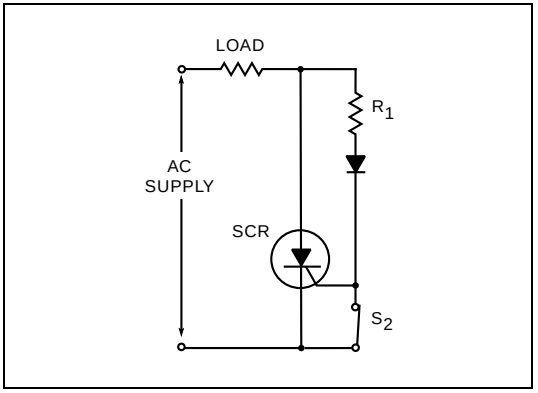


Figure 1.33 Static Switches — Half-wave SCR, Gate Shunt Switch

Simple resistor/capacitor/diode combinations trigger and control SCRs over the full 180 electrical degree range, performing well at commercial temperatures. These types of circuits operate most satisfactorily when SCRs have fairly strong gate sensitivities. Since in a scheme of this type a resistor must supply all of the gate drive required to turn on the SCR, the less sensitive the gate, the lower the resistance must be, and the greater the power rating. The same applies for triacs as shown in Figures 1.32 and 1.33.

Figures 1.34 and 1.35 show a very simple variable resistance half-wave circuit. It provides phase retard from essentially zero (SCR full "on") to 90 electrical degrees of the anode voltage wave (SCR half "on"). Diode CR_1 blocks reverse gate voltage on the negative half-cycle of anode supply voltage. It is necessary to rate blocking to at least the peak value of the AC supply voltage. Do not extend the retard angle beyond the 90-degree point because the trigger circuit supply voltage and the trigger voltage producing the gate current to fire I_{GF} are in phase. When $E_{AC} = E_m$, at the peak of the AC supply voltage, the SCR can still trigger with the maximum value of resistance between anode and gate. Do not delay the conduction beyond 90 electrical degrees with this circuit since the SCR triggers and latches into conduction upon reaching I_{GT} the first time.

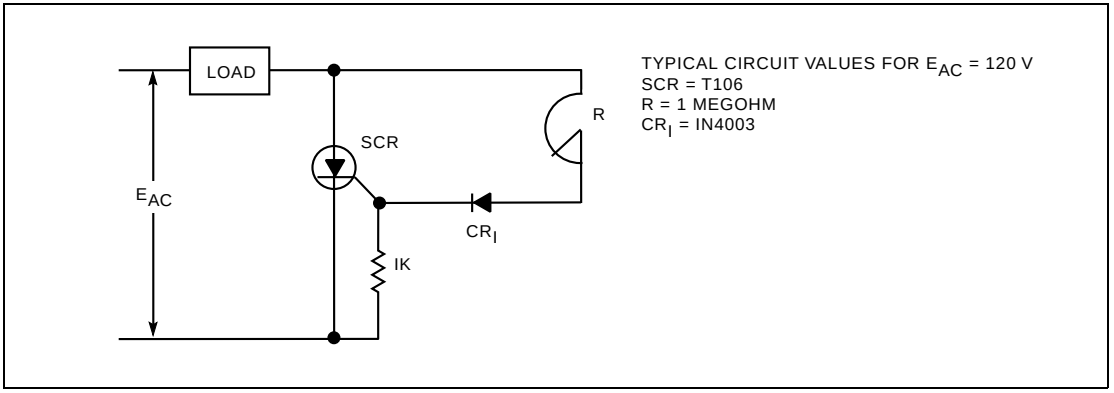


Figure 1.34 Simple Half-wave Variable Resistor Phase Control (Limited Range of Control) — Circuit Schematic

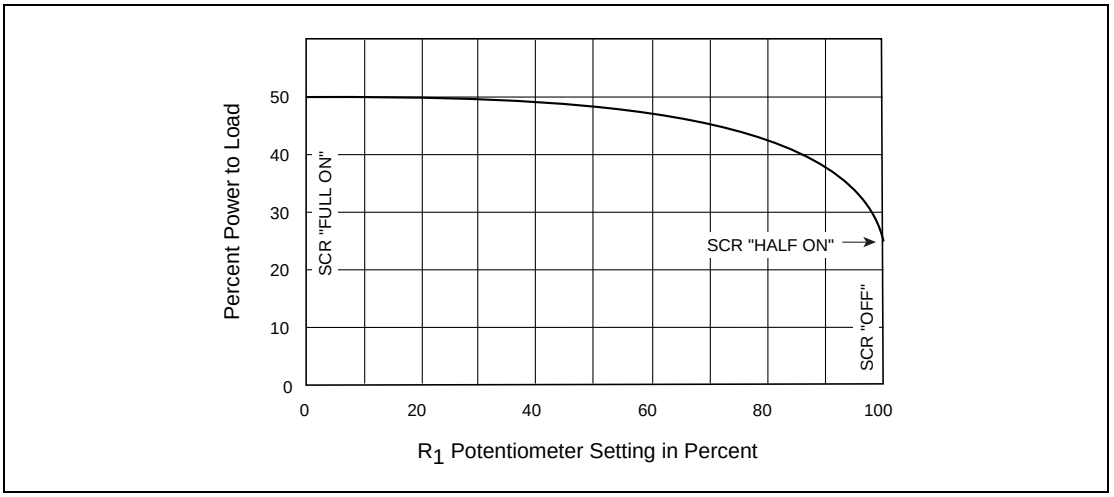


Figure 1.35 Simple Half-wave Variable Resistor Phase Control (Limited Range of Control) — Transfer Function

Figure 1.36 shows a graph of the transfer function of this circuit based on choosing the potentiometer R so that the SCR just does not fire at the maximum setting. The transfer function is very non-linear and the repeatibility of setting is not possible either with different SCRs or with temperature due to I_{GT} variation.

Figures 1.36 and 1.37 show an R-C-Diode circuit giving full half-cycle control (180 electrical degrees). On the positive half-cycle of SCR anode voltage the capacitor charges to the trigger point of the SCR in a time determined by the RC time constant and the rising anode voltage. The top plate of the capacitor charges to the peak of the negative voltage cycle through diode CR_2 on the negative half-cycle, resetting it for the next charging cycle.

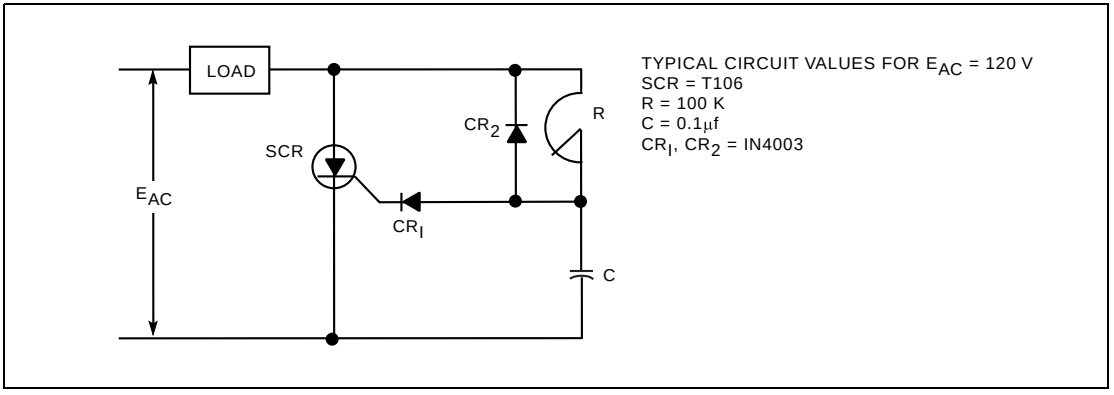


Figure 1.36 Simple Half-wave RC-diode Phase Control (Full 180° Control Range) — Circuit Schematic

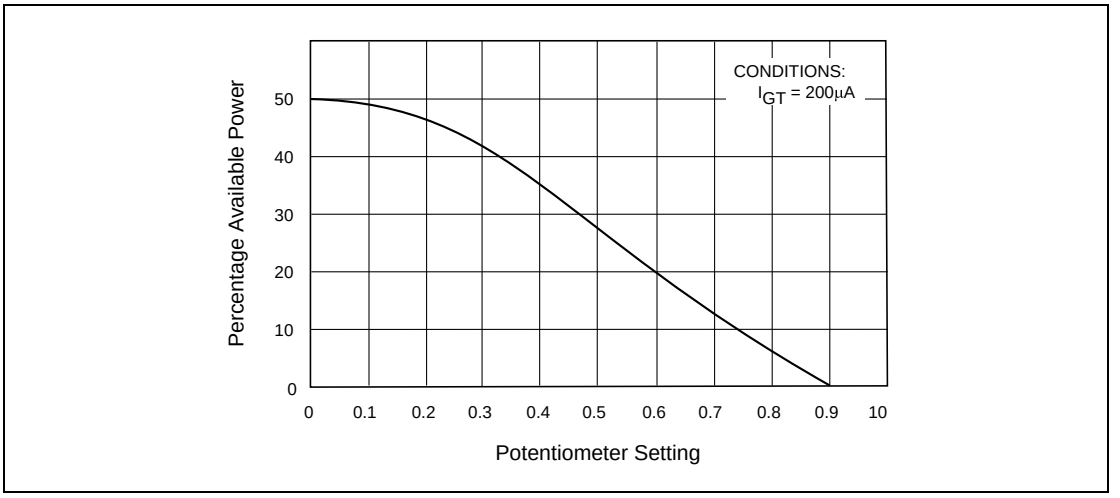


Figure 1.37 Simple Half-wave RC-diode Phase Control (Full 180° Control Range) — Transfer Function

Select the capacitor so that its charging current is high compared with I_{GT} at the instant of the latest desired firing angle since the line voltage through the resistor must supply the triggering current. Conversely, select the maximum value of R to produce I_{GT} at the latest desired firing angle, minus IR drop in the load at that point; then select C to produce V_{GT} at that point in time. However, similar to all simple RC triggering methods, non-linear output results as the transfer characteristic shows in Figure 1.38. Remember that the output varies with temperature and different devices because it depends so heavily on I_{GT}.

Figure 1.38 illustrates a slave circuit arrangement in which an independent half-wave circuit (SCR_2) triggers on one half-cycle at a predetermined phase angle. On the following half-cycle the slave circuit triggers SCR_1 at the same phase angle relative to that half-cycle. Capacitor C charges and discharges to the same voltage at the same time constant when SCR_2 does not trigger. The voltage across C is not sufficient to trigger SCR_1. As SCR_2 is triggered, capacitor C upon discharging sees a time integral of line voltage different from the one seen upon charging by the time integral of voltage appearing across the load. This action resets the capacitor to a voltage level related to the trigger delay angle of SCR_2. When the anode of SCR_1 swings positive on the next half-cycle it triggers at the end of this delay angle.

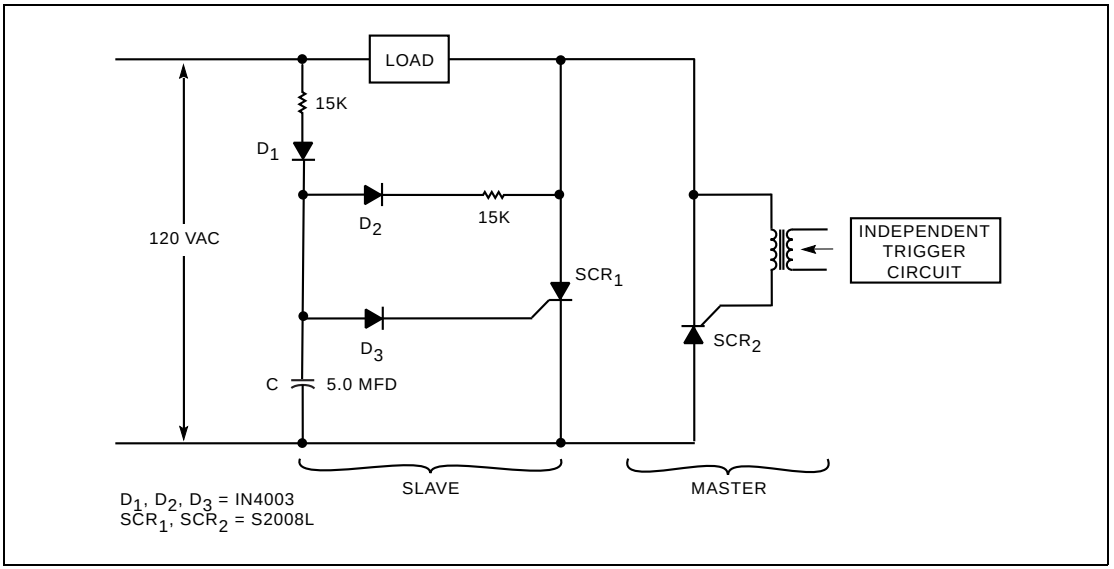


Figure 1.38 Three-Terminal, Full-wave, RC-diode Slaving Circuit for Full-wave Phase Control

AC Thyratron-type Phase Shift Trigger Circuits

Figure 1.39 illustrates a full-wave phase-controlled rectifier employing an R-C or R-L phase shift network to delay the gate signal with respect to the anode voltage on the SCRs. Thyratrons use many adaptations of this type of phase shift circuit.

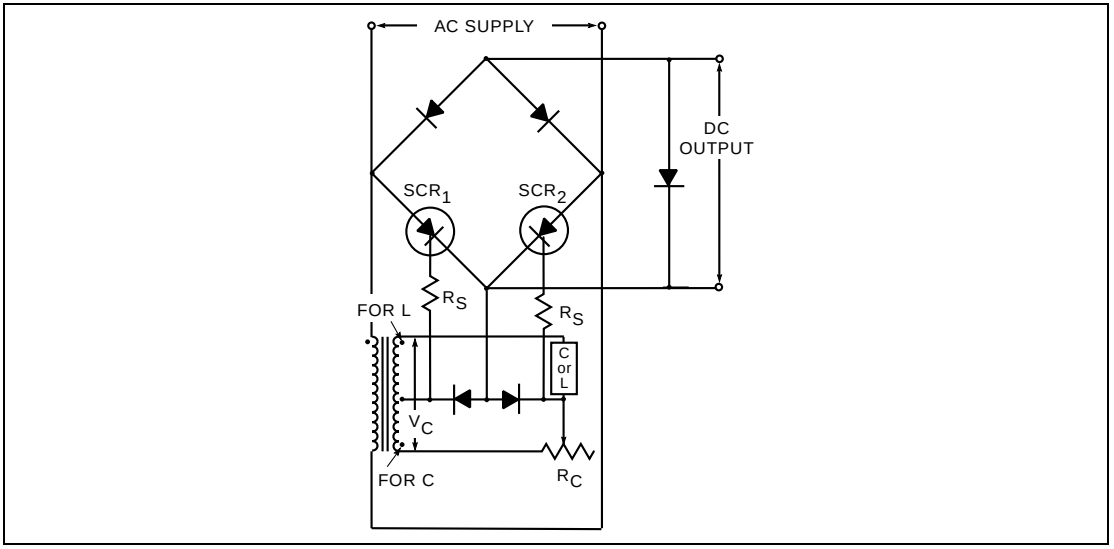


Figure 1.39 R-C or R-L Phase Shift Network Control of Single Phase Bridge Output

When using most SCRs, observe the following criteria to provide the maximum range of phase shift and positive triggering over the particular SCRs temperature range without exceeding the gate voltage and current limitations:

- Peak value of V_C > 25 volts
- $\frac{1}{2\pi fC}$ or $2\pi fL \leq \frac{Vc}{2} - 9$ where

  C = capacitance in farads
  L = inductance in henries
  V_C = peak end-to-end secondary voltage of control transformer
  f = frequency of power system
- $R_s = \frac{V_c - 20}{0.2}$ where R_S = series resistance in ohms
- $R_c \geq \frac{10}{2\pi fC}$ $10(2\pi fL)$ or $10(2\pi fL)$

Because of the frequency dependence of this type of phase shift circuit, the selection of adequate L or C components becomes easier at higher operating frequencies.

Saturable Reactor Trigger Circuits

Saturable reactors can provide a fairly steep wavefront of gate current together with a convenient means of control from a low-level DC or AC signal. This type of control is adaptable to feedback systems and provides the additional advantage of multiple, electrically-isolated inputs and outputs for more complex circuits.

Continuously Variable Control

Figure 1.40 shows a typical half-wave magnetic amplifier-type trigger circuit. Obtain the gate signal for triggering the SCR from winding 3-4 of transformer T_1. The winding 3-4 of T_2 presents a high impedance to the gate signal when the core of T_2 is unsaturated so that only a small voltage develops across R_3. When the core of T_2 saturates, the impedance of winding 3-4 of T_2 decreases by several orders of magnitude so that a large voltage appears at the gate of the SCR, causing it to trigger. Resistor R_2 limits the gate current to the rated value and resistor R_2 limits the gate voltage produced by the magnetizing current of winding 3-4 of T_2 so that the SCR does not trigger before the core of T_2 saturates. Diode CR_2 serves the dual purpose of preventing a reverse voltage on the gate of the SCR and preventing any reverse current through winding 3-4 which would produce an undesired reset of the core T_2.

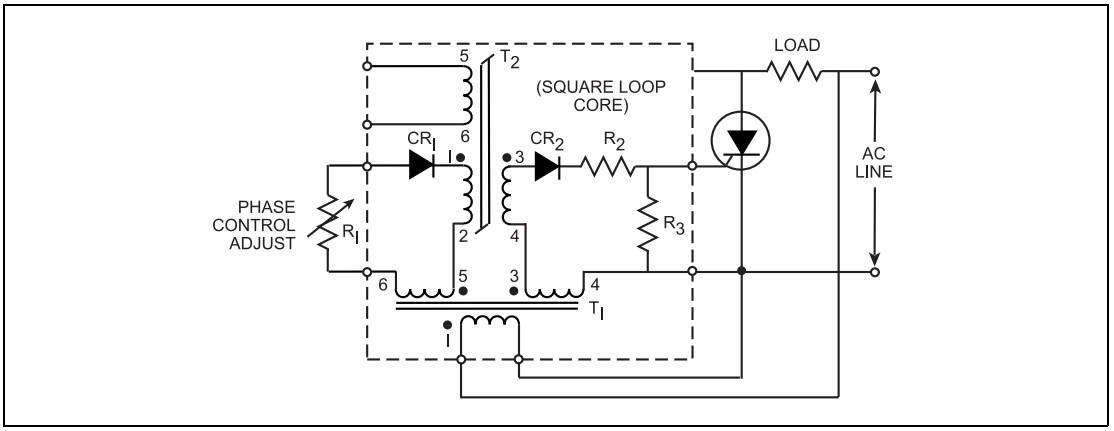


Figure 1.40 Typical Half-wave Magnetic Trigger Circuit

Control signals can be applied to either input 1 or input 2 or both. Input 2 operates in the reset mode by controlling the reset voltage on winding 1-2 of T_2 during the negative half-cycle. The setting of the potentiometer R_1 determines the amount of reset of the core during the negative half-cycle, which in turn determines the phase angle of the SCR conduction during the positive half-cycle. use other control circuits, such as a transistor amplifier stage, in place of R_1. Since winding 5-6 of T_1 furnishes power, auxiliary power supply is not necessary. Input 1 operates in the MMF (magnetomotive force) made by controlling the current through the winding 5-6 and the core flux level, which in turn determines the trigger angle. The current for input 1 requires an external power supply or a current-generating transducer.

Add more output windings to T_2 for triggering several SCRs in parallel or in series. Also, it is possible to add more control windings of the reset or MMF type to T_2. Combining two or more half-wave circuits achieves full-wave and multiple-phase operation.

On-Off Magnetic Trigger Circuits

Magnetic trigger circuits designed for phase control applications (shown in Figure 1.40) require the use of saturable cores large enough to allow the output winding to sustain the gate voltage signal for a full half-cycle without saturating. The magnetic trigger circuits shown in Figures 1.41 and 1.42 permit the use of smaller and less expensive cores for simple on-off control since sustaining the gate voltage signal for a full half-cycle does not require output winding. In addition, these circuits have the advantage of not requiring the use of an auxiliary supply transformer.

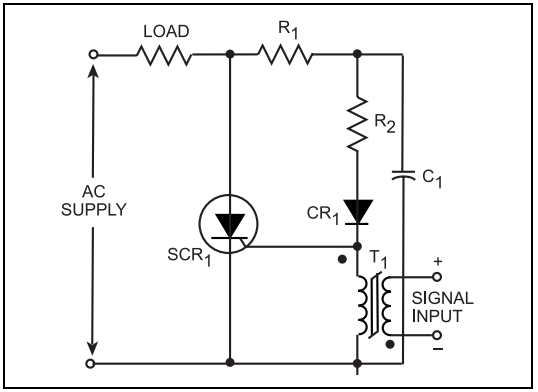


Figure 1.41 Half-wave On-Off Magnetic Trigger Circuits —Shunt Configuration

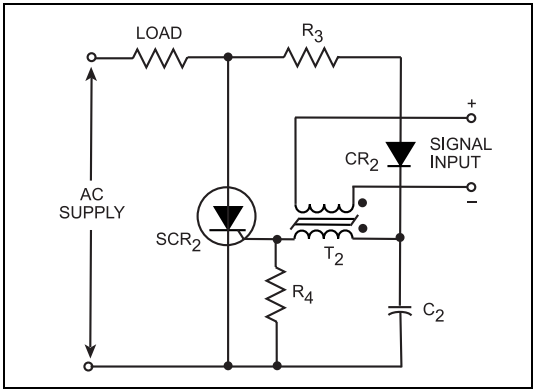


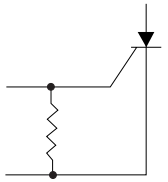
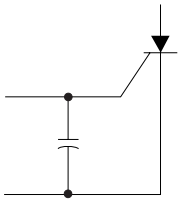
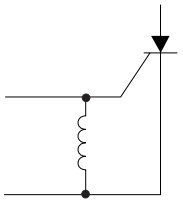
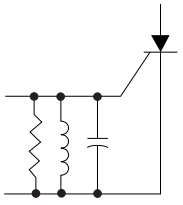
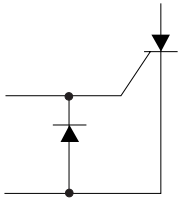
Figure 1.42 Half-wave On-Off Magnetic Trigger Circuits — Series Configuration

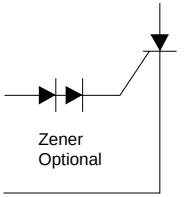
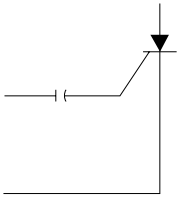
Figure 1.41 shows one winding of saturable transformer T_1 connected in shunt with the gate of SCR_1. If T_1 is unsaturated, the current through R_1, R_2 and CR_1 flows into the gate of SCR_1 during the first part of the positive half-cycle and causes SCR_1 to turn on. If T_1 is saturated, the current through R_1, R_2 and CR_1 diverts from the gate by the low saturated impedance of the winding of T_1. When T_1 is saturated, it can be reset, and the SCR can be made to trigger by a positive voltage on the signal input. Capacitor C_1 provides filtering for the gate signal to prevent undesired triggering due to fast transients on the AC supply.

Figure 1.42 shows one winding of saturable transformer T_2 connected in series with capacitor C_2 and the gate of SCR_2. If T_2 is unsaturated, the current through R_3 and CR_2 charges C_2 during the initial part of the positive half-cycle. T_2 saturates after a few degrees of the positive half-cycle and permits a rapid discharge of C_2 into the gate of SCR_2, causing SCR_2 to trigger. If T_2 is initially saturated at the beginning of the positive half-cycle, the winding of T_2 diverts the current from C_2 and prevents C_2 from being charged. Resistor R_4 prevents the voltage at the gate of SCR_2 produced by the current through R_3 from exceeding the maximum gate voltage that will not trigger the SCR. When T_2 is saturated, it can be reset and the SCR can be made to trigger by a positive voltage at the signal input.

The circuits shown in Figures 1.41 and 1.42 permit the SCR to perform the function of an AC contactor with an isolated DC control winding. Modifications of these circuits permit full-wave operation with normally open, normally closed, or latching operation.

The following table summarizes the pros and cons of using various gate terminations:

Gate Termination	Primary Purpose	Related Effects
Gate-Cathode Resistance 	(1) Increase dv/dt capability (2) Keep gate clamped to assure V_{FB} capability (3) Lowers t_{off} time	Raises the device latching and holding current
Gate-Cathode Capacitance 	(1) Increase dv/dt capability (2) Remove high frequency noise	(1) Increases delay time (2) Increases turn-on interval (3) Lowers gate signal rise time (4) Lowers di/dt capability (5) Increases t_{off} time
Gate-Cathode Inductance 	(1) Decrease DC gate sensitivity (2) Decrease t_{off} time	(1) Negative gate current increases holding current and causes gate area to drop out of conduction (2) In pulse gating the gate signal tail may cause the device to drop out of conduction
Gate-Cathode LC Resonant Circuit 	Frequency selection	Unless circuit is “damped” the positive and negative gate current may inhibit conduction or bring about sporadic anode current
Reverse Diode 	(1) Supply reverse bias in off period (2) Protect gate and gate supply for reverse transients (3) Lowers t_{off} time	Isolates the gate if high impedance signal source is used w/o sustained diode current in the negative cycle

Gate Termination	Primar;y Purpose	Related Effects
Series Zener 	Decrease threshold sensitivity	(1) Affects gate signal rise time and di/dt rating (2) Isolates the gate
Capacitive Coupling 	Isolate gate circuit DC component	In narrow gate pulses and low impedance sources the I_{gt} is followed by reverse gate signals which may inhibit conduction

Semiconductor Trigger-Pulse Generators

The simple resistor and capacitor-triggering circuits depend heavily on the specific triggering characteristic of each SCR used. In addition, the power level in the control circuit is high because the entire triggering current must flow through the resistance. Furthermore, they do not readily lend themselves to automatic, self-programmed, or feedback control systems.

On the other hand pulse triggering can accommodate wide tolerances in triggering characteristics by overdriving the gate. Since the required triggering energy (I_{GT} V_{GT} t) can be stored slowly, then discharged rapidly at the desired instant of triggering the power level in pulse control circuits may also be quite low. The use of pulse triggering enables small, low-power, signal-type components and transducers to control large, high-current thyristors.

While a multitude of semiconductors and circuits can produce adequate triggering pulses, this chapter presents only those most adept at performing this function.

Basic Relaxation Oscillation Criteria

Most devices used to produce trigger pulses (such as the unijunction transistor, diac trigger diode, the silicon unilateral and bilateral switches, programmable unijunction transistors, neon lamps, and so on) operate by discharging a capacitor into the thyristor gate. They function in a basic relaxation oscillator circuit by means of a negative resistance characteristic. Specifications for these devices usually include the voltage and current required to achieve negative resistance when approached from either the conducting or non-conducting states.

To relate these specifications to the criteria for oscillation, consider the elementary relaxation oscillator circuit shown in Figure 1.43 using a trigger device with voltage to switch V_S, current to switch I_S, holding voltage V_H, and holding current I_H. Figure 1.45 shows a graph of the device characteristic curve, along

with load lines representing R_1 and R_2. If R_1 increases to the maximum value that sustains oscillations, its load line intersects the device curve at a point (1) where the negative resistance slope of the device curve is equal to the load line for R_2. This point (1) is very close to I_S and V_S, but not quite the same since the specification of these values is at the point where the slope of the curve is vertical, representing zero dynamic resistance.

Upon reaching triggering point (1), the operating point transfers to point (2), discharging the capacitor with a peak pulse current i_p and producing a peak pulse voltage e_p across the load resistor R_2 (including the thyristor gate impedance). The discharge of the capacitor follows the device curve from point (2) to point (3), where the negative resistance slope is once again tangential with the R_2 load line. The operation then transfers from point (3) to point (4), the capacitor re-charges through R_1 and the oscillation continues.

Changing the minimum value of R_1 sustains oscillation, and its new load line intersects the device curve at point (3). Any smaller value causes the device to remain conducting at some stable operating point between (2) and (3). Increasing R_1 beyond the maximum oscillating value causes operation to cease at some point between (1) and the origin.

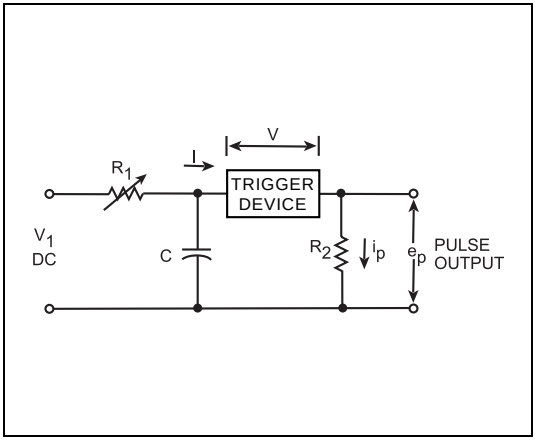


Figure 1.43 Basic Relaxation Oscillator Circuit

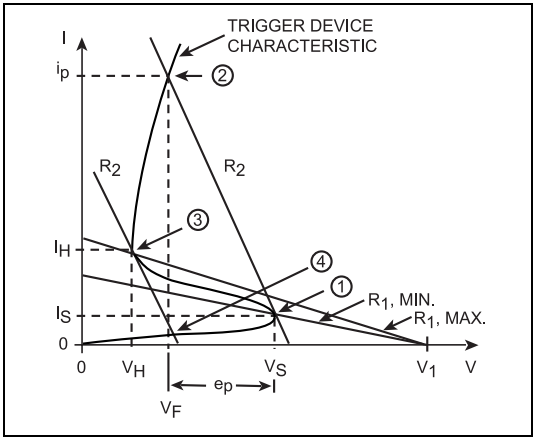


Figure 1.44 Basic Relaxation Oscillator Characteristics

A very important factor not apparent in Figures 1.43 and 1.44, and often not specified for a device, is switching time, or rise time. A device which slowly switches from point (1) to point (2) never gets to point (2) since it is discharging the capacitor as it goes and reaches the device curve somewhere between points (2) and (3). This switching time can be a limiting factor if it is a significant fraction of the discharge time-constant, R_2C.

The magnitude of pulse voltage e_p and pulse current i_p appearing at the load (resistor R_2 in this circuit) is dependent upon the characteristic curve of the device and relation between its switching time and the discharge time-constant, R_2C. The peak pulse voltage e_p is simply the difference between the switching voltage V_S and the conduction voltage drop V_F for values of R_2C large in comparison with the switching time of the device. Find the peak pulse current under this condition from the intersection of the R_2 load line, and the characteristic curve.

The effective device resistance during switching when R_2C is smaller reduces both e_p and i_p, approaching the switching time. Reducing peak current, and extending the pulse time accordingly, decreases the probability of triggering a thyristor.

Since the effect of switching time is not readily apparent from the characteristic curve, devices intended for thyristor triggering generally specify the peak pulse voltage across R_2 (where the value of R_2 is chosen to represent typical gate impedance) when discharging a given size capacitor typical for its application.

The following table shows the correlation of the parameter terminologies used in various switching devices with the points on the general characteristic curve:

Terminology on Figures 1.43 and 1.44	Unilateral Devices			Bilateral Devices				
	UJT	SUS	PUT	SBS	ST4	DIAC	Neon	STS
V_S	V_P *	V_S	V_P *	V_S	V_S	$V_{(BO)}$	V_f	V_S
I_S	I_P	I_S	I_P *	I_S	I_S	$I_{(BO)}$		I_S
V_H	V_F	V_H	V_V *	V_H			V_o	
I_H	I_V *	I_H	I_V *	I_H				I_H
e_p	V_{0B1}	V_O	e_p	V_O	V_O	e_p		V_O
i_p							i_p	

* Determined externally by circuit

Unijunction Transistor (UJT)

The UJT has three terminals:

- Emitter (E)
- Base-one (B_1)
- Base-two (B_2)

Between B_1 and B_2 the unijunction has the characteristics of an ordinary resistance. This resistance is the interbase resistance (R_{BB}) and at 25°C has values in the range from 4.7K to 9.1K.

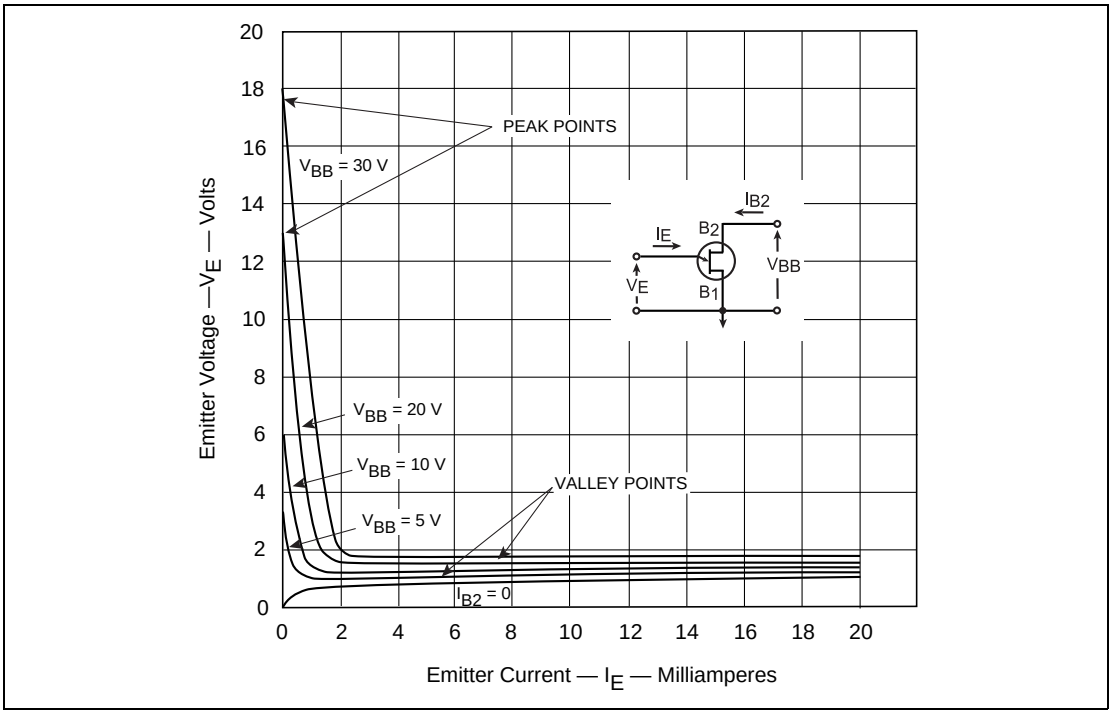


Figure 1.45 2N2646 Unijunction Transistor Symbol and Emitter Input Characteristics

Figure 1.45 shows the normal biasing conditions for a typical UJT. If the emitter voltage V_E is less than the emitter peak point voltage V_P, the emitter is reverse biased and only a small reverse leakage current I_{EO} flows. When V_E equals V_P and the emitter current I_E is greater than the peak point current I_P, the UJT turns on. The resistance between the emitter and B_1 is very low, and the series resistance of the emitter to B_1 external circuit in the on condition primarily limits the emitter current.

The peak point voltage of the UJT varies in proportion to the interbase voltage V_{BB}:

$$V_P = \eta V_{BB} + V_D \text{ where parameter } \eta = \text{the intrinsic standoff ratio}$$

The value of η lies between 0.51 and 0.82, and the voltage V_D (the equivalent emitter diode voltage) is approximately .5 volt at 25°C depending on the particular type of UJT. V_P decreases with temperature, the temperature coefficient being about -3mV/°C for the 2N2646-47 (-2mV/°C for 2N489 series). The variation of the peak point voltage with temperature may be ascribed to the change in V_D (also η for 2N2646-47 series). It is possible to compensate for this temperature change by using the positive temperature coefficient R_{BB}. When choosing resistor R_{B2} correctly, this increase in V_{BB} compensates for the decrease in V_P in the above equation if resistor R_{B2} is chosen correctly. Over a temperature range of -40°C to 100°C, the following equation gives an approximate value of R_{B2} for the majority of 2N2646 and 2N2647 UJT's:

$$R_{B2} \approx \frac{10000}{\eta V_1}$$

The following equation gives a value of R_{B2} for the 2N489 MIL series, 2N1671A and B, and the 2N2160.

$$R_{B2} \approx \frac{0.4R_{BB}}{\eta V_1} + \frac{(1-\eta)R_{B1}}{\eta}$$

See "Unijunction Temperature Compensation" (Reference 9 under Chapter 1 in the References section) for a discussion of quantitative data and techniques for temperature compensation on an individual and general basis in very high performance circuits over extreme temperature ranges.

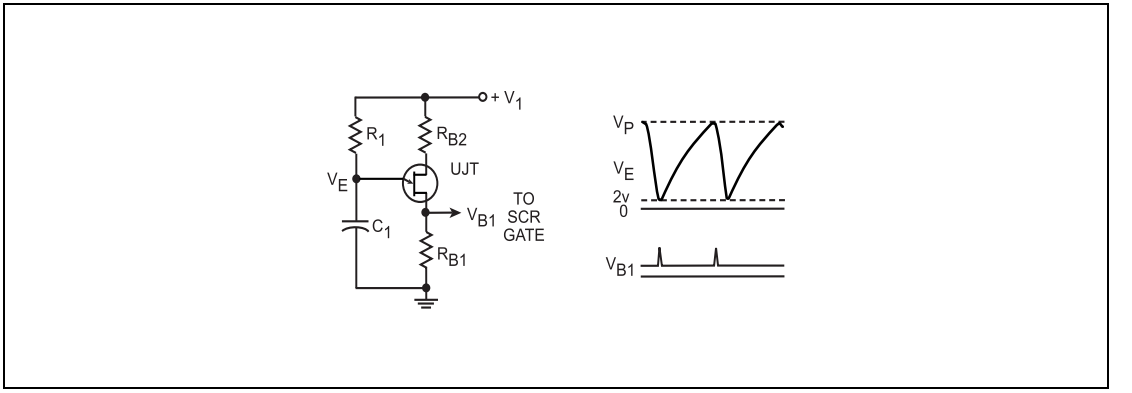


Figure 1.46 Basic Unijunction Transistor Relaxation Oscillator Trigger Circuit with Typical Waveforms

Basic UJT Pulse Trigger Circuit

The basic UJT trigger circuit used in applications with the SCR is the simple relaxation oscillator shown in Figure 1.46. In this circuit the capacitor C_1 charges through R_1 until the emitter voltage reaches V_P, at which time the UJT turns on and discharges C_1 through R_{B1}. The emitter ceases to conduct, the UJT turns off, and the cycle repeats when the emitter voltage reaches a value of approximately 2 volts. The period of oscillation, T, is relatively independent of the supply voltage and temperature:

$$T = \frac{1}{f} \approx R_1 C_1 \log n \frac{1}{1-\eta} = 2.3 R_1 C_1 \log 10 \frac{1}{1-\eta}$$

For an approximate nominal value of intrinsic standoff ratio $\eta = 0.63$, $T = R_1C_1$.

The design conditions of the UJT triggering circuit are very broad. In general, R_{B1} is limited to a value below 100 ohms although values up to 2K or 3K are possible in some applications. The resistor R_1 is limited to a value between 3K and 3 Meg. The lower limit on R_1 is set by the requirement that the load line formed by R_1 and V_1 intersect the emitter characteristic curve of Figure 1.45 to the loft of the valley point; otherwise, the UJT in Figure 1.46 does not turn off. The upper limit on R_1 is set by the requirement that the current flowing into the emitter at the peak point must be greater than I_P for the UJT to turn on. The recommended range of supply voltage V_1 is 10 volts to 35 volts. The allowable power dissipation of the UJT determines this range on the low end.

When the pulse output (V_{B1}) of the circuit shown in Figure 1.46 is coupled directly to the gate of SCRs, the value of R_{B1} should be low enough to prevent the DC SCR gate voltage (due to interbase current)

from exceeding the SCR non-trigger V_{GT} at temperature (as shown in Figure 1.21). To meet this criterion, choose R_{B1} based on the following inequality:

$$\frac{R_{B1}V_1}{R_{BB}(min) + R_{B1}R_{B2}} < V_{GT}\ (min\ at\ temperature)$$

For the 2N681 types at a maximum junction temperature of 125°C, V_{GT} (max) is 0.25 volt. For a supply voltage of 35 volts or less, $R_{B1} \leq 50$ ohms. These limitations do not apply if the pulse output from the UJT triggering circuit is coupled to the gates of the SCRs by means of transformers or capacitors.

Designing the UJT Trigger Circuit

The 2N2646 and 2N2647 UJTs are specifically characterized for SCR trigger circuits and are factory tested to ensure reliable operation with all types of SCRs over their respective temperature ranges.

Achieve the design of a suitable UJT trigger circuit rapidly and easily by using the design curves given in Figures 1.47 and 1.48 for the 2N2646 and 2N2647, respectively. These curves give the minimum supply voltage V_1 required to guarantee triggering of various types of SCRs over the indicated temperature range as a function of the UJT emitter capacitor C_1 and the B_1 coupling resistor R_{B1} or B_1 coupling transformer. The value of resistor R_1 is not important for the purposes of the design provided that it is within the limits required for the UJT to oscillate. If R_{B2} is significantly greater than 100 ohms, the minimum supply voltage V_1 shown in Figures 1.47 and 1.48 uses the following equation:

$$V_1' \approx \frac{(2200 + R_{B2})V_1}{2300}$$

In all cases use a resistance of 100 ohms or greater in series with either B_2 or in series with the power supply to protect the UJT from possible thermal runaway. This is particularly important when operating at high ambient temperatures, at high supply voltages, or with large values of emitter capacitance.

Consider the following example using Figures 1.47 and 1.48 in the practical design of an SCR trigger circuit:

Problem:
A circuit is required to trigger a 2N1773 series SCR at the lowest possible supply voltage with a 2N2646 UJT and pulse transformer coupling. The value of capacitance, chosen on the basis of operating frequency, is 0.1 μf, and temperature compensation is desired. Assume η = 0/66 for a nominal value.

Solution:
Based on the chart in Figure 1.47, consider Curve I with the supply voltage V_1 not exceeding V_1 (max) = 35V. On Curve I the minimum supply voltage for a value of C_1 = 0.1 μf is about V_1 = 12 volts. Determine the value for R_{B2} as follows (nearest standard value):

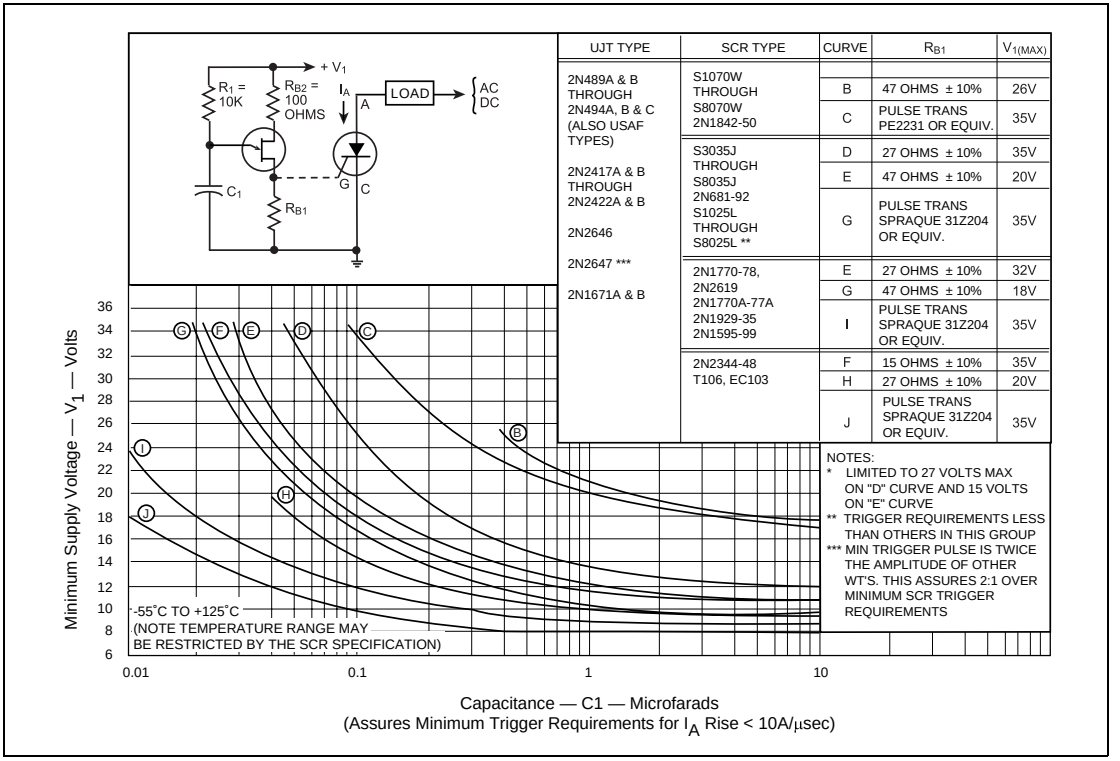
$$R_{B2} \approx \frac{10000}{(0.66)(12)} = 1260 \approx 1000\ ohms$$

This value of R_{B2} requires an increase in the supply voltage to a value V_1 in accordance with the following equation:

$$V_1 = \frac{2300}{(2200 + 1000)}(12) \approx 17 volts$$

A suitable design for this problem is C_1 = 0.1 µf, R_{B2} = 1K ohms, and V_1 = 17 volts.

If R_{B2} causes V_1 (from the above equation) to be larger than can be attained practically or economically, use the 2N489 series, the 2N1671A, or the 2N1671B. (The previous equation yields a lower value of R_{B2}.) Alternatively, if extreme temperature compensation is not necessary, or if the temperature range to which the 2N2646/47 UJTs are subjected is not great, use a value of RB2 ≥ 100 ohms.



UJT TYPE	SCR TYPE	CURVE	R_{B1}	$V_{1(MAX)}$
2N489A & B THROUGH 2N494A, B & C (ALSO USAF TYPES)	S1070W THROUGH S8070W 2N1842-50	B	47 OHMS ± 10%	26V
		C	PULSE TRANS PE2231 OR EQUIV.	35V
2N2417A & B THROUGH 2N2422A & B	S3035J THROUGH S8035J 2N681-92 S1025L THROUGH S8025L **	D	27 OHMS ± 10%	35V
		E	47 OHMS ± 10%	20V
		G	PULSE TRANS SPRAQUE 31Z204 OR EQUIV.	35V
2N2646	2N1770-78, 2N2619 2N1770A-77A 2N1929-35 2N1595-99	E	27 OHMS ± 10%	32V
2N2647 ***		G	47 OHMS ± 10%	18V
2N1671A & B		I	PULSE TRANS SPRAQUE 31Z204 OR EQUIV.	35V
	2N2344-48 T106, EC103	F	15 OHMS ± 10%	35V
		H	27 OHMS ± 10%	20V
		J	PULSE TRANS SPRAQUE 31Z204 OR EQUIV.	35V

NOTES:
* LIMITED TO 27 VOLTS MAX ON "D" CURVE AND 15 VOLTS ON "E" CURVE
** TRIGGER REQUIREMENTS LESS THAN OTHERS IN THIS GROUP
*** MIN TRIGGER PULSE IS TWICE THE AMPLITUDE OF OTHER WT'S. THIS ASSURES 2:1 OVER MINIMUM SCR TRIGGER REQUIREMENTS

Figure 1.47 UJT Circuit Design Curves (-55° to 125°C)

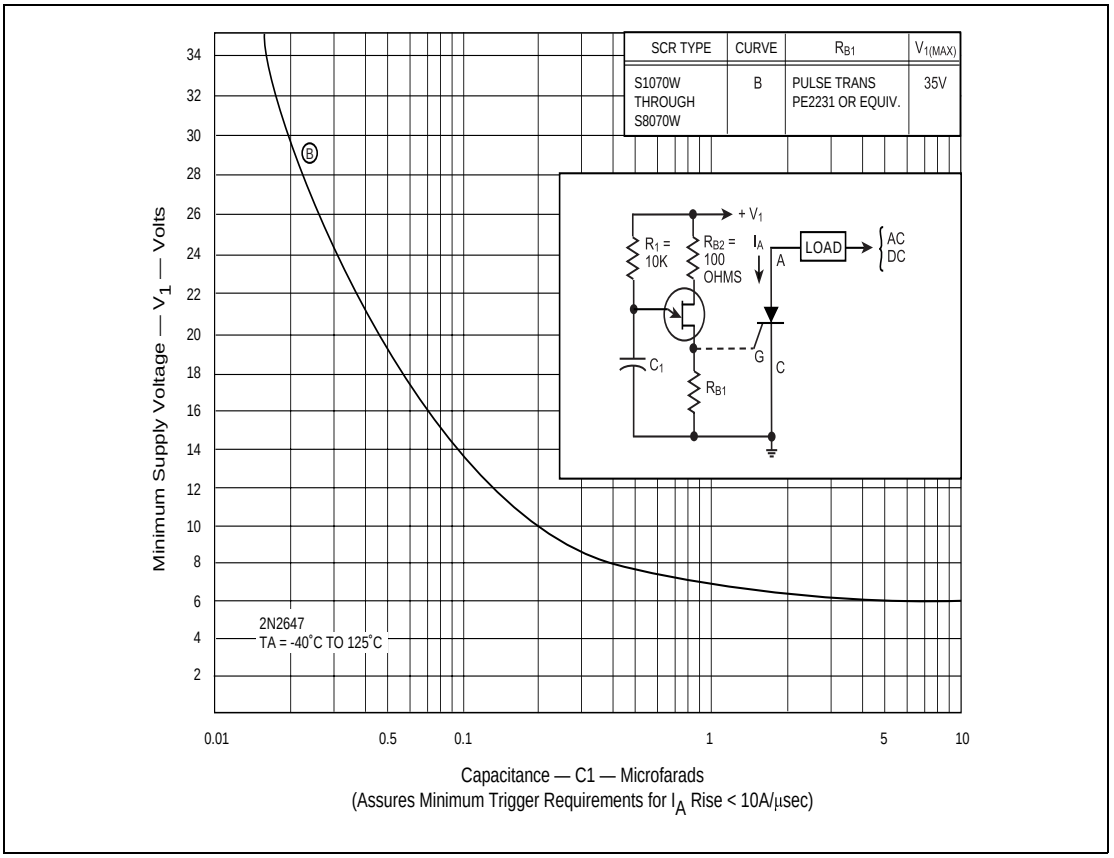


Figure 1.48 UJT Circuit Design Curves (-40° to 125°C)

Do not use a UJT to trigger SCRs that handle more than 70 Amps. Use a PUT trigger circuit (shown in Figures 1.49 and 1.50), or a pulse amplifier must boost the UJT output into the gate.

Programmable Unijunction Transistor (PUT)

The PUT trigger device is a small thyristor with an anode gate as shown in Figure 1.49. The device remains in its off state until the anode voltage exceeds the gate voltage by one diode forward voltage drop if the gate is maintained at a constant potential. At this voltage the peak point is achieved and the drive turns on. In the relaxation oscillator also shown in Figure 1.50, the supply voltage by the resistor divider, R_1 and R_2 maintains the gate voltage of the PUT. This voltage determines the peak point voltage, V_P. The peak point current I_P and the valley point current I_V both depend upon the equivalent impedance on the gate, $R_1 R_2/(R_1 + R_2)$, and the source voltage, E_S. R_T and C_T control the frequency along with R_1 and R_2 since the period of oscillation is approximately as follows:

$$t \approx R_T C_T \log n \left(\frac{E_S}{E_S - V_P}\right) \qquad t \approx R_T C_T \log n \left(1 + \frac{R_2}{R_1}\right)$$

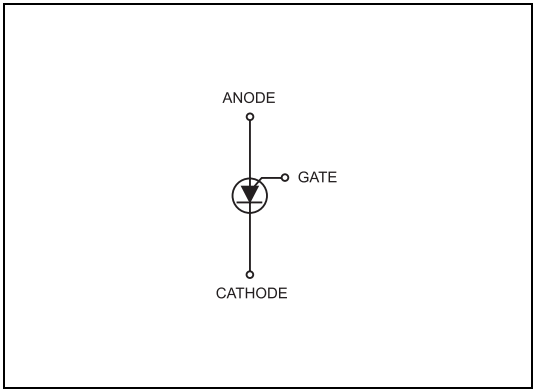


Figure 1.49 PUT Relaxation Oscillator —Device Termination

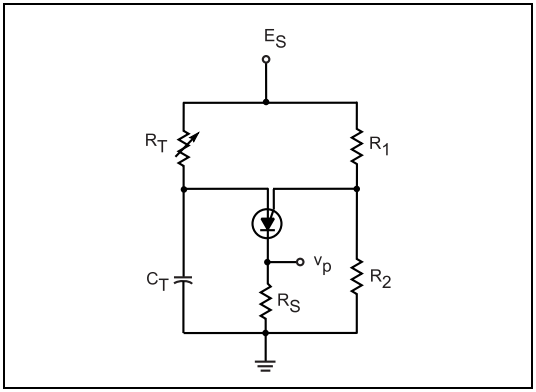


Figure 1.50 PUT Relaxation Oscillator — Typical Current

The primary difference between the two PUTs (2N6027 and 2N6028) is in the peak point current. The 2N6028 is characterized specifically for long interval timers and other applications requiring low leakage and low peak point current. The 2N6027 are characterized for general use where the low peak point current of the 2N6028 is not essential. Applications of the 2N6027 include timers, high gain phase control circuits, and relaxation oscillator. The other important asset of the PUTs, which makes them particularly suitable for triggering high current SCRs, is its high peak pulse current output. Due to the PNPN nature of this device (as opposed to conductivity modulation), the forward conductance is high and the rise time is fast. The dynamic resistance of the PUT in the saturation region is approximately 3 ohms. Rate of rise V_o is typically 10nS (with a maximum of 80 nS specified). Healthy ouput pulses are available from capacitors as low as .01 μfd. For more details on device operation and trigger circuit design using this particular device, see References 14 and 15 under Chapter 1 in the References section.

Designing the PUT Relaxation Oscillator and Timer Circuits

A systematic approach to the design of a PUT oscillator circuit appears complex precisely because it is such a versatile device. A further complication arises because so much performance variation can be programmed into the circuit by the voltage divider R_1 and R_2.

Consider the following key guide posts:

- Consider peak point control I_P - I_P only in the case of a very long interval timer. Both R_T and C_T are large, the latter having low equivalent parallel resistance.
- Valley Current, I_V is a key parameter in free-running relaxation oscillators operating from a DC supply. Most trigger circuits derive their supply voltage from the “off-state” SCR. When the PUT triggers this SCR, its supply voltage collapses and it commutates off.
- Offset Voltage, V_T determines the minimum value of R_1 and so V_T only plays a role in long interval timers.

Design Problem:
Design a free-running relaxation oscillator capable of triggering an S2012 SCR flasher from a 12V supply. The operating frequency must be adjustable from 5 to 50 pulses per minute.

Solution:
Refer to Figure 1.49 for the basic circuit. No problem is anticipated with I_P since the frequencies are relatively high, but I_V may be troublesome.

The selection of C_T is crucial since too small a value will not fire the SCR and too large a value leads straight to I_V problems.

Determine the value of V_P and C_T to trigger the S2012 from Figure 1.27.

Plot on the same graph the time integral of current pulse to be used and the time integral of the trigger current pulses required by Figure 1.51. These curves represent the charge to be delivered to the gate and the charge required to trigger as a function of time. If at any time the delivered charge exceeds the required charge, the device turns on. Figure 1.51 illustrates this technique for the S2012 SCR and a decaying exponent current pulse with a peak of 80 mA and an R-C constant of 8 μsec. The device turns on since the two curves intersect at 3.6 μsec after the start of the pulse. Either the peak current or the capacitor value could increase if no intersection occurs.

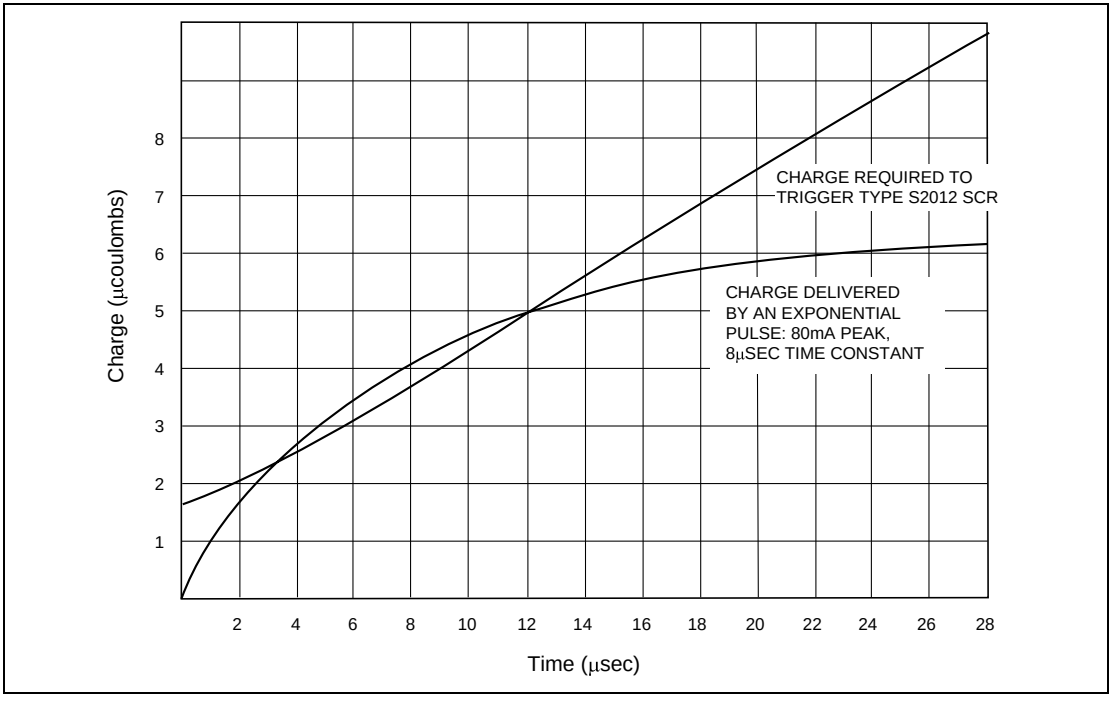


Figure 1.51 Charge to Trigger an Exponential Pulse

The above technique provides a useful indication of SCR pulse triggering requirements. However, since the characteristic contains sizeable variations, it is important to incorporate a reasonable safety factor in the trigger circuit design.

Let R_S = 39 ohms. Then since $R_S C_T$ = 8 µsec, $C_T \approx 0.2$ µf. The peak triggering current of 80 mA determines V_P, as follows:

$$V_P = I_P \bullet R_S + 1V$$
$$= (80mA)(39\Omega) + 1V = 4.1$$

where 1V is the approximate PUT on-state voltage

The computed value of η is as follows:

$$\eta = \frac{V_P}{E_S} = \frac{4.1}{12} \approx 1/3$$

Use the following equations to find the timing pot R_T.

$$R_{T(MAX)} = \frac{1}{C_T(\log n)\left(\frac{1}{12-4.1}\right) f_{min}} = 2.5\ Meg$$

$$R_{T(min)} = \frac{1}{C_T(\log n)\left(\frac{12}{12-4.1}\right) f_{max}} = 250K$$

The maximum anode current occurs at the maximum frequency when R is a minimum:

$$I_{V(max)} \approx \frac{E_S}{R_{T(min)}} \approx \frac{12}{250} ma \approx 48\mu a$$

I_V (min) of the 2N6027 is 70µa for I_G = IMA which allows adequate safety margins. Therefore, to find R_1 and R_2, solve the following equations:

$$\text{for } \eta = 1/3, I_G = 2/3\frac{E_S}{R_G}; \therefore R_G = 8K\ ohms$$

$$\frac{R_2}{R_1 + R_2} = \frac{V_P}{E_S} = \eta$$

The solutions for R_1 and R_2 are:

$$R_1 = \frac{R_G}{\eta} \qquad R_2 = \frac{R_G}{1-\eta}$$

Since η - 1/3, then R_1 = 24K and R_2 = 12K ohms

If needing other frequency ranges, either switch in difference capacitors for C_T or vary R_2 to achieve the same result.

Figures 1.52 and 1.53 show the effect of the voltage divider ratio $R_2 / (R_1 + R_2)$ on the period of oscillation.

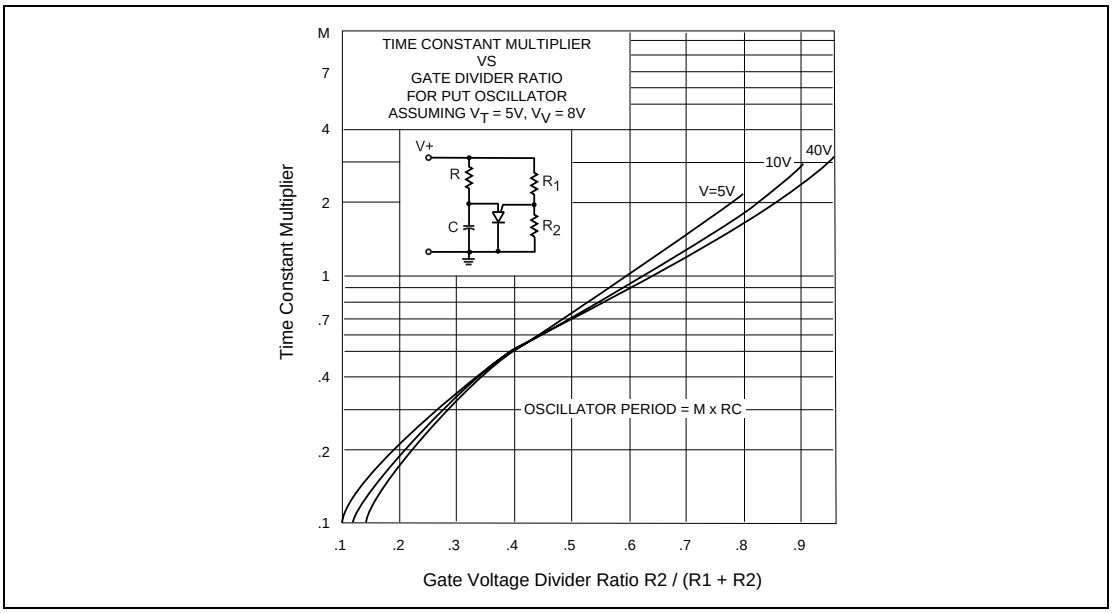


Figure 1.52 Effect of $R_2 / (R_1 + R_2)$ on Oscillator Frequency—PUT Oscillator

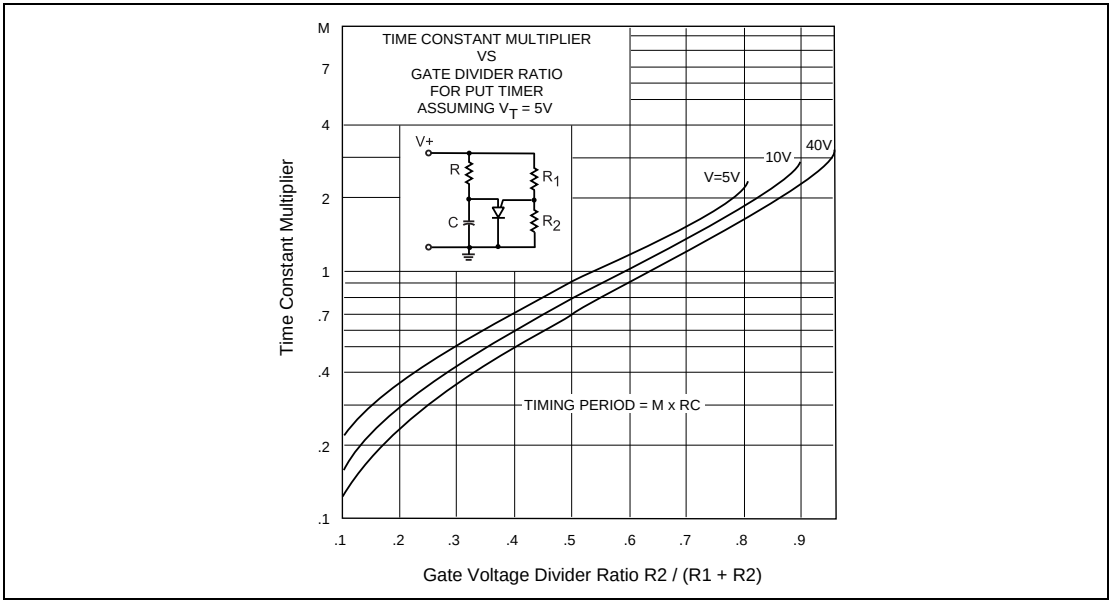


Figure 1.53 Effect of $R_2 / (R_1 + R_2)$ on Oscillator Frequency—PUT Timer

Silicon Unilateral Switch (SUS)

The SUS, such as 2N4987, is essentially a miniature SCR having an anode gate (instead of the usual cathode gate) and a built-in low-voltage avalanche diode between the gate and cathode. Figure 1.54 shows the symbol for the SUS and its equivalent circuit. Figure 1.55 shows its anode-to-cathode electrical characteristic for no external connection to the gate terminal.

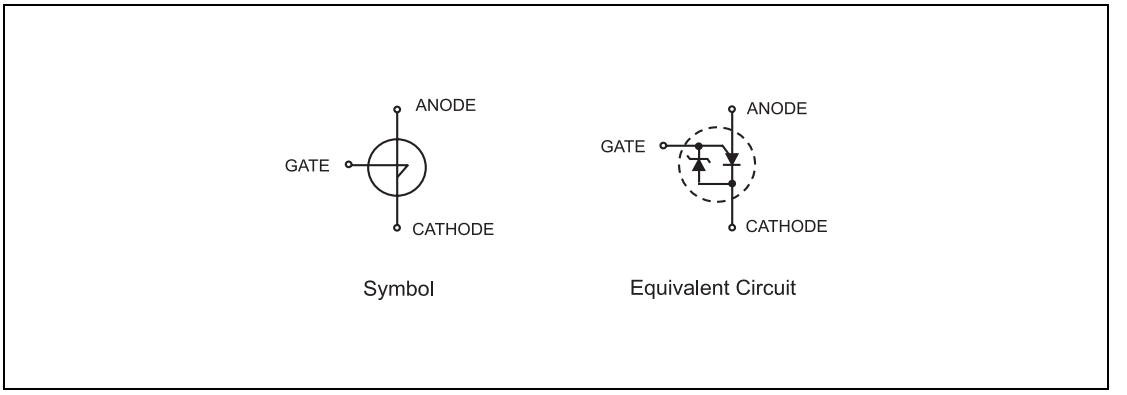


Figure 1.54 Silicon Unilateral Switch (SUS)

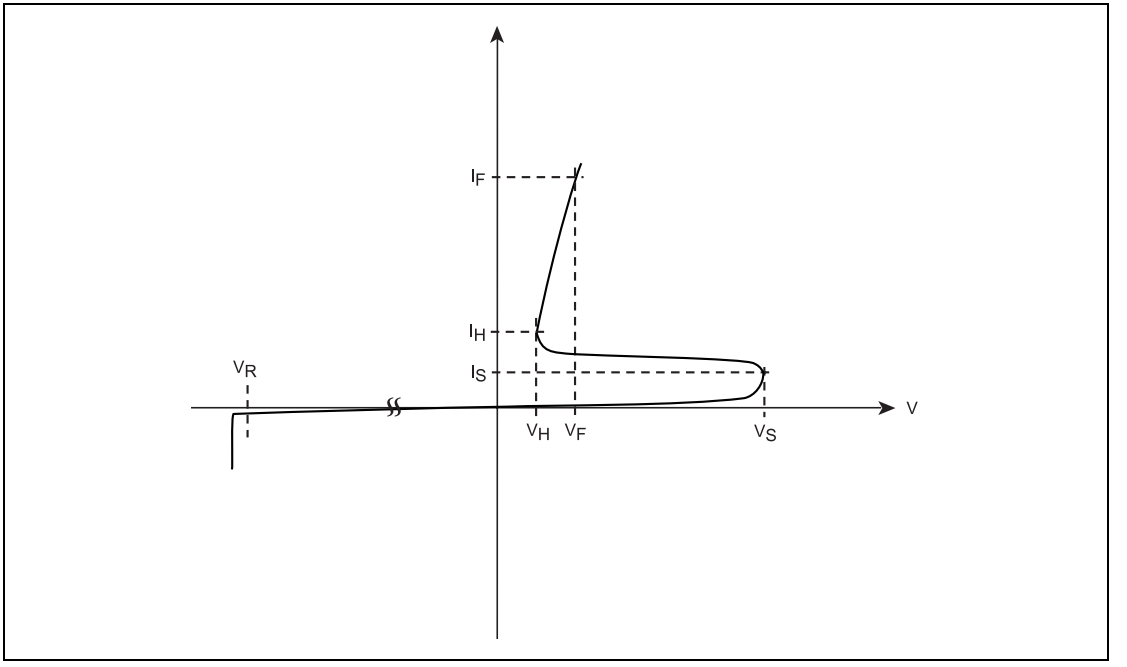


Figure 1.55 SUS Characteristic Curve

Use the SUS usually in the basic relaxation oscillator circuit shown in Figure 1.43. Its characteristics follow the same criteria for oscillation. The following table shows 2N4987 specifications:

2N4987 Specifications	
Switching Voltage V_S	6 to 10 volts
Switching Current I_S	0.5 ma, maximum
Holding Current V_H	Not specified (≈ 0.7 V at 25°C)
Holding Current I_H	1.5 ma, maximum
Forward Voltage V_F (at I_F = 175 ma)	1.5 volts
Reverse Voltage Rating V_R	30 volts
Peak Pulse Voltage V_O	3.5 volts minimum

The peak pulse voltage V_O specification is very important for thyristor triggering applications since it is the only realistic figure-of-merit that indicates the ability of the triggering device to transfer charge from the capacitor to the thyristor gate. Measure this voltage with the SUS operating in the circuit of Figure 1.43, where V_1 = 15 volts, R_1 = 10 K ohms, C = 0.1 µf, and R_2 = 20 ohms. Measure the peak pulse voltage across resistor R_2. The magnitude of the pulse voltage depends both upon the difference between V_S and V_F and upon switching time. The component values used in the pulse test are adequate for triggering most thyristors.

The major difference in function between the SUS and the UJT is that the SUS switches at a fixed voltage, determined by its internal avalanche diode, rather than a fraction (n) of another voltage. Also note that I_S is much higher in the SUS than in the UJT and is also very close to I_H. These factors restrict the upper and lower limits of frequency or time-delay which are practical with the SUS.

For synchronization, lock-out, or forced switching, apply bias or pulse signals to the gate terminal of the SUS. For these purposes, treat the SUS as an N-gate SCR.

(For more information, see Reference 12 under Chapter 1 in the References section.)

Silicon Bilateral Switch (SBS)

The SBS, such as the 2N4991, is essentially two identical SUS structures arranged in inverse-parallel, as shown in Figures 1.56 and 1.57. It is particularly useful for triggering the bidirectional triode thyristors (triacs) with alternate positive and negative gate pulses since it operates as a switch with both polarities of applied voltage. Obtain this operation by using an alternating voltage supply for V_1 in Figures 1.43 and 1.44, rather than the DC supply shown.

Specifications for the SBS 2N4991 are identical to those of the SUS 2N4987 with the exception of reverse voltage ratings, which is not applicable to the SBS.

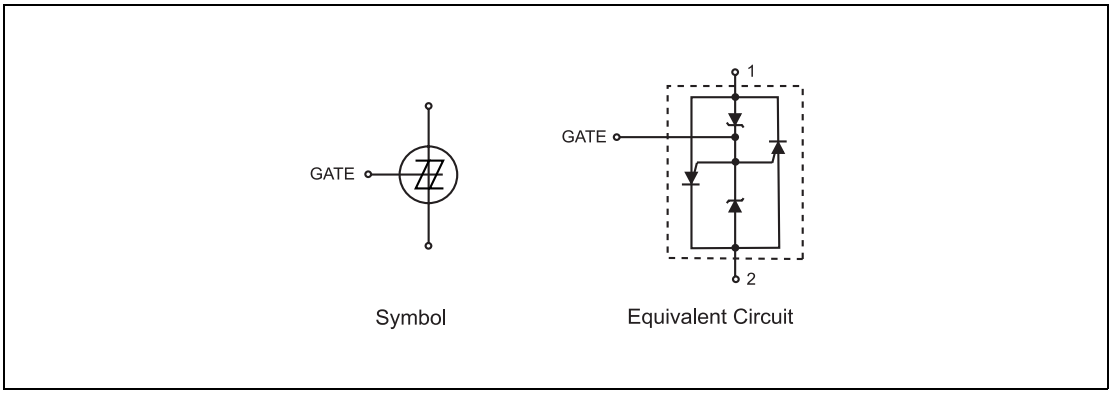


Figure 1.56 Silicon Bilateral Switch (SUS)

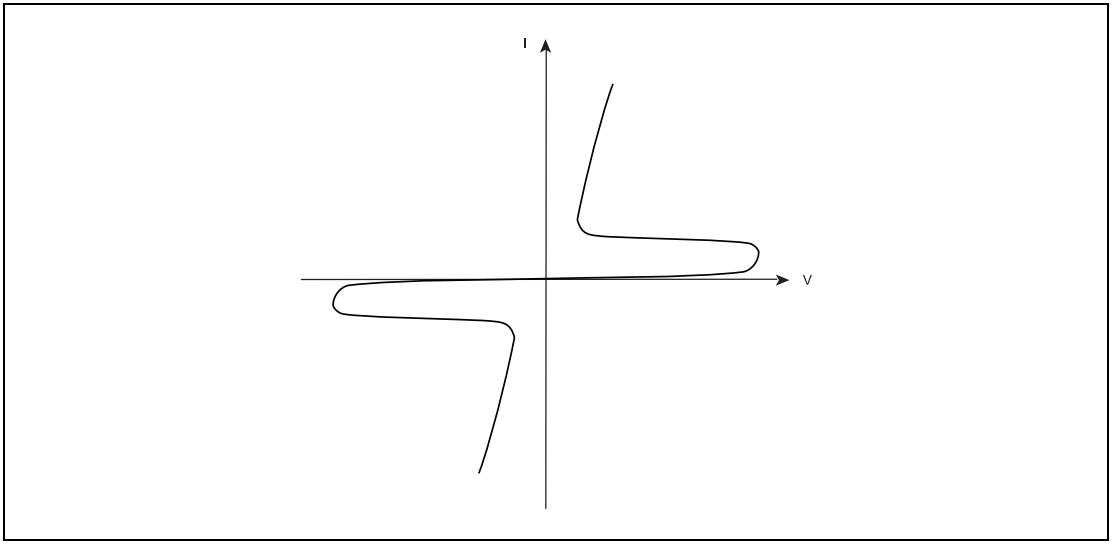


Figure 1.57 SBS Characteristic Curve

Bilateral Silicon Trigger Switch (STS)

The newer "HS" series of bilateral Silicon Trigger Switch (STS) offers low breakover voltages in an economical DO-35 package and glass-passivated junctions for reliability. (See Figure 1.58.)

The (STS) devices switch from the blocking mode to full conduction when the applied voltage, of either polarity, exceeds the Breakover Voltage (V_{BO}). (See Figure 1.59.) Combined with a small capacitor, the STS will provide the necessary firing current for SCR or triac devices with its full breakback characteristic. The "HS" series is not only bilateral but is also very symmetrical and ideal for either full-wave or bidirectional thyristor controls. For applications requiring very low triggering voltages, the HS-10, STS with a triggering voltage (V_{BO}) of 8-10 volts, allows for phase-controlling even a 24VAC line.

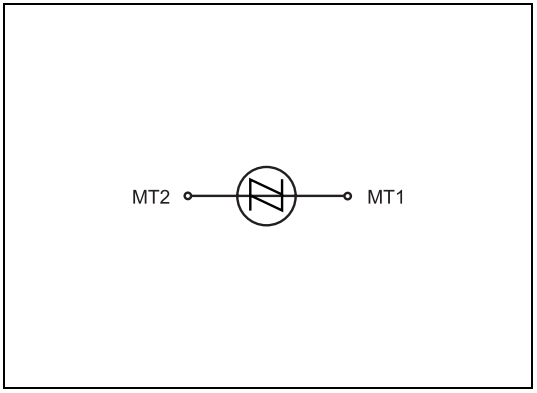


Figure 1.58 Symbol of Bilateral Trigger Switch

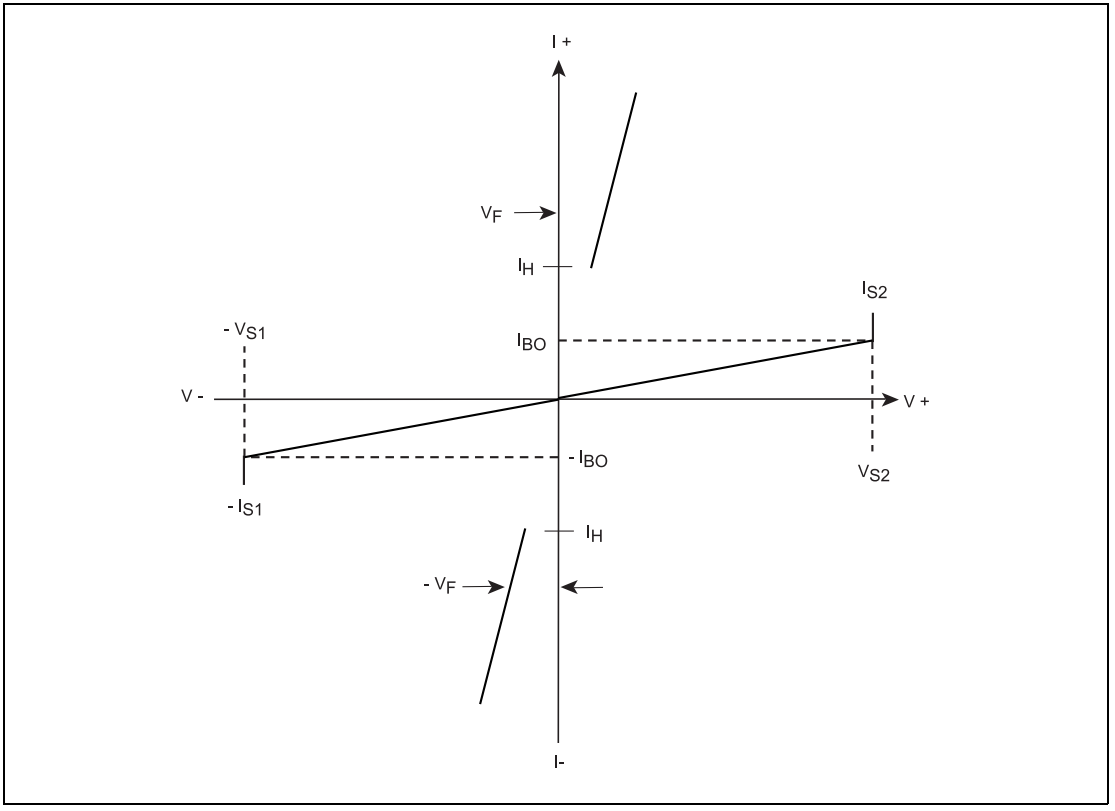


Figure 1.59 STS Characteristic Curve

Bilateral Trigger Diode (DIAC)

The diac, such as the HT series, is essentially a transistor structure which exhibits a negative resistance characteristic above a given switching current I_{BO}. (See Figure 1.60.) The characteristic curve of Figure 1.61 shows that this negative resistance region extends over the full operating range of currents above $I_{(BO)}$ and so the concept of a holding current I_H does not apply.

Use the diac in the simple relaxation oscillator circuit as shown in Figures 1.43 and 1.44. The criteria for oscillation are the same. The supply voltage for the oscillator circuit V_1 for alternating pulse output may be an alternating voltage.

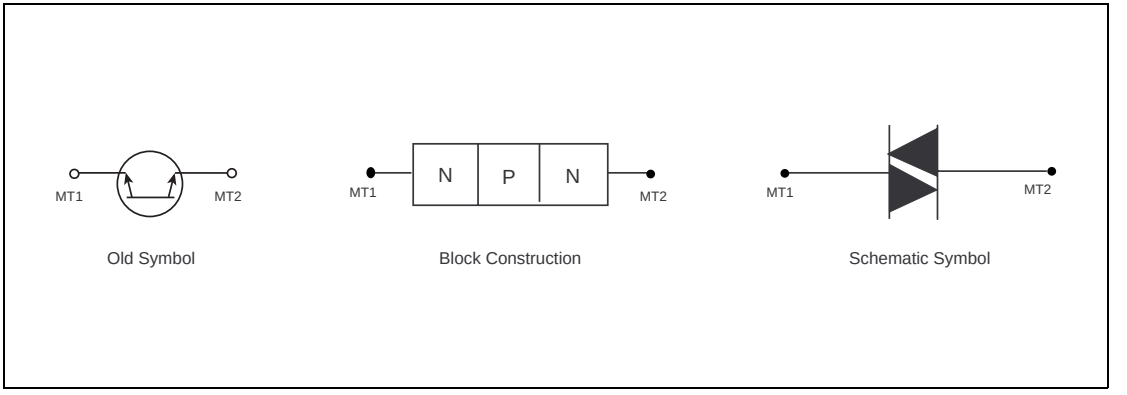


Figure 1.60 Symbol of Bilateral Trigger Diode (Diac)

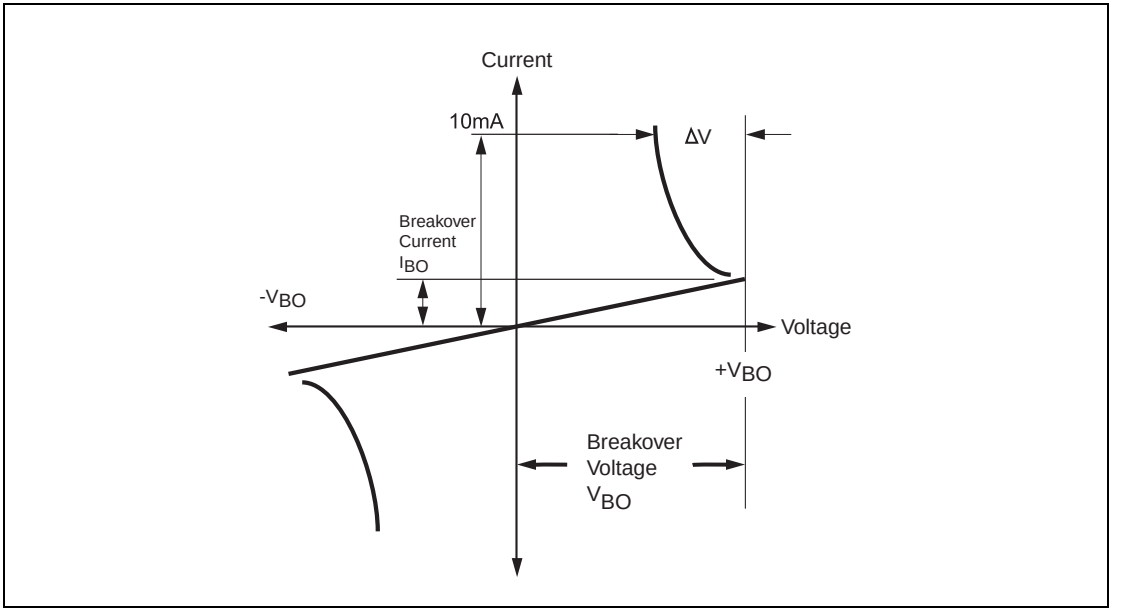


Figure 1.61 Diac Characteristic Curve

The following table shows HT32 diac specifications:

HT32 Specifications	
V_{BO}	27 to 37 volts
I_{BO}	25 μamp (maximum)
V_{BB}	10 volts (minimum) @ 10 ma

The peak pulse voltage V_{BB} is measured under the same conditions used with the SUS and SBS—R_2 = 20 ohms; C = 0.1 microfarad. This minimum value V_{BB} is established to ensure proper conditions of supply voltage and load impedance in the power circuit of the triac since the HT 32 is used primarily to trigger triacs.

Asymmetrical AC Trigger Switch (ST4)

The ST4 is an integrated triac trigger circuit that provides wide-range, hysteresis-free phase control of voltage. This performance is possible with a minimum number of circuit components and at low cost.

The equivalent circuit and characteristic curve in Figures 1.62 and 1.63 show that the ST4 behaves like a zener diode in series with an SBS. The zener diode provides the asymmetry since now switching voltage V_{S1} is increased by the avalanche voltage of the zener.

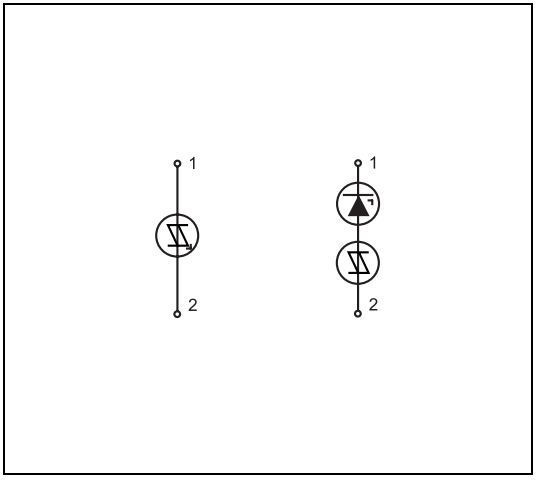


Figure 1.62 Symbol of Asymmetrical AC Trigger Switch (ST4) and Equivalent Circuit

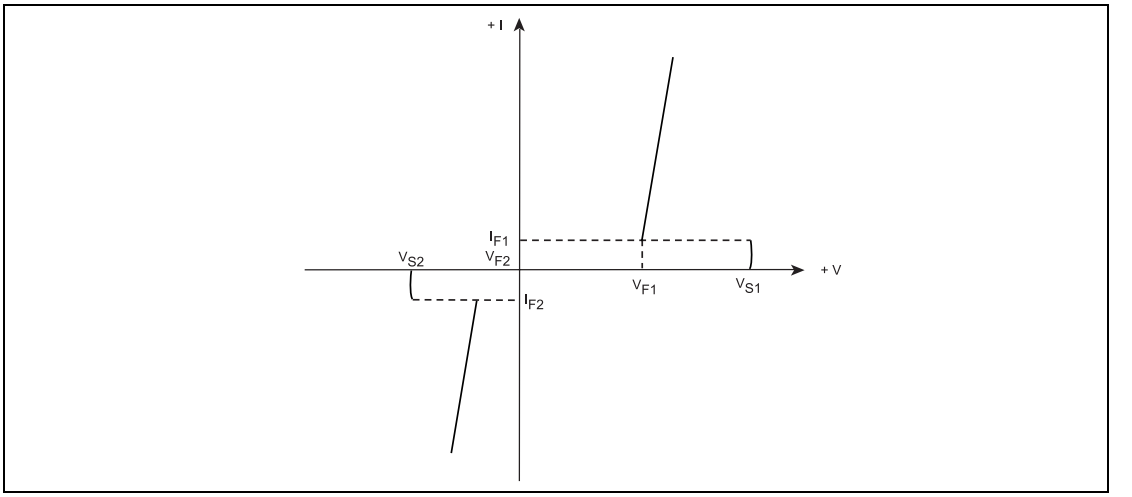


Figure 1.63 ST4 Characteristic Curve

The following table shows ST4 specifications:

ST4 Specifications	
Switching Voltage	V_{S1} — 14 to 18 volts
	V_{S2} — 7 to 9 volts
Switching Current	I_{S1}, I_{S2} — 80 µa (25°C)
	I_{S1}, I_{S2} — 160 µa (-55°C)
On-State Voltages	V_{F1} — 7 to 10 volts
	V_{F2} — 1.6 volts (max)
Peak Pulse Voltage	V_O —3.5 volts minimum

Other Trigger Devices

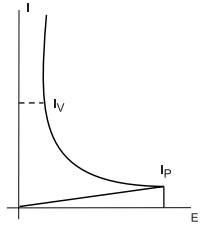
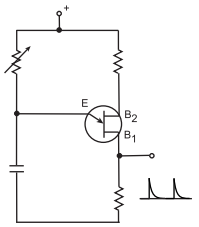
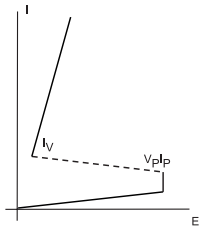
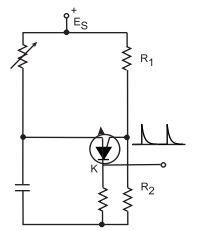
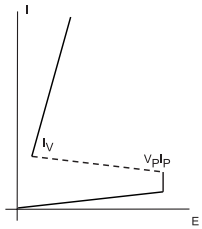
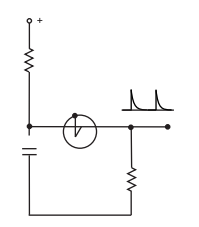
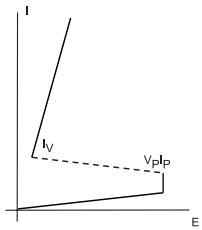
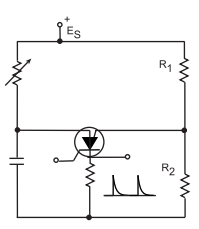
Several other unilateral and bilateral switching devices exist with characteristics similar to those presented previously in this chapter. In general, all operate as relaxation oscillators and are subject to the same criteria for oscillation. The maximum switching time must be known if the peak pulse voltage (or current) output is not specified. Otherwise, the trigger circuit must be over-designed by a factor depending upon the uncertainty of the unknowns.

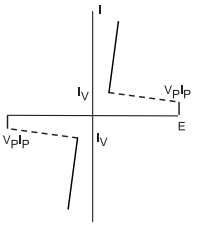
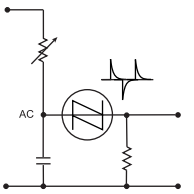
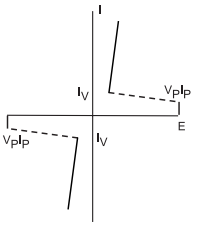
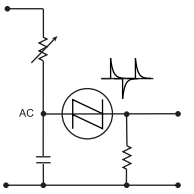
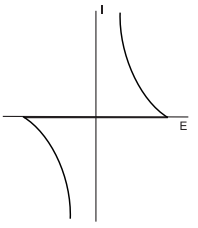
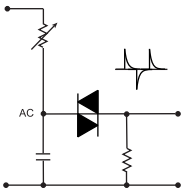
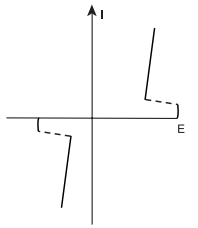
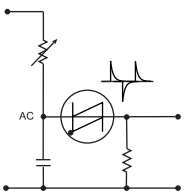
Specialized integrated circuits could be and have been designed to meet the need where a large demand exists for the same type triggering source. Various monolithic integrated triggering circuits are available that feature “zero-voltage” switching to minimize RFI. Similarly, linear ICs are available for phase control circuits.

Another method of triggering employs light-sensitive or light-activated devices. This method offers speed along with incomparable electrical isolation.

Summary of Semiconductor Trigger Devices

The following table summarizes the electrical characteristics of the widely-used triggering devices:

	Class		Major Types		V_P Peak Point Voltage	I_P (max) Peak Point Current	I_V (min) Valley Current	T_{on} Turn On Time
	E-I Characteristics	Basic Circuit						
Unidirectional	UJT—Unijunction Transistor							
			**TO-5:** 2N489A 2N489B 2N1671A 2N1671B 2N1671C	**TO-18:** 2N2417A 2N2417B 5G515 5G516 2N2646 2N2647	Fixed Fraction of Interbase Voltage	12 µa 6 µa 25 µa 6 µa 2 µa 5 µa 2 µa	8 ma 8 ma 8 ma 8 ma 8 ma 4 ma 8 ma	1.2 µsec Typ
	PUT—Programmable Unijunction Transistor							
			2N6027 2N6028		$\frac{R_2 E_S}{R_1 + R_2}$	As low as 2 µa As low as .15 µa (Function of R_1 and R_2)	70 µa 25 µa (Function of R_1 and R_2)	80 µsec Max
	SUS—Silicon Unilateral Switch							
			**TO-18:** 2N4983 2N4984 2N4985 2N4986	**TO-98:** 2N4987 2N4988 2N4989 2N4990	6-10 V 7.5-9 V 7.5-8.2 V 7.9 V	500 µa 150 µa 300 µa 200 µa	1.5 ma .5 ma 1.0 ma .75 ma	1.0 µsec Max
	SCS—Silicon Control Switch							
			3N84		$\frac{R_2 E_S}{R_1 + R_2}$ (40 V max)	Function of R_1 and R_2	10 ma Max (Function of R_1 and R_2)	1.5 µsec Max

	Class		Major Types		V_P Peak Point Voltage	I_P (max) Peak Point Current	I_V (min) Valley Current	T_{on} Turn On Time
	E-I Characteristics	Basic Circuit						
Bidirectional	SBS—Silicon Bilateral Switch							
			**TO-18:** 2N4993	**TO-98:** 2N4991 2N4992	6-10 V 7.5-9 V	500 µa 120 µa	1.5 ma .5 ma	1.0 µsec Max
	STS—Silicon Trigger Switch							
			**DO-35:** HS10 HS20		8-12 V 18-24 V	100 µa 100 µa	.5 ma .5 ma	1.0 µsec
	DIAC							
			**DO-35:** HT series		27-70 V	500 µa	Very high	1 µsec Typ
	ATS—Assymetrical AC Trigger Switch (ST4)							
			ST4		14-18 V 7-9 V	80 µa 80 µa		1 µsec

Neon Glow Lamps as Trigger Devices

Many consider using the low-priced neon glow lamps for triggering thyristors. The characteristics of the glow lamp are quite similar to those of the diac except for magnitude. The switching voltage is generally on the order of 90 volts and the switching current is extremely small (below 1μa). However, the switching time is large in comparison with semiconductor devices, and the peak pulse voltage is usually not specified.

The 5AH is an isotope-stabilized neon glow lamp now being used in many low-cost SCR control circuits. The 5AH lamp has the following specifications:

5AH Lamp Specifications	
V_S	60 to 100 volts
I_S	Not specified
V_F	Approximately 60 volts at 5 ma
V_H	Not specified
I_H	Not specified
I_P	25 ma (minimum)

Measure the peak pulse current i_p in a 20-ohm resistor when discharging a 0.1 μf capacitor. Therefore, the minimum peak pulse voltage is 0.5 volts under this condition. The specification also includes an indication of the operating life of the lamp: 5000 hours operation, on the average, at 5 mA DC results in a 5-volt change in V_S or V_F. This is not correlated to hours operation in a relaxation oscillator at 120 Hz.

Glow lamps are useful for thyristor triggering under the following conditions:

- Thyristor I_{GT} is 10 mA or less.
- Wide tolerance in V_S is acceptable.
- Minimum pulse voltage, measured in sample lot, must be several times minimum required to trigger the thyristor.
- Change in V_S and pulse output with operating time is acceptable.
- Cost is of primary importance.
- Five percent loss in RMS voltage at full power is tolerable.

Neon Lamp Trigger Circuits

Neon lamp SCR phase-controlled trigger circuits have the promise of combining the low cost of the RC diode circuit with improved performance. In addition, the possibility exists in such a relatively simple yet high impedance circuit to exercise control over the charging rate of the trigger capacitor with suitable devices responsive to light, heat, pressure, and so on.

Figure 1.64 shows a half-wave AC phase-controlled circuit using a 5AH as the trigger for a two-terminal system. The 5AH triggers when the voltage across the two 0.1 MFD capacitors reaches the breakdown

voltage of the lamp. Obtain control can be obtained full off to 95% of the half-wave RMS output voltage. Obtain full power with the addition of the switch across the SCR.

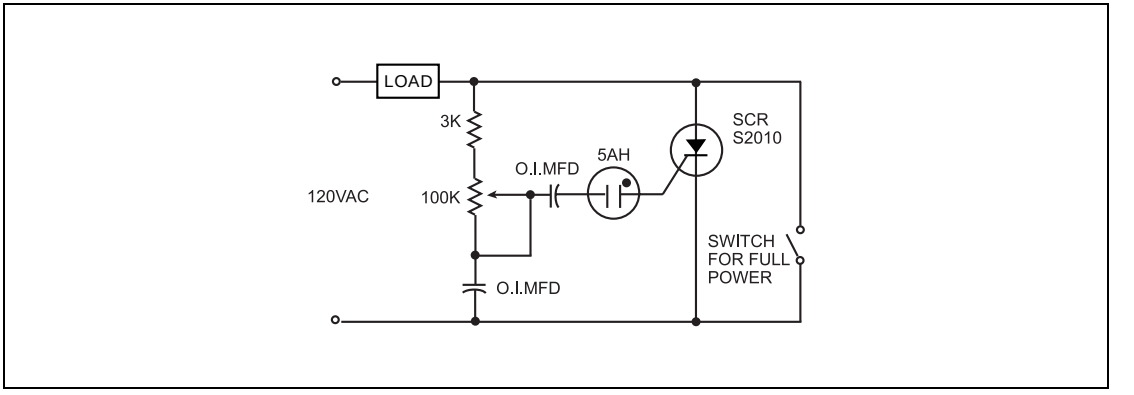


Figure 1.64 Half-wave/Two Terminal

Figure 1.65 shows a transformer-coupled full-wave AC phase-controlled circuit using a 5AH as the trigger for a two-terminal system. The 5AH performs the same as in the half-wave circuit but the pulse transformer allows the SCRs to alternate in firing. Choose the resistor R and the pulse transformer to give proper shape of the pulse to the gate of the SCR. Some loss of load voltage occurs but amounts only to about 5% in terms of total RMS output voltage.

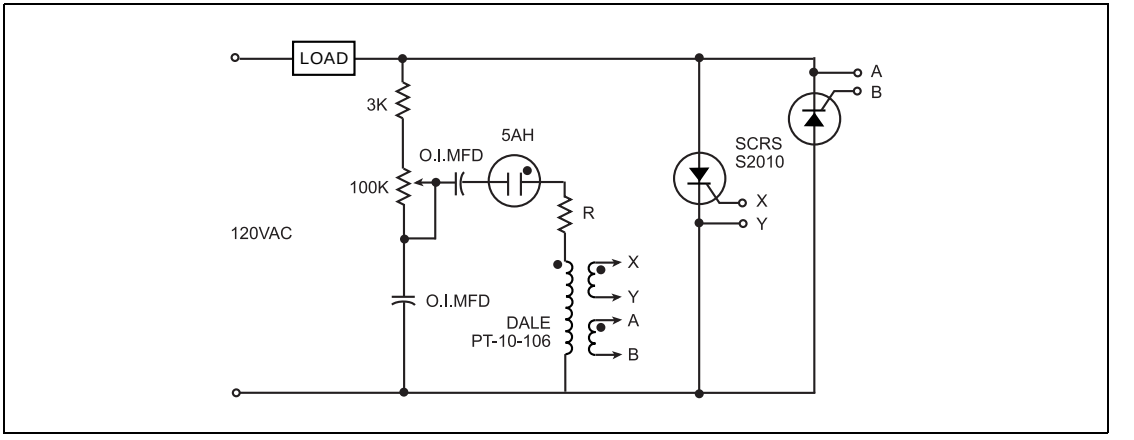


Figure 1.65 Full-Wave Transformer Coupled/Two Terminal

Pulse Transformers

Pulse transformers are often used to couple a trigger-pulse generator to a thyristor in order to obtain electrical isolation between the two circuits. The pulse transformers of many vendors are suitable for this purpose. Although circuit diagrams in this manual show several specific model numbers, this manual does not serve as a testing or approval function.

The transformers usually used for thyristor control are either 1:1 two-winding, or 1:1:1 three-winding types. As shown in Figure 1.66, connect the transformer directly between gate and cathode, use a series resistor R to either reduce the SCR holding current or to balance gate currents in a three-winding transformer connected to two SCRs, or use a series diode D to prevent reverse gate current in the case of ringing or reversal of the pulse transformer output voltage. The diode also reduces holding current of the SCR. In some cases where high noise levels are present, it may be necessary to load the secondary of the transfomer with a resistor to prevent false triggering.

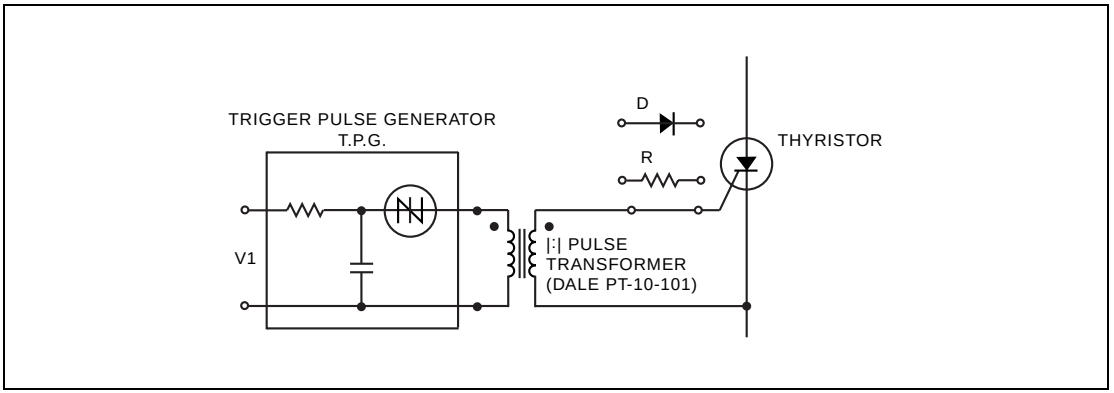


Figure 1.66 Basic Pulse Transformer Coupling

Figures 1.67 through 1.69 show several ways of using a transformer to drive an inverse-parallel pair of SCRs. The three-winding transformer provides full isolation as shown in Figure 1.67. Where such isolation is not required, use a two-winding transformer either in a series mode (Figure 1.70) or a parallel mode (Figure 1.71). In any case, the pulse generator must supply enough energy to trigger both SCRs, and the pulse transformer (plus any additional balancing resistors) must supply sufficient gate current to both SCRs under worst-case conditions of unbalanced gate impedances.

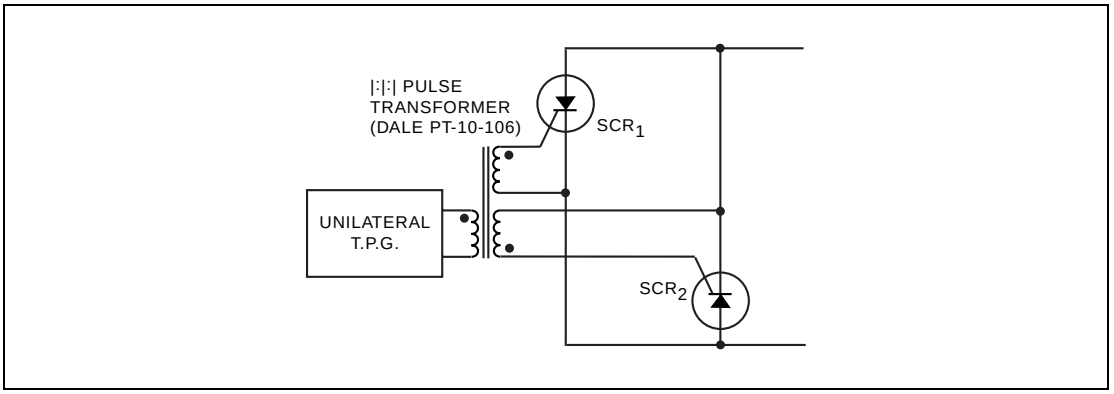


Figure 1.67 Pulse Transformer Connections for Two SCRs—Three-Winding

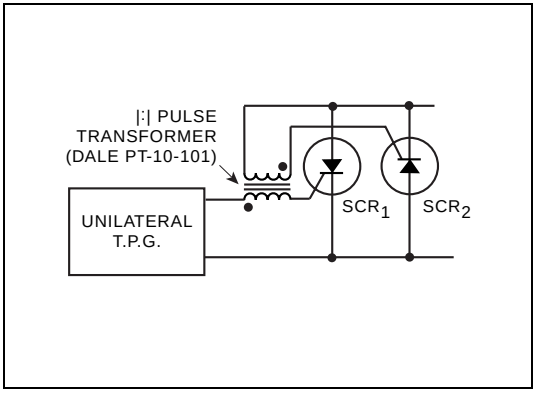


Figure 1.68 Pulse Transformer Connections for Two SCRs—Two-Winding, Series Mode

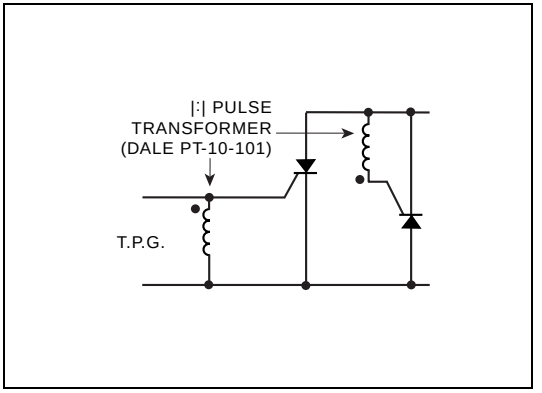


Figure 1.69 Pulse Transformer Connections for Two SCRs—Two-Winding, Parallel Mode

Efficiency is one of the prime requirements of a trigger pulse transformer. The simplest test is to use the desired trigger pulse generator to drive a 20-ohm resistor alone and then drive the same resistor through the pulse transformer. The transformer is perfect if the pulse waveforms across the resistor are the same under both conditions. Expect some loss, however, and compensate by increasing drive from the generator.

Consider the following transformer design factors:

- Design primary magnetizing inductance high enough so that magnetizing current is low, in comparison with pulse current, during the pulse time.
- Since most pulse generators are unilateral, core saturation must be avoided.
- Design tight coupling between primary and secondary, for single-SCR control, or design specified leakage reactance to assist in balancing currents for multiple-SCR control.
- Insulation between windings must be adequate for the application, including transients.
- Interwinding capacitance is usually insignificant but may be a path for undesirable stray signals at high frequencies.

Synchronization Methods

In the basic trigger circuit in Figure 1.70, the UJT can trigger at any intermediate part of the cycle by reducing either the interbase voltage alone or the supply voltage V_1. This results in an equivalent decrease in V_P in accordance with the following equation and causes the UJT to trigger if V_P drops below the instantaneous value of V_E.

$$V_P = \eta V_{BB} + V_D \quad \text{where parameter } \eta = \text{the intrinsic standoff ratio}$$

Therefore, use the B_2 terminal or the main supply voltage to synchronize the basic trigger circuit. Figure 1.70 illustrates the use of a negative synchronizing pulse at B_2.

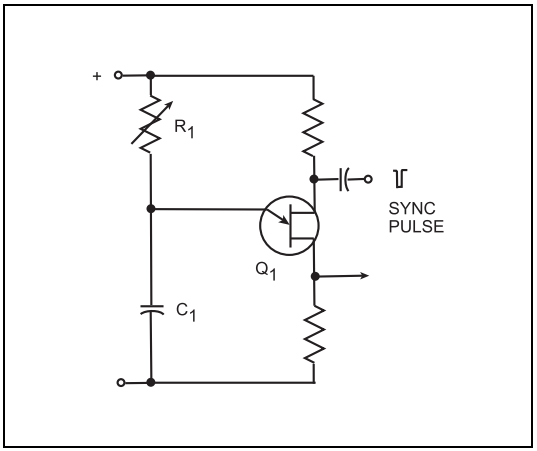


Figure 1.70 Pulse Synchronization of UJT Relaxation Oscillator

Figures 1.71 and 1.72 show two methods of achieving synchronization with the AC line. Use a full-wave rectified signal obtained from a rectifier bridge or a similar source to supply both power and synchronizing signal to the trigger circuit. Use Zener diode CR_1 to clip and regulate the peaks of the AC as indicated in Figures 1.71 and 1.72.

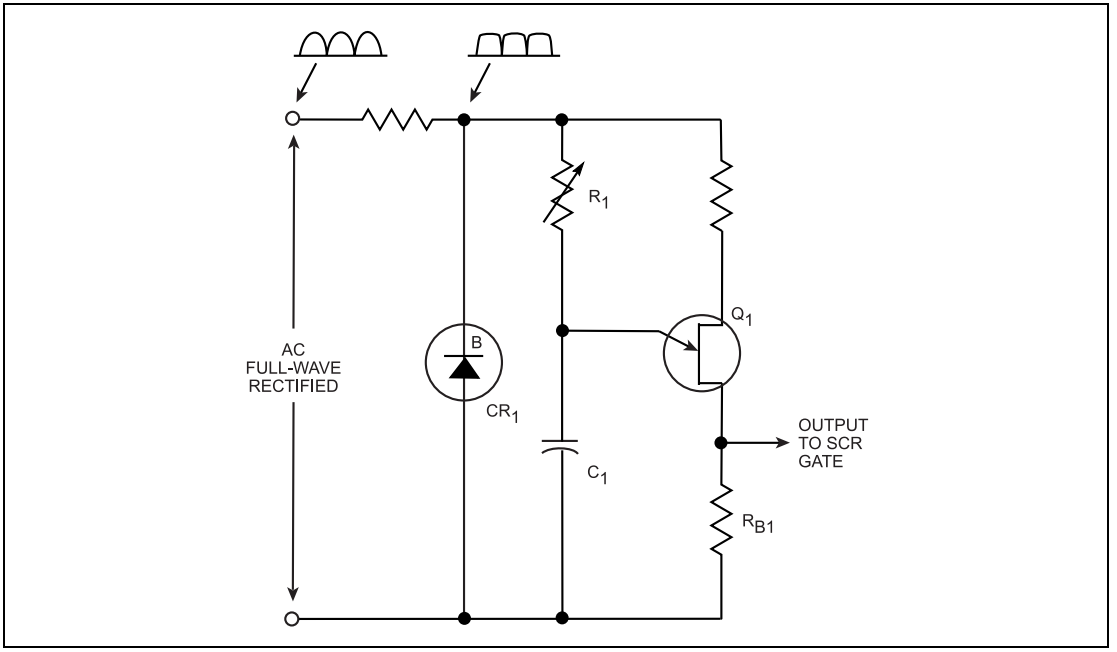


Figure 1.71 Circuit for Synchronization to AC Line—Single Discharge

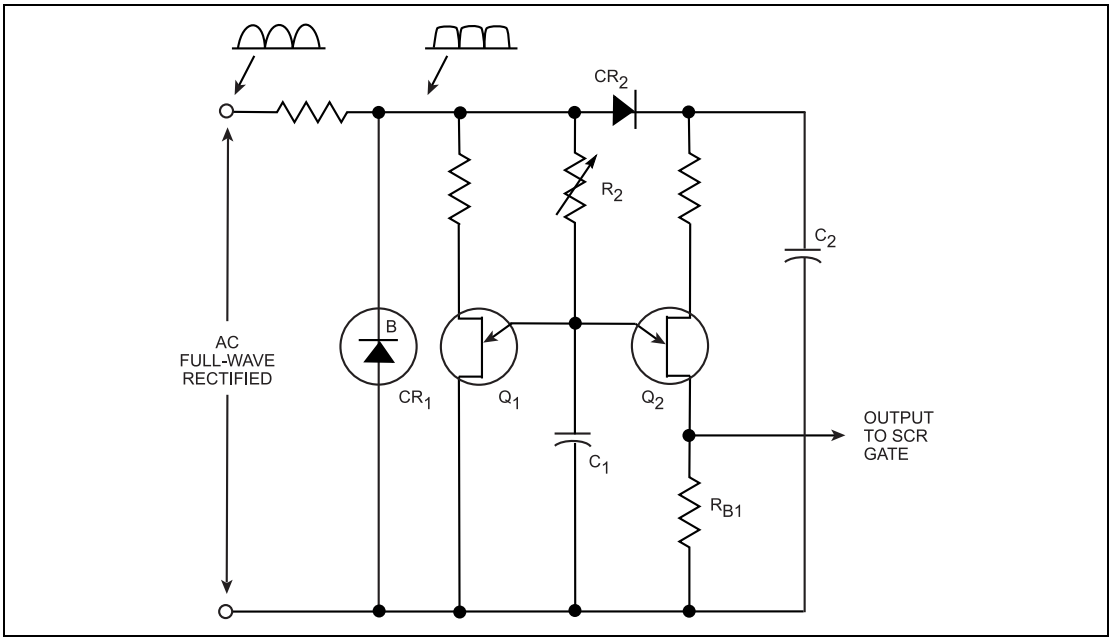


Figure 1.72 Circuit for Synchronization to AC Line—Dual Discharge

At the end of each half-cycle the voltage at B_2 of Q_1 drops to zero, causing Q_1 to trigger. Then, the capacitor C_1 discharges at the beginning of each half-cycle and the trigger circuits synchronize with the line. Figure 1.71 shows a pulse produced at the output at the end of each half-cycle which causes the SCR to trigger and produces a small current in the load. Use a second UJT for discharging the capacitor at the end of the half-cycle if this is undesirable. (See Figure 1.72.) Use diode CR_1 and capacitor C_2 to supply a constant DC voltage to Q_2. The voltage across Q_1 drops to zero each half-cycle, causing C_1 to discharge through Q_1 rather than through the load RB_1. Choose the UJTs so that Q_1 has a higher standoff ratio than Q_2.

Synchronization of a PUT circuit is exactly analogous to the UJT since their operation is so similar.

Trigger Circuits for Inverters

Inverter circuits usually require trigger pulses delivered alternately to two SCRs. Many methods and types of circuits can perform this function, several of which are described in the following sections.

Transistorized Flip-Flops

The transistor flip-flop is a very fundamental and useful circuit for driving SCR or triac gates. The transistor may drive the gates directly through a transformer or through a pulse shaper. It is necessary to design the transformer to avoid saturation at the lowest operating frequency and highest supply voltage. Use a UJT or a PUT relaxation oscillator to drive the flip-flop for precise timing or connect it as a free-running multivibrator.

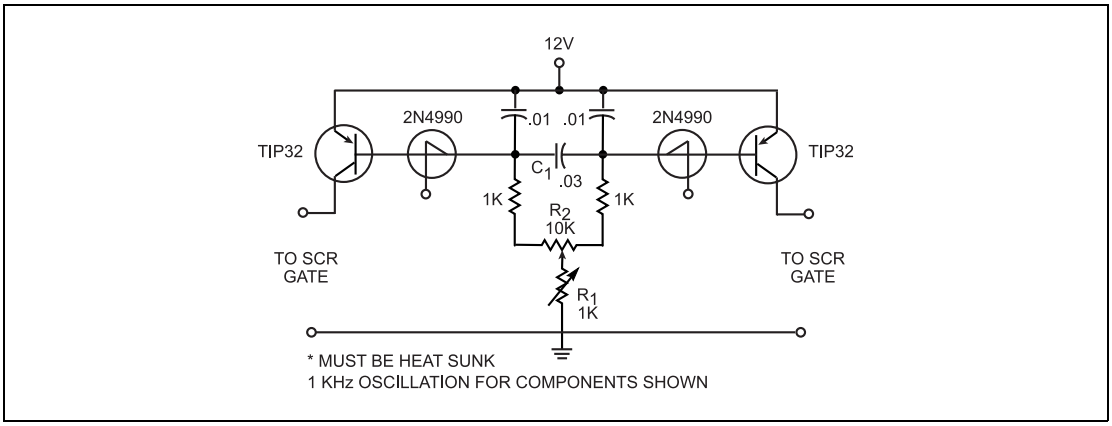


Figure 1.73 Transistorized Flip-flop Trigger Circuits for Two Inverter SCRs—1 KHz Oscillation

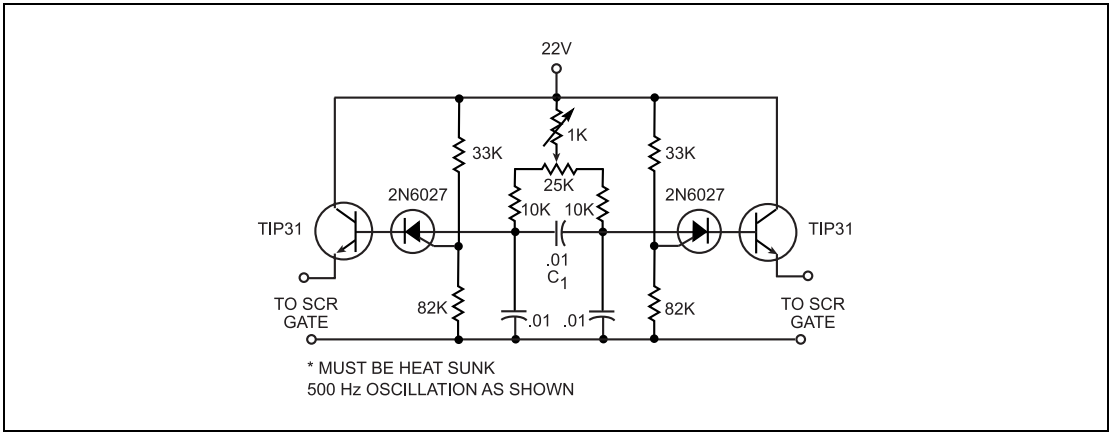


Figure 1.74 Transistorized Flip-flop Trigger Circuits for Two Inverter SCRs—500 Hz Oscillation

Figures 1.73 and 1.74 show two approaches that provide alternate output pulses required by many inverter circuits. Obtain alternate output pulses by cross coupling two relaxation oscillator circuits by capacitor C_1. Potentiometer R_1 trims frequency, and R_2 trims symmetry. Both circuits offer the same rise times and have an upper frequency limit of 20 kHz, but the circuit with the PUT does possess greater versatility and higher output voltages. The oscillation frequency of the latter can vary either by changing the capacitors or by varying the gate bias on the PUT.

PUT Flip-Flop Trigger Circuit

This flip-flop circuit consists of two relaxation oscillator circuits coupled together as shown in Figure 1.75. When one of the two trigger devices is in the “on state,” the other is always in the “off state.” Turning on one device instantaneously produces a negative voltage on the other due to the presence of capacitor C_T. This shifts it to the “off state.” R_1 adjusts the frequency, and R_2 trims the symmetry. Outputs V_1 and V_2 can couple to additional stages of amplification before coupling to the gate.

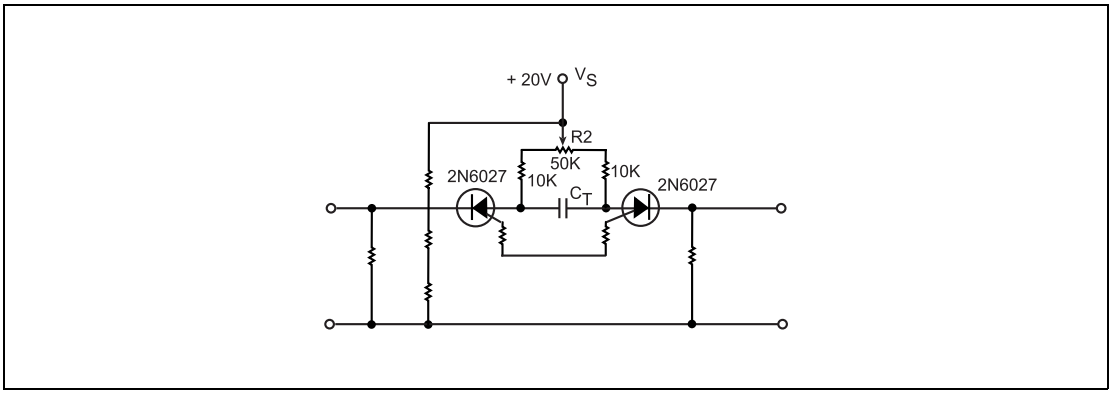


Figure 1.75 PUT Flip-flop Trigger Circuit

Pulse Amplification and Shaping

Consideration of SCR trigger requirements may reveal that the output of a pulse generator is not of sufficient amplitude and/or its output rise time is too slow. Bolster the output with little additional expense to meet the stringent gate requirements of SCRs working at high frequencies and high di/dt.

Figures 1.76 through 1.80 show several gate amplifier circuits. The circuit in Figure 1.76 uses a transistor amplifier saturated during the duration of the relaxation oscillator pulse. This allows C_1 to discharge into the SCR.

The availability of SCRs with highly sensitive gates permits use of these devices to trigger higher-rated SCRs as shown in Figure 1.79. EC103B as SCR_1 requires less than 200 microamperes of gate signal to trigger. Current then flows through R_2, SCR_1, and into the gate of SCR_2. This device turns on and shunts the main power away from SCR_1. In addition to providing a means of triggering high-current SCRs by low-level signals from high-impedance sources, this type of triggering yields positive triggering from pulsed gate signals even with highly inductive loads due to the much lower latching current requirements of the EC103B in comparison with the higher-rated SCRs. The gate of SCR_2 is driven by a trigger signal with SCR_1 latched into conduction which is maintained until SCR_2 is forced into conduction. R_2 limits the current through SCR_1 to a value within its rating. SCR_1 must meet the same voltage requirements as SCR_2. However, its current duty is generally of a pulsed nature and negligible. Several types of SCRs have amplifying gates, in which the predriver SCRs are internal to the device as shown in Figure 1.80.

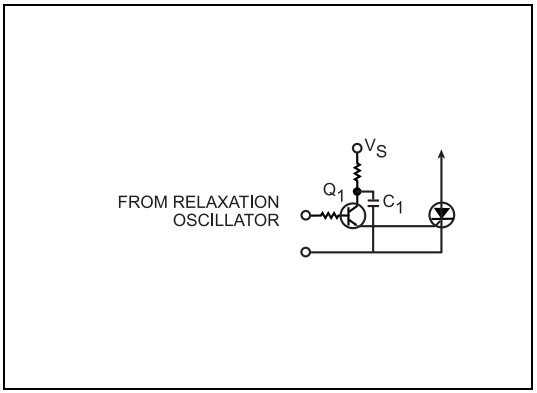


Figure 1.76 Trigger Pulse Amplifier Circuits—Transistor Pulse Amplifier

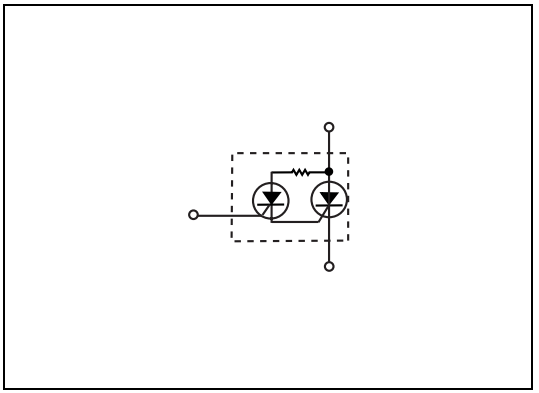


Figure 1.78 Trigger Pulse Amplifier Circuits—Amplifying Gate SCR

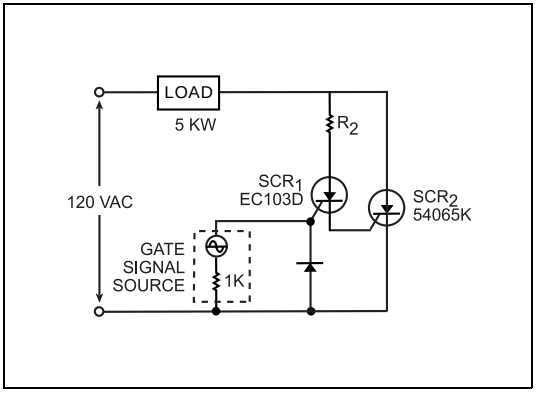


Figure 1.77 Trigger Pulse Amplifier Circuits—Use of Low Current SCR as a Gate Signal Amplifier

Predrivers are particularly useful when it is necessary to maintain the trigger voltage for the entire conduction period. Under these conditions, the power dissipation in the gate of the power device may be excessive. Figure 1.79 shows a technique of maintaining trigger drive during the conduction period in the form of a pulse train, reducing the average gate dissipation. The transistor multivibrator provides alternate driving voltages to the two unijunction transistor oscillators. The outputs of these oscillators provide the alternating pulse train sequence required for inverter circuits.

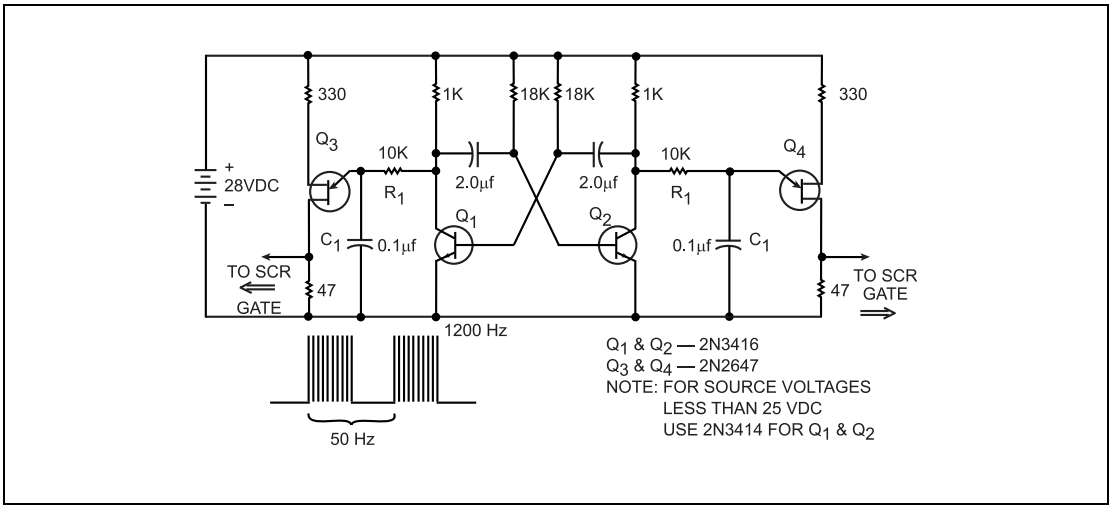


Figure 1.79 Trigger Circuit Providing Train of Pulses

It is desirable to trigger with a fast rise-time pulse for some high-current switching applications. The circuit shown in Figure 1.80 can sharpen slow-rising pulse. The diode D_1 conducts when a pulse appears at the input of this circuit, charging the capacitor. The forward drop across the diode ensures a positive gate-to-anode voltage on the PUT and prevents it from switching. The diode becomes reverse biased and the PUT switches on when the capacitor charges to the peak voltage of the pulse. The consequent pulse delivered to the SCR has a rise time of 50 to 100 nanoseconds determined by the PUT turn-on characteristics.

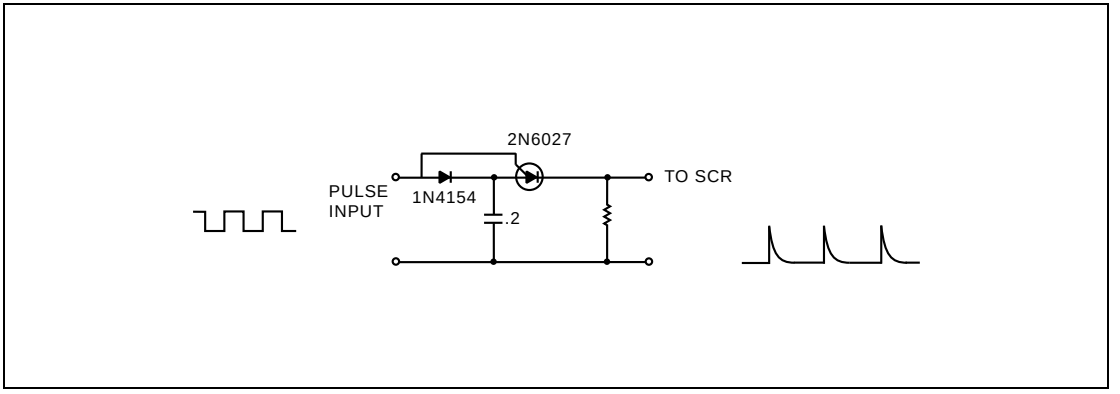


Figure 1.80 Pulse Sharpener Using a PUT

Remember that for fast-rising current loads, an SCR may require a fast-rising high-level rectangular pulse to assure triggering. Using reactive pulse-forming networks or blocking oscillators can shape rectangular pulses. However, these circuits are relatively costly and large. Figure 1.81 shows a circuit which will generate rectangular pulses of 10 µsec pulse width at repetition rates up to 20 kHz and does not require any inductive elements. This circuit is designed to adequately trigger most SCRs even under

the most stringent di/dt conditions with a 20-volt amplitude and 20-ohm source impedance. The UJT operates as a conventional relaxation oscillator whose frequency may be controlled by any of the techniques previously mentioned. The UJT output pulses drive a four-transistor amplifier circuit which improves the rise time and extends the pulse width to approximately 10 µsec.

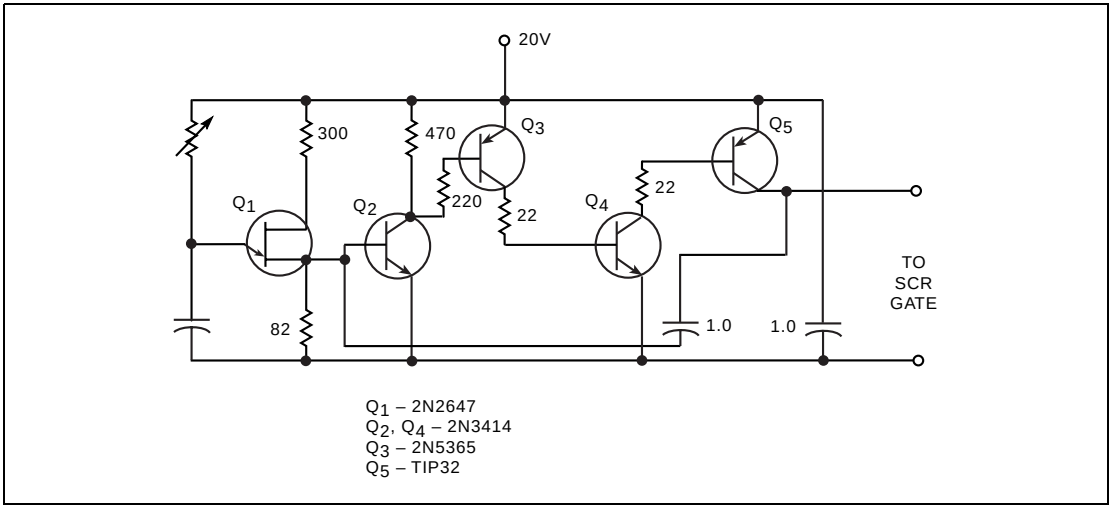


Figure 1.81 High di/dt Trigger Circuit

Depending on the nature of the control input signal, consider other types of SCRs for triggering larger SCRs. LASCR is an option where direct triggering by light is required. Also, the LASCR in conjunction with a suitable light source provides a simple way in which to obtain electrical isolation in SCR control circuitry.

Gating Triacs and Alternistors On in Various Quadrants

Gating quadrants of triacs and alternistors are an often misunderstood parameter of thyristor type devices. These quadrants are not related to the 360° in one AC sine wave. Consider these quadrants as gating modes. Figure 1.82 shows a definition of gating quadrants.

Remember that the gate signal is always referenced to the MT1 or cathode lead. (Do NOT place a load between MT1 terminal and power supply reference, as shown in Figure 1.83.)

Also, consider the polarity of the gate pulses as related to the MT1 lead and the polarity of the voltage (which half-cycle) on the MT2 lead with respect to MT1.

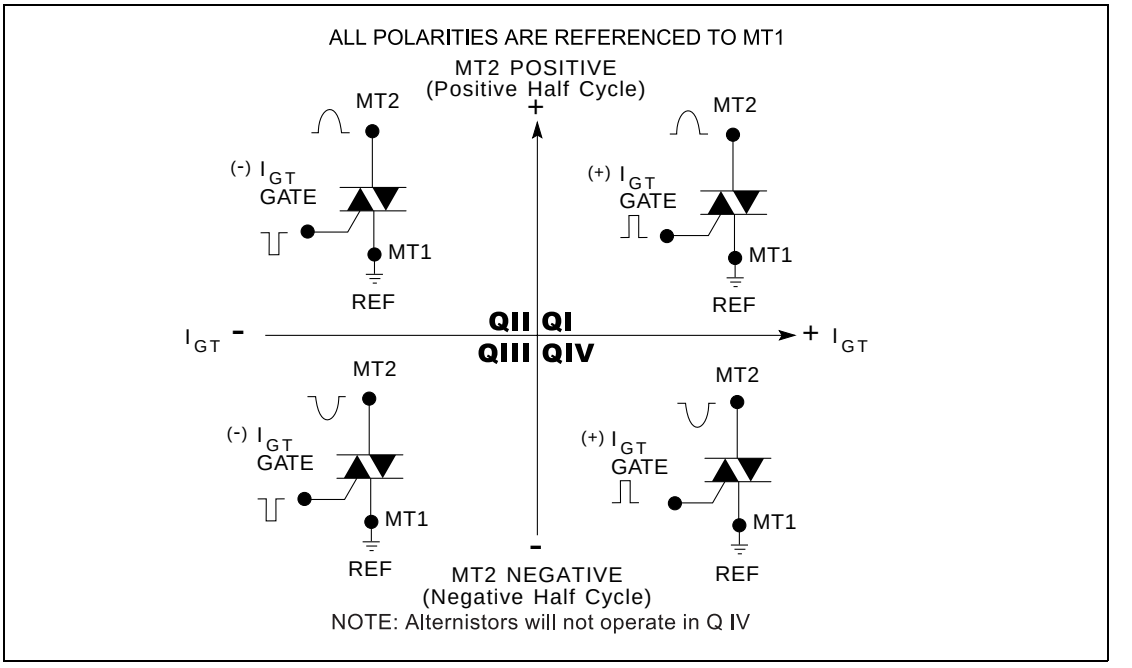


Figure 1.82 Definition of Quadrants

Teccor's sensitive gate triacs may be gated on in all four quadrants. Figures 1.84 and 1.85 show a gate synchronized to MT2 with an in-phase signal using QI and QIII or applying unipolar signals (gate always positive or always negative). If applying a positive signal to the gate (Figures 1.83 and 1.86), the triac is turning on in QI (during the positive half-cycle) and QIV (during the negative half-cycle). If applying a negative signal to the gate (Figure 1.87), the triac gates on in Quadrant II (QII) (during the positive half-cycle of the AC line) and in QIII (during the negative half-cycle).

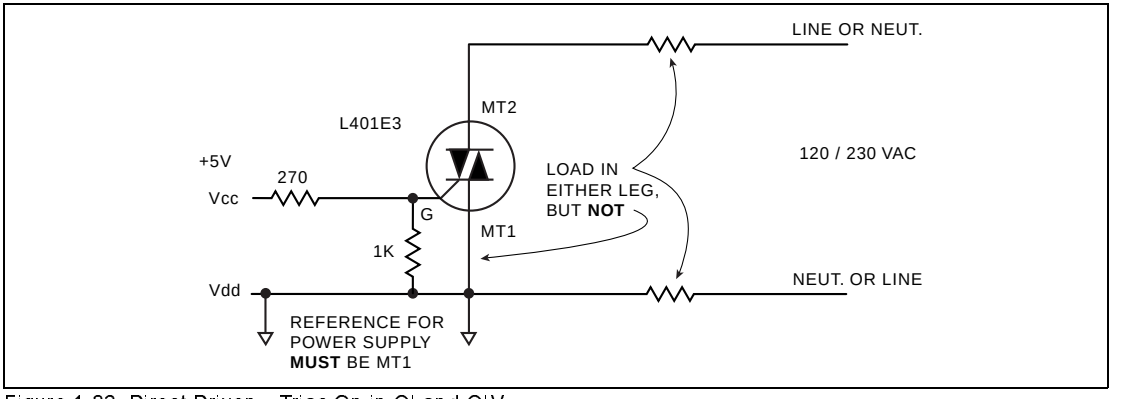


Figure 1.83 Direct Driven—Triac On in QI and QIV

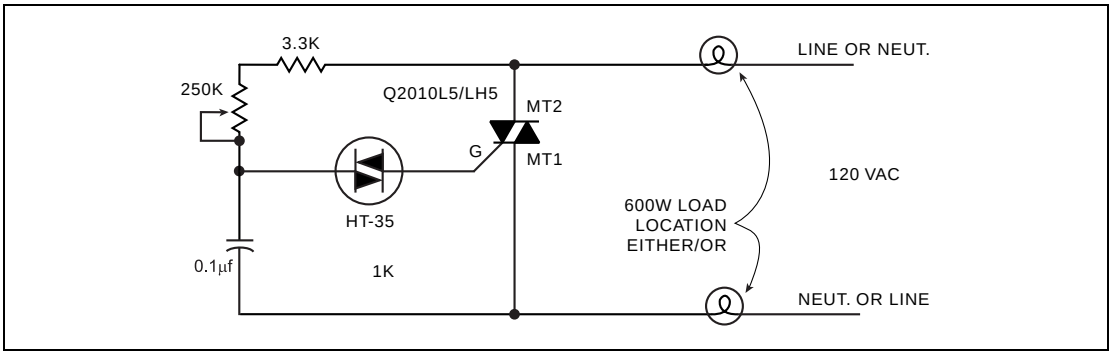


Figure 1.84 In-phase Gating Circu\it—Triac/Alternistor On in QI and QIII

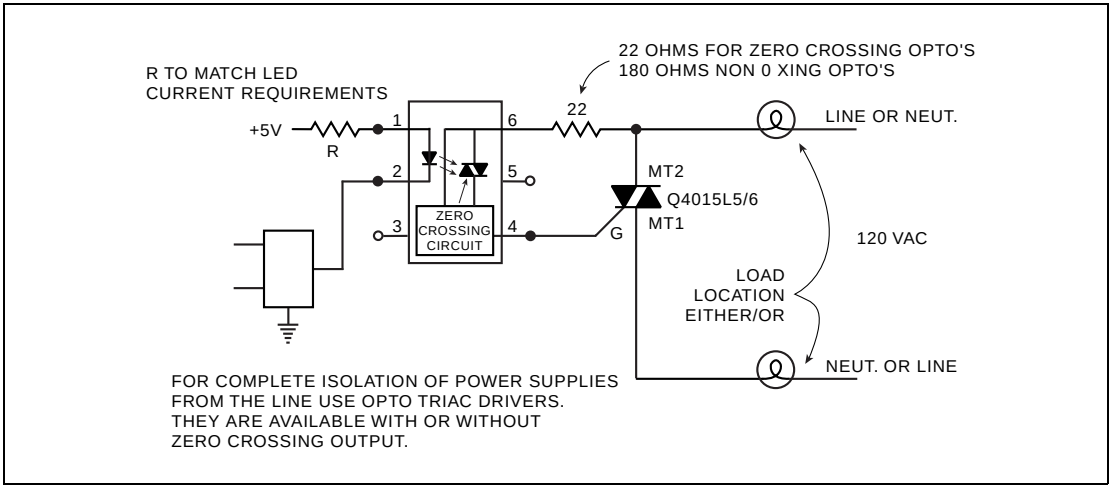


Figure 1.85 In-phase Gating Circuit Using Opto Couplers—Triac/Alternistor On in QI and QIII

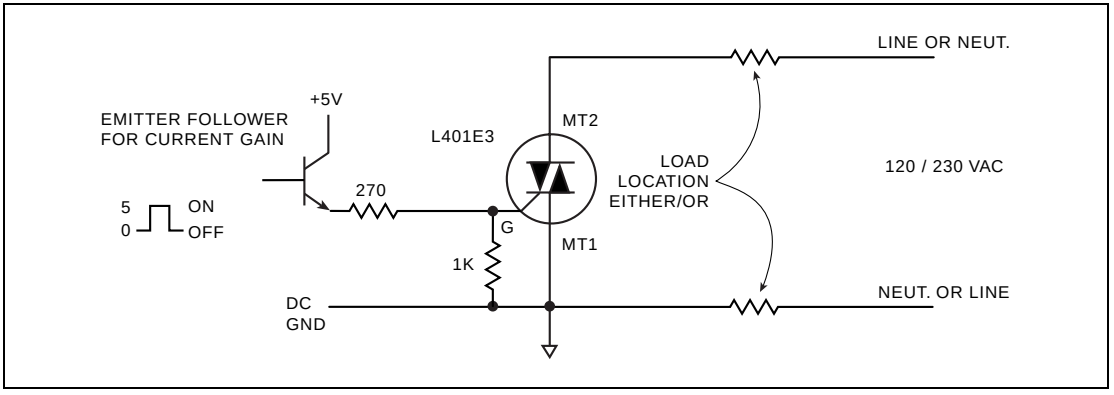


Figure 1.86 Amplified Drive Circuit—Triac On in QI and QIV

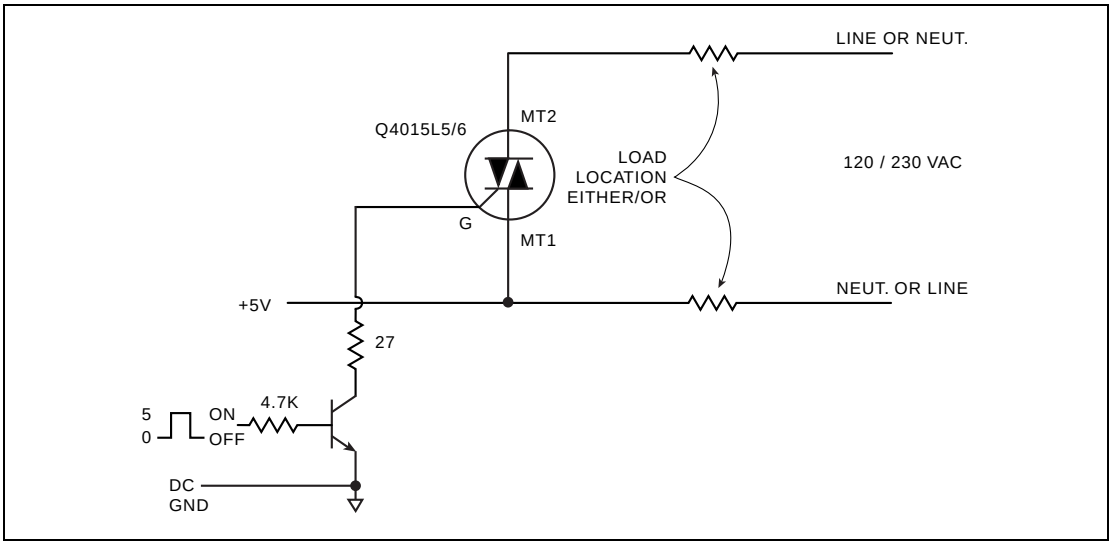


Figure 1.87 Modified Drive Circuit—Triac/Alternistor On in QII and QIII

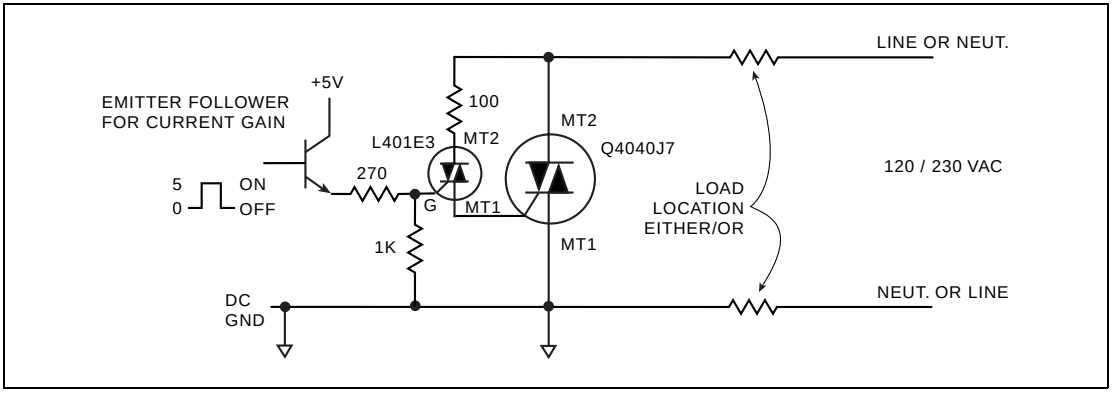


Figure 1.88 Amplified Gate Triac On in QI and QIV, Resulting in Alternistor On in QI and QIII