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AN80994

Design Considerations for Electrical Fast Transient (EFT) Immunity

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Associated Part Family: All PSoC
Related Application Notes: AN2155, AN78175, AN96475

AN80994 describes best practices for improving electrical fast transient (EFT) immunity in embedded system designs. This application note discusses the effects of fast transients on mixed-signal embedded controllers, and provides methods to improve EFT immunity and design recommendations that can help mitigate the effects. It also summarizes the IEC 61000-4-4 EFT test requirements.

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Safety Notice

EFT testing involves hazardous voltages.

Electrical safety principles must be duly followed.

Consult a certified safety technician.

1 Introduction

This application note discusses the effects of electrical fast transients (EFT) on embedded controllers and recommends hardware and firmware techniques to mitigate them. This application note also explains a set of guidelines that a designer can use to build a system that is immune to such transients.

International standards have been developed to describe the characteristics of transients. These standards also provide guidance to the product designer on the testing methodologies for compliance. The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 (for EFT) by International Electrotechnical Commission (IEC).

The section, What is EFT?, describes EFT and the characteristics of the test waveform per IEC 61000-4-4. The next section, Failure Modes, talks about the effects the transients can have on embedded systems. The Troubleshooting and Methods to Improve EFT Immunity of a Failing System section presents tips on debugging and lists some possible methods to improve EFT immunity of a failing system.

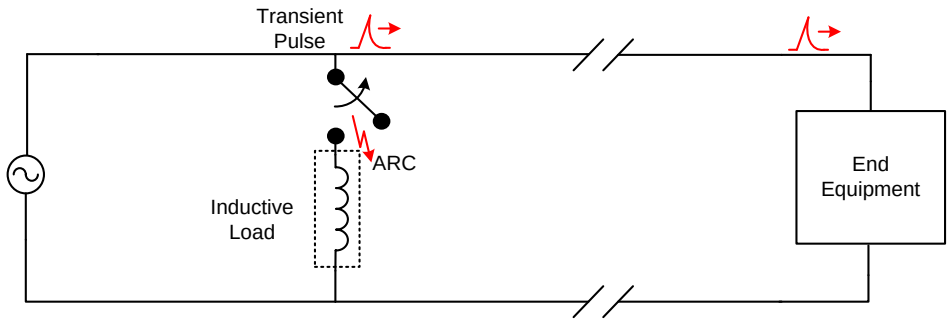
The primary goal of a design engineer is to ensure proper operation and performance of an end product even when used in a non-conducive environment. More often than not, emphasis is placed on the functional aspects of the product than on system itself. Design engineers must consider aspects of product design, including but not limited to electromagnetic interference and immunity requirements. If a product fails to meet compliance tests (EFT or otherwise), redesign or rework is required. This significantly increases the cost of design. These costs are in addition to delayed timelines, customer dissatisfaction, and loss of market share. Therefore, it is vital for the design engineer to start a regime of mitigation immediately in parallel with the system design. The Design Considerations and Mitigation Techniques section describes how a system design engineer can pre-empt EFT-related issues by considering certain design-time principles. This application note mainly focuses on considerations for target board design. It also summarizes some important design considerations for a system and its power supply. Furthermore, it also provides firmware techniques that can be incorporated for error detection and recovery mechanism.

The appendix presents a summary of the IEC 61000-4-4 standard. The application note also provides references for further reading.

2 What is EFT?

Inductive loads such as relays, switch contactors, or heavy-duty motors when de-energized produce bursts of narrow high-frequency transients on the power distribution system. These fast transients can also be produced when the utility provider switches in or out the power factor correction equipment. A common cause of power line transients is sparking that occurs whenever an AC power cord is plugged in, equipment is switched off, or when circuit breakers are opened or closed. Figure 1 shows how transients are generated and coupled to end equipment over power lines.

Figure 1. Generation and Coupling of Transient Noise to End Equipment

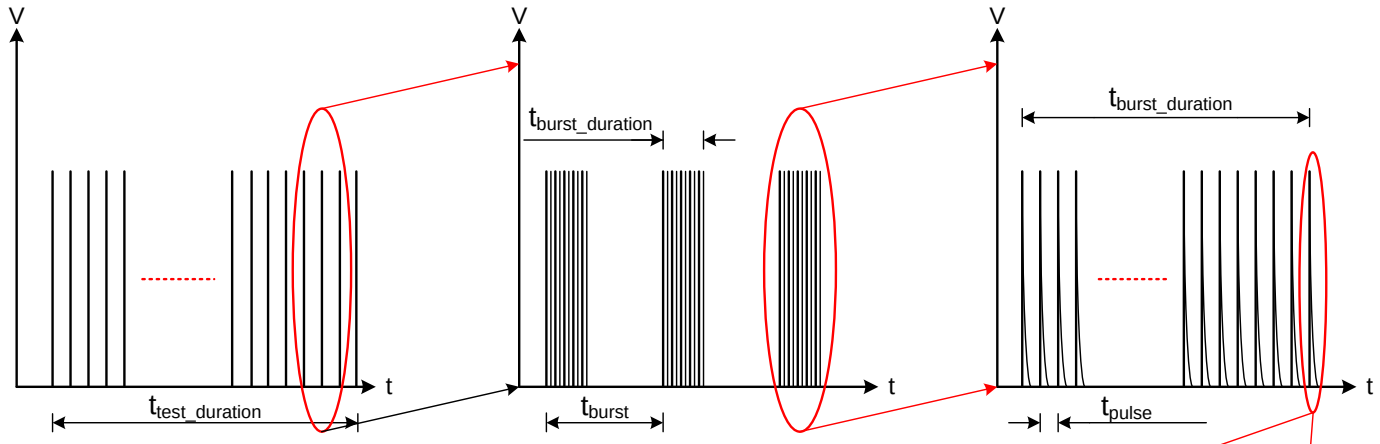


The IEC 61000-4-4 specification defines the test voltage waveform that is intended to simulate the transients created by switching of inductive loads on AC power lines. The specification also defines the requirements for immunity to repetitive fast transients and the necessary test methods for systems.

The EFT waveform, as defined by the IEC 61000-4-4 standard, is intended to be used by manufacturers to test the performance of equipment when subjected to fast transients. Primarily, the testing involves injection of EFT pulses into the equipment's AC power supply lines. The EFT waveform can also be injected into the signal and control lines, and earth connections to simulate the coupling of transient noise onto these lines. The pulse waveform has a high amplitude (0.5 - 4 kV), short rise time, high repetition rate, and a low energy content. IEC 61000-4-4 also defines test levels based on the amplitude of the pulse waveform. Figure 2 shows the waveform shape as defined in the IEC 61000-4-4 specification. It consists of a burst of 75 pulses repeated every 300 milliseconds for a duration of 1 minute. Both positive and negative polarity EFT pulses are injected during testing.

As such, the test is intended to show the immunity of electrical and electronic equipment when subjected to such fast transients. There are international standards that specify the requirements for the transient immunity performance with respect to specific class of equipment. For example, European Union's EN 55024 describes the test requirements and performance criteria for information technology equipment. Similarly, IEC 61547 describes the test requirements and performance criteria for lighting equipment. All of these standards derive their requirements and test methodologies from IEC 61000-4-4. Consult your local standards body to obtain relevant immunity performance standards for the equipment being designed.

Figure 2. EFT Test Pulse Waveform



$t_{test\_duration}$: ≥ 1 minute

$t_{burst\_duration}$: 15 msec @ 5 kHz burst
0.75 msec @ 100 kHz burst

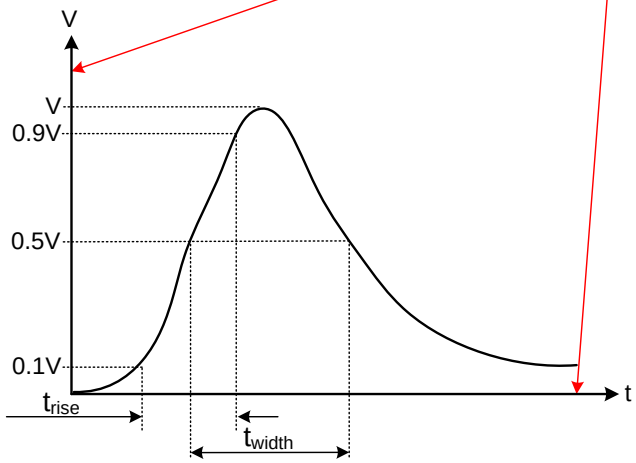
t_{burst}: 300 msec

t_{pulse} : 200 µsec @ 5 kHz burst
10 µsec @ 100 kHz burst

t_{rise}: 5 ns ± 30%

t_{width}: 50 ns ± 30%

V : peak voltage



2.1 Characteristics of EFT Waveform

Figure 2 shows the wave shape of a single pulse terminated into a 50 ohm load as defined by the IEC 61000-4-4 specification. Each individual pulse is a double exponential waveform characterized by a 5 ns rise time and a 50 ns pulse width. IEC 61000-4-4 defines various test levels for EFT immunity. The peak voltage increases as the test level increases. Table 1 lists the peak voltage V of the pulse, shown in Figure 2, for each test level.

Table 1. IEC 61000-4-4 Test Levels

Level	Power Supply Terminal		I/O Signals/Data Terminals	
	Peak Voltage (kV)	Repetition Rate (kHz)	Peak Voltage (kV)	Repetition Rate (kHz)
1	0.5	5 or 100	0.25	5 or 100
2	1	5 or 100	0.5	5 or 100
3	2	5 or 100	1.0	5 or 100
4	4	5 or 100	2.0	5 or 100
X[a]	Special	Special	Special	Special

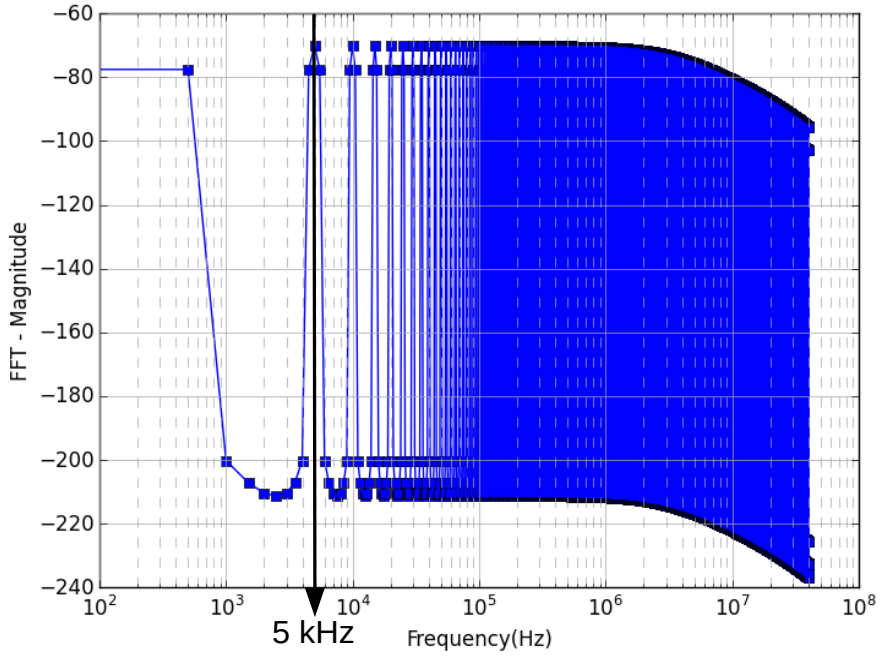
Note 1: Use of 5-kHz repetition rates is typical; however, 100 kHz is closer to a real world scenario.

Note 2: The terminals to be tested have to be determined by the manufacturer.

[a] "X" is a special level. This level must be specified in the equipment specification.

It helps to understand the frequency spectrum of the EFT burst. Figure 3 shows the spectrum of a burst of pulses at 5 kHz. Note how the burst frequency (5 kHz) manifests itself as one of the dominant amplitudes in the spectrum. This is an interesting point to consider. The EFT pulse is generally easier to filter but it becomes rather difficult when the burst of lower frequency (5 or 100 kHz) is introduced. If the low-frequency burst itself is repeated every 300 ms, another component of 3.33 Hz is also introduced.

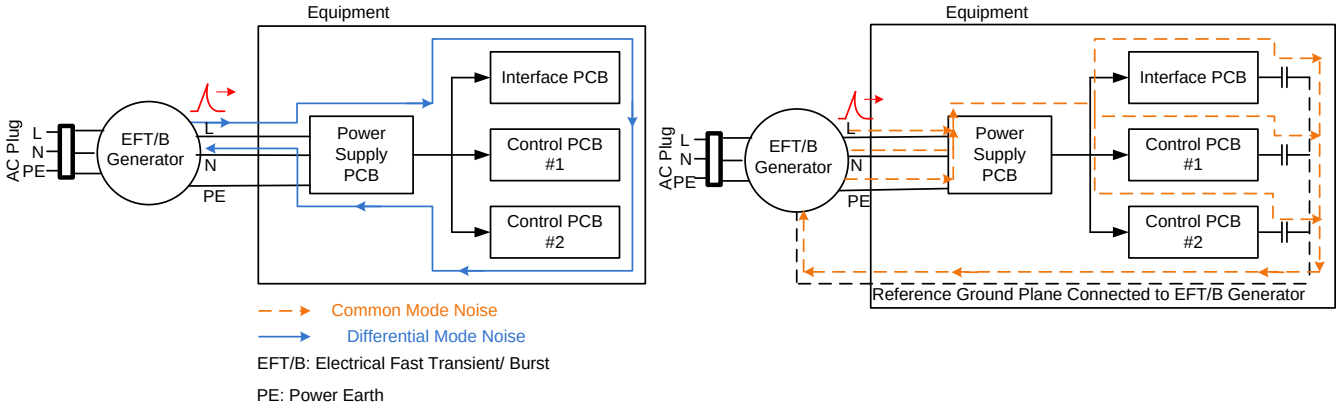
Figure 3. EFT – 5 kHz Burst: Frequency Spectrum



3 Failure Modes

Transient-induced noise conductively couples to the end equipment via the AC power cord, DC power, and signal/control lines. Within the equipment, if proper filtering is not used, the noise can propagate to different PCBs as shown in Figure 4. There can be direct or indirect coupling of noise in the equipment. Direct coupling is when the transient, manifested as noise flows through vulnerable circuits via supply, ground, signal, or control lines. Indirect coupling occurs to an adjacent conductive surface by electromagnetic radiation.

Figure 4. A Possible Propagation Path of Differential and Common Mode Noise Induced by Positive Polarity Transient in Equipment



As shown in Figure 4, the transient-induced noise is both common mode and differential mode noise. Common-mode noise is present or “common” to both conductors and is typically “in phase” within the conductors. Differential noise is present on only one conductor or present in opposite phase in both conductors.

Embedded controllers are designed to generate and act on signals such as high-speed serial communication clocks that have timing specifications comparable to that of transient-induced noise. Therefore, transient-induced noise is likely to interfere with these signals. In a broad classification, the following blocks, pins, and signals are most influenced by transient-induced noise:

- Power and ground signals
- Reset circuits
- Clock/oscillator signals
- Edge-sensitive triggers
- High-frequency digital signals
- Analog signals
- Communication blocks such as I2C, SPI, UART
- CPU
- Flash/RAM

When transient-induced noise affects one or more of these blocks, the following types of system failures can occur:

- Reset
- Latch-Up

- Corruption of Analog and Digital Signals
- Communication Failure
- Memory Corruption

3.1 Reset

Due to transient-induced noise, the device can undergo one of the following resets:

- External reset
- Power-on reset
- Low Voltage Detect (LVD) based reset
- Brownout reset
- Watchdog reset
- Software reset

An external reset can be triggered by the transient-induced noise on the reset pin. Therefore, an external reset can happen due to supply voltage dips or ground reference shift, depending on whether the reset pin is active HIGH or LOW. Some controllers have alternate reset pins. In such cases, the device can reset due to the noise on alternate reset pins also.

Figure 5. Transient Noise Waveform on Supply Line Measured at the Output of an AC-DC Converter

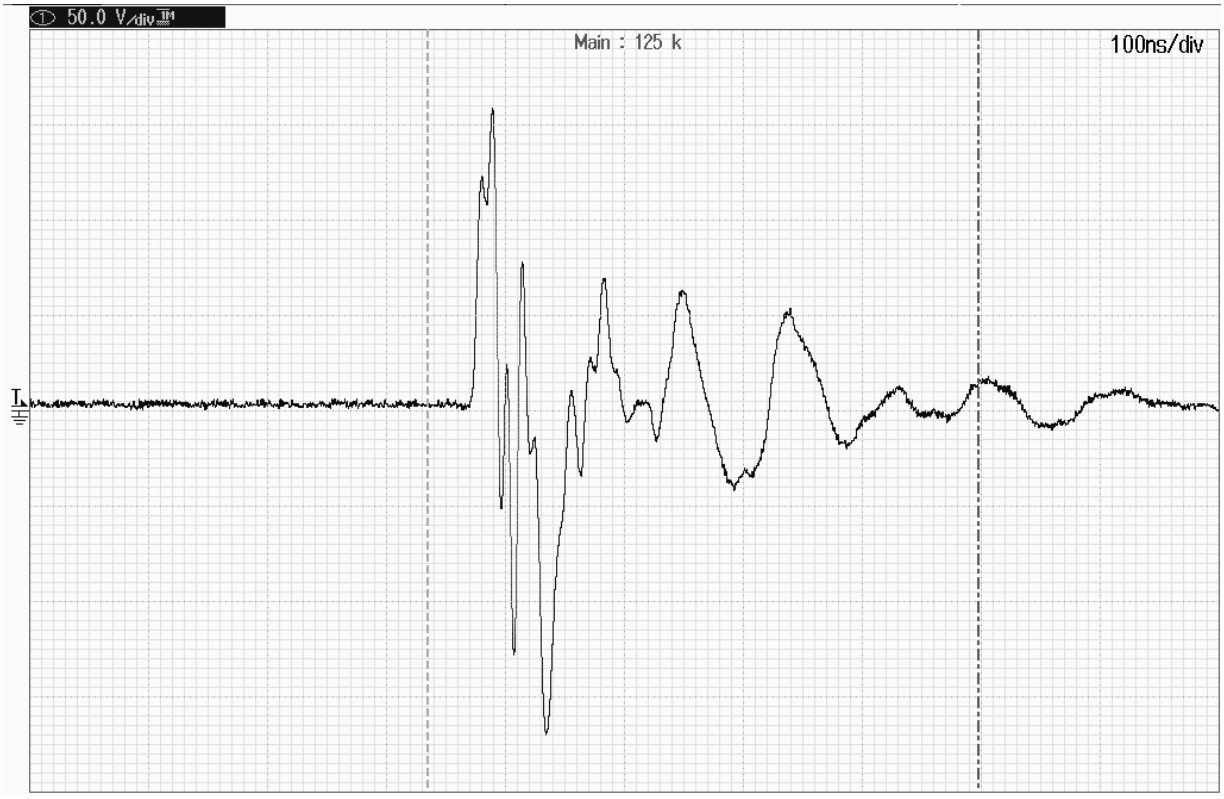


Figure 5 shows the waveform on the supply line measured at the output of an AC-DC converter when the EFT test waveform is injected into the converter. As you can see, the peak voltage is ~350 V. When there is load such as a controller circuit on the output of the AC-DC converter, the characteristics of the noise seen by the noise might vary depending on the filters, decoupling network at the supply inputs of the controller.

Resets due to Power On, LVD, and brownout occur in the following cases:

- Transient-induced noise pulls down the supply voltage
- Transient-induced noise shifts the ground reference
- Transient-induced noise triggers the ESD clamp circuits on I/Os so that the effective supply voltage seen by the device dips triggering the brown out reset.

Power-on reset occurs if the effective supply voltage is below the device operating voltage range. When brownout and LVD based reset are enabled in the controller, these events can occur when the effective supply voltage is below the trip voltage and stays there beyond the minimum time.

A watchdog reset occurs if the firmware fails to clear the watchdog timer in time. This is due to unexpected firmware operation typically caused by a failing subsystem such as CPU or flash.

A software reset occurs if the master device wants to reset the slave upon detecting abnormal behavior in the system such as when the master receives wrong data due to the loss of signal integrity. A software reset can also occur if the code execution is not normal and enters an exception. This abnormal code execution can be due to a corrupted state in the CPU, clock, flash, or RAM.

3.2 Latch-Up

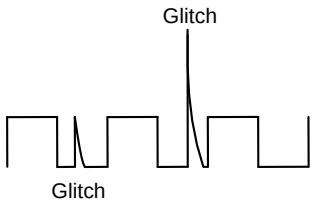
Latch-Up is a situation where the transient-induced noise does not actually do the damage. It just sets things up so that the power supply can destroy the part or the circuit becomes nonfunctional without a power cycle reset. The ground bounce or shifting of the ground reference due to transient-induced noise can drive CMOS circuits into latch-up. Specifically, it is the creation of a low-impedance path between the power supply rails of a CMOS circuit, triggering a parasitic current carrying path which disrupts proper functioning of the device. A power cycle is required to correct this situation. Latch-up can lead to the destruction of the device due to overcurrent.

3.3 Corruption of Analog and Digital Signals

Fast digital circuits are more prone to EFT-based failures than low-bandwidth digital or slow analog circuits.

Edge-sensitive inputs are more vulnerable to transient-induced noise. Even with low-pass filtering, a sufficiently large transient can inject enough energy to disrupt the device operation. It is also possible that the transients propagate as glitches as shown in Figure 6. These glitches can be mistaken as valid data pulses in case of high-speed digital inputs such as clock and data inputs.

Figure 6. Glitches on I/O Signals Caused by Transients



The oscillator/external clock pins can also be affected by the transient noise. The transients itself can be interpreted as valid clock pulses by the controller.

A transient appearing at the analog input pin of analog blocks can result in distorted data due to the signal disruption. The effect is worse for low-level analog signal processing.

Usually input/output ports on controllers have multiple functions. The transient event that disrupts normal operation of the pin/port can do so by changing the pin state, drive mode, or the pin function. In extreme cases, the transient event can actually trigger the ESD protection blocks on the pin and cause the controller to enter a latched-up state.

3.4 Communication Failure

Commonly used communication protocols in embedded applications are I2C, SPI, and UART. Communication failure can happen due to the following:

- Malfunctioning of the communication block in the controller

  The block might get damaged or stressed by the transient-induced noise propagating to the internal circuitry through supply and ground.

- Clock stretch or glitch on clock lines

  Glitches on clock signal might disrupt the operation. On the other hand, the clock might be stretched if the device fails to receive ACKs from the other device. This can be due to the malfunctioning of the internal blocks or malfunctioning of the master device that is required to send ACKs. The clock might also be stretched when the operational state machine within the controller breaks.

- Loss of signal integrity

  Due to high noise on supply and ground to which communication lines are referenced, the signal integrity may be compromised such that the protocol specification is violated.

- Malfunctioning of transceiver device

  The I^2C, SPI master/slave, or the transmitter/receiver at the other end of the UART communication may be vulnerable to the transient noise. Reset, damage, or malfunctioning of those devices can break the communication.

- Interface between data viewing system, i.e., computer and the controller such as USB-to-UART Bridge, RS232, the UART level translator, and the serial cable may malfunction.

Inherently, UART is more stable than I^2C or SPI protocol because in the UART protocol, the signal is sampled at the center of the bit time window unlike I^2C or SPI where the signal is sampled at the clock edges. The level translator when used for UART communication, by the virtue of higher voltage level, improves the signal margin and hence the SNR.

3.5 Memory Corruption

Transient-induced noise can damage memories such as flash or RAM due to them interfering with system clocks or flash write voltages. When the memory gets corrupted, the system can fail to start due to a flash checksum error or can lose the functionality due to corrupted data or code in flash or RAM. Flash corruption might be permanent or might require power cycle or reprogramming to recover the normal state. On the other hand, RAM corruption might require a power cycle or any other reset to resume normal operation.

The subsystem failure can be either permanent or temporary. If the damage is permanent, it is easy to detect. If the damage is temporary, such as latch-up or memory corruption, power-cycling the equipment might recover the normal state of operation. When subjected to an EFT test, subsystems can be partially damaged but can still be fully functional. When stressed by a power supply, high temperature, or abnormal operating conditions, the damaged component can then fail permanently. This latent effect is difficult to identify and solve.

4 Performance Criteria

The loss of functionality or degradation of performance of a controller, relative to the performance as defined by its specifications, per IEC 61000-4-4, can be categorized into the following criteria

Table 2. Performance Criteria

Criteria	Description
Performance Criteria A	Normal performance after the test is within limits as specified by the manufacturer.
Performance Criteria B	Temporary loss of function or degradation of the performance during the test; the controller recovers to its normal performance without any intervention after the test.
Performance Criteria C	Temporary loss of function or degradation of the performance during the test; the controller recovers to its normal performance with intervention after the test.
Performance Criteria D	Loss of function or degradation of the performance during the test; the controller does not recover owing to damage.

It is important to note that a condition assessed as failure for a particular system may not be a failure with respect to another system. For example, an industrial process controller cannot tolerate intermittent device resets during EFT testing but a user interface may. Therefore, give due consideration to the end-application requirements and its ability to tolerate transient noise.

5 Troubleshooting and Methods to Improve EFT Immunity of a Failing System

Effective troubleshooting of problems due to transient-induced noise is nontrivial even though it is often overlooked as part of system compliance testing and bring-up. Designers should ascertain the probable causes for each failure observed as part of compliance testing. The designer and the person responsible for running compliance tests must work together to isolate the causes for the failures.

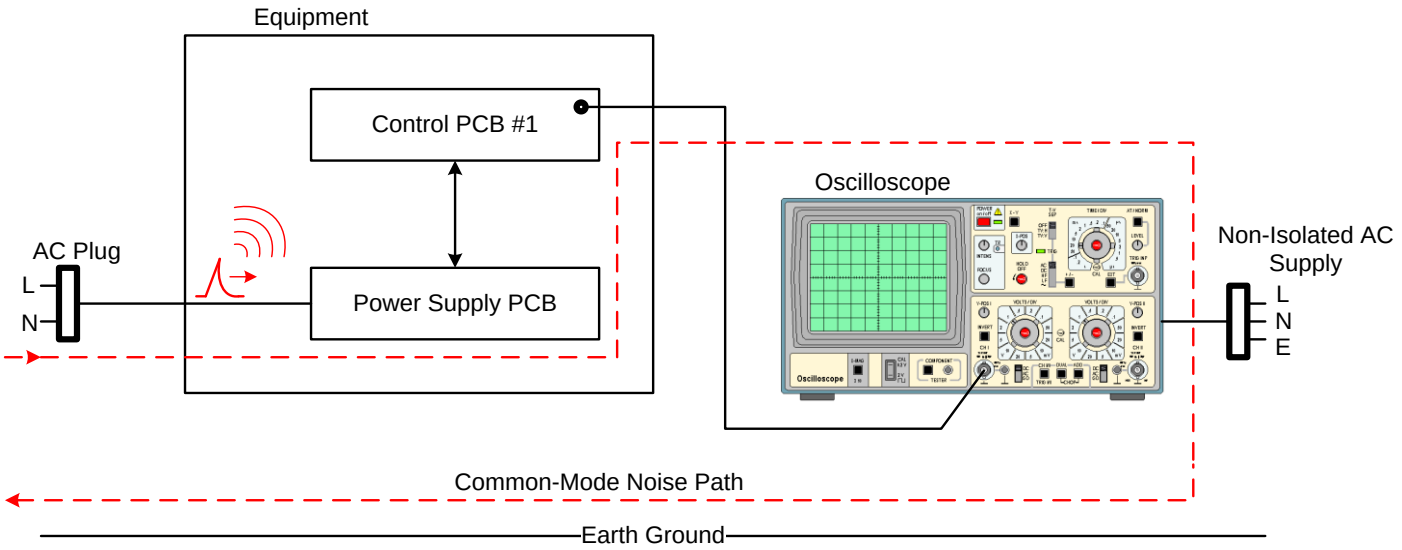
Most failures that occur in systems employing microcontrollers can be quickly identified if due cognizance is paid to the type of failure. You should identify the failure modes discussed in the previous section occurring in a system during or after EFT tests and their causes.

Once you understand the probable causes for the associated failures, take a step-by-step approach to debug the cause. Some tips for troubleshooting are:

1. When looking for a reset-related issue, probe the supply pins of the controller during the test and look for obvious reasons. Place a debug routine in the firmware that can visually indicate a reset.
2. In the case of a latch-up, observe whether the current drawn by the controller is beyond its normal ratings. If that is not the case, look for a firmware freeze by introducing debug routines.
3. For analog or clock-related issues, probe the associated I/O lines for noise or glitches. Pay attention to clock stretches if the communications to the device are hampered.
4. For flash/RAM corruptions, place a firmware debug routine such as a port pin toggling and monitor the pin status to check if the firmware flow is as intended. Read susceptible memory contents during and after the tests.

Note that it is advised to use oscilloscopes with isolated earth grounds. Failing to do so might cause the oscilloscope earth ground to shunt transient noise thus giving wrong readings. In a typical oscilloscope, the signal ground is connected to the earth ground internally. Refer to Figure 7.

Figure 7. Transient Noise Shunted Through the Oscilloscope



When you already have an equipment failing due to transient noise, try and fix the issues with the following:

- Corrections at system level such as optimization of system connectors and cable routing.
- Layout changes and usage of filters at hardware level
- Immunity techniques at firmware level

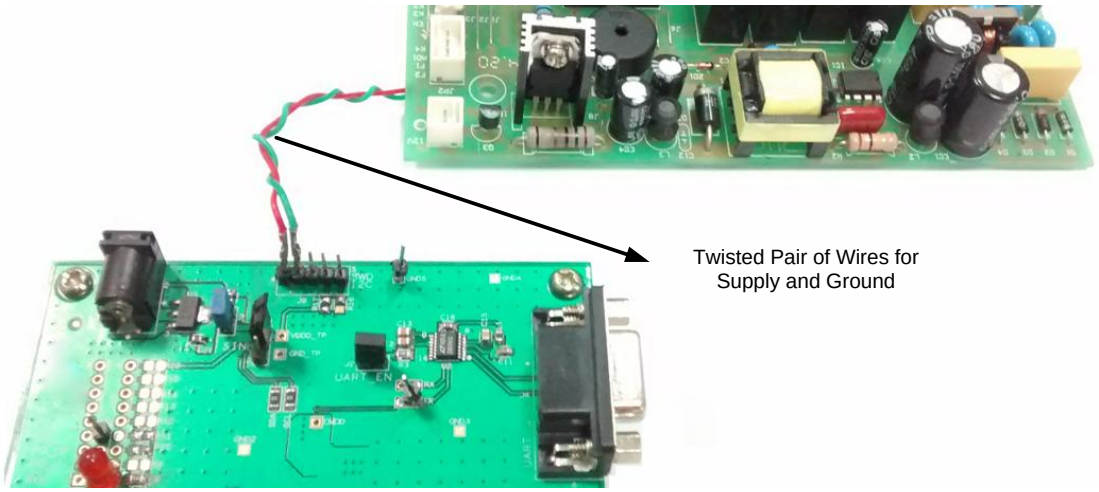
5.1 System

There are some basic considerations at the system level that, if not taken care of, can make the system vulnerable to transient-induced noise. Some common considerations that can help improve EFT immunity are:

5.1.1 System Connectors

Optimize power and signal connections for transient suppressions at the point of entry by keeping the wires as short as possible or by twisting supply and ground and/or signal and ground wires around, if they are long as shown in Figure 8. This will minimize the coupling between sensitive signals on the target board and external noise sources.

Figure 8. System Power Connections between the Target Board and the Power Board



5.1.2 System Cable Routing

Do not route filtered and unfiltered lines in a single cable bundle or close to each other. Keep the lines from noise generators such as relays and inductive loads away from sensitive lines such as low-level analog signals, and communication lines such as I^2C, SCL, SDA, and UART.

5.1.3 Soldering Practices

Employ good soldering of wires or components; improper or dry soldering will increase the inductance on the path. A good design should have the least inductance (and therefore, the least impedance) on the current path. Refer to electronics assembly standard IPC-A-610F for more details on the soldering practices.

5.1.4 System Testing

Place the system in its nominal operating condition for EFT tests. Test the target board in its end system as it will avoid any potential field failures. Tune the system prototype in its end system for EFT immunity. By adhering to the test specification, you can correctly evaluate the immunity performance of the equipment.

5.1.5 Supply and Signal Line Connections

If you have provision for connection of supply, ground and signal/control lines at multiple points on a board, it is not necessary that connection at any point yields the same performance. For example, in Figure 9, the supply and ground (GND) entry points are such that the decoupling and bulk capacitors are bypassed and the controller sees all the noise. The current loop formed is L1. The noise picked by supply or ground flows through the controller. This might even lead to a controller reset.

To avoid this situation, change the ground entry point to the board as shown in Figure 10. The decoupling and bulk capacitors come into effect here. Loops L2 and L3 are formed. Current through L2 flows through the controller and is the filtered current. The high-frequency noise takes L3.

Figure 9. Improper Power Entry Points Where Supply and Ground Bypass the Filter Capacitors and Feed the Controller Directly

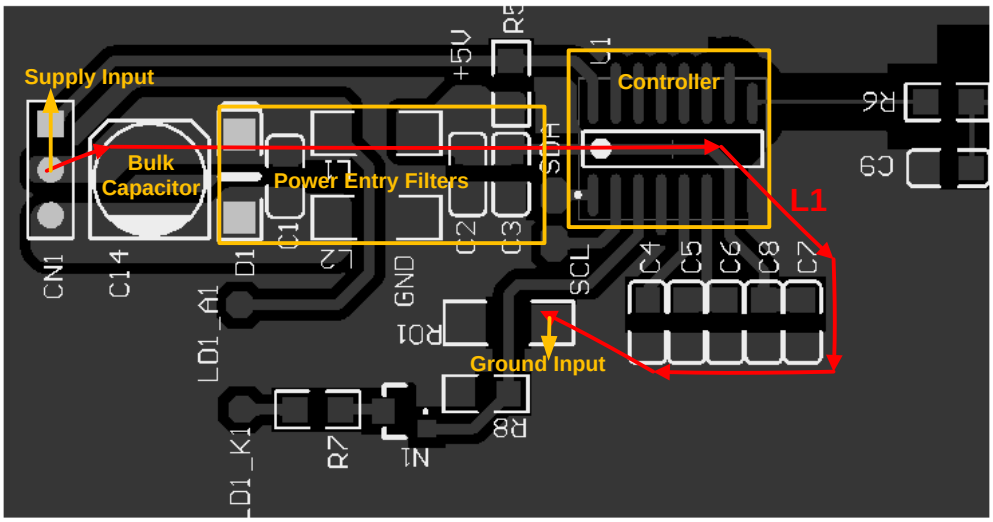
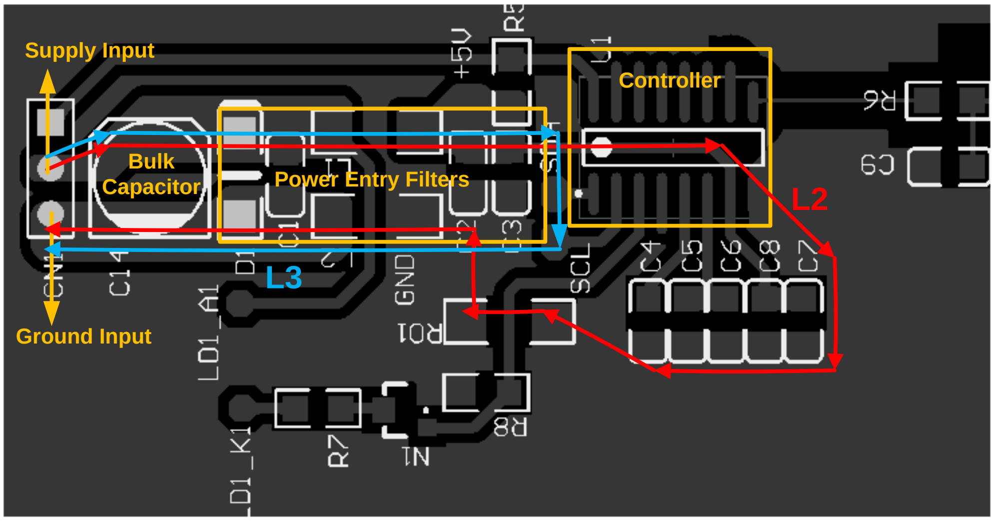


Figure 10. Corrected Power Entry Points Where Decoupling Capacitors Filter the Power Lines and Feed the Controller



5.2 PCB Layout

Review the PCB layout and pay attention to critical sections of the PCB such as below:

5.2.1 Decoupling/Bypass Network

A poor layout of the PCB can nullify the effect of decoupling/bypassing capacitors on the board. Consider the following for the decoupling network.

Do not place vias before the bypassing capacitors with reference to the point of entry of power supply to route the supply to different functional blocks. In such cases, the supply is routed off to the other part of the circuit even before the supply sees bypass capacitors, nullifying the effect of the bypass capacitors. Improper routing can bypass the decoupling capacitors and thus letting the controller see the supply and ground lines with coupled noise directly.

The supply and ground routing should be such that the decoupling capacitors should source power to the controller. Figure 11 and Figure 12 give an example of a bad and corrected routing. In Figure 11, L1 is formed between the supply entry point and the V_{DD} pin of the controller. Note that the supply path L1 bypasses the bulk and the decoupling capacitors. In Figure 12, the trace routing is such that supply passes through the bulk and decoupling capacitors (through the path L2) before it reaches the controller.

Figure 11. Improper Layout: Decoupling Capacitors Bypassed

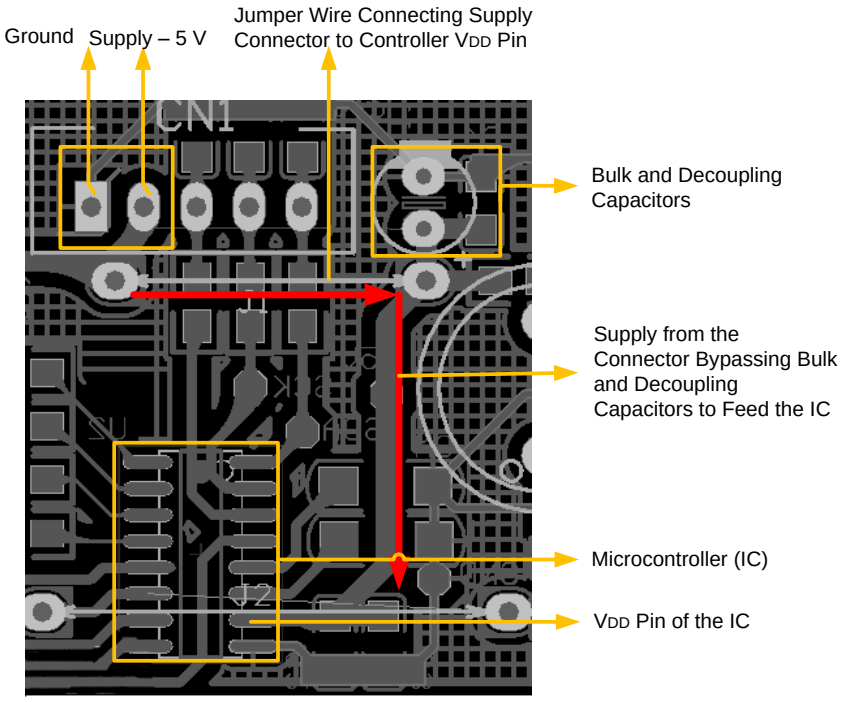
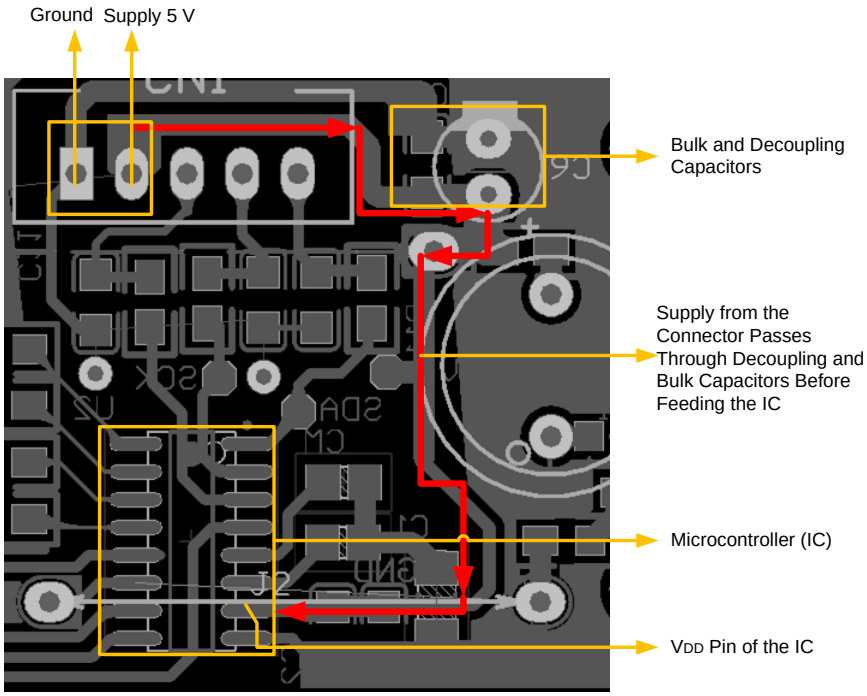


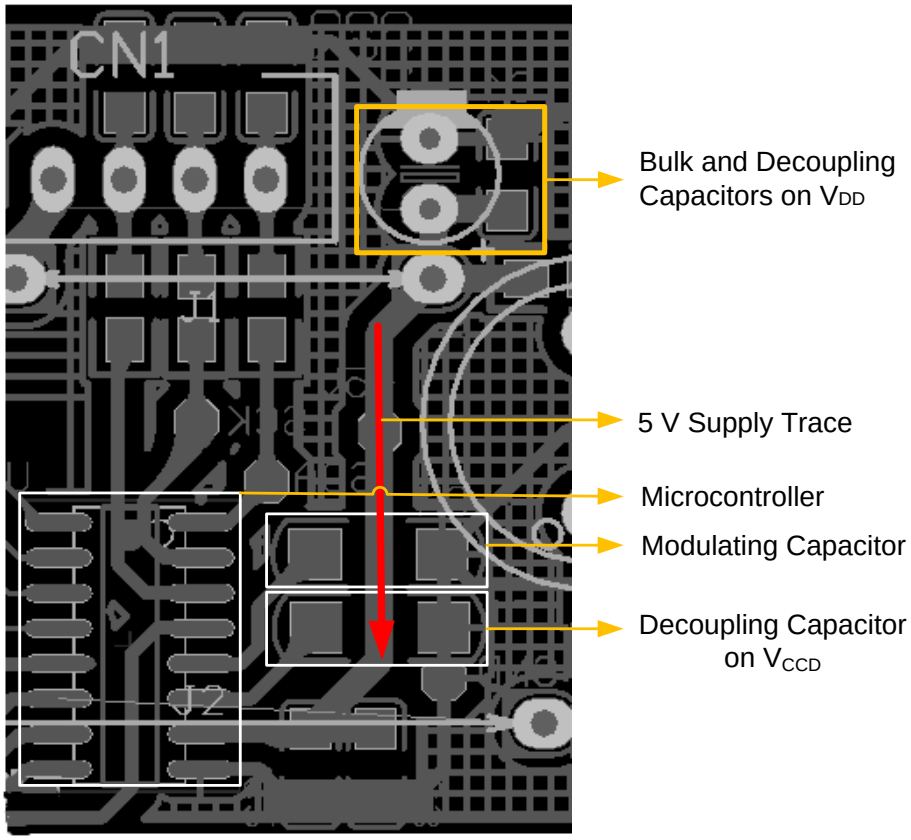
Figure 12. Corrected Layout: Decoupling Capacitors Effective



5.2.2 Signal Interaction

Check for any noisy signals such as unfiltered supply crossing sensitive signals or components.

Figure 13. Example Layout for Signals Crossover



In Figure 13, the 5 V unfiltered supply line passes under the decoupling capacitor for an internally regulated quiet supply and a modulating capacitor required for CapSense functionality. The noise on the 5 V supply can couple to both the regulated supply and the modulated signal.

If you find any mistakes in the layout similar to this, try correcting the PCB. Note that not all layout issues can be corrected on the existing board. For major layout improvements or once the corrected layout is tested and proven to be passing EFT tests, you will need to go for a board re-spin. Section Design Considerations and Mitigation Techniques capture the PCB schematic and layout recommendations in detail.

5.3 Schematics

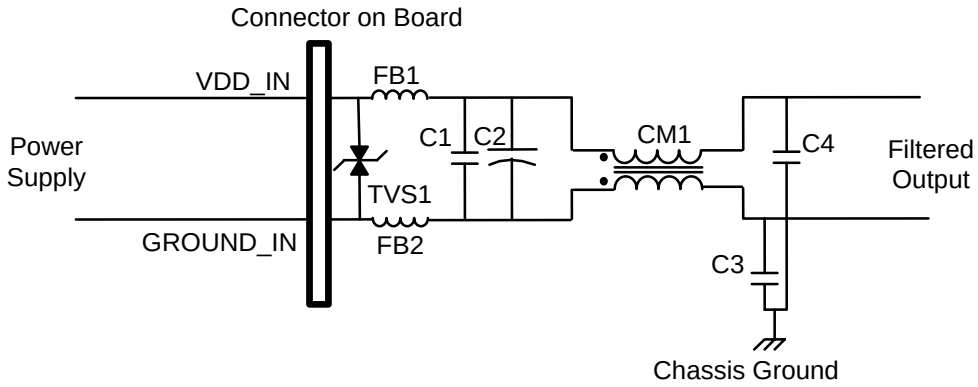
Use filters to improve the performance of a failing board. Filters for different parts of circuits of a board are given below:

5.3.1 Point-of-Power-Entry Filters

- TVS diodes (TVS1), example1: SMAJ6.0CA from Littlefuse
- Ferrite beads (FB1, FB2), example1: BLM18PG331SN1 from Murata
- Bypass capacitors (C1), typical range1: 0.1 µF – 1 µF
- Bulk capacitor (C2), typical range1: 10 µF – 100 µF
- Common mode chokes, typical range1: 2-10 mH; example1: 50475C (5000 Series) from Murata

- Bypass capacitors (C3, C4), typical range1: 0.1 nF - 1 µF

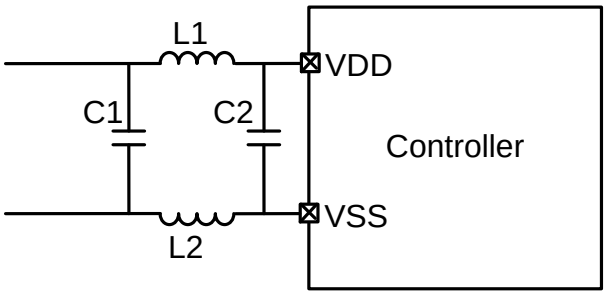
Figure 14. Point-of-Power-Entry Filter Schematics



5.3.2 Filters on Supply Pins of a Controller

- Filter capacitor (C1), typical value1: 1 µF
- Inductors (L1, L2), typical value1: 4.7 µH, example1: RL-1505 series from Renco, USA.
- Decoupling capacitor (C2), typical range1: 0.01 µF– 0.1 µF

Figure 15. Filters Near the Supply Pins of a Controller

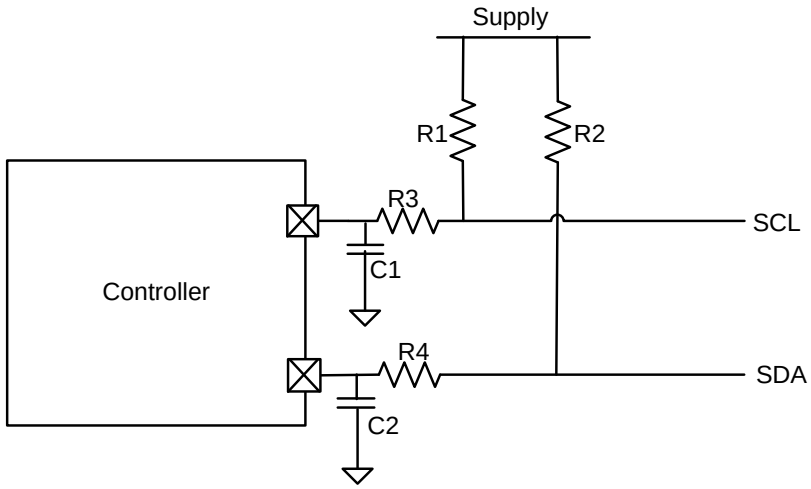


5.3.3 Filters on Communication Lines

5.3.3.1 I²C Lines

- Pull-up resistors (R1, R2), typical range1: 4.7 kΩ - 10 kΩ
- Series resistors (R3, R4), typical range1: 100 Ω - 330 Ω
- Filter capacitors (C1, C2), typical value1: 10 nF

Figure 16. Filters on I²C Lines

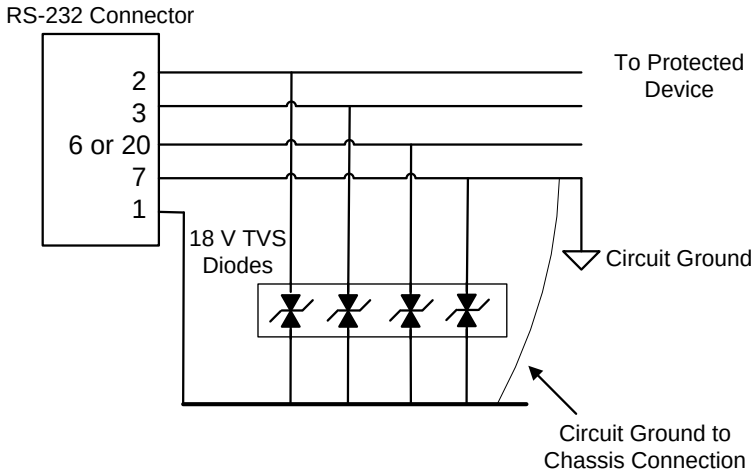


Note that similar filters are applicable to SPI lines as well.

5.3.3.2 UART Lines

- Galvanically isolated level translator. Alternatively, use an RS232 level translator and power the level translator with the filtered supply and ground.
- TVS diodes

Figure 17: TVS Diode Filters on UART Lines

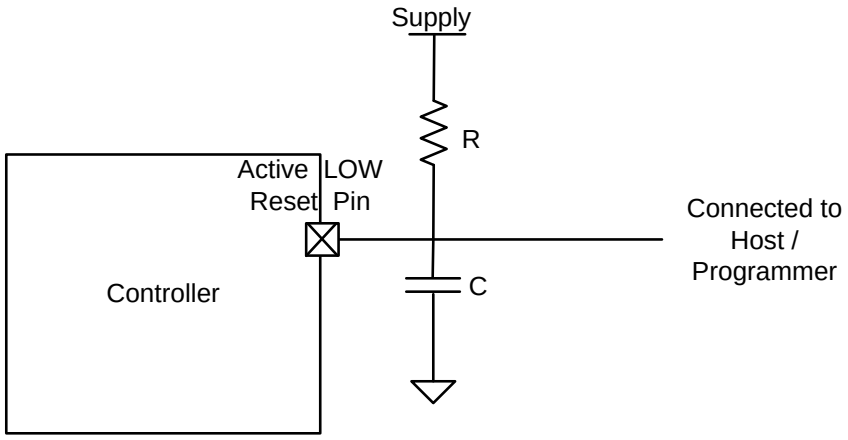


5.3.3.3 Filters on Reset and Interrupt Pins

- Pull-up Resistor (R), typical value1: 10 kΩ
- Filter capacitor (C), typical value[1]: 0.1 µF

[1] The typical values and examples are indicative only. You need to choose the type of filters and their values depending on your application. The Design Considerations and Mitigation Techniques section guides you in choosing filters and their values in detail.

Figure 18. Filters on Reset Pin



For active HIGH reset pins, use a pull-down resistor and a filter capacitor to ground. Similarly, pay attention to any alternate reset pins. Use similar filters for interrupt lines.

5.3.3.4 Filters on I/O Lines

- RC filters near the connector for signals leaving the board
- RC filter near the pin for incoming signals

Choose values depending on the frequency of the signal on the I/O lines such that the cut-off frequency is ten times more than the signal frequency.

Terminate the unused I/Os to supply or ground, preferably in the hardware (on board) via resistors of typical value1 of 10 kΩ.

Apart from fixes at system and hardware level, you can also have techniques in the firmware to detect the undesired effects caused by transient-induced noise and implement workarounds for them. Some of the useful techniques are captured in the Firmware Techniques section in this document.

Also, the power supply may not have good filters to mitigate common mode and differential mode noise caused by transients. However, it is often hard and risky to modify a power supply unless the board is redesigned. Therefore, this should be considered as the last step in fixing the EFT issues in a failing system if none of the other techniques works. Refer to the Power Supply Design Considerations section for more details.

6 Design Considerations and Mitigation Techniques

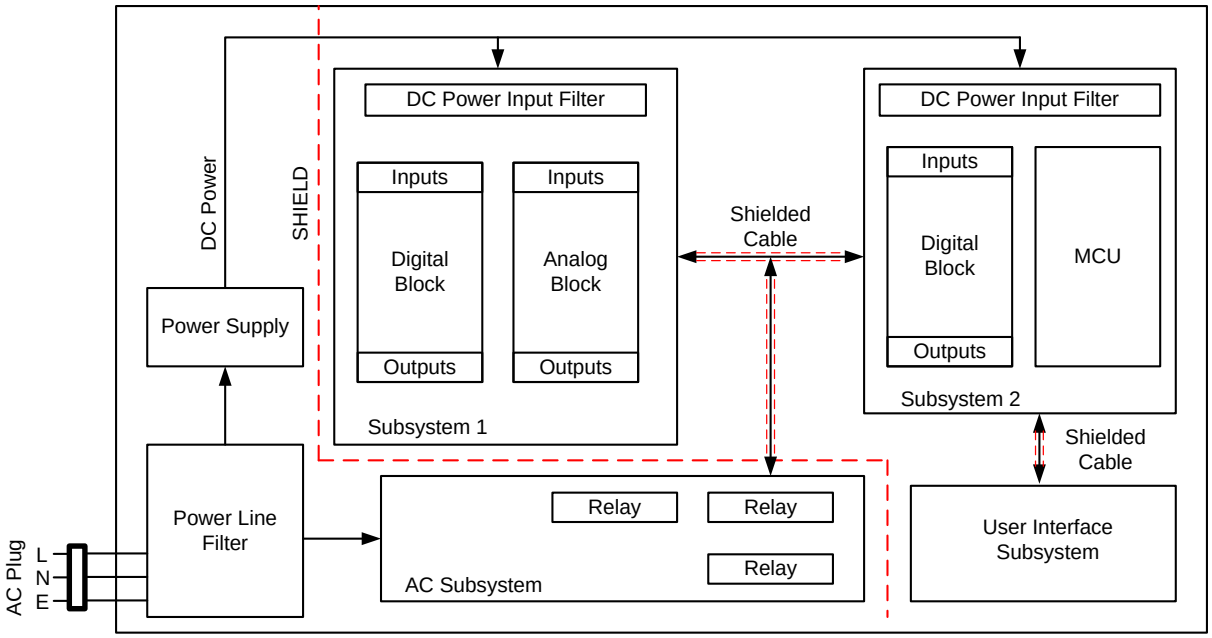
The techniques to mitigate the failures due to transient noise primarily include,

1. Reflect the transient energy back to the source by providing a least-impedance return path
2. Dissipate the transient energy before it propagates to sensitive circuits
3. Design firmware/software immune to transient-induced noise

The areas in which the mitigation techniques can be applied can be divided into different zones.

1. System-Level Considerations
2. Power Supply Design Considerations
3. Target Board Design Considerations
4. Firmware Techniques

Figure 19. Subsystems in a Typical Electronic System



The performance of equipment depends on the controller design and package, hardware design, system design, and firmware. Your first line of defense should be a good power supply. As far as the target board is concerned, aim for an optimized layout for transient-immunity. You can use filters to further improve the immunity.

System design is of utmost importance and hence give as much importance to it as any other design aspect such as hardware or firmware. A PCB with a good design can still fail due to system issues. In the following sections, system considerations and power supply design considerations are summarized. Target board schematics and layout guidelines are captured in detail. Firmware techniques for error-detection and recovery are summarized.

6.1 System-Level Considerations

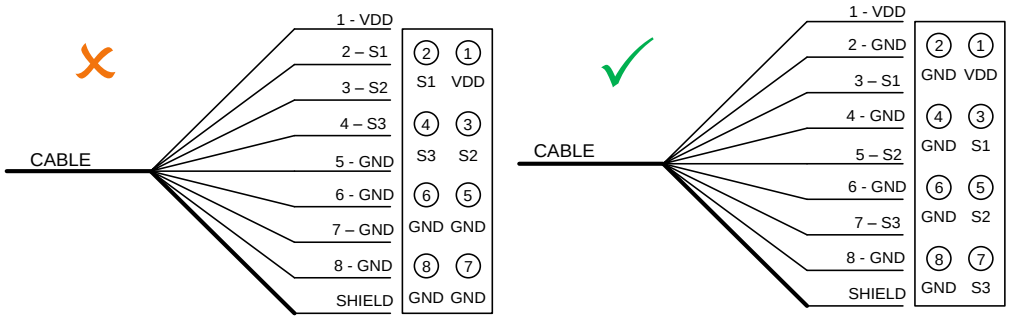
6.1.1 Placement of Subsystems and Subsystem Components With Respect To the Power Supply

A proper placement of subsystems (and components within a subsystem) is crucial for better immunity to transient-induced noise. Incorporate subsystems by logical grouping of functions in system designs Proper placement of these sub-systems makes trace routing simpler. While doing the placement, it is important to physically separate (or electrically protect all subsystems) from the power supplies. The physical separation of subsystems from power supplies can be achieved using separate PCBs. If it is not possible to physically separate the subsystems from the power supply, a shield (a metal enclosure) can be used to protect the subsystems from radiated transient-induced noise from the power supply area as shown in Figure 19. Conducted transient noise can be attenuated using appropriate filter topologies.

6.1.2 Power/Signal Entry and Cable Routing

Route power lines and signal lines separately, both between subsystems connected by cables and on a printed circuit board. Shield the critical signals that enter a target board from noise by placing them adjacent to filtered ground lines, as shown in Figure 20.

Figure 20. Power/Signal Routing in Cable



Protect power supply cables that are being routed to sensitive circuits by using ferrite bead filters. Refer to Target Board Design Considerations for more details.

6.1.3 Location of On-Board Connectors

Placing on-board connectors towards the edge of the boards not only gives sufficient mechanical stability to the board but also provides an easy way for the designer to effectively decouple in-bound transient-induced noise.

6.2 Power Supply Design Considerations

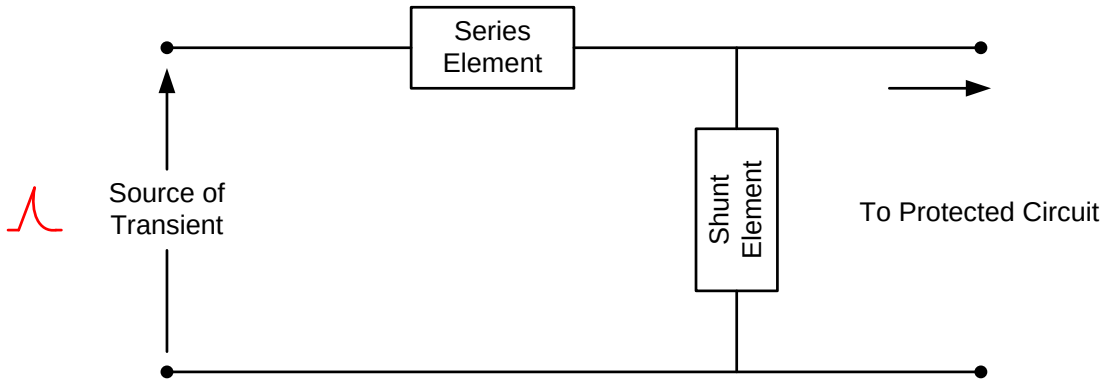
Transient suppression is often required at the AC or DC power entry point. Most power line filters can handle the low-energy, fast transients. Additional suppression can be achieved on the power line by using common-mode chokes made of ferrite core. Linear power supplies using transformers are more immune due to the galvanic isolation and series impedance offered by the transformer. With the use of switching-power supplies, power controllers can be susceptible to noise. This section provides considerations for power supply schematic and layout design for transient immunity.

Transient-protection networks should be used to suppress any incoming transients on the power supply. These networks should perform the following functions:

- Limit the voltage
- Limit/divert the current
- Dissipate the transient energy
- Respond fast and
- Survive the transient

The general configuration of a transient-suppression network is shown in Figure 21. The network consists of a series element and a shunt element. The series element limits the transient current through the shunt element. It is usually an inductor or a ferrite bead. It is important to note that the series element must exist in the network; if not, very high transient currents can flow through the shunt element. The shunt element is typically a non-linear voltage-clamping device. It has a very high impedance during normal operation to reduce the leakage current and a very low impedance when a transient occurs.

Figure 21. Transient-Protection Network



Some examples of series elements are given below:

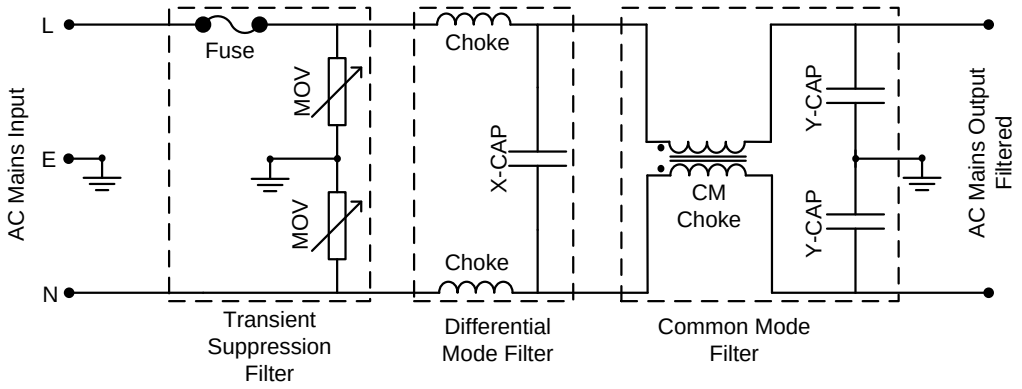
- **Common-mode chokes** are used to suppress common mode noise. This type of choke is made by winding inductors on the same core in bifilar configuration. These chokes theoretically offer infinite impedance to common-mode noise, and are the best defense against common mode-noise
- **Differential-mode filters** are typically inductors placed on each of the input lines to block differential-mode noise. Noise frequencies are relatively higher than signal frequencies and the differential-mode filters function as low-pass filters.

Some examples of shunt elements are given below:

- **Metal oxide varistors (MOVs)** are voltage-clamping devices. MOVs dissipate all the energy from the transient events and degrade gradually. However, they are rated to a few million transient events and are the best devices for protecting equipment from AC power line surges.
- **X capacitors:** Placement of line-line (or line-neutral) X capacitors is recommended on the AC side to avoid damage to rectifier diodes that are typically used in the AC-DC converters. X capacitors made of metallized film are recommended because they can recover quickly and to full functionality after a transient event. X capacitors also function as EMI suppression capacitors.
- **Y capacitors:** Y capacitors are placed between lie/neutral and the earth ground. These capacitors are used in powerline filters to decouple the common-mode noise (such as EFT) either generated within the equipment or propagated through the AC mains. However, Y capacitors need to be very reliable because they are critical to the safety of the equipment in use. The capacitance value of Y capacitors is usually low (less than 10 nF) to reduce the current when an AC voltage is applied and to reduce the stored charge in the case of a DC offset.
- **TVS diode:** Protection of downstream voltage regulators' input with a protection device is essential in an equipment running with the AC power. TVS diodes are commonly used on the DC power lines as they do not have the current-carrying capacity or the energy-dissipation capacity as MOVs. However, their response time is very small and are good for immunity against transients on the DC power lines. For more details on TVS diodes usage and selection, refer to Target Board Design Considerations.

Figure 22 shows an example transient-suppression network for an AC-powered equipment that uses all the above mentioned series and shunt elements.

Figure 22. Example Transient Suppression Network



A multi-layer PCB with power and ground planes provides a better transient immunity than a single-layer or double-layer board. However, note that, this is not always practical, especially in a board employing AC-DC converters. Typically, the AC side on the board is restricted to two layers to maintain insulation strength.

When designing (two or more layers) boards with AC-DC converters, maintain proper creepage distances. Place and route components by taking into consideration the source and sink characteristics at the circuit level. Avoid ground planes on the AC side, unless such copper pour is being used as a heat exchanger. You can use spark gaps on the PCB depending upon the severity of the expected transient. Connect protection devices to ground (or earth ground) in a way that minimizes series inductance.

6.3 Target Board Design Considerations

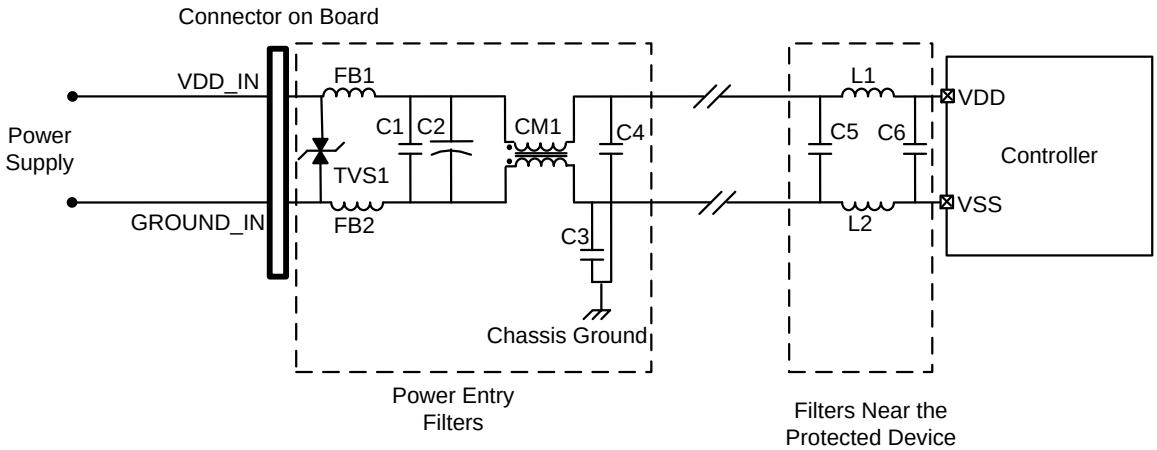
6.3.1 Schematics

The objective of filtering circuits on the target board is to protect the components on the board from coupled transient noise, preferably at the entry point. In the previous sections, you learned that the noise due to EFT is both common mode and differential mode. In this section, you will see some of the useful filter components and filter schemes to eliminate both types of noise on a target board.

Supply-Line Filters

Power supply lines to the board are the common entry points for transient noise. Ensure reliable filtering of the transient on the supply lines. Figure 23 is a schematic representation of relative placement of filter components on supply lines.

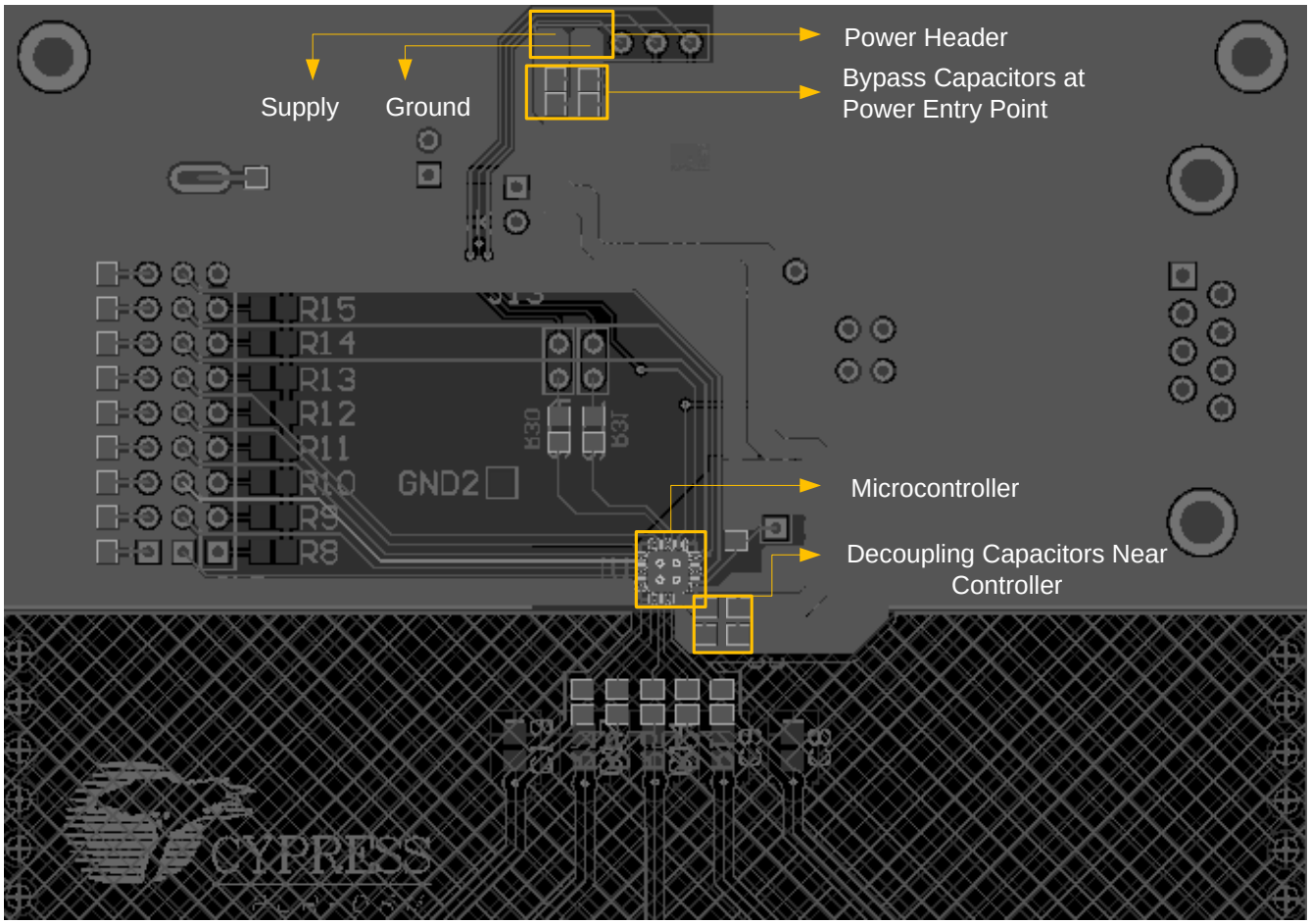
Figure 23. Schematic Representation of Relative Placement of Filter Components on Supply Lines



- FB1, FB2- SMT ferrite beads
- TVS1- TVS diode
- C1- Bypass capacitor
- C2- Bulk capacitor
- C3, C4 - Bypass capacitors to chassis ground
- C5, C6 – Filter/decoupling capacitors
- CM1- Common mode choke
- L1, L2- Inductors

In a PCB, where the controller to be protected and the connector on board are electrically close, you can place the filter components in the order shown in Figure 23. If the controller to be protected is far from the connector, place TVS diodes, ferrite beads, bypass capacitors, bulk capacitors, or common mode chokes near the power-entry points. Otherwise, noise may be coupled to other parts of the board by conduction or radiation; it is difficult to filter out the distributed noise. Place the inductors and filter/decoupling capacitors close to the device to be protected.

Figure 24. Board Design with Bypass Capacitors at the Power Entry Point and Decoupling Capacitors Near the Controller



Bypass, Decoupling, and Bulk Capacitors

The rule of thumb is that each functional block of the circuit has its own decoupling and bypassing components.

A bypass capacitor diverts unwanted common-mode noise from components or cables coupling from one area to another. This is essential to creating an AC shunt to remove undesired energy from entering susceptible areas, in addition to providing other functions of filtering. A decoupling capacitor breaks the coupling between different parts of the circuit to avoid errant signals and noise propagating between stages of the system. The decoupling capacitor also provides a localized source of instantaneous high-frequency current for devices and is useful in reducing peak current surges.

A bulk capacitor helps maintain a constant DC voltage and current level to components when all signal pins switch simultaneously under maximum capacitive load. It also prevents voltage dropouts due to di/dt surges generated by components.

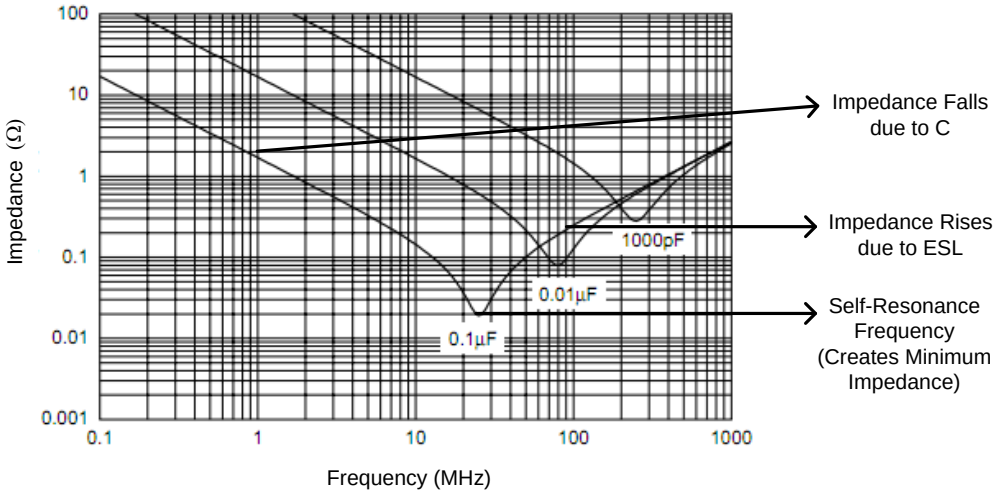
To select the bypass or the decoupling capacitors properly, determine the frequency bandwidth of the circuit to be protected. The bandwidth mainly depends on the operating frequency.

6.3.1.1.1 Equivalent Series Inductance (ESL) and Equivalent Series Resistance (ESR)

The effective bandwidth of a capacitor depends on its self-resonance frequency, caused by the presence of an ESL. Real capacitors are not ideal, so some inductance is always present that affects the capacitor impedance. The inductance comes from three sources: the capacitor itself, the interconnecting PCB traces and vias, and the lead frame inside the IC.

Because of this combination of capacitance and inductance, the decoupling network will, at some frequency, become resonant. As shown in Figure 25, below the resonant frequency, the decoupling network is capacitive and an effective bypass. Above the resonant frequency, the circuit becomes inductive and with its impedance increase with frequency, is no more an effective bypass.

Figure 25. Impedance - Frequency Curve of GRM15 Series Capacitors from Murata



Decoupling capacitors must supply high-frequency currents; therefore, they should be low-inductance, high-frequency capacitors. Ceramic capacitors are best suited for high-frequency operation, and they are used most frequently for bypassing/decoupling. A multilayer capacitor construction when combined with the surface mount technology can produce almost ideal high-frequency capacitors. Therefore, multilayer ceramic capacitors are preferred. Smaller packages generally have lower inductance.

Another important parameter that you need to keep in mind is ESR. This represents the impedance that the capacitor offers to the DC current. Choose capacitors that have the least ESR.

6.3.1.1.2 Voltage and Temperature Coefficients

Give due importance to the voltage and temperature coefficient specifications of a capacitor, that can greatly affect the device capacitance under normal operation conditions. A capacitor that is rated at 1 µF and max voltage of 6.3V, may be less than 0.1 µF at 5 volts. The voltage and temperature coefficient can vary greatly between packages. A 0805 package may have a better voltage coefficient than a 0603 package. Capacitors with a dielectric of NPO, X5R, and X7R (or the ones with better temperature coefficients) make excellent bypass/decoupling capacitors and are available in values between 100s of pF to several µFs.

Note: It is good practice to check the datasheets for values of capacitors, specifically the working voltage and the DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the DC bias is a significant percentage of the rated working voltage.

A good policy is to select the highest capacitance in the smallest package. Some wide-bandwidth systems may require more than one capacitor used in parallel due to the described frequency limitation. For example, PSoC devices may operate at different frequencies to decrease power consumption. Place smaller capacitors in parallel with larger capacitors to increase the frequency response range. Use at least one decoupling capacitor for each power pin of each IC on the board.

Refer to the device data sheet of the specific controller for supply decoupling requirements. Typical values of decoupling capacitors for a PSoC 4 device are:

- For each V_{DDIO} pin, provide a 0.1-µF ceramic capacitor.
- For each V_{DDD} and V_{DDA} pins, provide a 0.1-µF ceramic capacitor and a bulk of 1-µF ceramic capacitor.
- For regulator output, connect 1-µF ceramic capacitor each between V_{CCD} and V_{SSD} and between V_{CCA} and V_{SSA} using as short a trace as possible.
- For internal bandgap, provide 1-µF ceramic capacitor between V_{REF} and V_{SSA}. This is optional.

Refer to the device datasheets for the recommended decoupling capacitor values.

Place smaller values of decoupling capacitors closer to the controller as they can respond to high frequency current requirements faster.

LC Filter

The low-pass filter is the most commonly used filter circuit to suppress transients. A simple low-pass LC filter, which is a second-order filter, is represented in Figure 26.

Figure 26. LC Filter Network

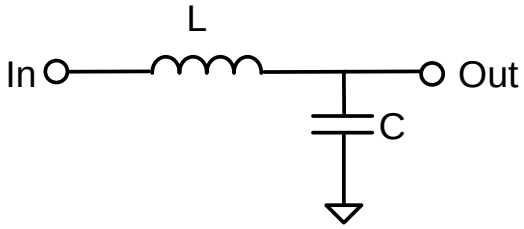


Figure 27. Frequency Response of an LC Filter

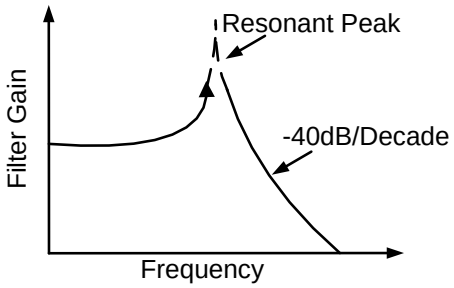


Figure 27 shows the frequency response of a low-pass LC filter. Note that the attenuation rate is 40 dB/decade. An LC filter is preferred to RC filter for the following reasons:

- The attenuation rate is 40 dB/decade for an LC filter, whereas it is 20 dB/decade for an RC filter.
- Resistors offer impedance even to a DC current, which is not desired and cause dissipation losses. The DC resistance of inductors is generally less than that of resistors and offer required impedance only at the frequency of interest.

Transient noise can propagate on both supply and ground. Therefore, it is recommended that you have inductors on both supply and ground lines along with capacitors to form an LC filter as shown in Figure 23 (L1, L2, and C6). Inductors block the high frequency transient noise; the shunt capacitors divert the high-frequency noise to the source.

From the frequency response of EFT test waveform (see Figure 3), you can see that most of the energy is concentrated in the low MHz range and at the burst frequency (5 kHz). As it propagates down to the target board passing through the AC-DC power supply, the transient-induced noise may also have components in the 100s of kHz range. The inductance and capacitance values should be such that the cut-off frequency of the LC filter is one decade lower than the noise frequency. A filter with the cut-off frequency chosen for transient pulse-frequency components helps in attenuating the average transient energy, thus improving the immunity.

Wire-wound inductors serve as EMI filters and are useful to about 50 MHz. The cores on which the wires are wound can be of two types, air and magnetic. Magnetic inductors are made from two types of core material: iron and ferrite. Ferrite core inductors are better than air-core or iron-core for transient noise immunity as they have a higher loss factor. Ferrite core also provides a high current capacity with lower wire turns. Shielded or toroidal inductors are preferred as they confine their magnetic and electric fields within a limited space thus avoiding interference.

Another important parameter while selecting inductors is the current rating. If the current through the inductor in your application exceeds the rated current, the inductor might get damaged. The important current parameters for an inductor are saturation current (Isat), RMS current (Irms), and DC current (I_{DC}).

It is very important to consider the definitions and conditions at which the above current values are rated by the manufacturers of an inductor. For instance, Isat from one manufacturer may be the current at which inductance reduces by 5 percent whereas it is 20 percent for inductor from another manufacturer.

Place LC filters close to the supply and ground pins of the controller. If there are constraints in the layout, make sure that the electrical distance and essentially the total impedance between supply and the filter component, and ground and the filter component are same.

TVS Diodes

Clamping devices protect circuits from high transient voltages. Under normal conditions, clamping devices have a very large resistance in parallel with a capacitance. When the surge voltage exceeds the breakdown voltage, clamping devices dynamically reduce their resistance to maintain a constant clamping voltage. Polymer and metal oxide varistor, zener diodes, and transorbs (or TVS diodes) are all clamping devices. The most common ones used for transient suppression are MOVs and TVS diodes.

TVS diodes combine a low clamping voltage with a low resistance and a fast response time. These devices provide additional protection for controllers that usually contain internal transient-protection circuits. Knowledge of the controller's internal transient protection circuit can be beneficial in selecting external TVS diodes. External TVS diodes provide a higher level of transient protection because internal circuits might not be rated as required. The TVS diode's main function is to limit the current through the protected circuit by decreasing the impressed transient voltage.

A unidirectional TVS diode is suited for protecting circuit nodes with unidirectional signals; for example: incoming serial communication clock lines into a board. A bidirectional TVS diode is best for protecting nodes with bidirectional signals, where the voltage level swings above and below the reference node; for example: AC output voltage of a step-down transformer.

Select a TVS diode depending on the polarity of the signal expected on the node. Choose a diode with a working voltage that is greater than the operating voltage of the system. The clamping voltage of the diode chosen must be less than the specified transient voltage for the protected circuit while the breakdown voltage must be above the operating voltage of the system.

TVS diodes with a lower parasitic capacitance react faster to transients. In addition, signal integrity can be maintained if the protected signals are high frequency in nature. Hence, select TVS diodes of low parasitic capacitance.

Ferrite Beads

Ferrite beads suppress high-frequency noise in electronic circuits. They can remove the noise energy by converting it into heat energy.

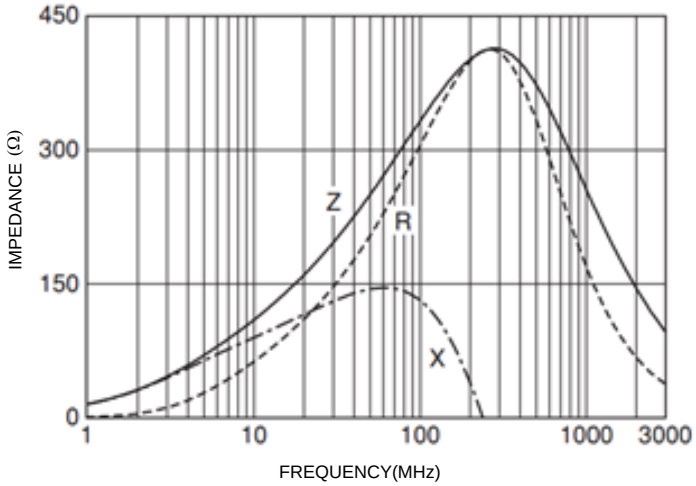
Ferrite beads are generally useful to suppress noise over MHz range. Since the noise due to EFT on the DC power lines comprises of frequencies both in MHz and in several kHz range, it is often difficult to choose ferrite beads which offer enough impedance (50 Ω – 100 Ω) at all noise frequency component ranges. Therefore, for better EFT immunity, it is recommended to use inductors for LC filters as explained in the LC Filter section. Use ferrite beads at the power entry point on the power cables, which can filter out transient noise in MHz range and coupled RF noise. Other frequency components can be filtered by specific filters such as LC filters, bypass capacitors on the board.

A widely used parameter for a ferrite bead is “impedance at 100 MHz” (unit: Ω @100 MHz). Apart from that, you should also know its overall impedance-frequency characteristics, especially in the frequency range of interest.

Figure 28 gives an example with a ferrite bead (part number BLM18PG331SN1 from Murata). Z stands for its impedance, which is a vector sum of R (resistance) and X (reactance). The impedance is 330 Ω at 100 MHz, and it becomes the highest at about 300 MHz.

When selecting a ferrite bead for your application, it is a good practice to let the frequency at which the highest impedance comes out be central in the noise frequency range.

Figure 28. Impedance-Frequency Characteristics of a Ferrite Bead (BLM18PG331SN1 from Murata)



Other parameters to note while selecting ferrite beads are:

- Rated current – this is determined by the wire size or gauge used inside the inductor
- Saturation current – this is a function of the ferrite material, It is the current when flowing through the coil beyond which it is unable to set up any more magnetic flux in the ferrite
- DCR max – this is the maximum DC resistance of the coil, useful in determining winding or resistive losses

Place ferrite beads at the point of entry to suppress any incoming noise at its source. Ferrite beads are also used as interference filters for electronic cabling.

Common-Mode Filters

Common-mode filters/chokes are designed to filter out the common-mode noise. Because a significant portion of the noise due to EFT is common mode, these filters can be used to improve the immunity to EFT.

The differential-mode current, flowing in opposite directions through the choke windings, creates equal and opposite magnetic fields, which cancel each other out. This results in the choke presenting zero impedance to the differential mode signal, which passes through the choke unchanged.

The common-mode current, flowing in the same direction through each of the choke windings, creates equal and in-phase magnetic fields that add together. This results in the choke presenting a high impedance to the common-mode signal, which passes through the choke, getting heavily attenuated. The actual attenuation (or common-mode rejection) depends on the relative magnitudes of the choke impedance and the load impedance.

Similar to inductors, you must consider parameters such as current rating and DC resistance before selecting the component for your application. Another important parameter is the leakage inductance. This determines the degree of differential-mode inductance present. Leakage inductance provides differential-mode filtering. Too much leakage inductance, however, can cause the common-mode choke to saturate at a low value of AC-power current, and it is an undesirable characteristic.

If you have a chassis ground in your application, you can also use chassis bypass capacitors from the supply to chassis and board ground to chassis to provide a low-impedance path to common-mode noise.

6.3.2 Signal Line Filters

6.3.2.1 Communication Lines: Filters on I²C/SPI lines

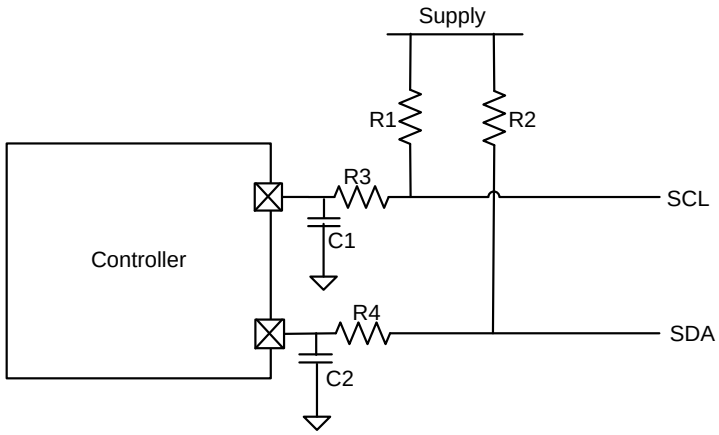
Place the following filter components on I²C/SPI lines:

- **Pull-up resistors on I2C/SPI lines:** The pull-up should be designed based on the series resistance, trace capacitance, and clock speed. Refer to the I2C specification for guidance. Choose a value between typically 2.2 kΩ and 10 kΩ, depending on bus parameters.

- **Series resistors of 100-330 Ω on I2C/SPI lines:** The series resistor forms a low-pass filter with the trace and pin parasitic capacitance, and can filter out the high-frequency noise. Place the series resistor close to the pin. When I2C/SPI line switches from HIGH to LOW, the trace capacitance will take some finite time to discharge through the series resistor. In addition, when the I2C/SPI line switches from; LOW to HIGH, the trace capacitance and pin capacitance should charge to the supply voltage though the series resistor. The pull-up resistance and the series resistance form a potential divider and affects the V_{OL} level of the I2C/SPI lines. Therefore, it is important that you choose series resistors and pull-up resistors keeping all these factors in mind.

- **Filter capacitors on I2C/SPI lines:** This forms a low-pass filter along with the trace and pin parasitic capacitance with a series resistor, and can filter out the RF noise. However, this may affect the signal integrity of I2C protocol. Therefore, care must be taken such that the rise time and fall time delay caused by additional capacitors do not violate the I2C protocol.

Figure 29. Filters on I²C Lines

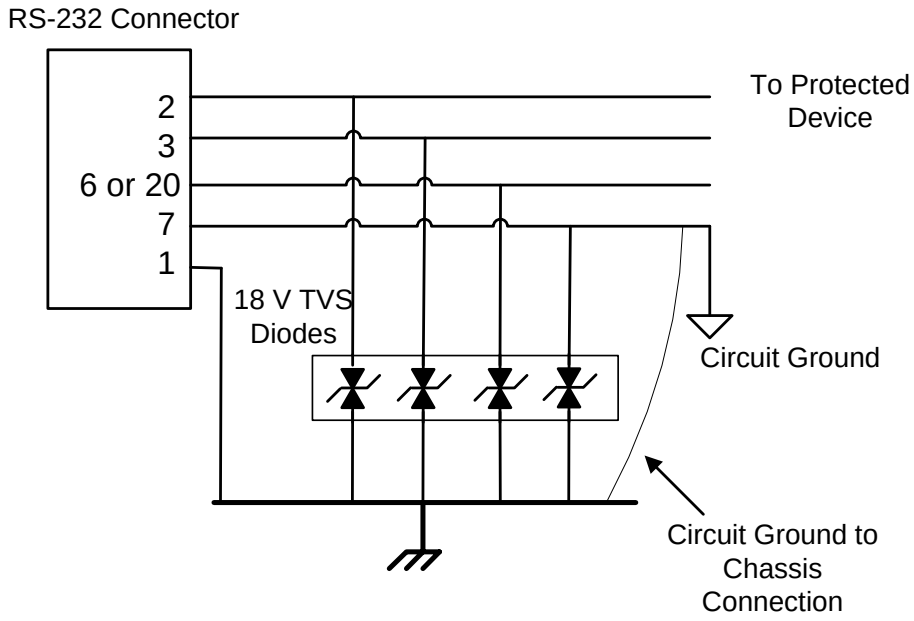


6.3.2.2 Communication Lines: Filters for UART

Use a galvanically isolated level translator. If it is not possible to use a galvanically isolated level translator, use an RS232 level translator IC for UART communication. Make sure that the filtered supply and ground power the level translator.

Figure 30 shows an RS-232 interface protected against transient overvoltage with four bidirectional TVS diodes. Note that even the ground conductor is protected with a TVS diode. This is often required because the internal connection between the circuit ground and the chassis ground might not be located at the point of cable entry and may not have a low inductance.

Figure 30. RS-232 Input Protected Against Transient Overvoltage with Four TVS Diodes.



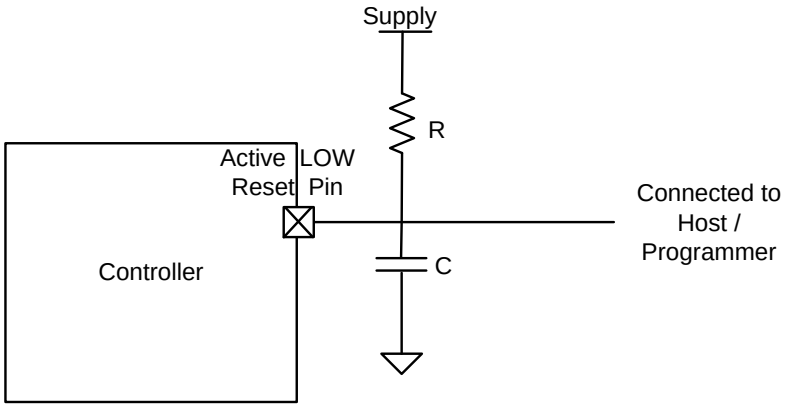
6.3.2.3 Reset and Interrupt Request Inputs

You must protect resets, interrupts, and any other critical control inputs that can change the operating state of a digital device against false triggering due to fast-rise-time transients by adding a capacitor or RC network as shown in Figure 31. PSoC devices incorporate an internal pull-up resistor with ~4.7 kΩ resistance on reset lines.

Edge-triggered interrupts are, as mentioned earlier, susceptible to noise. If possible, use level-triggered interrupts or sample the interrupt pin inside the ISR. Use proper line terminations for interrupt lines to reduce reflections, ringing, or overshoot, which can cause false interrupts.

Reset can be active LOW or active HIGH. Place an RC filter close to the device on reset lines on active LOW reset pins. For active HIGH reset pins, pull down both the resistor and the capacitor to ground. Make sure that you have proper filtering on alternate reset pins as well.

Figure 31. Filters on Reset Lines



6.3.2.4 I/O Lines

Transient noise can either be directly injected into I/O lines such as control lines or the noise when injected on power lines can propagate to the I/O lines. Therefore, it is important to protect these lines by using the following means.

- Using I/O line bidirectional TVS diodes
- Using low-pass RC network such that the cut-off frequency is 10 times more than the frequency of signal on the I/O line to ensure that the signal is not attenuated.
- Shielding input cables with braided or solid shields

For the I/O lines carrying signal to the controller from outside of the board, place an RC filter close to the controller pin. The TVS diode should be placed at the entry point near the connector. For the I/O lines carrying signal to outside of the board, place a low-pass RC filter at the connector at which the I/O lines leave the board.

Terminate the unused I/O lines to ground or supply through resistors of typical value of 10 kΩ.

How to Select Series Resistors

As resistors provide a voltage drop at DC only, small values (< 100 Ω) in series are more practical in applications. The resistor's end-to-end capacitance limits its impedance. For example, a 1-MΩ resistor at DC is not the same at 100 MHz. To improve transient immunity, use carbon or metal oxide resistors because they provide a low value of parasitic capacitance and inductance and can withstand short pulse overloads.

Some typical resistor types are the following:

- Surface Mount Technology (SMT) and thin-film resistors are good for high-frequency response but not for transient protection. They are composed of a thin metal layer (a few hundred angstroms), which limits the device's ability to withstand the EFT energy. In addition, EFT voltage tends to arc across SMT.
- Metal film resistors are suitable for high-power density or high-accuracy circuits but not for transient protection.
- Wire wound resistors are suitable for high-power handling circuits but not for high-frequency-sensitive circuits due to large inductance. Also, they are not available in surface mount form (without molding), making them unsuitable for applications with size and weight limitations.
- Foil-based resistors offer the best precision and stability and can better withstand EFT than thin-film and thick-film resistors. Their main disadvantage is a limit on the maximum value of approximately 150 kΩ.

Getting a system EFT test qualified might be an iterative process. It is recommended that you have footprints for the filter components on board and start the EFT tests with minimal components such as bypass and decoupling capacitors populated on the board. In order to improve immunity further, you can try using filters such as LC, common mode chokes, TVS diodes, and ferrite beads sequentially or combine more than one. Use bulk capacitors when the power supply design is not very good and you expect the output of the power supply to have ripples.

6.3.3 PCB Layout

You need to keep in mind two basic principles before designing a PCB for good transient immunity.

The first is that currents should be returned to their source as locally and compactly as possible, that is, through the smallest possible and least-impedance loop area. This applies to both transient noise and desired signal current.

1. The transient noise as discussed in the Failure Modes chapter can propagate through signal, ground, or any signal/control lines. The PCB layout should be such that there are short low-impedance paths for transient currents to return to the source at the point of entry of the noise. If the path is not low-impedance, the noise interferes with circuit elements including controllers, traces and components, and affect their functionality.. Short and low-impedance paths are also necessary to return the noise generated by circuit elements such as microcontroller or oscillators.
2. Keep the signal-carrying loops also small because high-frequency current carrying loops radiate. The radiated energy is proportional to the loop area. This radiated energy interferes with other signals and add to the effect of transient noise on these signals. Signals through larger loops are more susceptible to radiated energy.

The second is that a system should have only one reference plane. If a system has two reference planes, it causes signal integrity issues, which can be amplified by the transient noise. More than one reference plane also creates a dipole antenna that radiates energy. A single reference plane is not achieved if the reference planes and the connections of the reference planes do not have low impedance.

Floor Planning

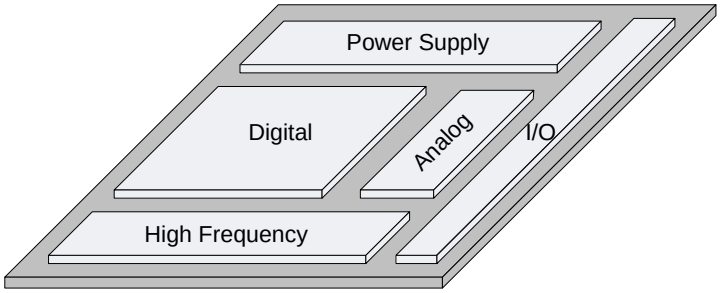
As already discussed previously how important it is to have proper subsystem placement to avoid cross coupling, floor planning is equally essential to keep the noisy circuits from affecting the noise-sensitive circuits on a PCB.

The rule of thumb is to divide a PCB by functional groups: analog, digital, power supply, and I/O. Try to avoid cases in which the traces of one group cross over to another group unless it is an interface trace between the groups. Keep each section as compact as possible. Partition the PCB into functional areas (sections), and place in each area only the corresponding components. Figure 32 shows an example of such partitioning.

There are two basic criteria for partitions:

- **Functionality-based:** Power circuitry, analog circuitry, digital circuitry, or I/O block
- **Signal-based:** High-frequency, low-frequency, high-power, or low-power

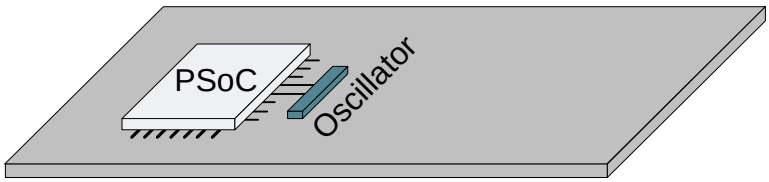
Figure 32. Typical Layout of the Board Functional Groups



Place the high-frequency circuits, which output signals from the PCB, close to the corresponding I/O connectors. To minimize coupling into I/O interconnects, place circuits with high-frequency signals that do not leave the PCB farther away from the I/O connectors. Try to keep all high-frequency signals on the same board. Minimize the length of high-frequency traces as much as possible. If high-frequency signals go outside the board, use transmission lines to attenuate reflections and radiations.

Keep oscillators and clock-generating ICs away from I/O traces and close to the chips they service, as Figure 33 shows. It is recommended that you use a guard ground ring around this circuitry or better yet use a shield casing called Faraday cage, which is connected to the board ground in order to avoid radiation and susceptibility. If a guard ring is used, connect the ring to ground at multiple points. Always choose the lowest clock frequency and the slowest rise and fall times for digital signals that meet system requirements. Filter (series terminate) the output of clock drivers to slow their rise and fall times and to reduce ringing.

Figure 33. Proper Placement of Oscillator



Carefully route the digital clock connections on the PCB. Try to place all clock traces adjacent to a ground plane. Do not place traces, other than ground, under crystals or any other inherently noisy circuits. Route the critical nets, such as clocks or data strobes, next to ground traces or ground plane.

Place voltage regulators and power supplies close to the power entry point. Do not route power signals parallel to high-noise traces.

Keep susceptible components (for example, a controller) away from the PCB edge. Place connectors on board edges. Try to place all connectors on one edge of the board. Place the interfacing components (I/O circuits) and their corresponding connectors close to the board edge.

Floor planning minimizes the propagation of transient noise and helps returning the noise to the source in the shortest path.

Trace Routing

Trace routing is important to avoid crosstalk among signals. It is also important because sensitive signals should be protected from radiated and conductive coupling. The transient noise that propagates through supply, ground, or signal/control lines can couple to sensitive parts of the circuit such as the reset line.

Crosstalk between signals is usually one of three types: conductive, capacitive, and inductive. To prevent crosstalk, the following design and layout techniques are useful during PCB layout:

As discussed in the previous section, floor planning helps in minimizing cross talks.

1. Minimize physical distance between components within any functional group during placement.
2. Minimize parallel routed trace lengths. This increases capacitive coupling. If the signals have to cross over each other, make sure they cross at a 90-degree angle to minimize the capacitance formed between these signals.
3. Provide sufficient spacing between traces to minimize inductive coupling.
4. Reduce the signal-ground reference distance separation. This forms distributed capacitance, which acts as bypass capacitor for high-frequency noise. Note that transient noise due to EFT can propagate through ground. So, reduce the signal-ground reference distance only if this ground is not the return path of the transient noise.

Trace routing is not limited to routing on PCB. As discussed previously, it is also important to protect the signal lines running off the PCB from cross talks.

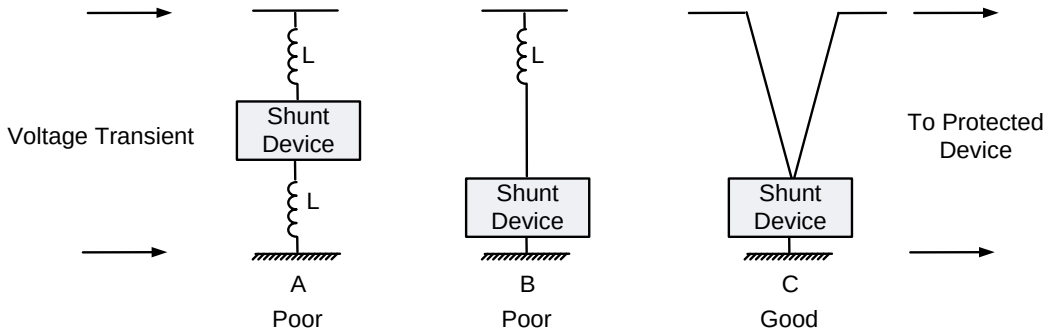
Refer to *Routing Analog and Digital Signals section* in AN57821- PSoC® 3, PSoC 4, and PSoC 5LP Mixed Signal Circuit Board Layout Considerations for more details on these techniques.

Trace Impedance

Every trace has a series inductance distributed along it and capacitance between the trace and the return path of the signal on the trace both of which increase the signal rise time. Every trace also has resistance, which reduces the signal amplitude. Therefore, every trace resembles a distributed RLC circuit to the circuit that is driving it. In most cases, the impedance is “uncontrolled.” This means that the distributed inductance and capacitance can (and probably do) vary in value from point to point along the trace. Therefore, the AC impedance varies from point to point along the trace.

You must ensure that the total impedance on the return path for noise and signal must be the lowest. The distributed inductance and capacitance can both be good and bad for transient suppression. An example of disadvantageous distributed inductance is when it is formed between a protected device like a controller and the decoupling capacitor. The trace inductance limits the bandwidth of the effectiveness of the shunt elements such as decoupling capacitors and TVS diodes. This also blocks any surge current flow from the decoupling capacitor to the controller when there is an instantaneous current requirement. Therefore, the layout should be such that these shunt elements have the least series impedance. Figure 34 shows good and bad layouts for a shunt device.

Figure 34. (A) and (B): Improper Shunt Element Layout; (C): Proper Shunt Element Layout



Distributed inductance and capacitance can affect the rise and fall time and therefore the signal integrity. However, distributed capacitance is also helpful in bypassing the high-frequency noise.

In summary, you must analyze the effect of distributed inductance and capacitance in a circuit and design accordingly.

For a single-layer PCB, use thick traces, larger SMT packages when traces are running beneath SMT packages, and thicker jumpers to connect the traces passing through the PCB.

Refer to AN57821- PSoC® 3, PSoC 4, and PSoC 5LP Mixed Signal Circuit Board Layout Considerations for more details on the calculation and effects of trace impedance.

Grounding

One of the most important design considerations for incorporating transient-suppression techniques within a PCB is providing optimal ground or supply and/or signal return loop control. Ground loops are a major contributor to the development and propagation of RF energy. This loop develops a voltage difference between two devices regardless of whether an inductance exists between these points. Inductance in a transmission line causes magnetic coupling of the RF current to occur between the source and the affected circuit, thereby increasing RF losses on the return path.

6.3.3.1 Ground Planes

At a PCB level, if your application does not have high-speed digital logic in MHz and sensitive analog circuits such as the ones dealing with low-level analog signals, having a single ground plane is sufficient. If otherwise, splitting the ground planes is beneficial but additional layers may be expensive for a given design. Even with two-layer boards, it is possible to provide partial planes under sensitive analog sections of the design. Whether you use ground planes or not, make sure that the return paths are as direct to the power supply as possible. Remember that ground planes may not improve your design if the path to the supply is not low-impedance, or the plane is too fragmented. Do not rely on copper fill in case of two layered boards; it can lead to narrow high-resistance paths that are not obvious without careful inspection. Route the ground with traces and supplement it with fill. Using a ‘star ground’ in a system is one method of preventing ground currents affecting noise-sensitive circuits. Star ground, also called reference ground, is the one point in a system where the ground planes of various domains such as analog, digital, and power connect.

Star ground connection can be done by using moats, logical partitioning or by placing cuts/voids in ground planes.

Usage of Moats: You can use moats in the ground plane to separate analog, digital, and power portions of the PCB. A moat is a notch in a polygon trace that allows you to eliminate common return paths. Moats should be at least 0.7-mm wide to prevent capacitive coupling. Figure 35 shows the proper use of moats.

Logical Partitioning: You can use only one ground plane and have a logical partition of the PCB into analog, digital, and power sections as shown in Figure 36. Route signals only in the corresponding section of the board (on all layers).If this is done properly, switching and transient noise on power lines do not couple with other circuits. You need to analyze the current flow and trace the current loops carefully before partitioning the ground plane.

Figure 35. Moat Use Example

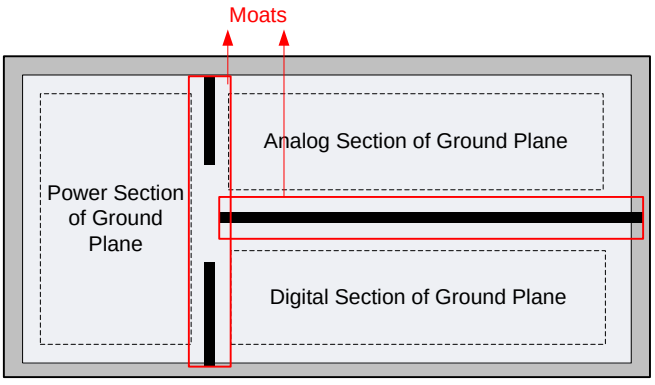
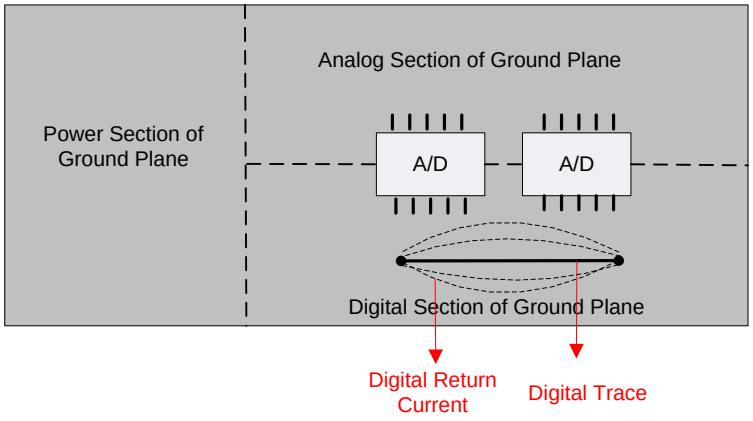


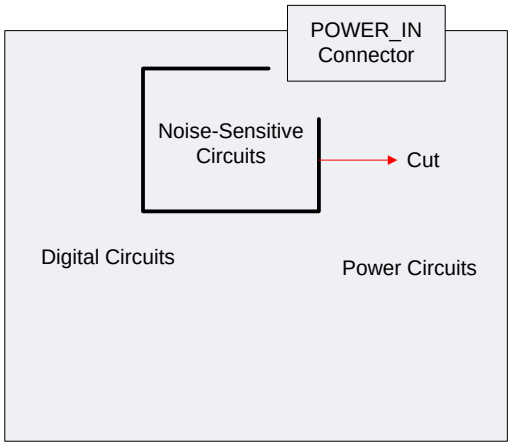
Figure 36. Ground Plane Partitioning



Usage of cuts/voids in ground plane: Another method to control ground currents is to selectively place openings or voids in the ground plane. The openings affect the current by forcing it to flow in a specific path, around or away from noise-sensitive circuits.

Figure 37 is an example implementation for selectively placing a cut in the ground plane. The example shows three grounds (analog, digital, and power) all on the same ground plane reference, with a cut placed around the noise-sensitive (analog) circuits forcing the ground return currents to flow around the critical area.

Figure 37. Ground Plane Cut Example



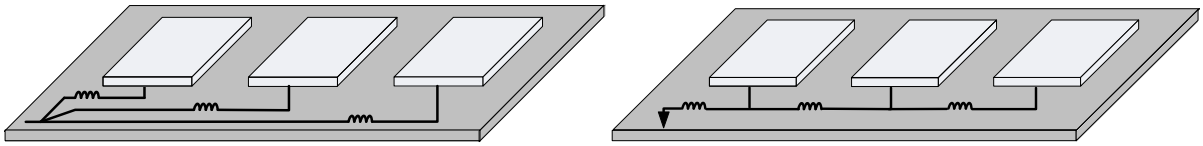
6.3.3.2 Ground Connections

There are three main methods of ground connections. Any of these can be employed within a particular functional sub-system.

6.3.3.2.1 Single-Point Grounding

- This can be implemented in parallel (Figure 38 A) or series (Figure 38 B). Parallel single-point grounding is the better method because the ground loops are isolated; preventing noise from one sub-system coupling to another. Series allows common-impedance coupling between the ground references of each subsystem. Hence, series single-point grounding is not recommended.
- Best for frequencies below 1 MHz such as in analog systems
- Has the largest number of ground loop currents. At higher frequencies (>1 MHz), these loops act as antennas and radiate RF energy, which may cause problems for other parts of the system.

Figure 38. (A) Parallel and (B) Series Connection

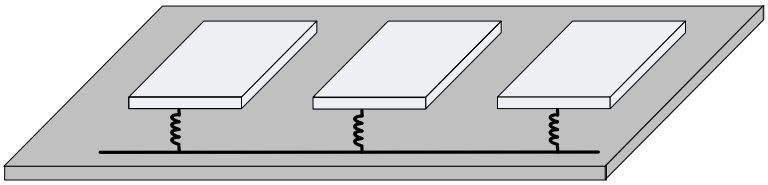


6.3.3.2.2 *Multipoint Grounding (Figure 39)*

- Preferred for frequencies above 1 MHz such as in digital systems
- Minimizes loop currents and ground impedance of planes
- Provides maximum EMI suppression at the PCB level

When using this scheme, keep the length of ground leads extremely short to minimize the inductance between components and ground planes. Otherwise, the added inductance may permit a resonance to occur when it forms a tuned resonant circuit with the distributed capacitance between the ground planes and chassis ground.

Figure 39. Multipoint Grounding



6.3.3.2.3 *Hybrid grounding: Combination of Single-Point and Multipoint Grounding in the Same System*

In this scheme, different ground methods for different functional sections of the PCB are used. Use a single-point ground for the analog portion of the PCB because most of the analog signal frequencies are below 1 MHz. For the digital portion, use either multipoint grounding.

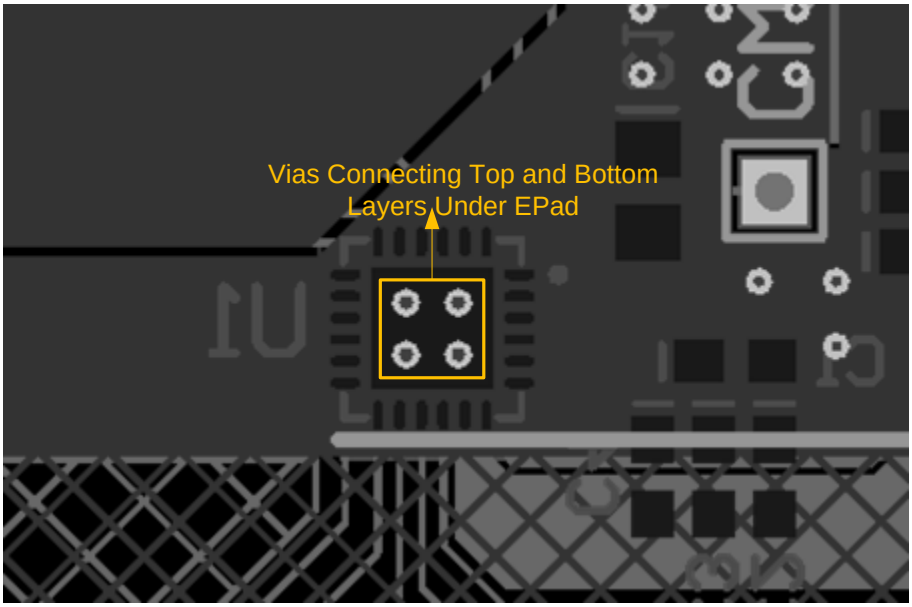
6.3.3.3 Other Guidelines on Grounding

- Put wide chassis ground traces or polygons in all layers of the PCB under connectors that go to the outside world. Tie all layers of the chassis ground traces together about every 13-mm with vias. This improves grounding connection on all layers.
- Connect controller ground pins to respective ground nets using a plane or a short-and-wide trace.
- Avoid using jumpers/wires to connect different areas of ground. Jumpers/wires increase the inductance on the return path.
- Consider using multilayer PCBs with separate ground and power planes that can dramatically reduce the impedance and inductive coupling (by 10 to 100 times over double-sided PCBs). Try to place each signal layer next to a ground or power layer.
- Connect different layers of ground with as many vias as possible that are equidistant to reduce the inductance.
- Fill the vias with solder or silver epoxy to further reduce the impedance and achieve better conductive properties.

Epads

There are certain packages of devices like QFN, which have center pad (Epad) for heat dissipation. Refer to the device datasheet for the Epad connection. Generally, datasheet either recommends to connect to ground or to leave it floating. If the recommendation is to ground the center pad, connect it to digital ground for best mechanical, thermal, and electrical performance. Connect the Epad to copper on both sides of the PCB to achieve the least impedance by using an array of vias in the area for Epad attachment.

Figure 40. Epad Connection



Vias

When idealized, one can think of vias as having zero effect on a design. This is far from reality, as vias have capacitance and inductance that cause the edge rate to decrease, and resistance that causes a signal to decrease in amplitude. Placing vias reduces the area through which currents can flow. Currents flow using the path of least impedance; therefore, placing a via in the direct path causes the current path to be indirect, causing addition of unnecessary noise to the circuit.

To achieve maximum transient suppression, make sure that vias do not impede the current flow to the filter components such as decoupling capacitors. Place vias so as not to increase the impedance on ground and supply traces, which might block high-frequency noise from returning to the source.

A typical example of placing vias is connecting a power plane to a decoupling capacitor and the power pin of an IC.

Figure 41 and Figure 42 show wrong via placements. In Figure 41, the capacitor and IC are on opposite sides of the power or ground plane. This implementation is almost the same as using no capacitor. Because the power or ground plane is between the IC (current load) and the capacitor, the power or ground plane sources the majority of power directly. The capacitor is now acting as a bulk power storage as opposed to the noise filter needed.

Figure 41. Capacitor, IC, and Via Orientation 1

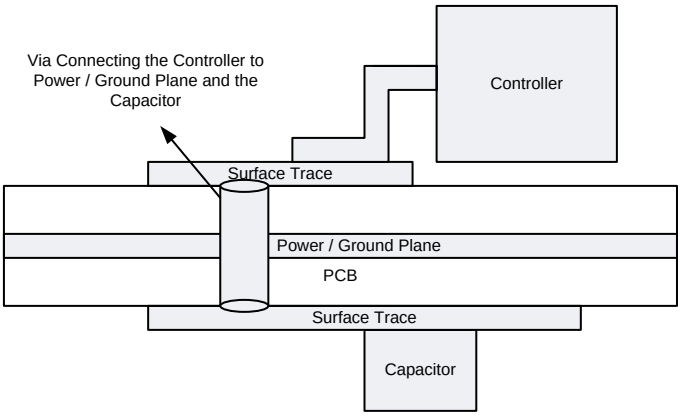
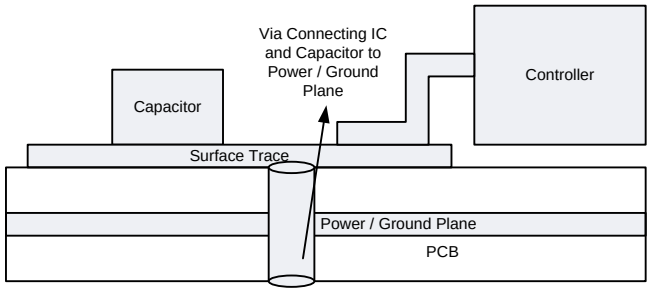


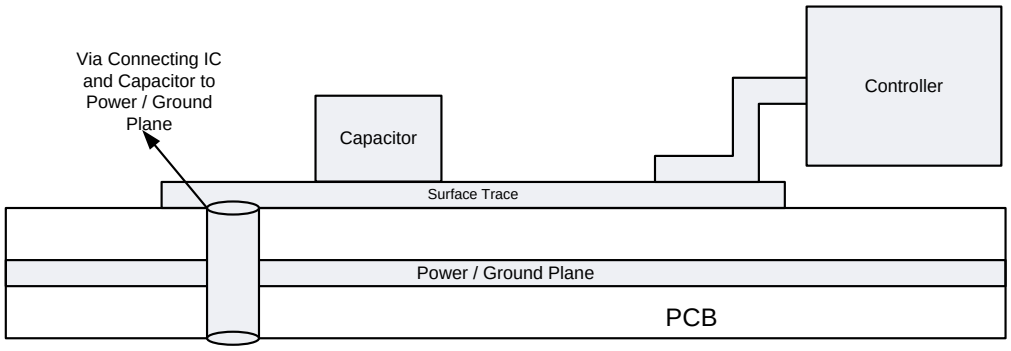
Figure 42. Capacitor, IC, and Via Orientation 2



In Figure 42, the capacitor and the IC are on the same side of the power or ground plane, with the via placed between them for connection to the power or ground plane. This implementation is slightly better than not using a capacitor. Because the power or ground plane via connection is between the IC (current load) and the capacitor, the power or ground plane sources the power in parallel with the capacitor. In this orientation, the capacitor accomplishes only a partial functionality.

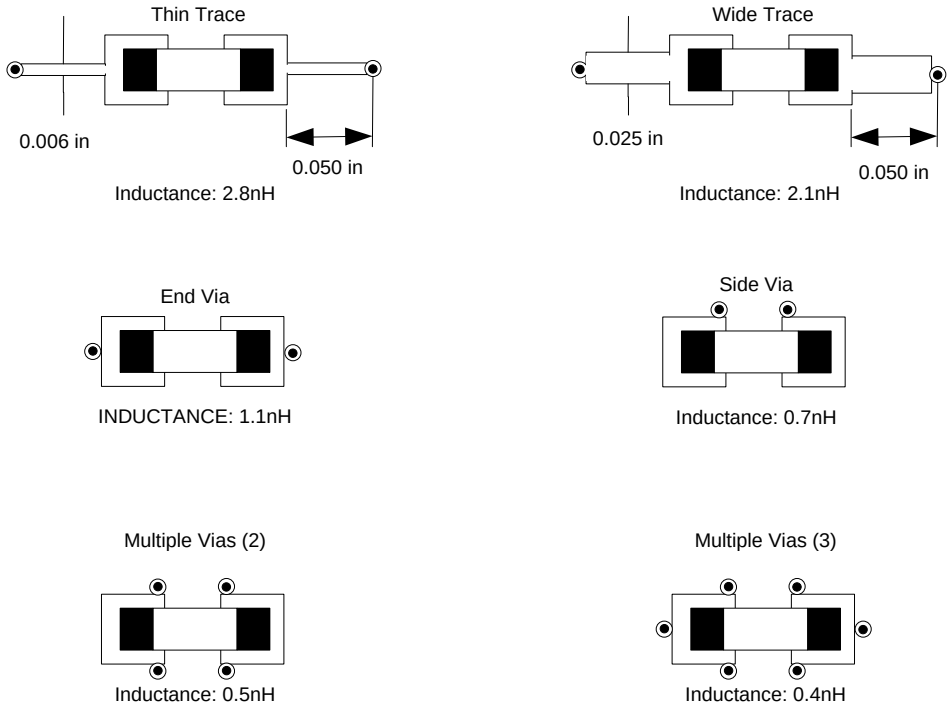
The capacitor and the IC on the same side of the power or ground plane, with the capacitor placed between the IC and the via connecting to the power or ground plane as shown in Figure 43 is the best implementation. Because the capacitor is between the power or ground plane via and the IC (current load), the capacitor is the first source of power for the IC. This allows the capacitor to function as required. It prevents unwanted power noise from reaching the power or ground plane and affecting other system components.

Figure 43. Capacitor, IC, and Via Orientation 3



Multiple vias reduce the inductance from the mounting pad to the power-ground-plane pair. However, the vias take up a lot of board space. Placing vias that carry opposite direction currents close together will also reduce the inductance as a result of mutual coupling. This is why the side-via configurations shown in Figure 44 have less inductance than the end-via configurations.

Figure 44. 0805 SMT Capacitor Schematic Showing Approximate Inductance Between the Mounting Pads and a Power Ground Pair

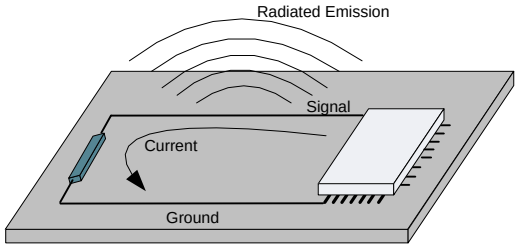


An example use case for multiple vias is when the decoupling capacitors are on one layer and the supply and ground from the source that feed the capacitors are on another layer. Use as many vias on the trace of the supply and ground at the point where the signal transitions to another layer to connect to the decoupling capacitor. This gives a low-impedance return path to the high-frequency noise.

Loop Area

All electronic circuits create current loops. Also, every current loop that carries current with frequency components is a radiator (antenna) of radio frequency energy. Therefore, all loops carrying current with transient noise are also radiators.

Figure 45. Example for Radiations from a Current-Carrying Loop



In order to reduce the susceptibility to transient noise, it is also important to minimize radiation. Radiation is directly proportional to the area of the loop, the current in the loop, and the square of the frequency of the signal..

Radiation can be controlled by the following means: reducing the frequency or harmonic content of the current, reducing the magnitude of the current, or reducing the loop area or all of them.

When you are dealing with transient noise, you do not have much control over the frequency components of the transient noise. By the time the noise propagates through AC-DC converter and to the target board, low-frequency components are dominant. In addition, the use of filters at the noise entry points also contribute to the reduction in high-frequency components.

Reduce the magnitude of the current flowing through critical loops. The most critical loops are those that are affected by transient noise, those that operate at higher frequencies, and where the signal is periodic.

Reduce the area of the most critical loops. Another important effect of loop size that you should not forget is the susceptibility to radiated noise. The bigger the loop size, the more susceptible is the signal in the loop to the external radiated noise. Therefore, keep the loop size to the minimum.

An example is a decoupling network. Keep the decoupling capacitor as close to the IC as possible to keep the loop area and inductance as small as possible.

6.4 Firmware Techniques

A properly designed firmware can go a long way in eliminating or minimizing errors caused by transients. Firmware should be designed in such a way that if a transient upsets the program, it does not lock up but recover gracefully.

Two basic steps are involved in writing transient-immune firmware:

- First, a fault must be detected.
- Second, the system must recover gracefully to a known stable state.

Firmware error-detecting and correcting techniques fall into three general categories:

1. Program Flow
2. Input/Output
3. Memory

6.4.1 Program Flow

6.4.1.1 Monitoring Correct Program Flow

To ensure system integrity, the firmware must monitor the program flow of various functions. You may use different techniques to do so. One method is “time-slot monitoring,” which periodically checks the status of the program counter and determines whether it is performing as expected. An example is the use of a simple timer interrupt to check program flow inside the ISR.

Fill unused memory with “jump to a safe location” commands. Thus, if the program counter falls into any unexpected location, the controller will execute a JMP instruction to a known state.

Fill unused interrupt vectors with pointers to an ISR that ensures the controller is placed into a safe known state. Never leave the interrupt vector location blank.

6.4.1.2 Using a Watchdog Timer

Some controllers such as PSoC have an integrated watchdog timer (WDT). Enable the WDT to protect against incorrect program execution. Employ the firmware to periodically check for the correct operation and reset the WDT. The WDT generates a system reset if the firmware has failed to clear the watchdog timely. You can use the System Reset Status Register to determine the cause of the last reset upon device restart.

6.4.1.3 Brownout Reset

A brownout reset is a circuit that forces the controller to reset if there is an interruption of power long enough to disrupt operation but not long enough to force a normal power-on reset.

PSoC 3, PSoC 4, and PSoC 5LP devices have an integrated voltage-monitoring circuitry, which provides many more options than typical brownout detectors. This circuitry detects both undervoltage and overvoltage conditions. Configure the protection circuit to reset the device immediately or generate an interrupt to allow the firmware to decide what action should be taken.

6.4.1.4 Firmware Tokens

A token is added at the entry and exit points of a function. The entry and exit tokens are set to the same value. If when exiting a function, the exit token does not match the entry token, then you may have jumped into the routine from somewhere else.

6.4.2 Input/Output

6.4.2.1 I/O Refresh

All critical I/O registers, such as I/O data ports, data control registers, and peripheral configuration registers, are flip-flop latches that may be flipped by a spurious noise passing through the circuit. Firmware should regularly test or refresh these registers to correct a possible flip of a bit that may cause a failure. You can then exit to an error recovery program, which minimizes the possible damage and helps recovering gracefully.

6.4.2.2 Polling of Inputs – Noise Filtering

In most controllers, I/Os are accessed by a reading of the CPU register via the data bus. Normally, this access is captured on the edge of the CPU system clock, and if a glitch occurs at the same time as reading, an error can occur.

To avoid this error condition, use a “polling” technique in firmware, read the pin several times within a short time, and take the dominant value as the true level. In a majority of cases, the CPU/system clock runs at higher frequencies than the external input signals, so the polling technique is easy to implement.

6.4.3 Memory

6.4.3.1 Error Detection

Changes in memory due to transient noise may not have an immediate effect, but may affect the system later. To detect memory corruptions, validate all data read from the memory before you use them. Many techniques exist for checking the validity of data. Use of single parity bit, checksums, cyclic redundancy checks (CRC), and various error-detecting codes exist. The degree of data memory protection required should be determined as part of the overall system specification.

6.4.3.2 Multiple Copies

A simple form of error detection is storing multiple copies of critical data, and comparing the two copies when reading the data back from the memory. Although simple, this method can be a drain on available memory space.

6.4.4 Class B Firmware to Detect Errors

Cypress provides the Class B Safety Software Library for PSoC 3, PSoC 4, and PSoC 5LP devices. APIs are included to maximize the application reliability through fault detection.

Table 3 lists the tests described and realized in the Class B library that meet the standard-compliance requirements for IEC 60730-1 Class B. Table 4 lists additional self-tests included in the library.

Some self-tests require the addition of the appropriate API function and **.c* and **.h* files from the Class B Safety Software Library. Other self-tests also require the addition of a schematic to the project.

Table 3. Self-Tests for IEC 60730-1 Class B Standard Compliance

Component	Test For
CPU registers	Stuck bits
Program counter	Jumps to the right address
Interrupt handling and execution	Proper interrupt calling and periodicity
Clock	Wrong frequency
Flash (invariable memory)	Memory corruption
EEPROM (invariable memory)	Memory corruption
SRAM (variable memory)	Stuck bits and proper memory addressing
Digital I/O	Stuck bits

Component	Test For
A/D and D/A converter	Proper functionality
Communications (UART, SPI)	Correct data receiving possibility

Table 4. Additional Self-Tests

Component	Test For
Watchdog	Chip reset
CapSense CSD	Sensor shorts, sensor disconnect, and modulator external component (Cmod and Rb) errors
Comparator	Proper comparator functionality

For more details, refer to the following:

- AN81828 - PSoC® 1 – IEC 60730 Class B Safety Software Library
- AN79973 - PSoC3 and PSoC5 CapSense CSD - IEC 60730 Class B Safety Software Library
- AN89056 - PSoC® 4 – IEC 60730 Class B and IEC 61508 SIL Safety Software Library

The firmware may execute required self-tests at device startup to check whether the controller is suitable for operation. It may also periodically run self-tests to verify that the device was not damaged during operation and that it works as intended. Some of these self-tests may mask off the failure due to transient noise. Therefore, although Class B firmware is incorporated in your application, make sure that the errors caused by transient noise are identified and appropriate recovery mechanisms are incorporated.

7 Summary

This application note gives engineers information on design guidelines and techniques for EFT immunity of an embedded controller-based application. The application note also explains the rationale behind EFT tests and explains EFT test waveform. Additionally, the application note explains the failure modes in a controller.

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- http://www.vishay.com/docs/ilb_ilbb_enote.pdf

2 This standard is not available for free. However, you can purchase a copy at www.iec.ch.

A Appendix A: IEC 61000-4-4 EFT Test Requirements

IEC 61000-4-4 relates to the immunity of electrical and electronic equipment to repetitive electrical fast transients/bursts (EFT/B). The IEC 61000-4-4 standard defines the test voltage waveform, the range of test levels, test equipment, verification procedures of test equipment, test setup, and the test procedure. IEC 61000-4-4 standard also gives specifications for laboratory and post-installation tests.

A.1 Test Levels

EFT test can be performed on AC/DC mains supply, earth, signal, and control ports. Table 1 shows the test levels defined by the standard applicable to power, ground, signal, and control ports of tche equipment.

Table 1 lists the peak voltage and repetition rate for each of the levels. Bursts repeating at 100 kHz provide a real-world transient repetition rate scenario. Equipment test plans must document what repetition rate is being used for testing the EUT.

The specification defines four severity levels in terms of an open-circuit voltage as a function of the installation environment. Select the test levels according to the end application objectives. Correlate the immunity tests with the test levels to establish a performance criteria for the environment in which the equipment is expected to operate. Based on common installation practices, the recommended selection of test levels for EFT/B testing according to the requirements of the electromagnetic environment, is given in Table 5.

Table 5. EFT/B Testing Severity Levels

Level	Attributes
1 – Well Protected	The environment in which the equipment is installed in is characterized by the following: - all transients are suppressed in the power supply and control circuits - there is clear separation between power supply and control circuits originating from other less protected environments - power supply cables are shielded and connected to earth - power supply protection is offered by appropriate filtering circuits Example: Corporate data center or a computer room.
2 - Protected	The environment in which the equipment is installed in is characterized by the following: - partial suppression of transients in the power supply and control circuits - incomplete or poor separation of power supply and control circuits originating from other less protected environments - physical separation of unshielded power supply and control cables from signal and communication cables Example : An industrial control room
3 – Typical Industrial	The equipment installation is characterized by the following: - no suppression of transients - incomplete or poor separation of power supply and control circuits originating from other less protected environments - poor separation between power supply, control, signal and communication cables - earth protection is available Example : A typical household or areas of industrial process environment

Level	Attributes
4 - Severe industrial	The equipment installation is characterized by the following: - no suppression of transients - no separation of power supply and control circuits originating from other less protected environments - no separation between power supply, control, signal and communication cables - common multicore cables used for control and signal lines Example: Power plants, open air relay rooms of electric substations.

Many manufacturers of equipment based on microcontrollers or PSoC such as home appliance or mobile phone are conservative and go for as high as Level 4 EFT test.

There is also a level 5 called a special level. This level is typically applied to equipment that need it and is documented in the technical specification documentation of the equipment. In this level, the separation of disturbance sources from the equipment's power/signal/control lines is different from those defined in levels 1 through 4.

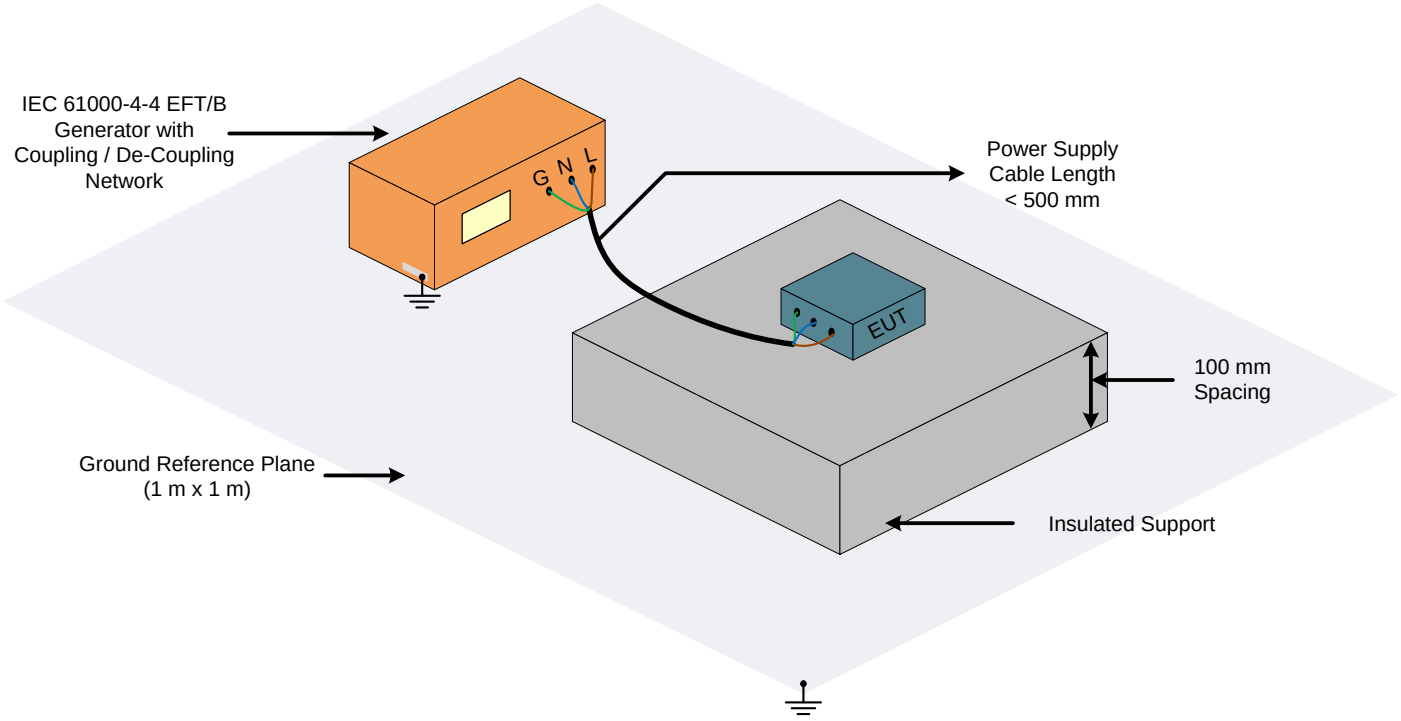
A.2 Test Setup

The test setup comprises the following:

- Equipment Under Test (EUT)
- Ground Reference Plane (GRP)
- Coupling Network
- Decoupling Network
- Test generator

It can include auxiliary equipment for measurement and verification purposes.

Figure 46. EFT Test Setup



1. A coupling/decoupling network is required for acceptance tests of AC/DC power supply ports. For acceptance tests on the lines connected to I/O and communication ports, coupling with capacitive coupling clamps is required. The clamp provides the ability of coupling the fast transients/bursts to the circuit under test without any galvanic connection to the terminals of the EUT's ports or shielding of the cables or any other part of the EUT. The clamps may also be used on AC/DC power supply ports only if the coupling/ decoupling network cannot be used.
2. For pre-compliance testing in laboratories, the test setup also includes a ground reference plane (GRP). Connect the GRP to the protective earth. Ensure that the potential difference between the protective earth and the neutral of the power supply is less than 1 V before proceeding with the test.
3. Test the floor/wall/ceiling-mounted equipment as stand-alone equipment. Mount the EUT on the insulated support that is 100 mm ± 10 mm thick. The GRP must extend beyond the EUT by at least 100 mm on all sides.
4. Place the EFT/B generator directly on the GRP and make the earth connections.
5. Connect the EUT to the earth system as specified by its specifications. No additional earth connections are allowed. The minimum distance between the EUT and other conductive structures must be 500 mm.
6. All cables to the EUT must be placed on the insulation support and must not be greater than 500 mm ± 50 mm in length. If the cable length is greater than the specified length, the excess length must be folded in the shape of '8' to avoid a flat coil and must be placed on the insulation support.

The following two types of tests are defined based on test environments:

1. Conformance or pre-compliance tests performed in laboratories
2. Post-installation tests performed on equipment in its final installed conditions

The preferred test method is testing performed in laboratories.

A.3 Test Procedure

The functionality of the EUT must be checked before and after the EFT test. The test procedure includes:

- the verification of the operating conditions in the laboratory
- the verification of the EFT waveform
- the test execution and
- the evaluation of the test results

A.3.1 Laboratory Operating Conditions

In order to minimize the effect of the environmental parameters on test results, the EUT must be subjected to the same temperature and humidity limits as specified in its documentation. Testing must be avoided if the relative humidity is high enough to cause condensation within the EUT. The electromagnetic conditions of the laboratory must be such as to guarantee an interference-free operation of the EUT.

A.3.2 EFT Waveform Verification

To ensure correct testing, the EFT waveform must be captured with an oscilloscope and documented before each test cycle. To do this, attenuators are typically used. The EFT waveform captured must comply with the recommendations of the IEC specification.

The EFT/B generator output should be connected to a 50-Ω and 1000-Ω termination and the voltage must be measured with an oscilloscope. Use an oscilloscope whose –3 dB bandwidth is at least 400 MHz. The rise time, pulse duration, and repetition rate of the impulses within a burst must be measured. For each set point voltage, the measured output voltage must be

- within (0.5 times the set point voltage ± 10%) for 50 Ω termination
- within (set point voltage ± 20%) for 1000 Ω termination
- rise time = 5 ns ± 30%
- duration of the pulse = 50 ns ± 30% for 50-Ω termination and 50 ns with a tolerance of -15 ns to +100 ns for 1000-Ω termination

For more information, see the EFT/B generator documentation on how to perform the waveform capture.

A.3.3 Test Execution

The EUT must be subjected to its normal operating conditions. The test must be carried out on a basis of a test plan. The test plan must include, apart from the functionality testing, the performance verification plan of the EUT. The test plan must specify the following:

- test level intended for the EUT
- EUT ports to be tested
- polarity of the test voltage (typically both polarities) and number of applications of the test voltage
- sequence of application of the test voltage to the EUT ports
- duration of the test must not be less than one minute; test time can be broken down into six 10 second bursts, separated by a 10 second pause
- any use of auxiliary equipment

A.3.4 Evaluation of Test Results

The test results must document the loss of functionality or degradation of performance of the EUT relative the performance defined by the manufacturer or the performance measured before the test. The performance classification is as in Table 2, per IEC 61000-4-4. Manufactures can define the effects on the EUT, which may be considered insignificant and therefore acceptable. For example, in some applications, if the device resets and recovers within the tolerance duration during the tests such that the functionality is not altered, device reset may not be considered as a failure.

It is generally recommended to subject the EUT to functional and performance testing after the EFT test. This would ascertain if there are any irreversible damages to the EUT and would provide a basis for future test cycles.

A.3.5 Test Report

The test report must contain all the information necessary for reproducibility of the results. The report must contain:

- description of the EUT and any auxiliary equipment
- operating conditions of the EUT
  - specific environmental conditions
  - specific conditions such as use of shielded enclosure
  - specific conditions necessary to enable the test to be performed such as hardware/firmware modifications
- test cases per the test plan
- performance level defined by the manufacturer
- effects on the EUT observed during or after the test
- rationale behind the pass/fail decision based on evaluation of test results

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3680914	SLDK	07/16/2012	New application note
*A	3757612	SLDK	09/27/2012	Title to be updated in the web and spec system to include application note number.
*B	4092935	SLDK	08/12/2013	Updated for PSoC 5LP. Corrected a hyperlink to AN78175. Other minor edits.
*C	4198510	JOZH	11/22/2013	Updated for PSoC 4. Moved the lists of ESD and EFT requirements to Appendix B and C.
*D	4607133	JOZH	12/24/2014	Updated Ferrite Beads section.
*E	4761918	SSHH/ NIDH	05/11/2015	Updated Introduction. Removed section “Test Board Design for EMC Immunity Testing”. Added references to getting started ANs for more details. Updated the document as per new template.
*F	4918073	SSHH/ SNVN	09/13/2015	Complete re-write of application note.
*G	5392017	SSHH	08/29/2016	Updated template Added reference to AN96475
*H	5700297	AESATP12	04/20/2017	Updated logo and copyright.

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