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SIMULATION OF COSMIC-RAY INDUCED SOFT ERRORS AND LATCHUP IN INTEGRATED-CIRCUIT COMPUTER MEMORIES*

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Summary. Soft errors have been induced in solid-state static RAM's by iron nuclei from the Lawrence Berkeley Laboratory (LBL) Bevalac, in experiments designed to prove the ability of iron-group cosmic rays to generate such errors. Subsequently, various de-lidded device types were tested in beams of argon and krypton ions from the LBL 88-inch Cyclotron, at energies near 2 MeV/nucleon. The latter tests showed that some devices are essentially immune to bit error while others are quite susceptible. Good agreement was obtained with model predictions in cases where the latter exist. Latchup, whose cause we attribute to individual heavy ions, was also observed in some device types.

Introduction

Anomalous triggering of digital circuits in spacecraft hardware can be caused by heavy cosmic rays. This hypothesis was first proposed in the literature by Binder et al.[1] Of late, increases in the use of LSI devices for space applications have generated added interest in the problem. Several discussions of the mechanism of error generation by cosmic rays in devices representing various types of technology have recently been published.[1,2,3] For memory devices, briefly stated, the mechanism involves the passage of a single, heavily ionizing particle through a microscopic sensitive region on the silicon chip. If the charge produced within the sensitive volume and swept out by the existing electric field exceeds a certain critical value, the circuit changes its state and a change in the memory contents is observed. There is no permanent damage to the cell, hence the name "soft error."

At this point we emphasize the fact that the process being considered is one where the ionization charge is produced directly by the heavy cosmic-ray particle, rather than via a nuclear interaction in or near the sensitive region. It should also be borne in mind that we are dealing with an environment totally unlike those commonly encountered in radiation testing, where the dose is distributed uniformly over the whole chip volume. Here, a dose of up to several Giga-rads (Si) is deposited in a track whose diameter is at most several hundred Å.[4] Thus, environments commonly used for radiation testing are inadequate for assessing device performance in the presence of cosmic rays.

It is well known that the rate of energy loss, dE/dx, of a charged particle passing through matter can be represented approximately by the expression

$$dE/dx = f(E)MZ^2/E \qquad (1)$$

where x is the distance traversed in units of mass per unit area, f(E) is a very slowly varying function of the particle energy E, while M and Z are the particle mass and atomic number, respectively. Thus, for a given energy, the heavier the particle, the more likely it is to produce an amount of charge which exceeds the threshold for memory upset. Figure 1 (Ref. 5), showing tracks in nuclear emulsion produced by cosmic rays of various atomic numbers, is a dramatic illustration of the dE/dx dependence upon Z. Since the intensity of heavy cosmic rays as a function of Z shows a pronounced peak around iron (Z=26) and abruptly decreases by two orders of magnitude for higher Z values,[1] tests which simulate the effects of iron nuclei can be assumed to represent a realistic heavy-ion environment in space. This environment is shown in Figure 2, where the intensity of iron nuclei is plotted as a function of energy both for the well-known galactic cosmic-ray component and for the September 1977 solar flare, as measured by J. Simpson's group at the University of Chicago.[6] While such flares may be quite rare and of relatively short duration, the possibility of their occurrence clearly needs to be considered in selecting devices for space applications.

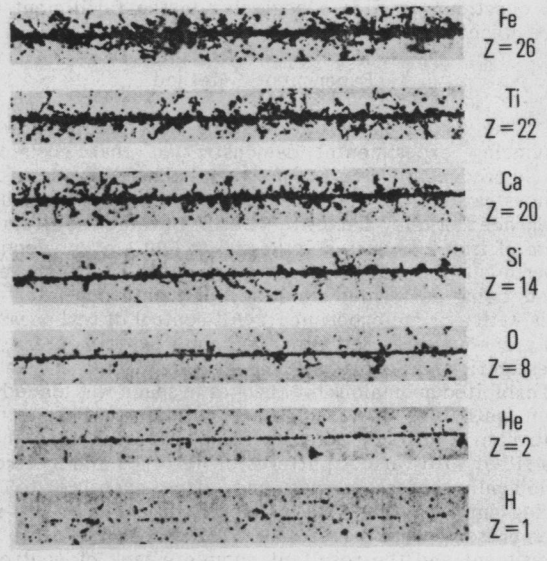

Fig. 1. Cosmic-ray Tracks in Nuclear Emulsion (Ref. 5).

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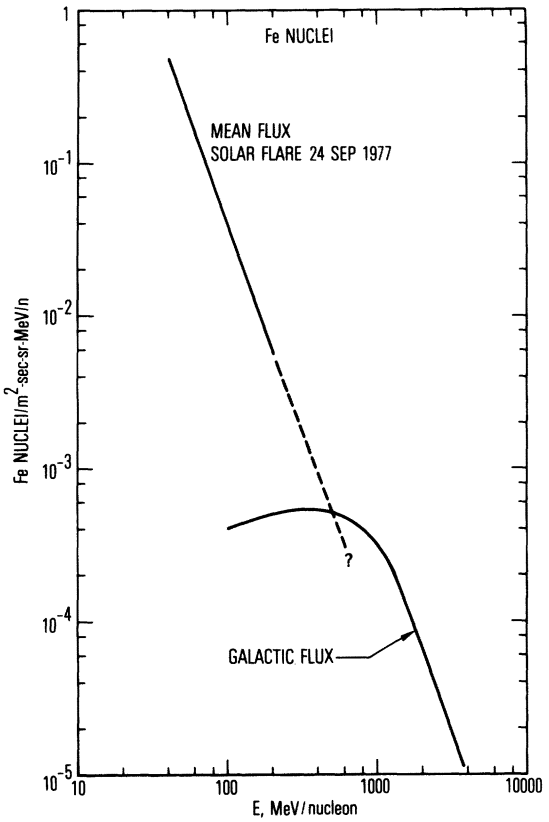

Fig. 2. Spectra of Galactic and Solar Cosmic-ray Iron Nuclei (Ref. 6).

In undertaking this study, we had three objectives in mind. First was the experimental demonstration of the fact that cosmic rays indeed are capable of inducing errors in solid state devices. The second objective was to test some parts already incorporated in future spacecraft designs and find replacement candidates for ones determined to be unsatisfactory. Finally, the third objective was to obtain data needed to test and refine models of the type developed in the references cited above. In the remainder of this paper, we hope to demonstrate the accomplishment of the first two limited objectives and to describe results which, while raising new questions, provide a beginning in the fulfillment of the third objective.

Experimental Method

The initial phase of the study was directed towards a convincing experimental demonstration that cosmic rays indeed produce bit errors in memories aboard spacecraft. This demonstration was performed in an experiment at the Lawrence Berkeley Laboratory (LBL) Bevalac facility, using a beam of iron ions with energies up to 600 MeV/nucleon. The experiment was one of several unrelated secondary experiments being performed simultaneously on a non-interference basis with a prime experiment. All control of test parameters and procedures resided with the prime experimenter. In our investigation, a Schottky TTL static RAM of the type which had exhibited anomalous bit changes in space was placed in the beam path and operated in conjunction with a remotely controlled micro-computer (μ-comp) system. The memory was filled with various patterns of 0's or 1's and interrogated periodically before, during and after exposure to beam. During interrogation, the memory addresses of bit errors, when present, were printed out. The secondary nature of the experiment and the resultant complete lack of control over beam properties and test conditions precluded any systematic quantitative study of parameters governing the bit-error rate.

Following a suggestion made by J. T. Blandford and J. C. Pickel[7] we continued the work using heavy ions from the LBL 88-inch Cyclotron, where, within the limitations of the accelerator and external beam-system design, complete control over all test conditions was possible. In order to simulate the worst-case energy deposits in space, it was decided to accelerate the heavy ions to energies in the 1-2 MeV/nucleon range, where the rate of energy loss is near maximum. Since, of the various beams available with reasonable intensity on the machine, argon came closest to iron in atomic number, the initial tests were conducted with argon. Following the initial runs with argon, a suitable krypton beam was successfully developed by the Cyclotron personnel to accommodate our need for ions with Z higher than that of iron. Krypton ions were used in all the subsequent runs to date, since by virtue of its high Z (36 vs 26 for Fe) the environment simulated in the laboratory would exceed the worst-case conditions encountered in space.

Figure 3 shows the experimental arrangement in schematic form. Because of the low beam energy, tests had to be performed in vacuum, using de-lidded chips. The particle beam was aligned and de-focussed by means of magnets approximately 10 m away from the vacuum chamber. After passing through a remotely controlled shutter, the beam entered the test chamber, shown in Figure 3, through a 5 cm diameter aperture, completely filling it. Downstream to the right, a circular 1.8 cm diameter aperture allowed the central portion of the beam to strike a transmission scintillation detector consisting of a 2.5 μm-thick scintillating foil coupled by means of a special light pipe to a photomultiplier tube (PMT). The PMT output pulses, caused by the passage of individual ions through the foil, were transmitted via a 50 Ohm coaxial cable to the experiment-control area and counted with conventional nuclear counting equipment. After being counted in the transmission counter, the ions illuminated a 1.8 cm diameter area on the sample board also shown in Figure 3.

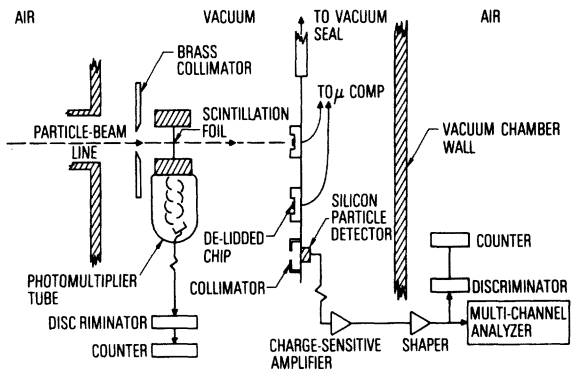

Fig. 3. Schematic Representation of Test-Sample Hardware and Beam Monitoring System.

De-lidded test devices were arranged on the sample board in a vertical row at intervals such that only a single device at any given time could be positioned in the beam path. The sample board was mounted on a frame attached to a round, stainless steel rod which passed through a sliding vacuum seal in the vacuum-chamber lid. This arrangement provided the vertical motion required to position the various devices in the beam path, and permitted changes in angle relative to the beam.

One of the positions on the sample board was reserved for a surface-barrier nuclear particle detector with an aperture 0.1 cm^2 in area (see Fig. 3). This detector was occasionally placed in the beam path and used to measure the beam energy as well as to provide an indication of beam uniformity. The beam energy was measured by displaying the detector pulse-height spectrum in the multi-channel analyzer (MCA), previously calibrated with radioactive alpha emitters and a precision pulser. Beam uniformity was checked by comparing

the ratio of the surface-barrier and transmission detector areas to the ratio of the respective counting rates measured in the two detectors.

The electronic system used to operate the memories during the tests evolved during the several months spanning the test period and will be described only briefly. Figure 4 is an extremely abbreviated functional block diagram of the system, showing connections to only one test chip. Provision was made to vary the bias on the individual test chips by placing an interface on the sample board, labelled "level translator" in Figure 4. All chips communicated via the level translator with a micro-computer located near, but outside the vacuum chamber. By means of appropriate switches, not shown in Figure 4, a current monitor could be inserted in any one of the bias lines leading to the chips. As shown in Figure 4, the bias supplies and a teletype used to communicate with the micro-computer were placed outside the beam area, in the control room. The output of the bias-current monitor, also in the control room, could be used to close the beam shutter if the bias current exceeded a preset value as, for example, in a latched condition.

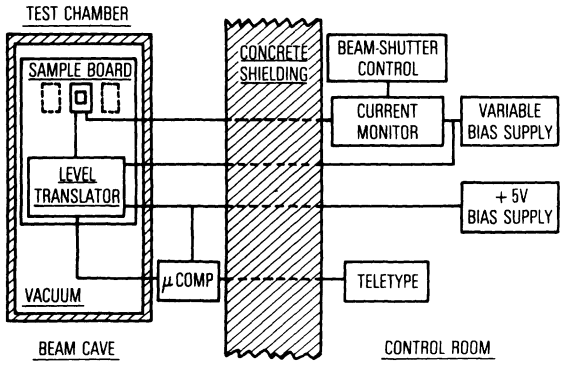

Fig. 4. Simplified Block Diagram of Circuits Used to Operate Test Memory Chips.

With minor variations, the tests were carried out according to the procedure outlined below. With all the beam optics adjustment complete and the surface-barrier detector in the beam path, the beam intensity was adjusted to a level between 10 and 10,000 particles/(cm^2 sec). Generally, the runs were started at the lower intensity level and went higher, depending on previous test results. At the same time, the various chip-interrogation commands were sent to insure proper system operation and verify the absence of bit-errors. The interrogation sequences were implemented both with the beam shutter open and closed. Upon successful conclusion of the interrogation sequence, the shutter was closed and a test chip placed in the beam path and rotated to a predetermined angle with respect to the beam. Next the current monitor was inserted in the line and the bias supply adjusted to a predetermined value. Upon another successful interrogation for absence of errors, the chip was ready for beam exposure which lasted anywhere between ten seconds and several minutes, depending on the test history and beam intensity. The shutter was opened manually and closed after the desired exposure duration, unless the current monitor caused the shutter to close earlier. All system parameters in effect during the exposure were recorded on data sheets and the chip again interrogated for errors. If no errors were detected at a given angle, the bias was lowered and following another interrogation the exposure repeated, until a threshold bias for errors could be found, or until a bias level was reached below which the chip would cease to function reliably. If the minimum operating bias was reached without beam-induced errors being detected, the procedure was repeated at larger angles until errors were detected or until the maximum angle of approximately 75 deg was reached. A sample exposure record consisting of several data runs is shown in Table 1. The chip-orientation angle is defined as the angle between the incident beam direction and the normal to the exposed chip face.

Results

During the Bevalac phase of the study, we found that the iron beam produced bit errors when an appropriate amount of shielding was placed upstream of the test device. While the test conditions precluded any accurate measurement of beam intensity or energy, we estimate that ions with energies between 20 and 100 MeV/nucleon, striking the chip at angles close to 90 degrees produced the errors. Within the statistical uncertainty, the errors were found to be randomly scattered throughout the 64-bit memory.

Table 2 shows a summary of the test results obtained from the LBL 88-inch Cyclotron runs. In case of the first three devices shown, no errors could be induced at any angle or bias. Since the maximum energy deposited in these devices by the krypton beam exceeded the maximum energy which heavy cosmic rays of the iron group can deposit, these devices were judged to be immune to the space cosmic-ray environment.

The next device type in Table 2, the CD4061 256 x 1 RAM, exhibited errors at angles above approximately 60 degrees and biases at or slightly below 5V. No errors were observed at any angle for bias levels above approximately 6V. Altogether four devices were tested and, apart from some differences in angles and biases at which error onset was observed, all showed consistent behavior. The numbers shown in the "measured cross-section" column of Table 2 were computed by dividing the number of bit errors observed during a given exposure by the total flux per unit area as determined by the PMT monitor. The statistical uncertainties in the data acquired so far are quite large (typically 20-50 percent), hence the approximate signs in front of all the numbers. The observed angular dependence of the cross-section for CD4061 did not appear to obey the cosine law and, if anything, remained constant out to 60 degrees with respect to the beam. None of the CD4061 devices showed errors in argon exposures, but during those exposures the option to vary the bias had not been available, and no subsequent tests with argon have been performed.

Table 1. Abbreviated Example of Data Recorded During Several Test Runs

Date	Run #	Part Type	Bias Level (volts)	Angle (deg)	Run Duration (sec)	Monitor Counts	Comments
6/7/79	22	CD4061	5.01	60	100	89087	4 flips
6/7/79	26	CD4061	6.09	60	290	100,000	no flips
6/8/79	106	93L425	7	0	2	2850	20 flips
6/8/79	110	HM6508	5.0	0	1	710	latched
6/8/79	111	HM6508	5.0	0	4	2520	latched
6/8/79	113	HM6508	5.0	0	3	1713	8 flips
6/8/79	132	TCC244	3.3	75	90	500,000	26 flips

Table 2. Summary of Test Results

Device Number	Organization	Technology	Test Results		Bit-Error Cross-Section (cm^2)
CDP1821	1024 x 1	SOS/Si gate	No errors		---
MM54C200D	256 x 1	CMOS/metal gate	No errors		---
74L78	2 x 1	TTL, Bipolar	No errors		---
CD4061	256 x 1	CMOS/metal gate	Errors when bias	5V	$\approx 2 \times 10^{-4}$
TCC244	256 x 4	C^2L/Si gate	Errors when bias and angle large	3.5 V,	$\approx 1 \times 10^{-4}$
93L425	1024 x 1	Bipolar	Errors		$\approx 1.5 \times 10^{-2}$
31L01	16 x 4	Schottky TTL	Errors		$\approx 1 \times 10^{-3}$
IM6518	1024 x 1	CMOS/Si gate	Errors		$\approx 3 \times 10^{-3}$
MM54C929	1024 x 1	CMOS/Si gate	Errors/latch		$\approx 1 \times 10^{-2}$
HM6508	1024 x 1	CMOS/Si gate	Errors/latch		$\approx 5 \times 10^{-3}$
HM6504	4096 x 1	CMOS/Si gate	Errors/latch		$\approx 5 \times 10^{-3}$

Errors in one TCC244 device were observed with krypton only, and only at the maximum attainable angle of approximately 75 degrees. Even then the bias had to be reduced below 3.5V before errors could be seen. Two devices were tested, and the other device showed no errors whatever.

When tested with krypton, the next three devices shown in Table 2 exhibited errors at 0^o to the beam, at all operating values of bias. At present no data exist for other angles, but since 0^o corresponds to a minimum energy deposit, it is presumed that errors occur at all angles. Of the three devices, only the 31L01 was exposed to argon as well as krypton and in both cases exhibited the same response.

We now come to the last three devices in Table 2, which besides being prone to error, have been found to be extremely susceptible to latchup. Both the MM54C929 and HM6504 were exposed to argon and krypton and exhibited equal susceptibility to latchup in both cases. One HM6508 was tested, with krypton only. During the initial tests with argon, one HM6504 and two MM54C929's were destroyed because the effect had not been anticipated and no provision existed for limiting the individual device bias current. In subsequent runs, to eliminate device self-destruction, the bias current was limited to approximately 50 mA. The MM54C929's and the one HM6508 device tested show a cross-section for latchup of approximately 1×10^{-3} cm^2, which is a factor of five to ten times less than the measured error cross-section. In case of the HM6504 the latchup and bit-error cross-sections appear to be roughly equal.

Discussion

Sivo et al.[3] have performed a theoretical analysis for several devices, of which two (TCC244 and CD4061) have been tested in the present study. Before comparing the test results with the model of Ref. 3, we review the relevant model parameters needed for the comparison. First, according to Ref. 3, the contribution of diffusion current to the charge collected at the circuit node prior to bit flip is small if not negligible. Hence, in computing the energy deposited by the 1.8 MeV/nucleon krypton ions in the test beam, we assume the depletion depth represents the junction thickness and neglect the contribution of the diffusion region. Second, we note that according to Ref. 3, the voltage swing, ΔV, required to produce a bit flip is equal to $0.8\ V_{DD}$, where V_{DD} is the bias on the device. Using manufacturer's data and the model, the authors of Ref. 3 compute the node capacitance C and thus obtain the critical charge, Q_{min}, required to produce bit-error:

$$Q_{min} = C\Delta V = 0.8\ C\ V_{DD}. \quad (2)$$

Since it is well known that in silicon 3.6 eV of energy is required to produce an electron-hole pair, the minimum energy deposit for bit flip, E^T_{min}, as predicted by the model is

$$E^T_{min} = 18\ C\ V_{DD}, \quad (3)$$

where E^T_{min} is in MeV, C is expressed in pF, and V_{DD} in volts. Finally, we note that according to the model of Ref. 3, the node capacitance C for the TCC244 device has a constant value of 1.2 pF at V_{DD} = 5V and 10V, while for CD4061, C = 0.50 and 0.44 at the two respective values of V_{DD}. For both devices, Ref. 3 quotes 3×10^{-4} cm for the depletion depth at a bias of 5V.

We now turn to a comparison of the test results with the model. The "measured" energy deposit, E^M_{min}, required for bit flip will be computed from the expression

$$E^M_{min} = h(v_{DD})\ \rho\ \frac{dE}{dx}(\mathrm{Cos}\,\phi)^{-1}, \quad (4)$$

where $h(V_{DD})$ is the depletion depth in cm at a bias V_{DD}, ρ is the density in gms/cm^3, $\frac{dE}{dx}$ is the energy loss of the test beam in MeV cm^2/gm and ϕ is the angle between the beam direction and the normal to the chip face. Using the values of 2.33 gm/cm^3 and 3.9×10^4 MeV cm^2/gm for the density and $\frac{dE}{dx}$ for silicon, respectively,

$$E^M_{min} = 9h(V_{DD})/\mathrm{Cos}\,\phi, \quad (5)$$

where h is expressed in microns. This value is to be compared with E^T_{min}, as computed from Eq. 3. Table 3 shows the values of E^M_{min} and E^T_{min} for the TCC244 and CD4061, together with values of the parameters used in the calculations. In the case of TCC244, the value of h at 3.5V was obtained from the value at 5V quoted in Ref. 3, by assuming that h varies as $\sqrt{V_{DD}}$, while for C, the value given at 5V was used.

Table 3. Comparison of Threshold Energy with Theoretical Predictions

Device Type	V_{DD} (V)	(deg)	C (pF)	h (μm)	E^{M}_{min} (MeV)	E^{t}_{min} (MeV)
TCC244	3.5	75	1.2	2.5	87	76
CD4061	5	60	0.5	3	54	45

The agreement between E^{T}_{min} and E^{M}_{min} is almost too good to be true, considering the uncertainties which enter into computing the model-parameter values. It should be recalled, however, that in the TCC244 case, one device showed no errors at all. Similarly, for the CD4061 case we selected the results for the single softest device of the four tested. It thus appears that either the model has a tendency to err in the conservative direction, since it underestimates the device energy thresholds, or it overestimates the depletion depth of the junction, resulting in an unduly large value of the "measured" energy threshold. In fact, if we take an expression for h such as the one given in Ref. 8, i.e.,

$$h \approx \left(\frac{2 \kappa \epsilon_0}{eN} V_{DD} \right)^{1/2} \quad (6)$$

where κ and ϵ_0 are the dielectric constant of silicon (≈ 12) and the permittivity of free space, respectively, while e is the electronic charge and N the doping concentration ($1 \times 10^{15}/cm^3$), we obtain, after putting in the appropriate numbers,

$$h = 1.15 (V_{DD})^{1/2}, \quad (7)$$

with h in microns. The respective values of E^{M}_{min} now become 75 MeV for TCC244 at 3.5V bias and 46 MeV for CD4061. Now we have better than 2% agreement in both cases, which can only be taken to be totally fortuitous!

In Table 2, we note that the measured total sensitive cell areas for TCC244 and CD4061 are between one and two orders of magnitude less than the same areas for the various other devices tested. According to the model of Ref. 3, the TCC244 and CD4061 sensitive areas are 4.5×10^{-3} and 3.1×10^{-3} cm^2, respectively. These values are an order of magnitude more than measured ones, but in excellent agreement with the values for the various devices in the lower half of Table 2. We can only surmise that the low experimental values are due to the fact that the measurements for the two types of devices have been performed near a threshold, which falls somewhere above the peak in the ion energy-deposit distribution. Clearly more work is needed to resolve this question, as well as to determine the angular dependence of the bit error rate.

As mentioned before, within statistical errors imposed by a small sample number, the cross-sections for latchup are somewhat less than the bit-flip cross-sections. The total number of latchup events for each device is so far less than ten, so inferences concerning fits to statistical distributions are premature. However, the results are not inconsistent with a single particle striking a sensitive region and inducing latchup. In fact, considering the fact that latchup is observed with fluxes as low as 10 ions per cm^2 per second, it is difficult if not impossible to conjure up any plausible collective or cumulative mechanism.

Summary and Conclusions

We have demonstrated experimentally the fact that cosmic rays are capable of causing soft errors in static, solid-state memory devices, and in some cases, latchup which may lead to the device destruction. Furthermore, our studies have shown, in agreement with model predictions, that some devices are for all practical purposes immune to upset by the cosmic-ray environment, and that in some cases at least, models can be developed which predict device performance in excellent agreement with experimental test results.

It would be very useful to extend the test program to devices whose threshold energy deposit for producing errors and/or latchup is less than the smallest value of energy deposit attainable with test beams used in the present study. Quantitative predictions of such device response to energetic-particle environments could then be obtained. This objective can be accomplished by using ions of lower atomic number and varying energy, until the threshold range of $\frac{dE}{dx}$ values is attained. Sector-focussed cyclotrons similar to the LBL 88 inch Cyclotron are ideal for this purpose, because of their ability to accelerate a large variety of heavy ions and to vary the ion energy over a wide range.

Acknowledgments

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