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BSIM3v3.1 Model

Parameters Extraction and Optimization

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1. Introduction and Motivation: -

BSIM3 was developed in an effort to solve the problems of semi-empirical models and as a complement to BSIM 1-2. It has extensive built-in dependencies of important dimensional and process parameters such as channel length, width, gate oxide thickness, junction depth, doping concentration, and so on.

The model has evolved through three different versions. The first version forms the original basis for the model but had some severe mathematical problems. The second version was largely a correction of these mathematical difficulties, and several new parameters were introduced. The third version that we are going to discuss here has become an industry standard for modeling deep-submicron MOS technologies. The model is suitable for both digital and analog applications because of better modeling of the output conductance. It also offers binning parameters for improving the model fits for smaller devices.

The main motivation to prepare this report is to provide MOSIS customers with information that help to understand the MOSIS parameter extraction and optimization procedure. MOSIS SPICE parameters are obtained from electrical measurements on a selected wafer and using a commercial extraction and optimization tool (Silvaco UTMOST III).

We measure I-V data on a large array of test transistors included in the MOSIS process Monitor. Model parameters are extracted using this I-V data such that the simulated I-V results compare closely with the measured I-V data. A parameter extraction phase pays close attention to physical significance of the primary model parameters while the optimization phases focus on the correction parameters that make the model fit the full range of device sizes in a particular process. The resulting parameter accuracy is tested by simulating benchmark test circuits (inverter and ring oscillator) contained on the MOSIS Process Monitor and comparing simulation results with measurements.

One must keep in mind that the BSIM3V3.1 model is only partly physical. Its physical foundation is more than overpowered by the very large number non-physical correction parameters that are used to get the model to work over a large range of channel dimensions in a deep sub-micrometer process. Each parameter value can vary not only from one fabrication process to another (even at the same feature size) but also from run to run by reflecting the actual measured transistor characteristics.

2. Model Equations: -

2.1. Threshold and Subthreshold Regions:

A) In the strong inversion region, the current along the channel of the transistor is given by: [1,2]

$$Ids = \mu_{eff} C_{ox} \frac{W}{L + V_{ds}\mu_{eff}\frac{1}{2u_{sat}}} \frac{(V_{gs} - V_{th} - A_{bulk}V_{ds}/2)V_{ds}}{} \quad \text{---------(2.1.1)}$$

$$\textit{Where,}\quad A_{bulk} = (1 + \frac{K_1}{2\sqrt{f - V_{bseff}}}\left\{\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_j X_{dep}}}\left[1 - A_{gs}V_{gst}(\frac{L_{eff}}{L_{eff} + 2\sqrt{X_j X_{dep}}})^2\right] + \right.$$

$$\left. + \frac{B_0}{W_{eff} + B_1}\right\})\frac{1}{1 + KETA * V_{bseff}} \quad \text{---------(2.1.2)}$$

V_{th} is *the* Threshold Voltage:

$$V_{th} = V_{th0} + k_1(\sqrt{|f - V_{bseff}|} - \sqrt{|f|}) - k_2 V_{bseff} + k_1(\sqrt{1 + \frac{NLX}{L_{eff}}} - 1)\sqrt{f} + (k_3 + k_{3b}V_{bseff})\frac{T_{ox}}{W_{eff} + W_0} f -$$

$$- D_{vt0w}[\exp(-D_{vt1w}\frac{W_{eff} * L_{eff}}{2l_{tw}}) + 2\exp(-D_{vt1w}\frac{W_{eff} * L_{eff}}{l_{tw}})](V_{bi} - f) - D_{vt0}[\exp(-D_{vt1}\frac{L_{eff}}{2l_t}) +$$

$$+ 2\exp(-D_{vt1}\frac{L_{eff}}{l_t})](V_{bi} - f) -$$

$$- [\exp(-D_{sub}\frac{L_{eff}}{2l_{t0}}) + 2\exp(-D_{sub}\frac{L_{eff}}{l_{t0}})](Etao + Etab)V_{ds} \quad \text{-------(2.1.3)}$$

For large device sizes the above expression can be reduced in to:

$$V_{th} \cong V_{th0} + k_1(\sqrt{f - V_{bseff}} - \sqrt{f}) - k_2 V_{bseff}$$

V_{th0} is the ideal threshold voltage of a long channel device at zero volt substrate bias.

Where V_{bseff} is Substrate bias with upper limit. [1,2] $Vbs \le 0.9(f - \frac{k_1^2}{4k_2^2}) = V_{bc}$,

$$V_{bseff} = V_{bc} + 0.5[V_{bs} - V_{bc} - DELTA + \sqrt{(V_{bs} - V_{bc} - DELTA)^2 - 4 * DELTA * V_{bc}}] \text{---(2.1.3}b\text{)}$$

If we examine equation (2.1.1) for a very small drain/source voltage

(V_{ds} value $\cong 0.05V$), we will see that ($V_{ds}\mu_{eff}$) is much less than ($2u_{sat}$) *and* also ($\frac{A_{bulk}}{2}V_{ds}^{2}$) is much less than one.

That will lead equation (2.1.1) to become, $Ids \cong \mu_{eff} C_{ox} \frac{W(V_{gs}-V_{th})}{L} V_{ds}$

(This is the classic equation of channel current for MOS device in the linear region.)

Where μ_{eff} is the mobility and given by

$$\mu_{eff} = \frac{\mu_0}{1+(U_a + U_c * V_{bseff})(\frac{V_{gst}+2V_{th}}{T_{ox}}) + U_b(\frac{V_{gst}+2V_{th}}{T_{ox}})^2} \qquad \text{---------(2.1.4)}$$

Here μ_0 is the parameter which represents the low field mobility (ideal mobility of a large device). The coefficents U_a, U_b and U_c are parameters that represent the reduction of the channel mobility by the vertical field.

$$V_{gst} = \frac{2n * v_t \ln[1+\exp(\frac{V_{gs}-V_{th}}{2n*v_t})]}{1+2n*Cox\sqrt{\frac{2f}{q\varepsilon_{si}N_{ch}}}\exp(\frac{-V_{gs}+V_{th}+2V_{off}}{2n*v_t})} \qquad \text{---------(2.1.5)}$$

v_t is the thermal voltage, $v_t = \frac{K_b T}{q}$

From the above equation it is possible to show that for large V_{gs} value, $V_{gst} \cong V_{gs} - V_{th}$ and for Vgs less than V_{th}, V_{gst} will be proportional to [$\exp(V_{gs}-V_{th})$]

B) The drain current equation in the subthreshold region is given by the following:

$$I_{ds} = I_{so}(1-\exp(-\frac{V_{ds}}{v_t}))\exp(\frac{V_{gs}-V_{th}-V_{eff}}{n*v_t}) \qquad \text{-------(2.1.6)}$$

Where $I_{so} = \mu_o \frac{W}{L}\sqrt{\frac{q\varepsilon_{si}N_{ch}}{2f_s}}v_t$

$$n = 1 + N_{factor}\frac{C_d}{C_{ox}} + \frac{(C_{dsc} + C_{dscd}V_{ds} + C_{dscb}V_{bseff})[\exp(-D_{vt1}\frac{L_{eff}}{2l_t}) + 2\exp(-D_{vt1}\frac{L_{eff}}{l_t})]}{C_{ox}} +$$

$$+\frac{C_{it}}{C_{ox}} \qquad \text{-------(2.1.7)}$$

$$l_t = \sqrt{\frac{\varepsilon_{si}T_{ox}X_{dep}}{\varepsilon_{ox}}}(1 + D_{vt2}V_{bs}),\ \ l_{tw} = \sqrt{\frac{\varepsilon_{si}T_{ox}X_{dep}}{\varepsilon_{ox}}}(1 + D_{vt2w}V_{bs})\ \ \&\ \ l_{t0} = \sqrt{\frac{\varepsilon_{si}T_{ox}X_{dep}}{\varepsilon_{ox}}}$$

C) The drain current equation in the saturated region:

$$I_{ds} = W * C_{ox}(V_{gst} - A_{bulk}V_{dsat})v_{sat}(1 + \frac{V_{ds} - V_{dsat}}{V_A})(1 + \frac{V_{ds} - V_{dsat}}{V_{ASCBE}}) \qquad \text{------(2.1.8)}$$

Where $V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a}$

$a = A_{bulk}^2 R_{ds}C_{ox}Wv_{sat} + (\frac{1}{l} - 1)A_{bulk},\ b = -[V_{gst}(\frac{2}{l} - 1) + A_{bulk}E_{sat}L + 3A_{bulk}R_{ds}C_{ox}Wv_{sat}V_{gst}]$

$c = E_{sat}LV_{gst} + 2R_{ds}C_{ox}Wv_{sat}V_{gst}^2,\ l = A_1V_{gst} + A_2$

$E_{sat} = \frac{2v_{sat}}{\mu_{eff}}$, v_{sat} is the carrier saturated velocity.

$V_A = f(\text{PCLM}, \text{PDIBLC1}, \text{PDIBLC2}, \text{PDIBLCB}, \text{P}_{\text{vag}}, \text{DROUT})$ is called the early voltage.

$V_{ASCBE} = f(\text{PSCBE1}, \text{PSCBE2})$ is the early voltage due to the substrate current induced body effect.

Detail expression for $V_A \& V_{ASCBE}$ can be found in [1,2], here it is given as a function of the parameters.

2.2. The Effective Channel Length and Width: -

The effective channel length and width model in BSIM3v3.1 is:

$$L_{eff} = L_{drawn} + XL - 2L_{\text{int}} - \frac{2LL}{L^{LLN}} - \frac{2LW}{W^{LWN}} - \frac{2LWL}{L^{LLN}W^{LWN}}$$

$LL, LLN, LW, LWL \& LWN$ are the length parameter that represent the short channel effect.--(2.2.1)
XL is the difference between the drawn channel length on the layout and the printed length on the wafer.

$$W_{eff} = W_{drawn} + XW - 2W_{\text{int}} - \frac{2WL}{L^{WLN}} - \frac{2WW}{W^{WWN}} - \frac{2WWL}{L^{WLN}W^{WWN}} - 2DWG * V_{gst} + DWB(\sqrt{f_s - V_{bseff}} - \sqrt{f_s})$$

$WL, WLN, WW, WWN, WWL, DWG \& DWB$ are the width parameters that represent narrow channel effect.
XW is the difference between the drawn channel width on the layout and the printed width on the wafer.

Usually it is enough to extract $L_{\text{int}} \& W_{\text{int}}$ for long channel device.

$L_{eff} \cong L_{drawn} + XL - 2L_{\text{int}}$

$W_{eff} \cong W_{drawn} + XW - 2W_{\text{int}}$

L_{int} and W_{int} are parameters that represent reduction of the channel length and width of the device due to Source / Drain diffuse.

2.3. Source/Drain Parasitic Resistance: -

Model for the parasitic resistance is a simple expression using the channel current equation in the linear region:

$$I_{ds} = \frac{V_{ds}}{R_{tot}} = \frac{V_{ds}}{R_{ch} + R_{ds}}$$

R_{ch} is the channel resistance calculated from equation (2.1.1)

$$R_{ch} = \left[\frac{I_{ds}}{V_{ds}}\right]^{-1} = \left[\mu_{eff} C_{ox} \frac{W}{L + V_{ds}\mu_{eff}\frac{1}{2u_{sat}}} \frac{(V_{gs} - V_{th} - A_{bulk}V_{ds}/2)}{}\right]^{-1}$$

R_{ds} is the parasitic resistance and given by :

$$R_{ds} = \frac{R_{\text{dsw}}[1 + P_{rwg}V_{gst} + P_{rwb}(\sqrt{f_s - V_{bseff}} - \sqrt{f_s})]}{(10^{-6}W_{eff})^{W_r}} \qquad \text{-------(2.3.1)}$$

Where $R_{dsw}, P_{rwg}, P_{rwb}$ & W_r are the parasitic resistance parameters.

3. Junction Capacitance Model: -

The Source and Drain capacitance is divided into two components, namely the area junction capacitance per unit area and the perimeter junction capacitance per unit length.

The total junction capacitance C_{Jcap} is found from:

$$C_{Jcap} = C_{JA} * A + C_{JP} * P \qquad \text{-----(3.1)}$$

Where A is the total junction area.
P is the total junction perimeter.

The area junction capacitance $C_{JA} = C_J(1 + M_J \frac{V_{bs}}{P_b})$ if $V_{bs} > 0$

and $C_{JA} = C_J(1 - \frac{V_{bs}}{P_b})^{- M_J}$ if $V_{bs} < 0$ ----(3.2)

The perimeter junction capacitance $C_{JP} = C_{Jsw}(1 + M_{Jsw} \frac{V_{bs}}{P_{bsw}})$ if $V_{bs} > 0$

and $C_{JP} = C_{JSW}(1 - \frac{V_{bs}}{P_{bSW}})^{- M_{JSW}}$ if $V_{bs} < 0$ ----(3.3)

4. Parameter Extraction and Optimization Strategies: -

MOSIS is using the following data measurement procedures for parameter extraction and optimization on a large array of test transistors included in the MOSIS Process Monitor.

- I_{ds} *Vs* V_{gs} data @ V_{ds} = Low Voltage with different V_{bs} values.
- I_{ds} *Vs* V_{gs} data @ V_{ds} = High Voltage with different V_{bs} values.
- I_{ds} *Vs* V_{ds} data @ V_{bs} = Low Voltage with different V_{gs} values.
- I_{ds} *Vs* V_{ds} data @ V_{bs} = High Voltage with different V_{gs} values.
- *C Vs V* data (Junction capacitance Vs Voltage)

Additional electrical measurements on the MOSIS Process Monitor also determine values of the following parameters:

- T_{ox} ---(Gate oxide thickness.)
- *CGDO* ---(Gate to Drain overlap capacitance.)
- *CGSO* ---(Gate to Source overlap capacitance.)
- R_{sh} ---(Sheet Resistance.)

Parameter extraction for each process technology start with an initial set of parameters that comes from, 1) Vendor supplied models. 2) Previous MOSIS models. 3) Extracted models from physical fundamentals. Using these setup parameters with the above four extracted parameters from the MOSIS Process Monitor the following nine optimization strategies are implemented.[3] (Note: Interaction between parameters that are optimized in a given strategy is controlled by the maximum and minimum limit of each parameter. The strategy presented here is a standard optimization strategy and it may vary from one technology to the other.)

Strategy 1: (Parameters in Threshold and Subthreshold Regions)

This local strategy is applied for the wide W and long L device only and the parameters are those in equation (2.1.3), (2.1.4) & (2.1.7).

- Target parameters are $V_{th0}, \mu_0, U_a, U_b, U_c, K_1, K_2, N_{factor} \& V_{off}$
- It requires I_{ds} *Vs* V_{gs} data @ V_{ds} = Low Voltage with different V_{bs} values.

Strategy 2: (Threshold Shift effect parameters)

This local strategy is applied for the narrow W and long L device only and the parameters are those in equation (2.1.3)& (2.2.1)

- Target parameters are $W_{\text{int}}, K_3, DWG, DWB, WL, WLN, WW, WWN, W_0 \& K_{3b}$
- I_{ds} *Vs* V_{gs} data @ V_{ds} = Low voltage with different V_{bs} values required.

Strategy 3: (Threshold Shift and Channel Resistance effects parameters)

This local strategy is applied for the wide W and short L device only and the parameters are those in equation (2.1.3), (2.1.7), (2.2.1)& (2.3.1)

- Target parameters are $L_{\text{int}}, LL, LLN, LW, LWN, R_{dsw}, D_{vt0}, D_{vt1}, D_{vt2}, NLX, P_{rwg}$ & P_{rwb}
- I_{ds} Vs V_{gs} data @ V_{ds} = Low voltage with different V_{bs} values required.

Strategy 4: (Threshold Shift and Channel Resistance effects Binning parameters)

A good model result can be obtained for carefully chosen target device sizes, but the simulation characteristics vary widely from the actual device characteristics when the channel length and width are varied from large to very small device size. This problem is handled in approach known as Model Binning.

BSIM3v3.1 follow the following implementation for all those parameters listed in [1] that can be binned. As an example for parameter P,

$$P = P_0 + \frac{LP}{L_{eff}} + \frac{WP}{W_{eff}} + \frac{PP}{L_{eff} * W_{eff}} \qquad \text{----------(4.1)}$$

P_0 is parameter for the large device size.

LP is Binning parameter for the length variation.

WP is Binning parameter for the width variation.

PP is Binning parameter for the length times width variation.

This local optimization strategy is applied for the small device size only (short channel and narrow width.)

- Target Binning parameters are PV_{th0}, PR_{dsw} and PK_2
- I_{ds} *Vs* V_{gs} data @ V_{ds} = Low voltage with different V_{bs} values required.

Strategy 5: (Low Bias Drain Saturated Current parameters.)

This local optimization strategy uses different geometry and the parameters are those in equation (2.1.2), (2.1.8), & (4.1).

- Target parameters are A_0, v_{sat}, B_1, Pv_{sat}, B_0, & A_{gs}
- I_{ds} *Vs* V_{ds} data @ V_{bs} = Low Voltage with different V_{gs} values required.
- For parameters A_0 & A_{gs} use wide W & long L device.
- For parameter v_{sat} use wide W & short L devices.
- For parameters B_0 & B_1 use narrow W & long L devices.
- For the Binning parameter Pv_{sat} use small size devices.

Strategy 6: (Low Bias Output Resistance Parameters)

The output resistance local optimization is the most difficult one and the user should careful in including or excluding certain device sizes. This strategy is usually applied for the short channel devices together with the long channel. If the wide W and long L device become the dominant factor for the optimization, this device can be excluded. This strategy and strategy #5 should be executed one after another several times to get a good result. The parameters that are going to be optimized in this strategy are those in equation (2.1.3), (2.1.3b) & (2.1.8).

- Target parameters are $PCLM$, $PDIBLC1$, $PDIBLC2$, P_{VAG}, $DROUT$, $DELTA$, $PSCBE1$, $PSCBE2$, $ETA0$, & $DSUB$.

- *RDS Vs* V_{ds} data @ V_{bs} = Low Voltage with different V_{gs} values required.

Strategy 7: (High Bias Drain Saturated Current parameters)

This local optimization strategy uses different geometry and the parameters are those in equation (2.1.2) & (4.1).

- Target parameters are KETA, WKETA, LKETA, and PKETA.
- I_{ds} *Vs* V_{ds} data @ V_{bs} = High Voltage with different V_{gs} values required.
- For parameter KETA use wide W & long L device only.
- For binning parameter WKETA use narrow W & long L devices only.
- For binning parameter LKETA use wide W & short L devices only.
- For Binning parameter PKETA use small devices only.

Strategy 8: (High Bias Output Resistance Parameters)

This local optimization strategy is usually applied for the short channel devices together with the long channel and the parameters that are going to be optimized in this strategy are those in equation (2.1.3) & (2.1.8).

- Target parameters are ETAB and PDIBLCB.
- RDS Vs V_{ds} data @ V_{bs} = High voltage with different V_{gs} values required.

Strategy 9: (Junction Capacitance Parameters)

This global optimization strategy uses the junction capacitance data to optimize the parameters listed in equation (3.2) & (3.3). Junction capacitance verses voltage measurements are taken on two junction capacitors: One with an area dominated structure and the other with a perimeter-dominated structure.

- Target parameters are C_J, M_J, P_b, C_{JSW}, M_{Jsw}, and P_{bSW}

5. References: -

[1] Department of Electrical Engineering and Computer Sciences University of California, Burkeley. "BSIM3v3 Users' Manual (Final Version), "1996.

[2] Daniel Foty, "Mosfet Modeling with Spice, " Prentice - Hall, Inc. 1997.

[3] Silvaco Simulation Standard, "Local Optimization Templates for Extracting BSIM3v3.1 Parameters in UTMOST III." VOL 9, No 1, January 1998.