Single Event Upsets in Deep-Submicrometer Technologies Due to Charge Sharing

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***Abstract*—Circuit and 3-D technology computer aided design mixed-mode simulations show that the single event upset vulnerability of 130- and 90-nm hardened latches to low linear energy transfer (LET) particles is due to charge sharing between multiple nodes as a result of a single ion strike. The low LET vulnerability of the hardened latches is verified experimentally.**

***Index Terms*—Alpha particles, charge sharing, dual interlocked cell (DICE) latch, neutrons, parasitic bipolar transistor, radiation hardened by design, single event circuit characterization, single event upset (SEU).**

I. Introduction

THE NODAL charge to represent a logic state is steadily decreasing with decreasing technology feature size. Many methods have been developed to increase the charge requirement for storage elements, thereby reducing the soft error rates [1]–[3]. Additionally, design-based approaches are in use that utilize redundant storage nodes to retain data [4]. Such designs are considered single event upset (SEU) immune for low energy ions because a single ion hit at a storage node does not cause an upset. However, such designs are vulnerable to single-event ion hits that result in multiple nodes collecting charge as observed in SRAM designs by Velazco *et al.* [5]. For deep-submicrometer technologies, the proximity of circuit nodes results in charge collection at multiple nodes from a single ion strike (i.e., charge sharing) [6]–[8].

In this paper, circuit and 3-D technology computer aided design (TCAD) mixed-mode simulations are used to characterize charge sharing between sensitive pairs of devices and the resulting upsets in a hardened storage cell for commercial 130- and 90-nm twin-well bulk CMOS processes. The simulation results were verified with experimental data showing upsets due to charge sharing in hardened latch design for both technology nodes when exposed to low energy ions.

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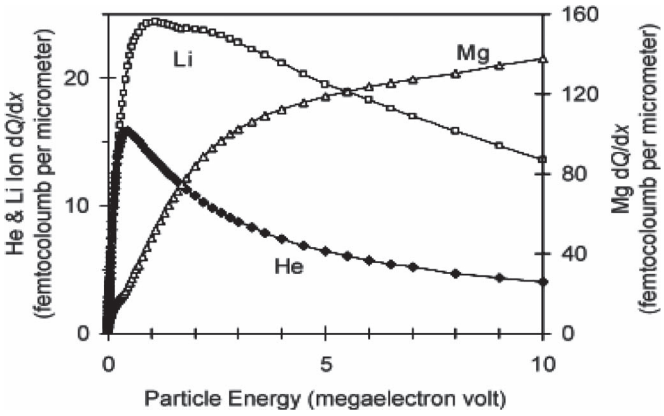

Fig. 1. LET converted into charge generation per linear distance for some ions in silicon [9].

II. Background

The ground-level radiation environment is dominated by alpha particles and neutrons. The alpha particles of concern are those emitted by the packaging materials which typically range from 4 to 6 MeV [9]. Recent work has verified the substantial increase of device susceptibility to alpha particles [10]. The increased purity of materials used in packaging has reduced the alpha emission rates from rates as high as 100 α/h cm^2 down to levels below 0.001 α/h cm^2 [9]. However, secondary reactions producing alpha particles are still a concern. Neutrons themselves do not cause direct ionization in silicon; however, the inelastic interaction of neutrons with silicon does generate energized particles. Such particles (typically Mg, Li, or Al and protons or secondary alpha's) have higher energy than alpha particles and are capable of generating enough electron–hole pairs (EHPs) through direct ionization to cause an upset.

Fig. 1 [9] shows the charge generation per linear distance for Al, Mg, and Li particles in silicon. The neutron-generated ion particle energy ranges from 1 to 10 MeV, as shown in Fig. 1. The amount of charge deposited at such energy ranges is on the order of tens to hundreds of femtoCoulomb (fCs). For advanced technologies at such high charge deposition, the physical proximity of devices may result in these particles traversing through multiple sensitive volumes resulting in multiple nodes collecting charge. For terrestrial radiation environment,

the multiple node charge collection can be due to neutron-generated particles which can result in multiple particle tracks and alpha particles which traverse at very oblique angles. For space environment, the multiple node charge collection can be attributed to the long track length from highly energetic ions coming in at an angle.

This paper examines the parameters affecting charge sharing due to single event between adjacent devices. Based on 3-D TCAD simulations, two different latch designs were fabricated at 130- and 90-nm technology nodes and exposed to ions to verify that charge sharing was responsible for causing upsets in hardened latch designs. The presence of charge sharing in these advanced technologies will require additional design rules to reduce soft errors.

III. Charge Sharing

Charge sharing is of concern for deep-submicrometer technologies due to higher packing densities, reduced nodal charge, and reduced spacing between devices. For the following charge-sharing discussion, the *struck node* is defined as the *active node*, and the *adjacent node* sharing charge is defined as the *passive node*. The 3-D TCAD devices used in the charge-sharing study were calibrated commercial 130- and 90-nm twin-well option bulk CMOS devices and were simulated in the OFF-state [8]. The drain of the active device was struck at normal angle (0°) using ions with different linear energy transfer (LET) values, and the resulting charge collection at the drain of the passive node was monitored. LET is typically used instead of mega-electronvolts for an incident ion as it is a better representative of the severity of an ion hit. LET is defined as the energy loss per unit path length, normalized by the density of the material. A calculation of the charge deposited per unit length can be determined if the LET of the ion, the average energy needed to create an EHP for a material, and the density of the material are known [11], [12].

Fig. 2(a) [8] shows simulation results for charge sharing between two PMOS devices in an n-well for 130-nm process (similar trends were observed for two NMOS devices), and Fig. 2(b) shows charge sharing between two NMOS devices in a p-well for 90-nm process (similar trends were observed for two PMOS devices). Charge sharing between NMOS and PMOS devices in different wells was minimal for the low LETs at both technology nodes [8]. These simulation results show that with decreasing distance between an active device and a passive device, the amount of charge collected on the passive device increases. These curves clearly show the need for understanding charge-sharing effects in advanced technologies.

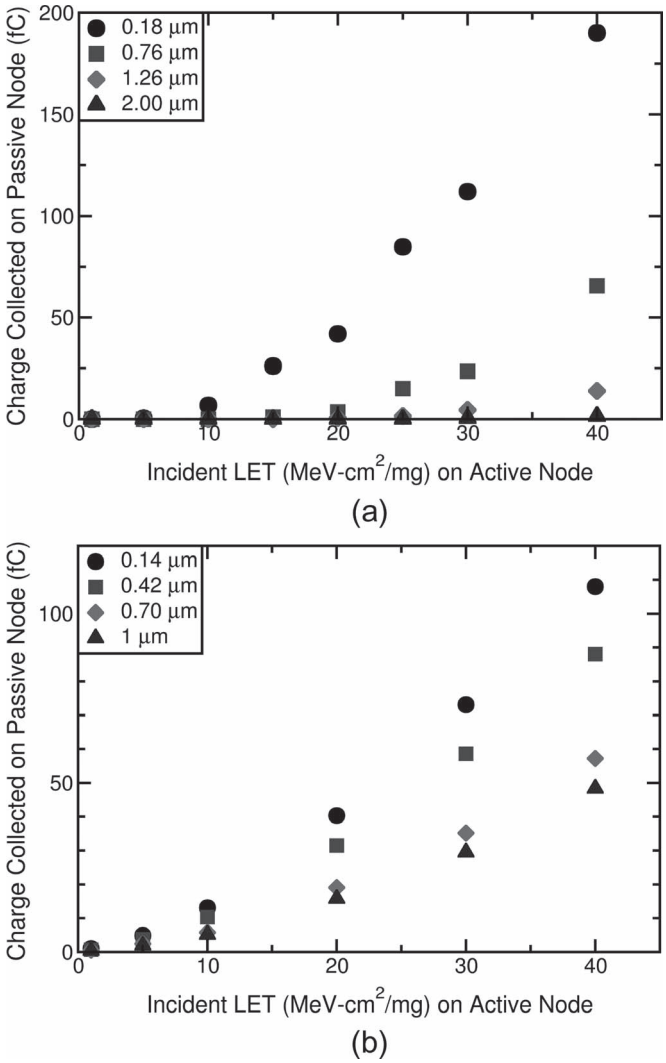

Fig. 2. (a) Nodal separation of two PMOS devices (active/passive); passive device shows an increase in charge collection with decreasing distance between the devices in a commercial 130-nm technology [8]. (b) Nodal separation of two NMOS devices (active/passive); passive device shows an increase in charge collection with decreasing distance between the devices in a commercial 90-nm technology [8].

IV. Upsets Due to Charge Sharing

The experimental verification for the presence of charge sharing must be done indirectly due to the extremely short time periods of single-event transients involved. The technique used for this paper involves a latch design that does not upset when a single node collects charge, but upsets when multiple nodes collect charge. This design, called dual interlocked cell (DICE), is shown in Fig. 3 [4]. The conventional latch design involves

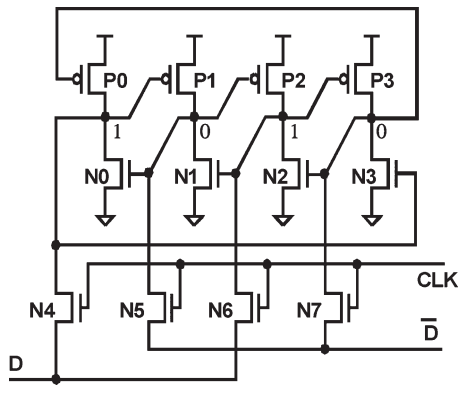

Fig. 3. DICE latch circuit: Interlocked design and use of redundant information storage make it hardened to single node charge collection upsets [4].

two storage nodes with back-to-back connected inverters (or NAND or NOR gates). DICE design has four storage nodes with four interconnected inverters (or NAND or NOR gates). The

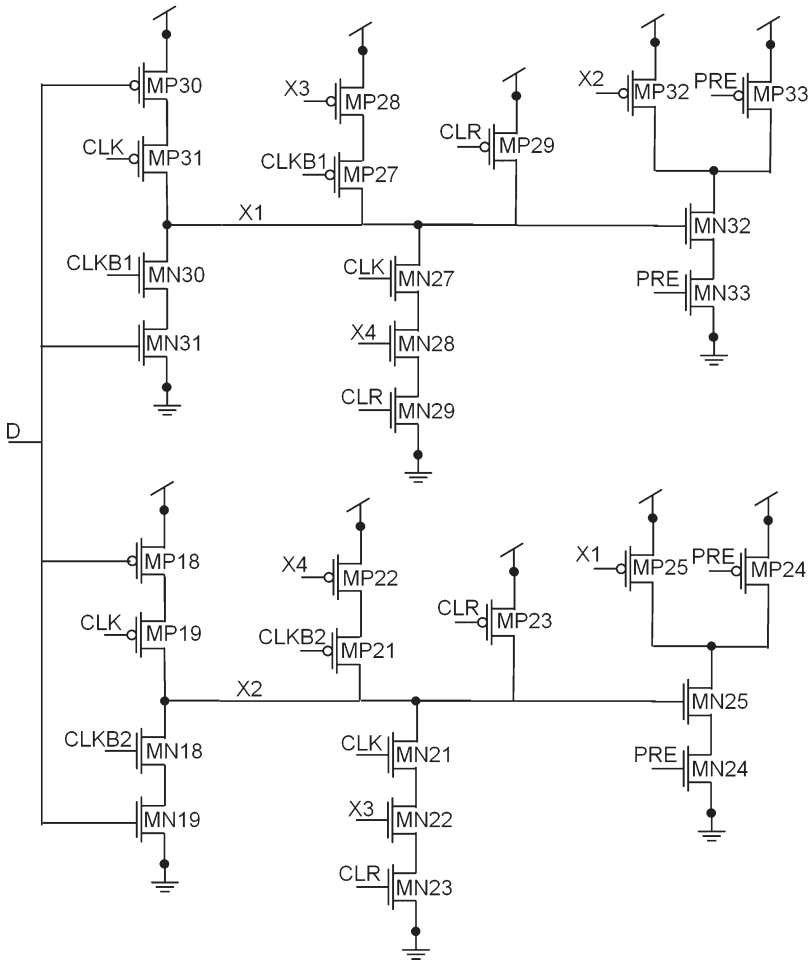

Fig. 4. Master stage of NAND-based DICE cell [13].

presence of four storage nodes and interlocked design requires changes in more than one storage node voltage to write into the cell. Typically, all four storage nodes are written into for improved write time. The advantage of this design is that when only one storage node voltage is changed, the time required for this voltage to propagate through the remaining three storage nodes is very high. As a result, for all practical purposes, DICE design is considered immune to an upset when only one of the storage nodes is perturbed. Fig. 4 [13] shows the master stage of NAND-based DICE flip-flop design used in this paper.

An exhaustive set of single-node hit circuit-level simulations was conducted on the 130- and 90-nm DICE latches using Cadence Spectre circuit simulator to confirm that a single-node hit will not cause an upset for the DICE latch shown in Fig. 4. The simulations were conducted using the double-exponential current pulse [11] with a rise time of 7 ps, a fall time of 200 ps, and the peak current adjusted to vary the charge deposited on the node from 1 fC to 1 pC. The simulation results from the single-node hit confirmed the hardness of the DICE latch to single-node hit upsets.

For charge-sharing simulations, layouts of a clocked DICE latch were generated using commercial 130- and 90-nm technology design rules. By using these layouts and an exhaustive set of circuit simulations, sensitive pairs of devices in physical proximity were identified. Sensitive pairs are defined as two transistors that, upon simultaneous charge collection, cause the DICE latch to upset. To identify such sensitive pairs, exhaustive circuit simulations were carried out for the following four possible input states:

1) when data (D in Fig. 4) are high and clock is high;
2) when data are high and clock is low;
3) when data are low and clock is high;
4) when data are low and clock is low.

The double-exponential current pulse was used to inject charge at the drain of the sensitive pairs and the required charge at each node to cause an upset recorded. The DICE latch design consisted of 66 transistors, which resulted in 4356 sensitive pairs for each input state. As charge sharing is a strong function of layout, and the layout may contain any of these nodes in physical proximity, all possible combinations of sensitive pairs were simulated. The circuit simulations identified a total of 124 unique pairs of sensitive devices; 48 of which are PMOS–NMOS pairs, 56 are PMOS–PMOS pairs, and 20 are NMOS–NMOS pairs. These sensitive pairs are due to the circuit function and are independent of the layout of the DICE latch.

The generated layout of the 130- and 90-nm DICE latches was used to identify the sensitive pairs of transistors that were in physical proximity to each other. It should be noted that the generated DICE layouts are used for the heavy-ion experiments

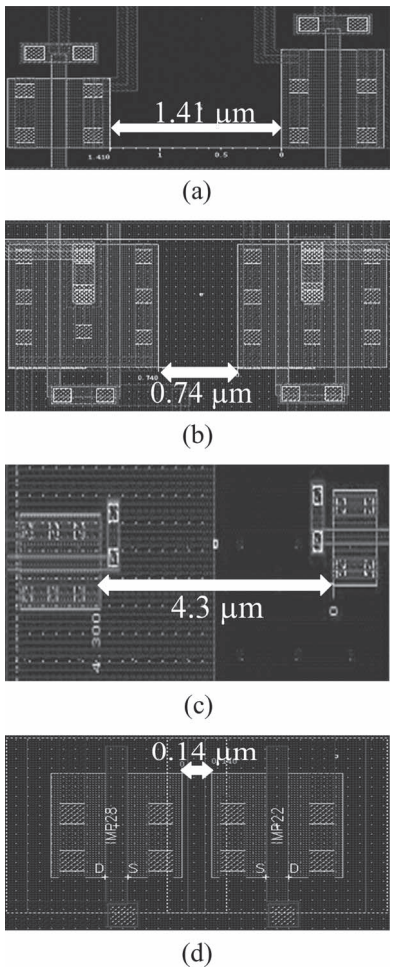

Fig. 5. (a) Excerpt showing the layout proximity of sensitive NMOS pair MN28–MN18 in the 130-nm DICE layout with a nodal separation of 1.41 μm. (b) Excerpt showing the layout proximity of sensitive PMOS pair MP28–MP22 in the 130-nm DICE layout with a nodal separation of 0.74 μm. (c) Excerpt showing the layout proximity of sensitive PMOS–NMOS pair MP25–MN30 in the 130-nm DICE layout with a nodal separation of 4.3 μm. (d) Excerpt showing the layout proximity of sensitive PMOS pair MP28–MP22 in the 90-nm DICE layout with a nodal separation of 0.14 μm.

described in the later section. Four case-study sensitive pairs were selected.

1) NMOS pair (MN18 and MN28) selected for 130-nm case study with nodal separation of 1.41 μm, as shown in Fig. 5(a)—this pair of devices was sensitive when data were low and clock was high.
2) PMOS pair (MP22 and MP28) selected for 130-nm case study with nodal separation of 0.74 μm, as shown in Fig. 5(b)—this pair of devices was sensitive when both data and clock are high.
3) PMOS–NMOS pair (MP25 and MN30) selected for 130-nm case study with a nodal separation of 4.3 μm, as shown in Fig. 5(c)—this pair of devices was sensitive when both data and clock are high.
4) PMOS pair (MP22 and MP28) selected for 90-nm case study with a nodal separation of 0.14 μm, as shown in Fig. 5(d)—this pair of devices was sensitive when both data and clock are high.

For 90-nm pair, only one sensitive pair was selected for illustration, as the same circuit was used for 130 and 90 nm, and the upset mechanism is consistent for both technology nodes. SE simulations were used to generate SHMOO plots for the four selected sensitive pairs, as shown in Fig. 6(a)–(d). The charge contours in this figure show an upset region with the amount of charge needed on each transistor to cause an upset in the DICE latch. It should be noted that the charge contours are an approximation due to the use of a constant pulsewidth for the varied charge depositions.

The next step was to use 3-D calibrated models to determine the amount of charge collected on both the active and passive nodes as a result of charge sharing. The model structures were developed using Synopsys TCAD tools [14] and calibrated to match electrical characteristics of the commercial 130- and 90-nm twin-well bulk CMOS using structural information available from multiple sources [15], [16]. Both the active and passive devices were included in the 3-D TCAD model with physical dimensions shown in Fig. 7(a)–(d). The simulations were conducted in mixed-mode environment with the charge-sharing devices in 3-D TCAD and the DICE subcircuit in the 130- and 90-nm compact models. It should be noted that the case-study sensitive pairs used in the 3-D TCAD mixed-mode simulations match the dimensions used in the respective DICE layouts.

The devices are simulated in the OFF-state, the drain of the active device was struck using different LET values, and the resulting charge collection at both device nodes was monitored. Current pulses at both the active and passive nodes were integrated in the 3-D TCAD mixed-mode simulations to obtain the total amount of charge collected by each node. Simulations were carried out not only for normal single-event strikes but also for 45° and 60° angle strikes. The angles used were selected such that the ion would hit the drain of the active device and pass under the passive device to yield a worst case scenario estimate.

The tables below show the results for the 3-D TCAD mixed-mode simulations. Results indicate that charge sharing occurs more readily between devices in the same wells (i.e., from PMOS to PMOS and NMOS to NMOS), as shown in Tables I–III, with very little charge sharing occurring across a well boundary (i.e., between PMOS and NMOS), as shown in Tables IV and V. Similar effects have been shown by Olson *et al.* [6], and recent papers succeeding this work have further validated these findings [17], [18]. As expected, the amount of charge collected by the active node is high for ions hitting the node at 0° (perpendicular to the plane of Si substrate). The amount of charge collected by the active node in such cases is high due to drift, diffusion, and the turn on of parasitic bipolar transistor formed by the source, drain, and channel [8]. For angular hits, there is an increase in the amount of charge collected on the passive device due to the ion track path passing directly underneath the passive device [19]. The 3-D TCAD mixed-mode simulations clearly show that low LET particles may cause enough charge collection at sensitive node pairs to cause an upset in the DICE latch, as shown in the SHMOO plots of Fig. 6(a)–(d).

V. Experiment

A test chip utilizing an array of the conventional D-type flip-flop (DFF) cells and DICE cells was designed in a shift register

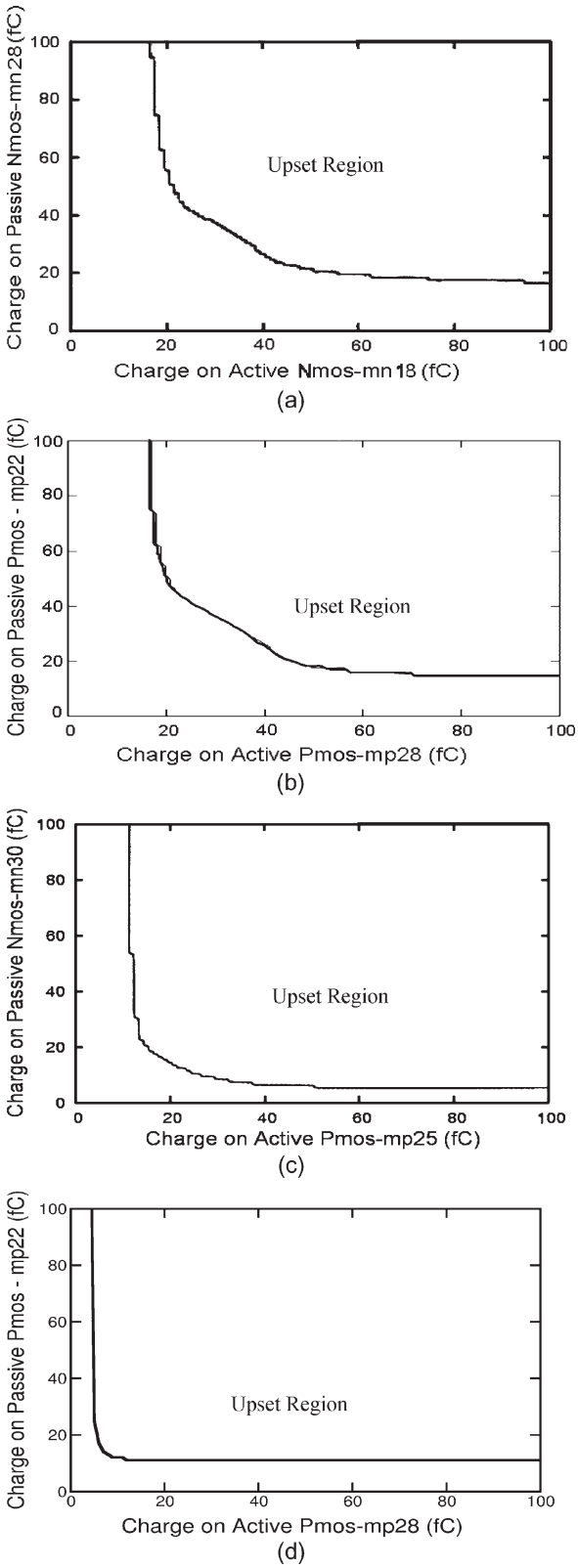

Fig. 6. (a) Upset/no-upset SHMOO plot for sensitive NMOS pair MN28–MN18 quantifies the charge sharing necessary for upset in the 130-nm DICE latch. (b) Upset/no-upset SHMOO plot for sensitive PMOS pair MP28–MP22 quantifies the charge sharing necessary for upset in the 130-nm DICE latch. (c) Upset/no-upset SHMOO plot for sensitive PMOS–NMOS pair MP25–MN30 quantifies the charge sharing necessary for upset in the 130-nm DICE latch. (d) Upset/no-upset SHMOO plot for sensitive PMOS–PMOS pair MP28–MP22 quantifies the charge sharing necessary for upset in the 90-nm DICE latch.

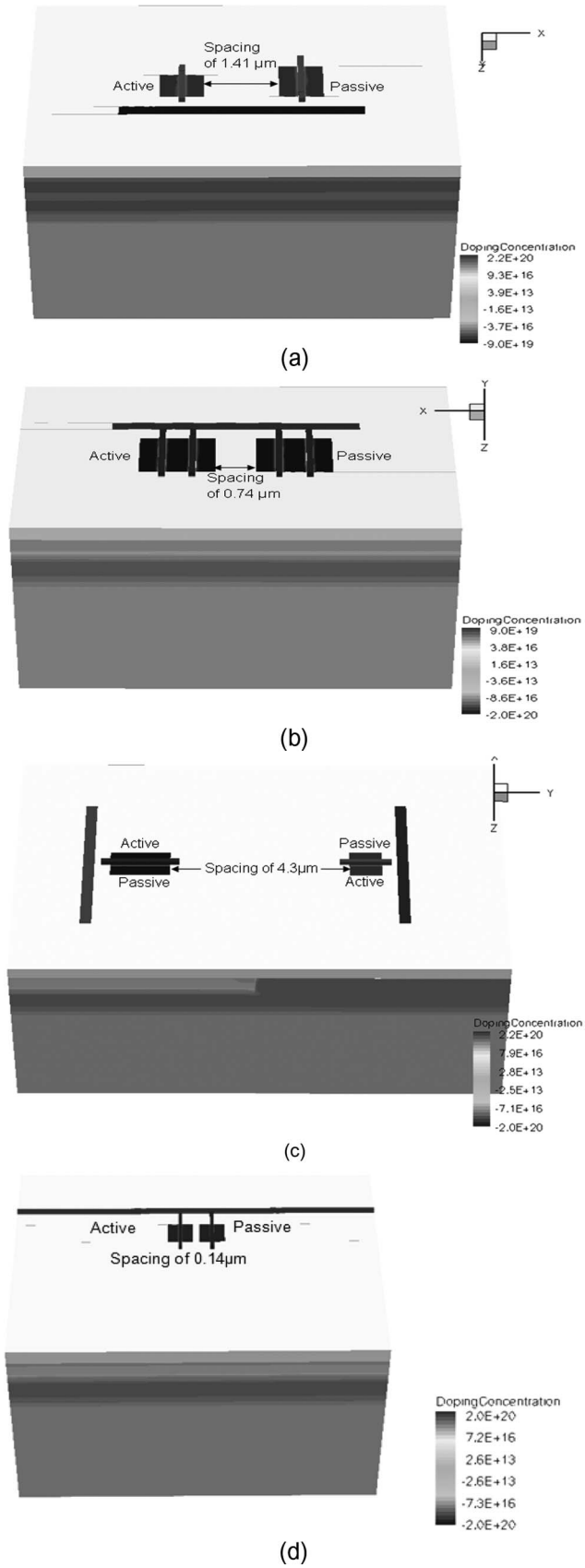

Fig. 7. (a) 3-D TCAD layout of simulated 130-nm NMOS pair with a nodal separation of 1.41 μm. (b) 3-D TCAD layout of simulated 130-nm PMOS pair with a nodal separation of 0.74 μm. (c) 3-D TCAD layout of simulated 130-nm PMOS–NMOS pair with a nodal separation of 4.3 μm. (d) 3-D TCAD layout of simulated 90-nm PMOS pair with a nodal separation of 0.14 μm.

TABLE I
CHARGE COLLECTED FOR NORMAL AND ANGLED HITS ON 130-nm NMOS PAIR

	LET (MeV-cm^2/mg)/Angle and total amount of charge collected (fC)				
	9.74 @60°	21.33 @0°	21.33 @60°	31.3 @0°	31.3 @45°
Active	48	221	110	333	227
Passive	35	9	81	14	93

TABLE II
CHARGE COLLECTED FOR NORMAL AND ANGLED HITS ON 130-nm PMOS PAIR

	LET (MeV-cm^2/mg)/Angle and total amount of charge collected (fC)				
	9.74 @60°	21.33 @0°	21.33 @60°	31.3 @0°	31.3 @45°
Active	106	474	378	779	484
Passive	118	42	254	119	254

TABLE III
CHARGE COLLECTED FOR NORMAL AND ANGLED HITS ON 90-nm PMOS PAIR

	LET (MeV-cm^2/mg)/Angle and total amount of charge collected (fC)			
	3.45 @0°	3.45 @60°	21.33 @0°	21.33 @60°
Active	17	18	68	72
Passive	4	15	37	95

TABLE IV
CHARGE COLLECTED FOR NORMAL AND ANGLED HITS ON 130-nm NMOS (ACTIVE)–PMOS (PASSIVE) PAIR

	LET (MeV-cm^2/mg)/Angle and total amount of charge collected (fC)				
	9.74 @60°	21.33 @0°	21.33 @60°	31.3 @0°	31.3 @45°
Active	73	229	172	337	344
Passive	0	0	16	0	0

TABLE V
CHARGE COLLECTED FOR NORMAL AND ANGLED HITS ON 130-nm PMOS (ACTIVE)–NMOS (PASSIVE) PAIR

	LET (MeV-cm^2/mg)/Angle and total amount of charge collected (fC)				
	9.74 @60°	21.33 @0°	21.33 @60°	31.3 @0°	31.3 @45°
Active	188	339	468	546	668
Passive	0	0	2	0	0

fashion and fabricated in commercial 130- and 90-nm CMOS technologies. Multiple shift registers were placed in parallel to isolate clock hits from individual node hits in both the DFF and DICE shift registers (clock line hits will result in upsets for all shift registers; individual hits will result in upsets in a single shift register). The designs were generated such that DFF cells would be vulnerable to the single and multiple node charge collections. The DICE cells, on the other hand, should not be vulnerable to the single node charge collection, but are vulnerable to the multiple node charge collection due to charge sharing. The DICE cell used in the experiment is the same DICE cell (Fig. 4) used in the circuit simulations and 3-D TCAD simulations as discussed in Section IV. The DICE cell layout is the same as the layout used for the 3-D TCAD simulations, with layout excerpts shown in Fig. 5(a)–(d) and 3-D TCAD matching versions shown in Fig. 7(a)–(d).

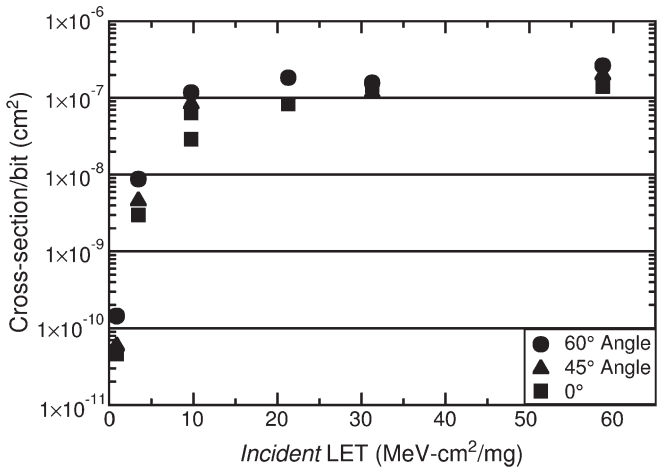

Fig. 8. DFF cross section of 130 nm; the upset threshold is well within the LET range for alpha particles and neutron-generated particles.

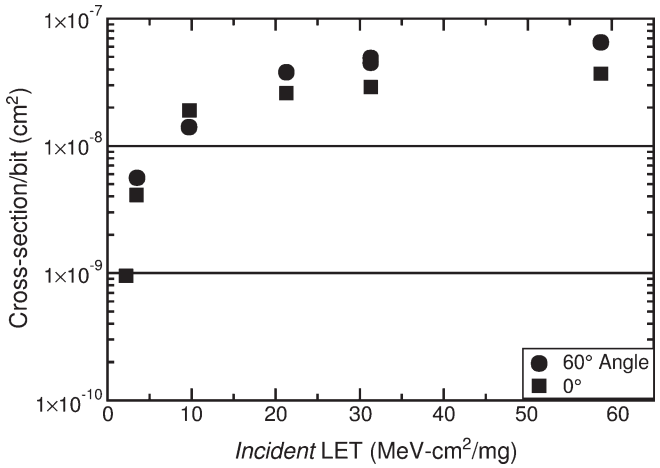

Fig. 9. DFF cross section of 90 nm; the upset threshold is well within the LET range for alpha particles and neutron-generated particles.

These designs were exposed to heavy ions at the Lawrence Berkeley National Laboratory. The ions used were argon, copper, xenon, neon, oxygen, boron, and krypton with LET ranging from 0.87 to 58.72 MeV $\cdot$ cm^2/mg. The angles used for exposure were 0°, 45°, and 60° from normal. Figs. 8 and 9 show the DFFs to be very vulnerable to low LET ions, and the upset threshold is well within the alpha particles and neutron-generated particle LET range. Due to the hardened nature of DICE cells and the low LET of particles, no upsets were expected except as a result of charge sharing between sensitive pairs. Figs. 10 and 11 show that the DICE cell upsets for LETs as low as 9.74 MeV $\cdot$ cm^2/mg for 130 nm and 3.45 MeV $\cdot$ cm^2/mg for 90-nm process. These upsets were consistent throughout the experiments and confirm the vulnerability of a hardened cell to SEU as a result of charge sharing between two sensitive nodes as shown in the circuit and 3-D mixed-mode simulation results.

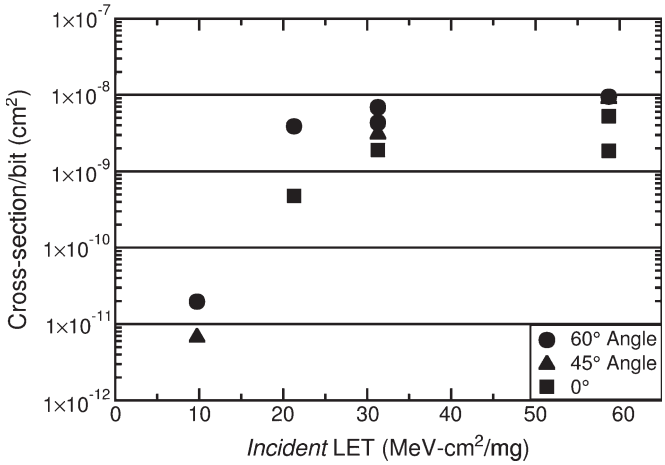

Fig. 10. Cross section of 130 nm shows the DICE upsets at LET values well below theoretical expectations and within the LET range for Mg.

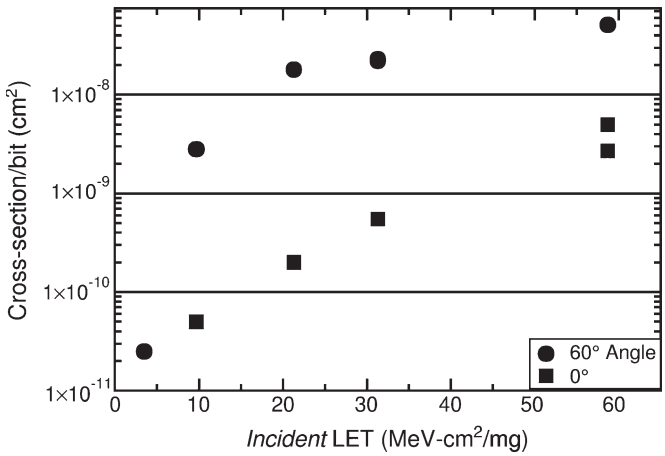

Fig. 11. Cross section of 90 nm shows the DICE upsets at LET values well below theoretical expectations and within the LET range for alpha particles and neutron-generated particles.

VI. Conclusion

Charge sharing is of major concern for deep-submicrometer technologies due to scaling trends such as reduced nodal charge, higher packing densities, and reduced spacing between devices. By using circuit-level and 3-D mixed-mode TCAD simulations, charge sharing is shown to make a hardened cell (DICE) vulnerable to SEU at low LET as a result of charge collection between a hit node and an adjacent device in proximity. The increased vulnerability of the hardened cell makes it susceptible to alpha particles and neutron-generated particles.

Experimental results at 130 and 90 nm confirm the predictions from simulation that unhardened latches are vulnerable to particles with terrestrial energies and that even DICE latches exhibit much lower threshold for the upset cross section owing to the charge-sharing effect. Charge sharing will be a growing problem as technology scales and devices get closer and require less charge to upset. The use of careful design layout (separating sensitive pairs in the layout design) and mitigation techniques such as guard rings [8] can help increase the SE hardness of this cell and other cells in a given design library.

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