Neutron-Induced Single Event Upsets in Static RAMS Observed at 10 KM Flight Altitude

J. Olsen, P. E. Becher, P. B. Fynbo, P. Raaby, and J. Schultz

Abstract—**Neutron induced single event upsets (SEUs) in static memory devices (SRAMs) have so far been seen only in laboratory environments. We report observations of 14 neutron induced SEUs at commercial aircraft flight altitudes as well. The observed SEU rate at 10 km flight altitude based on exposure of 160 standard 256 Kbit CMOS SRAMs is $4.8 \cdot 10^{-8}$ upsets/bit/day. In the laboratory 117 SRAMs of two different brands were irradiated with fast neutrons from a Pu-Be source. A total of 176 SEUs have been observed, among these are two SEU pairs. The upset rates from the laboratory tests are compared to those found in the airborne SRAMs.**

Introduction

The PERFORM system is a computer and software used in the cockpit of commercial aircraft for calculation of aircraft take-off performance data (weight, speed, etc.), developed and sold by DataFlight Europe (DFE). The hardware is a commercially available battery powered handheld computer used in two versions with respect to the SRAMs. (See Table I.)

All program code (approximately 500 Kb) is stored in the CMOS SRAM chips backed up by a NiCd battery.

The PERFORM system was used (in the Mk 1 version) by a major airline for intercontinental flights. The system was permanently installed in the cockpit and only removed occasionally by maintenance personnel.

After the PERFORM system had been in operational use on board the aircraft for some time bit errors occurred in the SRAMs. The PERFORM system was immediately suspended from operational use and the hardware was tested by the computer manufacturer according to RTCA/DO-160C [1]. The software was tested by DFE and finally a special version of the PERFORM system was developed and installed for test purposes on board a number of aircraft for more than six months.

The result was that all the test systems on board aircraft within one to three weeks showed the same error pattern as that found the first time (i.e., one, two or at most three bit flips). However, it was not possible to reproduce the error pattern in ground-based laboratory tests performed by the computer manufacturer and by DFE.

Manuscript received July 8, 1992; revised November 16, 1992.
J. Olsen was with the Nuclear Safety Research Department, Risø National Laboratory, DK-4000 Roskilde, Denmark. He is now retired.
P. E. Becher and P. B. Fynbo are with the Nuclear Safety Research Department, Risø National Laboratory, P.O. Box 49, DK-4000 Roskilde, Denmark.
P. Raaby and J. Schultz are with DataFlight Europe A/S, Birkerød Kongevej 44, DK-3460 Birkerød, Denmark.
IEEE Log Number 9207319.

TABLE I
PERTINENT DATA FOR THE TWO VERSIONS OF SRAMS IN THE COMPUTERS

Computer	SRAM Size	SRAM device	Technology
Mk 1	$16 \cdot 32K \cdot 8bit$	D43256 A6U-15LL	1.3 μm CMOS[1]
Mk 2	$7 \cdot 128K \cdot 8bit$	HM628128LR12	0.8 μm CMOS[1]

[1] n-channel memory cells with polysilicon resistors.

After more than six months of testing DFE contacted Risø National Laboratory (RNL). Within a short time RNL reproduced the bit error pattern that was seen in the airborne systems. This was done by irradiation of the computer by fast neutrons, whereas gamma radiation from Co-60 (approximately 0.5 Gy) induced no errors.

After this experience DFE developed a special test system and RNL continued to test the Mk 1 computers. Later, the Mk 2 version was included in the laboratory testing but not in the flight testing. This paper deals with results from the tests and includes a discussion of the results.

Radiation Environment at 10 km Altitude

Primary cosmic rays mainly consist of protons. However, alpha particles and heavier nuclei are also present. Neutrons are not present because of their short half-life. They are, however, produced in the atmosphere as secondary products by the primary cosmic radiation interacting with nitrogen and oxygen. As the main body of a modern civil aircraft is made of aluminum thicker than 1 mm and the penetration range of protons in aluminum is less than 1 mm for energies up to 10 MeV, it is expected that only neutrons will give a major contribution to SEUs.

According to UNSCEAR [2] the neutron flux at ground level is $8 \cdot 10^{-3}$ n/cm²/s. No information is given on the neutron spectrum. From data on absorbed dose index rates in [2] one can estimate the neutron flux at flight altitude and 50° geomagnetic latitude to be 200–400 times that at ground level, i.e., 2–3 n/cm²/s.

Nakamura *et al.* [3] give measured and calculated data for the neutron spectrum at various altitudes. The measured neutron flux below 10 MeV is roughly 0.8 n/cm²/s

0018-9499/93$03.00

at flight altitude and 24° geomagnetic latitude. This value compares fairly well with the flux value (2–3 $n/cm^2/s$) just inferred from [2], as we obtain the value 2 $n/cm^2/s$ by correcting for geomagnetic latitude [3]. Also heavy ions can contribute to the upsets, but since the atmospheric depth at 10 km altitude is about 270 g/cm^2, that is, ten times the mean interaction length for carbon or oxygen, and heavier ions are attenuated still stronger, it is expected that heavy ions are of minor importance at 10 km altitude.

Neutron Induced Processes in Silicon Chips

Neutrons have no charge and therefore they do not give rise to direct ionization when they penetrate silicon. They can only be stopped by interaction with nuclei. Two different kinds of processes in the silicon are of interest:

1) Elastic or inelastic scattering in the silicon. The energy of the neutron is transferred to a silicon nucleus (the recoil nucleus) which generates a large number of electron-hole pairs.
2) If the energy of the neutron is above a certain threshold value a proton or an alpha particle may escape from the nucleus. In this case both the recoil nucleus and the light particle will generate a large number of electron-hole pairs.

Alpha particles and protons can travel relatively long distances in silicon: for example, a 10 MeV alpha particle has a range of 70 μm. Therefore many light particles are assumed to have a range much greater than the device active volume and pass out of the silicon doing no damage. Heavy recoiling particles have a range which is only a fraction of a μm and are expected to give rise to most of the SEUs.

The calculations of SEUs are most conveniently carried out in terms of the burst generation rate concept introduced by Ziegler and Lanford [4]. This concept has also been used by Normand *et al.* [5], [6]. The burst generation rate in units of $cm^2/\mu m^3$, is defined as the macroscopic cross section for production of recoiling nuclei with energies greater than some specified energy. The SEU rate is obtained when BGR is integrated over the energies of the incoming neutron flux and the "active" volume of the silicon, where the charge is deposited.

Assuming that the relaxation time for recombination of electron-hole pairs is much smaller than the typical time between SEUs, the upsets follow the same law as radioactive decay. Accordingly, the probability that a memory element, known not to have failed at time t has still not failed at time $t + \tau$ is $\exp(-\lambda \cdot \tau)$, where λ is a parameter that depends on the experiment (type of chip, intensity of radiation, etc.).

In particular, the time between SEUs follows the same distribution. The mean time between SEUs is λ^{-1} and the number of SEUs in a time Δt is Poisson distributed with mean value and variance both equal to $\lambda \cdot \Delta t$.

For bi-stable circuit elements such as CMOS SRAMs a sudden 50% variation in charge may cause the device to invert. In general, for decreasing feature size of memory cells the expected critical charge decreases and the expected sensitivity to radiation increases. To generate an electron-hole pair in silicon an energy of 3.6 eV is needed. Thus the critical charge Q_c may be formed by deposition in the critical volume of an energy E_c:

$$E_c = 3.6\ \mathrm{eV} \cdot Q_c / 1.6 \cdot 10^{-19}\ C = Q_c \cdot 2.25 \cdot 10^{19}\ \mathrm{eV}/C. \tag{1}$$

Experimental Setup

A test setup was established at RNL. A neutron source (a cylinder 7-cm high and 3 cm in diameter) was placed in a test stand. The source is a mixture of Pu and Be powder. The computers containing the RAM chips under test were placed 30 cm from the source. According to the supplier, the strength of the source is $9.4 \cdot 10^6$ n/sec. Accordingly the flux at 30 cm is 830 $n/cm^2/sec$.

A computerized test system was used to monitor the upsets in the RAM. The basic idea in this test was that the total SRAM memory was filled with a known bit pattern (i.e., 01010101010101...) and the test software was then run in an infinite loop verifying the bit pattern at each run through the loop every 30 s.

If a bit was inverted, time, date and address of the bit were printed on the built-in printer of the computer, the bit flip was reset, and the testing was continued.

A series of tests over varying lengths of time was conducted. These tests included 6 Mk 1 and 3 Mk 2 computers. Hereby 96 different 32K · 8 bit SRAM chips (Mk 1) and 21 different 128K · 8bit. SRAM chips (Mk 2) were tested.

Results

It is expected on the basis of the physical processes involved, that the time intervals between SEUs follow an exponential distribution. This is tested using an ordinary chi-square test and is also illustrated graphically in Figs. 1 and 2, where the observed times between SEUs from the test setup are plotted against the expected values from an exponential distribution together with straight lines corresponding to the observed upset rates. In the chi-square test, the null hypothesis H_0 is that the data follow an exponential distribution, and the alternative H_1 is that the data are not exponentially distributed.

The test value for the Mk 1 computers is 3.25 with $df = 5$ (five degrees of freedom), corresponding to a level of significance of 65%. The test value for the Mk 2 computers is 7.81 with $df = 4$, corresponding to a level of significance of 10%.

The null hypothesis H_o can therefore not be rejected for any of the computers, at say a 5% level of significance. It is therefore reasonable to claim that the data follow an exponential distribution for both computers. Nevertheless, the data from the Mk 2 computers do include a few remarkably large observations. No physical explanation can be given at this time.

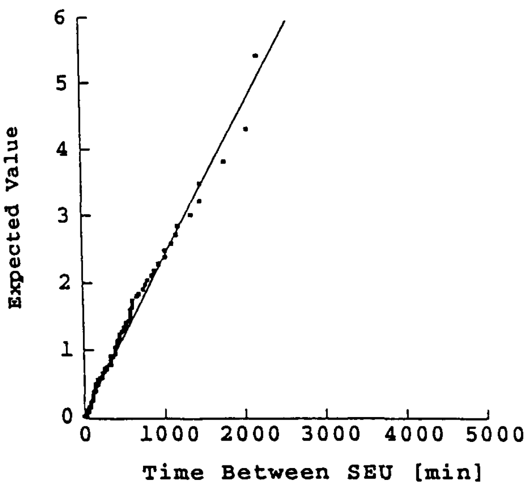

Fig. 1. Observed time between SEUs (min) in the laboratory tests plotted against the expected values from an exponential distribution for the Mk 1 computers.

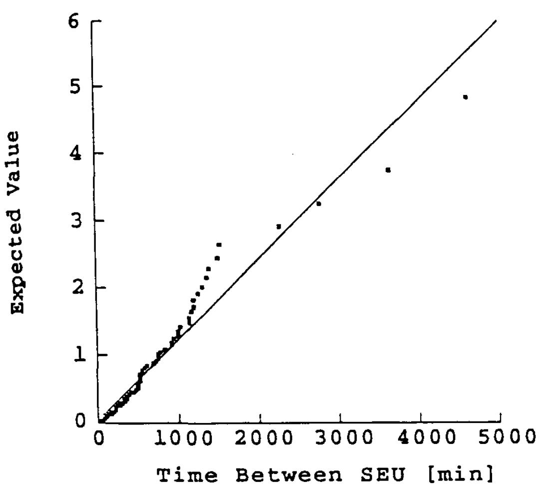

Fig. 2. Observed time between SEUs (min) in the laboratory tests plotted against the expected values from an exponential distribution for the Mk 2 computers.

The sensitivities of the two computers are comparable. As already noted, Mk 2 is 0.8 μm technology and Mk 1 is 1.3 μm technology. The sensitive volume and the critical charge are both proportional to the sensitive area. On the other hand, the burst generation rate, BGR, decreases strongly with increasing E_c [4]. The net effect of size is that small feature technology is more sensitive to neutron irradiation, other things being equal. *A priori*, it is therefore expected that the Mk 1 version has lower error rate (upsets/bit/day), but the tests showed this not to be the case. The reason for this must be that other factors than feature size influence the sensitivity.

During the neutron irradiation tests two SEU pairs were observed. An SEU pair is two SEUs in neighboring bits at the same time, i.e., within about 30 s, which is the time resolution of our test. An SEU pair is only counted as one SEU in Table II.

Fig. 3 shows the plot of the observed SEUs during the test period with the airborne computers (Mk 1). The tests at flight altitudes only gave a limited number of observations, 14 relevant data points were obtained. These are of great interest, since they reflect the influence of the actual neutron flux at the altitude and routes used by the airline. It can be seen in Fig. 3 that the data follow a straight line offset from the origin. Owing to the way the data were sampled, an SEU could remain unregistered for up to 50 h. This is the reason for the displacement from the origin. The number of bits used in the airborne computers was $3.11 \cdot 10^6$. The mean time between SEUs can be estimated to 162 flying hours or $4.8 \cdot 10^{-8}$ upsets/bit/day. Because of the small number of data points and the offset it is difficult to say more about the distribution of the time between the SEUs. However, the straight line suggests an exponential distribution.

Discussion

An estimate of the expected number of SEUs in the Mk 1 computers can be obtained from the following typical values: Charge collection in the sensitive circuit node (the drain node of the "off" transistor in the memory element) can result in a change of state of the memory element. The capacitance of this node is typically 0.01 pF (information from other vendors), the voltage is 5 V and a 50% change in the charge is needed to cause a bit to invert. Therefore, the critical charge, Q_c, is to be 0.025 pC and the critical energy is 0.6 MeV (equation 1). The burst generation rate, BGR, is then found from Fig. 7 in [4] to be about $7 \cdot 10^{-15}$ cm$^2/\mu$m^3 for neutrons with energy between 5 MeV and 10 MeV. The area of the drain node is estimated (no manufacturer information available) to be 10% of the total memory element size or 12 μm^2. The neutron sensitive thickness of the microchip is approximately 2 μm [5]. Thus, the sensitive volume for neutron irradiation is 24 μm^3. Finally, the upset rate is the product of volume, BGR and flux and it is equal to $3 \cdot 10^{-6}$ upsets/bit/day. (A factor of 0.25 has been introduced here to correct for the neutron spectrum of the Pu-Be source since only neutrons above 5 MeV contribute significantly.) This upset rate is so close to the experimental one, $9.09 \cdot 10^{-7}$ upsets/bit/day, that we can conclude that the SEUs observed in the tests are qualitatively understood.

In spite of their smaller feature size the Mk 2 computers are more resistant to neutron induced SEUs than the Mk 1 computers. This must result from differences in technology (e.g., doping levels) not directly related to feature size.

For airborne devices (Mk 1) the upset rate is $4.8 \cdot 10^{-8}$ upsets/bit/day. To obtain an estimate of the expected upset rate we note that Normand and Doherty [6] calculate a volumetric upset rate of about 10^{-9} upsets/bit/μm^3 for a silicon device with $E_c = 0.675$ MeV. The neutron spectrum applied in [6] is the one found at 37,000 ft (11.3

TABLE II
RESULTS FROM THE FAST NEUTRON IRRADIATION TEST

Computer	SEU observations	Mean time between SEUs	Tested bits per computer	Upsets/bit/day
Mk 1	112	395 min	$4.01 \cdot 10^6$	$9.09 \cdot 10^{-7}$
Mk 2	64	783 min	$7.13 \cdot 10^6$	$2.58 \cdot 10^{-7}$

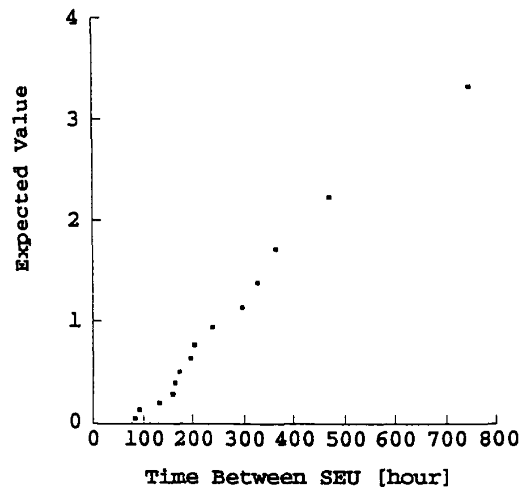

Fig. 3. Time between SEUs (hours) for the Mk 1 computers when airborne.

km) and includes the energy range 5 MeV–200 MeV. Applying the sensitive volume 24 μm^3 per bit and neglecting the small differences in flight altitude and E_c, we obtain a calculated upset rate of $2.4 \cdot 10^{-8}$ upsets/bit/day, just half of the observed value. Because the estimate is so close to experiment, we conclude that the SEUs observed in airborne CMOS SRAMs are due to neutrons.

Finally, we have observed two SEU pairs, that is, about 1 per cent of the SEUs are SEU pairs. They are probably due to (n, α) or (n, p)-processes, where the recoil nucleus and the light particle produce one error each, in neighboring bits. Both SEU pairs were found in the Mk 1 computers.

CONCLUSION

Neutron induced SEUs were observed both in airborne computers and in computers irradiated from a PuBe neutron source. The plots of the SEUs observed in the tests indicate that the SEUs are exponentially distributed, i.e., no accumulating effect has been observed. Most of the upsets are probably caused by nuclei recoiling after elastic or inelastic scattering of neutrons. However, the occurrence of SEU pairs suggests that light particles also contribute.

The number of induced upsets was estimated. The calculation was based on the burst generation rate concept of Ziegler and Lanford [4] and considered only the energy deposited by the neutron-induced recoils. Though the calculated upset rate is larger than the measured number of upsets, the agreement is still considered to be acceptable in view of the many uncertainties involved in the calculations: magnitude of the critical charge, sensitive volume, energy of the flux, etc.

To our knowledge this is the first documented observation of neutron induced SEUs at flight altitudes. As feature size in electronic components becomes smaller the components will become more sensitive to neutrons and it therefore would seem advisable to include neutron irradiation in the test procedures for airborne equipment.

ACKNOWLEDGMENT

The authors wish to thank Mr. V. Lemche, who performed the statistical analysis of the data.

REFERENCES

[1] RTCA/DO-160C, "*Environmental Conditions and Test Procedures for Airborne Equipment*," Washington, D.C., Radio Technical Commission for Aeronautics, 1989.

[2] UNSCEAR (United Nations Scientific Committee on the Effects of Atomic Radiation). "*Ionizing Radiation: Sources and Biological Effects*," New York: United Nations, 1982, p. 85.

[3] T. Nakamura, Y. Uwamino, T. Ohkubo, and A. Hara, "Altitude variation of cosmic-ray neutrons," *Health Physics*, vol. 53, pp. 509–517, 1987.

[4] J. F. Ziegler and W. A. Lanford, "Effect of cosmic rays on computer memories," *Science*, vol. 206, pp. 776–788, 1979.

[5] E. Normand, J. L. Wert, W. R. Doherty, D. L. Oberg, P. R. Measel, and T. L. Criswell, "Use of PuBe source to simulate neutron-induced single event upsets in static RAMs," *IEEE Trans. Nucl. Sci.*, vol. 35, pp. 1523–1528, 1988.

[6] E. Normand and W. R. Doherty, "Incorporation of ENDF-V neutron cross section data for calculating neutron-induced single event upsets," *IEEE Trans. Nucl. Sci.*, vol. 36, pp. 2349–2355, 1989.

[7] R. Silberberg, C. H. Tsao, and J. R. Letaw, "Neutron generated single-event upsets in the atmosphere." *IEEE Trans. Nucl. Sci.*, vol. 31, pp. 1183–1185, 1984.