Brief Papers

Ion Microbeam Probing of Sense Amplifiers to Analyze Single Event Upsets in a CMOS DRAM

Linda M. Geppert, Urs Bapst, David F. Heidel, and Keith A. Jenkins

Abstract—**By irradiating individual nodes of a CMOS DRAM composed of p-channel cells with a collimated microbeam of alpha particles, the relative sensitivity of circuit elements to single event upsets (SEU's) has been measured. The results show that alpha-particle hits on sensitive nodes within the sense amplifiers dominate the SEU rate. This domination is due to the presence in the sense amps of n-channel devices which can collect charge from the entire ion track. In contrast, the memory cells and bit lines contain only p^+ nodes in an n-well, which shields them from charge generated in the substrate.**

I. Introduction

RADIATION-induced single event upsets (SEU's) in CMOS DRAM's continue to be a concern, particularly as lower storage-node capacitances and lower operating voltages lead to smaller Q_{crit}, the amount of charge required to upset a cell. Blanket irradiation of these devices by a radioactive source (hot-source testing) can measure the overall failure rates. However, little information is obtained on the sensitivities of various circuit elements to SEU's.

A new instrument, an ion microbeam radiation system [1], has been used to probe the relative contribution of individual circuits and nodes of a CMOS DRAM to SEU's. This instrument, which uses mono-energetic collimated ions from a 3-MV tandem accelerator, can produce an ion beam with a diameter as small as 1 μm. The precise alignment capability of the system allows positioning of the beam to any location in the circuit with an accuracy of better than 1 μm. The mono-energetic beam with the device under vacuum simplifies the analysis of the experimental results.

II. Experiment

The chip studied in this report is a 20-ns access 128-kb$\times$4 high-speed CMOS DRAM using p-channel cells [2], fabricated with a 1-μm double-poly double-metal n-well process. This design utilizes a folded bit-line, half-V_{dd} sensing scheme. A small subsection of the array containing both cells and sense-amp circuits is shown in Fig. 1. The chip was irradiated with 10- and 100-μm-diameter beams of 3-MeV alpha particles. The 100-μm-diameter beam was used to compare the relative SEU rates of the cell array and the sense amps. The 10-μm-diameter beam was used to probe the individual nodes within the sense amp. Particle flux was on the order of 0.2 alphas/$\mu m^2 \cdot s$. The chip was oriented perpendicular to the beam.

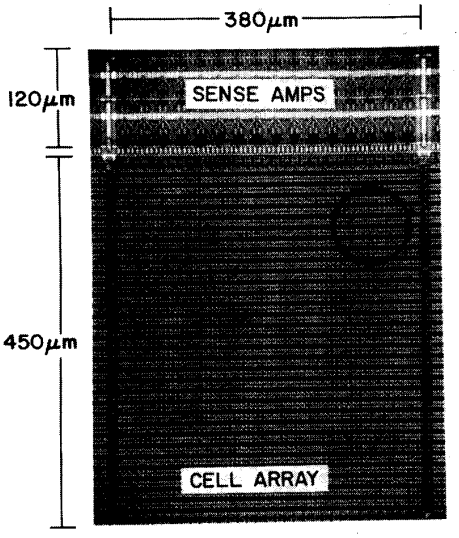

Fig. 1. Micrograph of the DRAM studied, showing memory cell array and sense amplifiers. The circle indicates the size of the ion beam used (100 μm) for the data in Fig. 2.

In order to measure SEU's, a simple pattern of all highs (5 V) or all lows (0 V) was written into the 512 cells contained in a subsection. The cells were refreshed at a cycle time which was varied in the experiments from 80 ns to 20 μs. After the refresh period, the states of the cells were read and the failure rate was recorded as fails per alpha.

In the first set of measurements, the sense-amp subsection was exposed to a 100-μm-diameter beam of alphas during writing and refreshing. Fails per alpha were recorded as a function of chip cycle time. The results are shown as the top curve in Fig. 2. The fail rate is observed to be inversely proportional to the cycle time, showing a dependence which is similar to bit-line fails. This arises from the fixed floating time of 10 ns per cycle from the end of precharge to the beginning of amplification during which both bit lines and sense amps are sensitive to upsets. There was no significant difference between low-to-high and high-to-low fail rates. A

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L. M. Geppert, D. F. Heidel, and K. A. Jenkins are with the Thomas J. Watson Research Center, IBM Research Division, Yorktown Heights, NY 10598.

U. Bapst was with the Thomas J. Watson Research Center, IBM Research Center, Yorktown Heights, NY 10598. He is now with the Zurich Research Laboratory, IBM Research Division, 8803 Rueschlikon, Switzerland.

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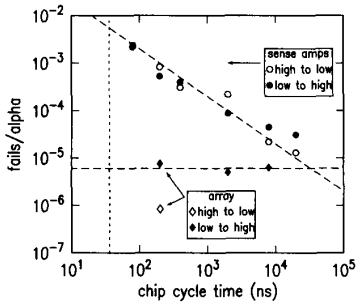

Fig. 2. Alpha-induced failure rate versus chip cycle time, for beam directed at cell array and sense amplifiers. Dotted line indicates minimum cycle time of the circuit.

significantly lower fail rate was observed, however, when the beam was directed at the cell subsection. Low-to-high fail rates were cycle-time independent, a behavior characteristic of memory cells. These results are also plotted in Fig. 2. Throughout a total of several minutes of exposure time, only one high-to-low fail was obtained. This fail is due to a bit-line node, since cells do not contribute to high-to-low fails. Due to this extremely low fail probability, cycle-time dependence of the bit-line node failure rate could not be obtained. However, it would be expected to follow a curve of inverse proportionality. At a cycle time of 80 ns, the shortest cycle time used in this experiment, the storage-node fail rate is more than two orders of magnitude smaller than the sense-amp fail rate. Extrapolated to the operational 36-ns cycle time (vertical broken line in Fig. 2) of this high-speed DRAM, the difference increases to approximately three orders of magnitude. The results clearly demonstrate the significant role of sense amplifiers to the overall failure rate.

To understand the high failure rate in the sense amp, a small 10-μm-diameter beam was used to probe within this region. The sense-amp circuit is shown at the top of Fig. 3. It contains cross-coupled n-channel and p-channel FET pairs which are laid out in a single line along the bit-line direction. The drain nodes of the four FET's are connected to the bit lines and therefore can contribute to SEU's. These nodes are 9 μm wide by 4 μm long. In the sense-amp circuitry there are two additional n-channel FET's which are used as multiplexing devices. They are about the same size as the sense-amp nodes and are also important charge collection sites. The physical layout of the sense-amp region is shown in Fig. 3.

In the measurement, the beam location was incremented in 5-μm steps along the sense amp in the bit-line direction, and the SEU rate was measured at each location. A cycle time of 200 ns was used. The results plotted in Fig. 3 show that fails occurred only when an n^+ node was exposed to the beam. No fails were observed in the regions between nodes. Nor were there any fails when the p^+ nodes were exposed. The pattern of low-to-high and high-to-low failures that was observed for the various n^+ nodes is consistent with the addressing scheme used in these measurements.

The cells and bit-line nodes are relatively insensitive to fails due to alpha-particle strikes, since the n-well shields these nodes against collection of any charge generated below the n-well, as shown in Fig. 4. The n-well is about 4 μm deep. The alpha particle travels about 11 μm into the silicon. In addition, some of the charge generated inside the well

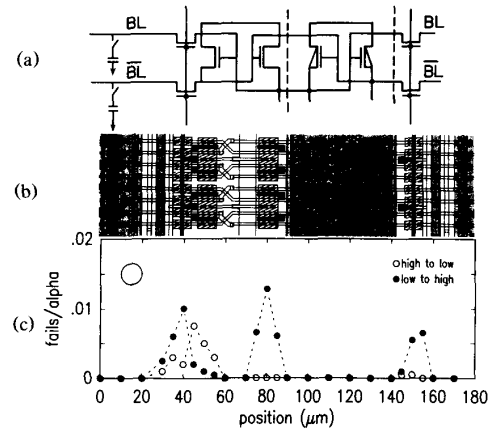

Fig. 3. (a) Circuit schematic of sense amplifiers. (b) Physical layout. (c) Alpha-induced failures in sense amplifiers irradiated by 10-μm beam (size indicated by circle) as a function of position.

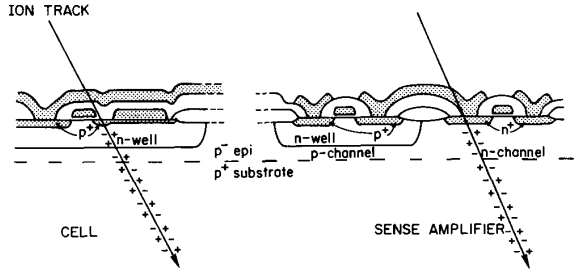

Fig. 4. Cross section of memory cell and sense-amplifier device.

crosses the n-well boundary and is collected by the substrate. In contrast, n^+ nodes such as those in the sense amp, which are not protected by a well, can collect charge from the entire ion track. The smaller funneling length of the p^+ nodes relative to the n^+ nodes, for the doping profiles used, further enhances these differences [3].

A Monte-Carlo technique [4] has been used to simulate collected charge for the geometries and conditions of this experiment. These simulations show that the maximum charge collected by the p^+ nodes in the n-well is about 20 fC for a vertically incident alpha. The n^+ nodes outside the n-well collect as much as 50 fC. This charge is collected by both funneling and diffusion mechanisms. The funneling length is approximately 1.5 μm inside the n-well. The failure rates of the n^+ nodes in the sense amp suggest that the Q_{crit} of the circuit is in the 40–50-fC range.

III. Discussion

The SEU rates presented here are in units of fails per alpha. In order to determine fails per unit time in a real environment where the entire chip is exposed to random particles, many factors must be considered such as the area ratio between the array and the sense amps, the angular dependence of the failure rate, and the energy of the alpha particles in the silicon. The ratio of array area to sense amp area for this chip is about 7.5:1. The angular dependence is important since nonorthogonal particle strikes will lead to

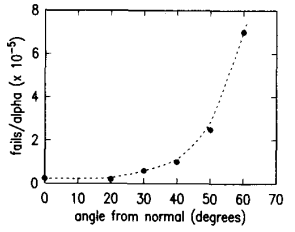

Fig. 5. Angular dependence of array fails.

more charge generated within the n-well, and thus to an increase in the fail rate. The fail rate of the cells as a function of angle has been measured, and shows a gradual increase in fails with increasing angle from normal incidence. Above 50° the rate increases sharply, and at 60° it is a factor of 30 greater than at 0°. The angle dependence of the array failures is shown in Fig. 5. The sense-amp failure rate should also show an increase at larger alpha-particle angles. The importance of the large-angle data depends strongly on the location of the source of the alpha particles, their energy, and chip passivation. The results presented here were taken on unpassivated chips with approximately 2 μm of material above the silicon surface. For passivated chips, alpha particles hitting at large angles will be significantly attenuated. Therefore to extrapolate the angular results to a real environment, detailed information about the source of the alpha particles must be known. Considering all these effects, particularly the area ratio and the weak angular dependence at small angles, it is estimated that hot-source testing would show the sense-amp fails to be approximately two orders of magnitude greater than cell or bit-line-node fails at a 36-ns cycle time. This estimate is consistent with hot-source data taken on this chip [2], [5].

IV. Conclusion

It was shown that the failure rate of CMOS DRAM's using p-channel cells can be dominated by the sense-amp circuits. The domination results from the effectiveness of shallow n-wells in protecting nodes from charge generated by ionizing radiation when the range of the particle exceeds the depth of the well. The result is that fails due to the unprotected nodes such as those in the sense amps totally dominate the failure rate.

Thus, if fail rates are to be significantly reduced, the nodes in the substrate must be made less sensitive. One method is the use of buried layers [4], [6] to reduce the charge collected by nodes in the substrate.

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Design of C-Testable DCVS Binary Array Dividers

Qiao Tong and Niraj K. Jha

Abstract—**Clocked differential cascode voltage switch (DCVS) circuits are dynamic CMOS circuits that have the advantage of being protected against test-set invalidation due to circuit delays and timing skews. In this paper we consider the problem of testing of DCVS binary array dividers. Both the nonrestoring and restoring array dividers are considered. We show that a DCVS nonrestoring array divider can be made C-testable with only either four or five vectors. These vectors detect all the detectable single stuck-at, stuck-open, and stuck-on faults in the circuit. The additional hardware required to achieve C-testability for an $n \times n$ nonrestoring array divider only consists of $n-1$ two-input XOR gates and one control input. We show that a restoring DCVS binary array divider can be made C-testable with only six vectors, which also detect all the detectable single stuck-at, stuck-open, and stuck-on faults in the circuit. The hardware overhead required for the C-testable design of the $n \times n$ restoring array divider consists of n two-input XOR gates and one control input.**

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The authors are with the Department of Electrical Engineering, Princeton University, Princeton, NJ 08544.

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I. Introduction

RAPID advances in the semiconductor industry have made possible the implementation of digital circuits with a very large number of devices on a single chip. Testing of high-complexity VLSI circuits has become very costly and difficult. However, iterative logic arrays (ILA's), which con-

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