MOSFET
Conceptos Básicos

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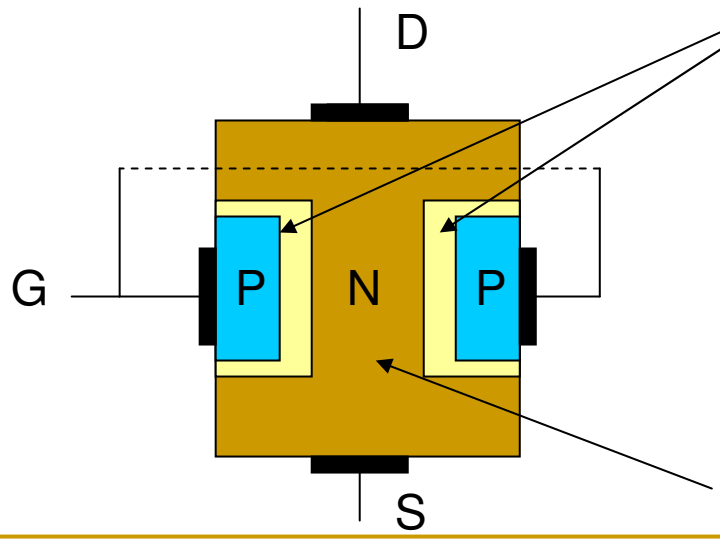
Introducción

- FET = Field Effect Transistor
  - Unipolar = solo un tipo de portador de carga
  - Controlado por voltaje
  - $I_D = F(V_{GS})$



Zonas de agotamiento

JFET:

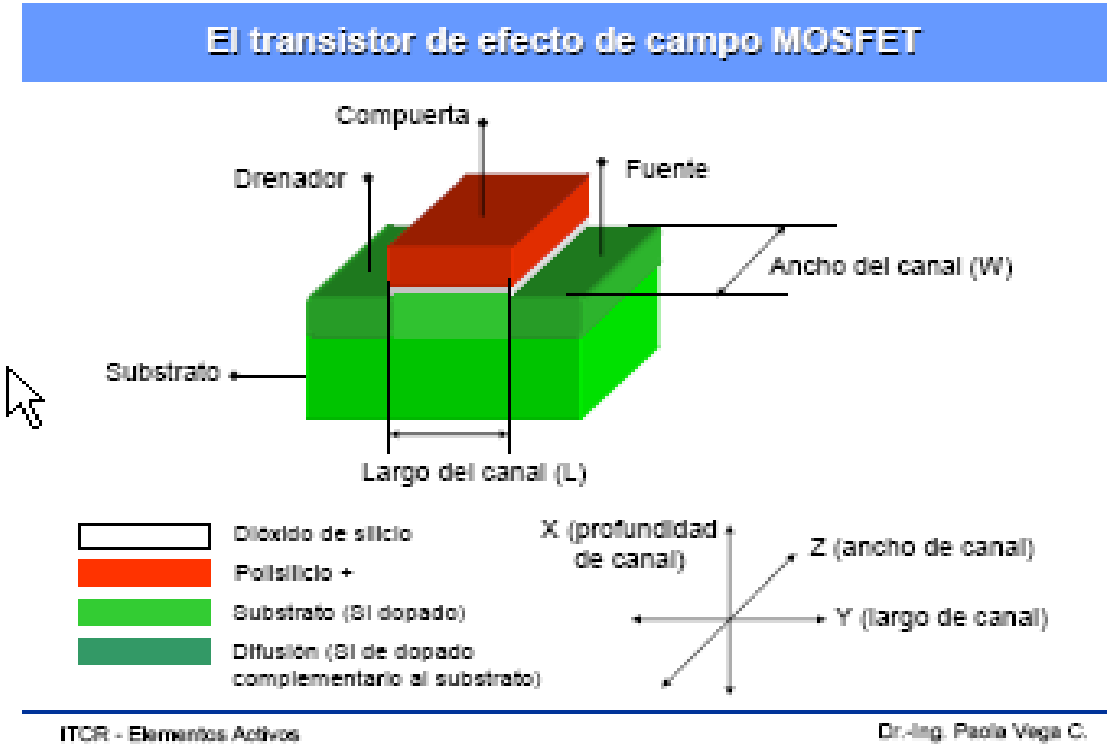
•Existe una zona de estrechamiento

•Cuando se aplica V_{DS} la zona de agotamiento no es uniforme

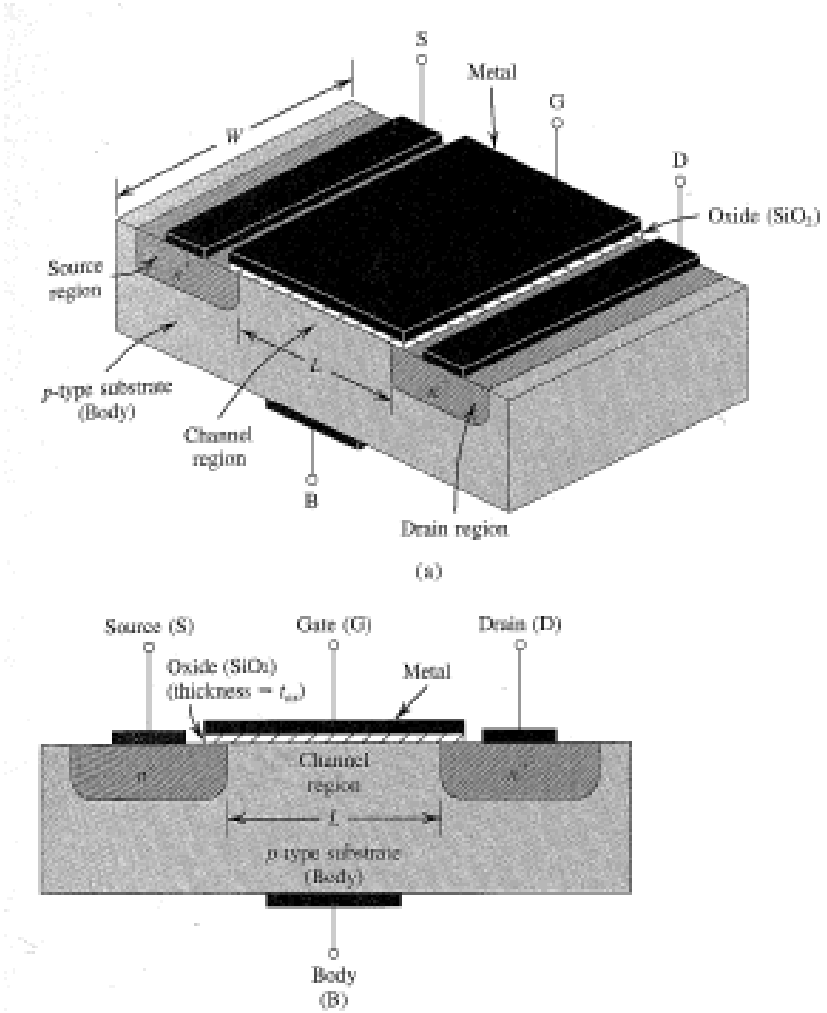
Zona de estrechamiento

Introducción

- MOSFET = Metal-Oxide FET = IG FET



Estructura del MOSFET



MOSFET consta de 4 terminales

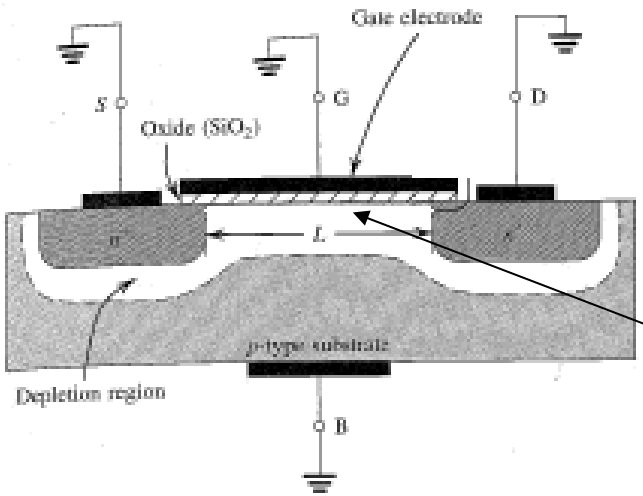
- Gate = compuerta
- Drain = drenaje
- Source= fuente
- Body o substrate = sustrato o cuerpo

Parámetros de construcción

- L = largo del canal
- W =ancho del dispositivo
- Tox = grosor de la capa de Si02

Modo de operación

- Cuando $V_{GS} = 0$
  - Dos diodos en serie
  - R_{DS} = 10^12 Ohmios

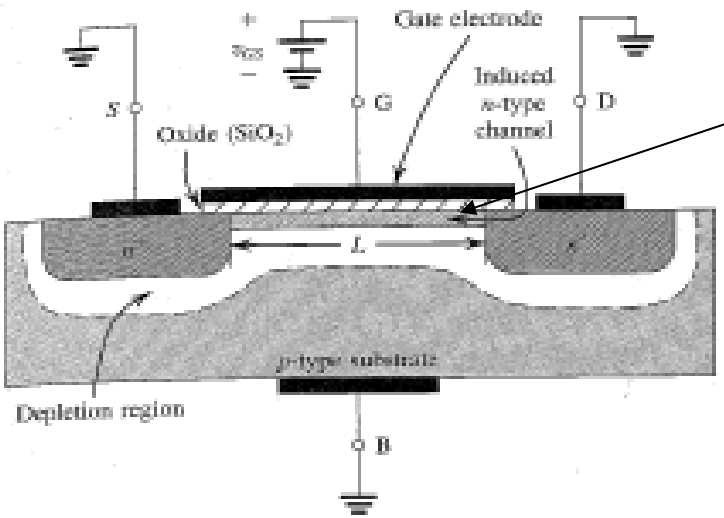


N-MOS

Región de agotamiento por unión PN
NO hay canal inducido

Creación de un canal de conducción

- Cuando se aplica un $V_{GS} > 0$ V



N-MOS

Región de agotamiento por unión PN
Se induce un canal tipo N en el sustrato P (capa de inversión)

La cantidad de V_{GS} requerido para la formación del canal → V_T

V_T depende del proceso de fabricación (0.5V-1V)

Formación de corriente de drenaje

<u>V_{DS} pequeño</u>

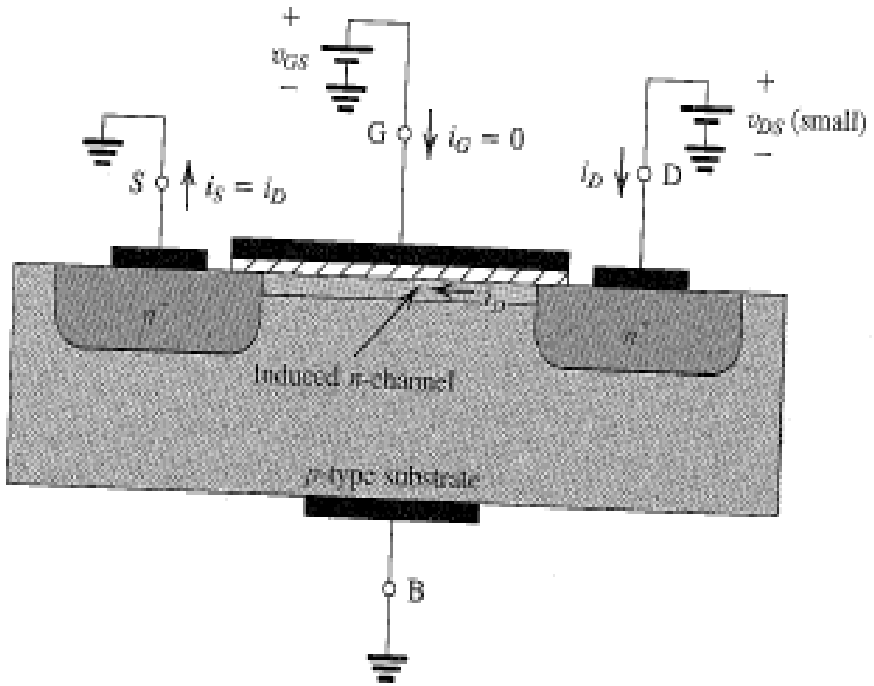


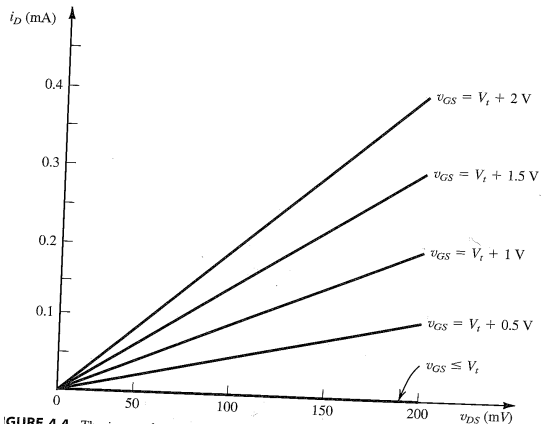
FIGURE 4.3 An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)v_{DS}$. Note that the depletion region is not shown (for simplicity).

(V_{GS}-V_T) = voltaje efectivo de conducción

V_{DS} esta en el orden de mV

La Resistencia del MOSFET es lineal y proporcional al voltaje efectivo de conducción

R_{DS} = F (V_{GS})



Formación de corriente de drenaje

<u>V_{DS} incrementado</u>

La caída de V_{DS} se da a lo largo del canal creando una I_{DS} que no es uniforme y un canal deformado

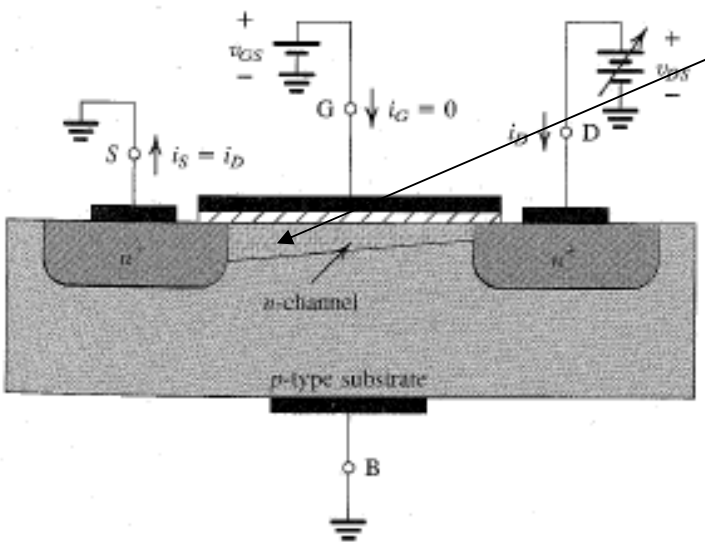
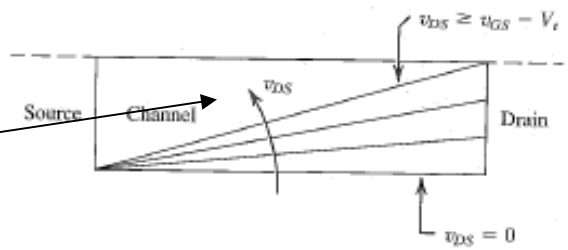


FIGURE 4.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value > V_t.

Si V_{DS} aumenta hasta alcanzar el voltaje efectivo de conducción del MOSFET → Saturación del canal

$V_{DS} = (V_{GS} - V_T) = V_{D\,sat}$

Deformación del canal conforme aumenta VDS



Corriente de drenaje en función de los parámetros de polarización

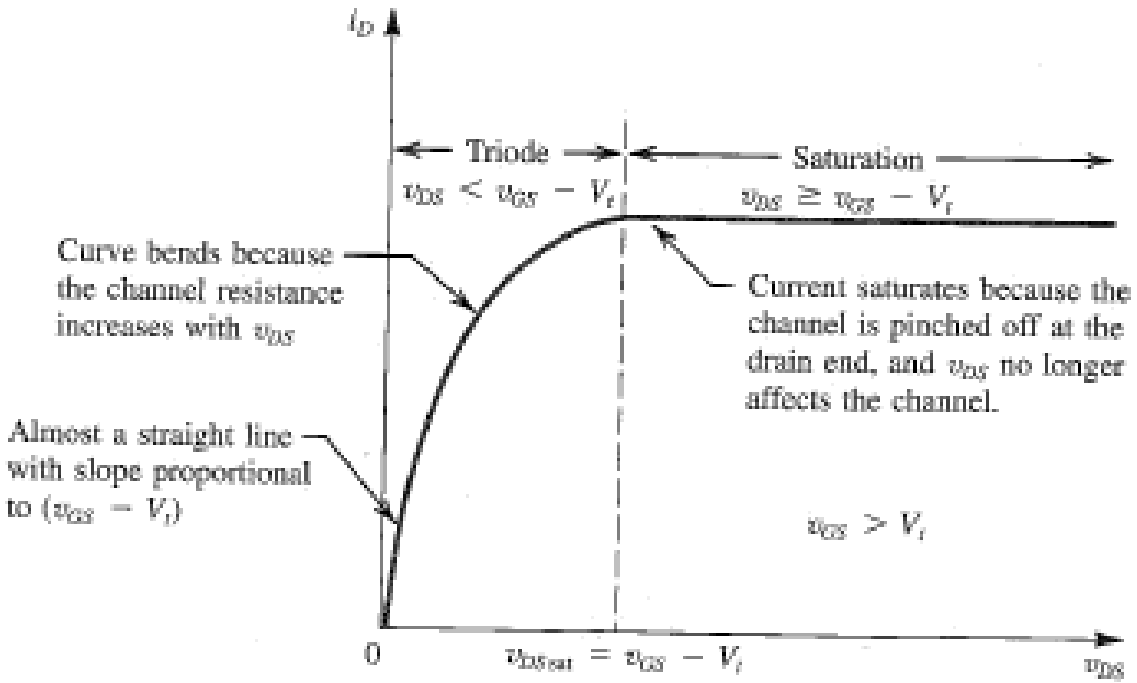


FIGURE 4.6 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} > V_t$.

Derivación de la corriente de drenaje en función del voltaje de drenaje-fuente

Región infinitesimal de la compuerta

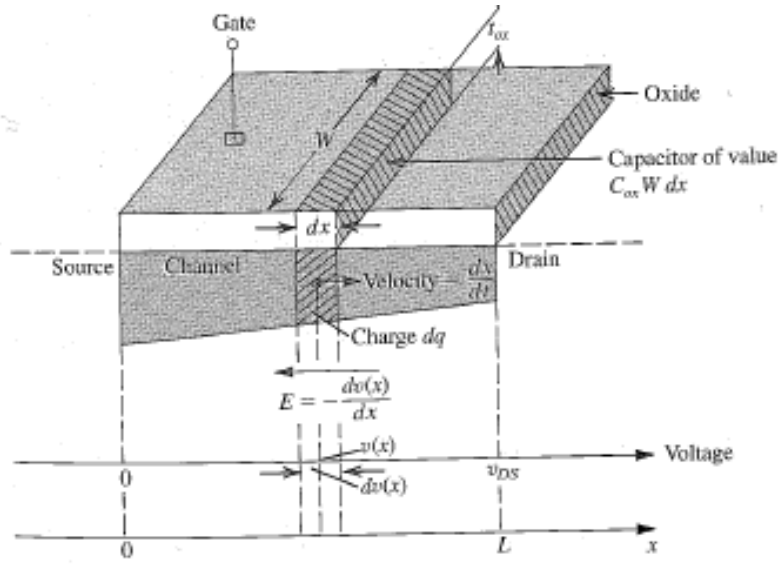


FIGURE 4.8 Derivation of the i_D–v_{DS} characteristic of the NMOS transistor.

Para análisis se considera operando en la región de Triodo → $V_{DS} < (V_{GS} - V_T)$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

where ε_{ox} is the permittivity of the silicon oxide,

$$\varepsilon_{ox} = 3.9\varepsilon_0 = 3.9 \times 8.854 \times 10^{-12} = 3.45 \times 10^{-11} \text{ F/m}$$

Derivación de la corriente de drenaje en función del voltaje de drenaje-fuente

$$dq = -C_{ox}(W\,dx)[v_{GS} - v(x) - V_t]$$

(dQ = C*dV)

$$\frac{dx}{dt} = -\mu_n E(x) = \mu_n \frac{dv(x)}{dx}$$

Velocidad de la corriente de drenaje

$$i = -\mu_n C_{ox} W[v_{GS} - v(x) - V_t]\frac{dv(x)}{dx}$$

$$i = \frac{dq}{dt}$$

$$= \frac{dq}{dx}\frac{dx}{dt}$$

$$\int_0^L i_D\,dx = \int_0^{v_{DS}} \mu_n C_{ox} W[v_{GS} - V_t - v(x)]\,dv(x)$$

$$i_D = (\mu_n C_{ox})\left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

$$i_D = k_n'\frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \quad \text{(Triode region)}$$

$$i_D = \frac{1}{2}k_n'\frac{W}{L}(v_{GS} - V_t)^2 \quad \text{(Saturation region)}$$

Variantes del MOSFET

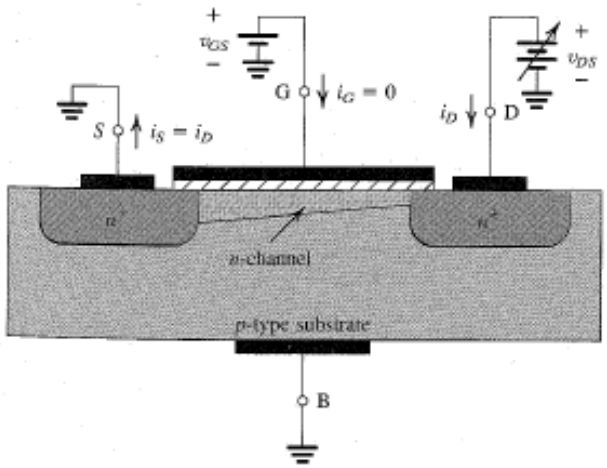


FIGURE 4.5 Operation of the enhancement NMOS transistor a acquires a tapered shape, and its resistance increases as v_{DS} is in value > V_t.

PMOS tiene el mismo principio de funcionamiento que NMOS solo que VGS, VDS y VT son negativos

CMOS →

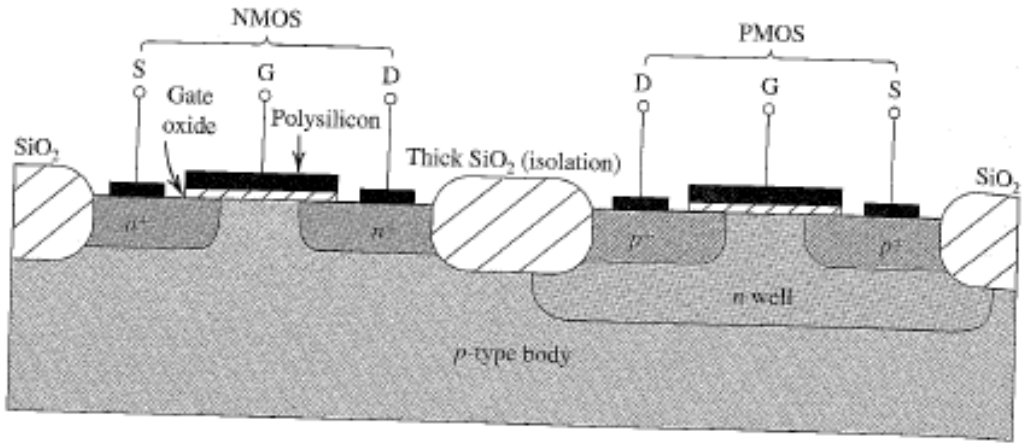


FIGURE 4.9 Cross-section of a CMOS integrated circuit. Note that the PMOS transistor is formed in a separate *n*-type region, known as an *n* well. Another arrangement is also possible in which an *n*-type body is used and the *n* device is formed in a *p* well. Not shown are the connections made to the *p*-type body and to the *n* well; the latter functions as the body terminal for the *p*-channel device.

Representación del dispositivo

Símbolo

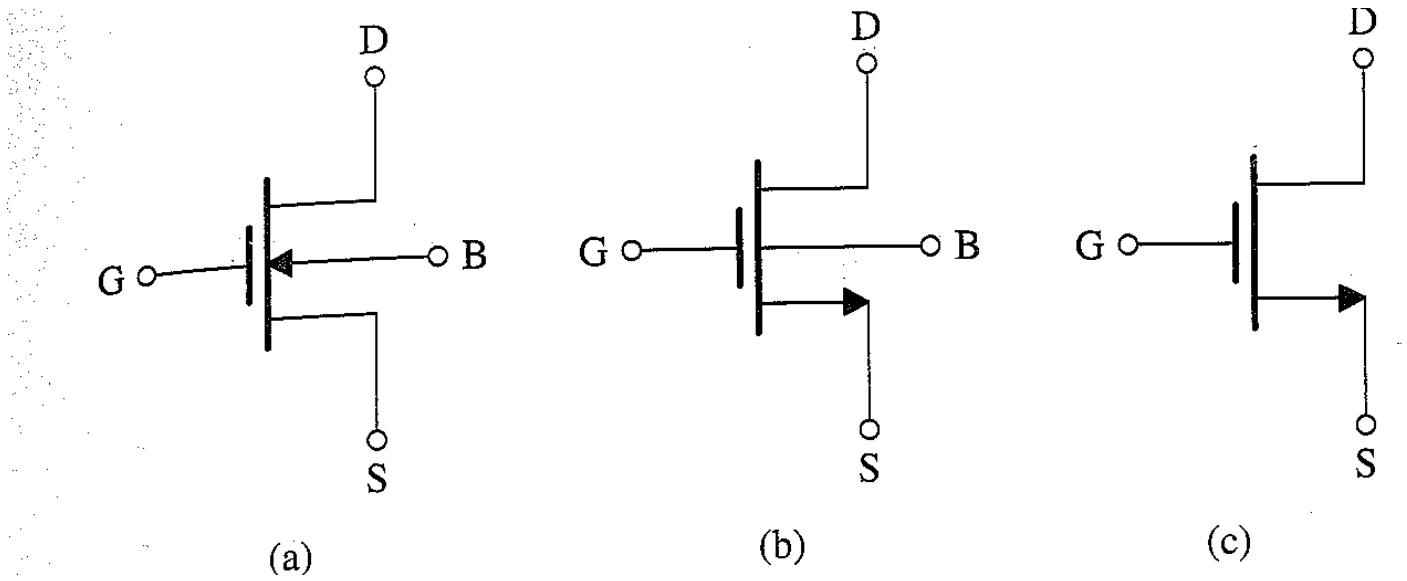
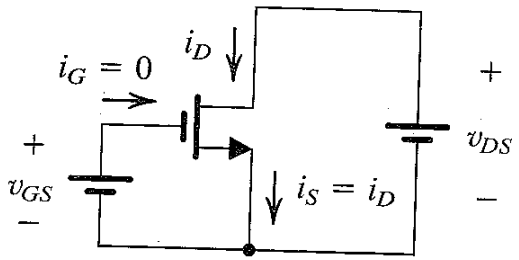
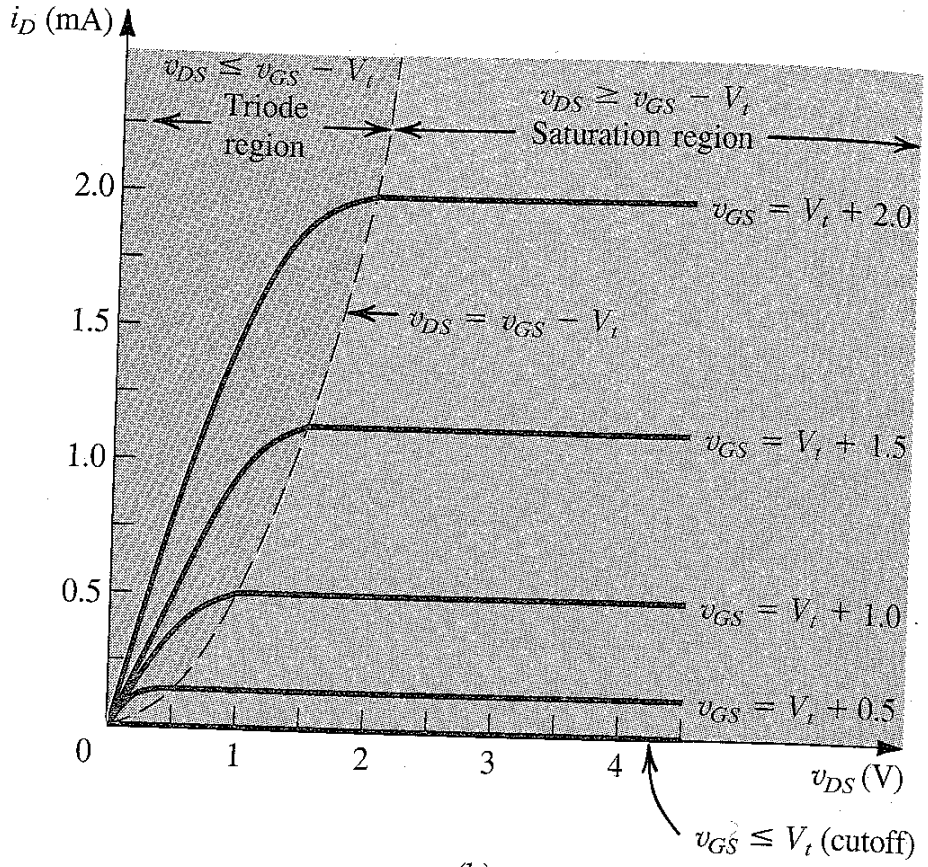


FIGURE 4.10 **(a)** Circuit symbol for the *n*-channel enhancement-type MOSFET. **(b)** Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., *n* channel). **(c)** Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

Zonas de operación del MOSFET



(a)



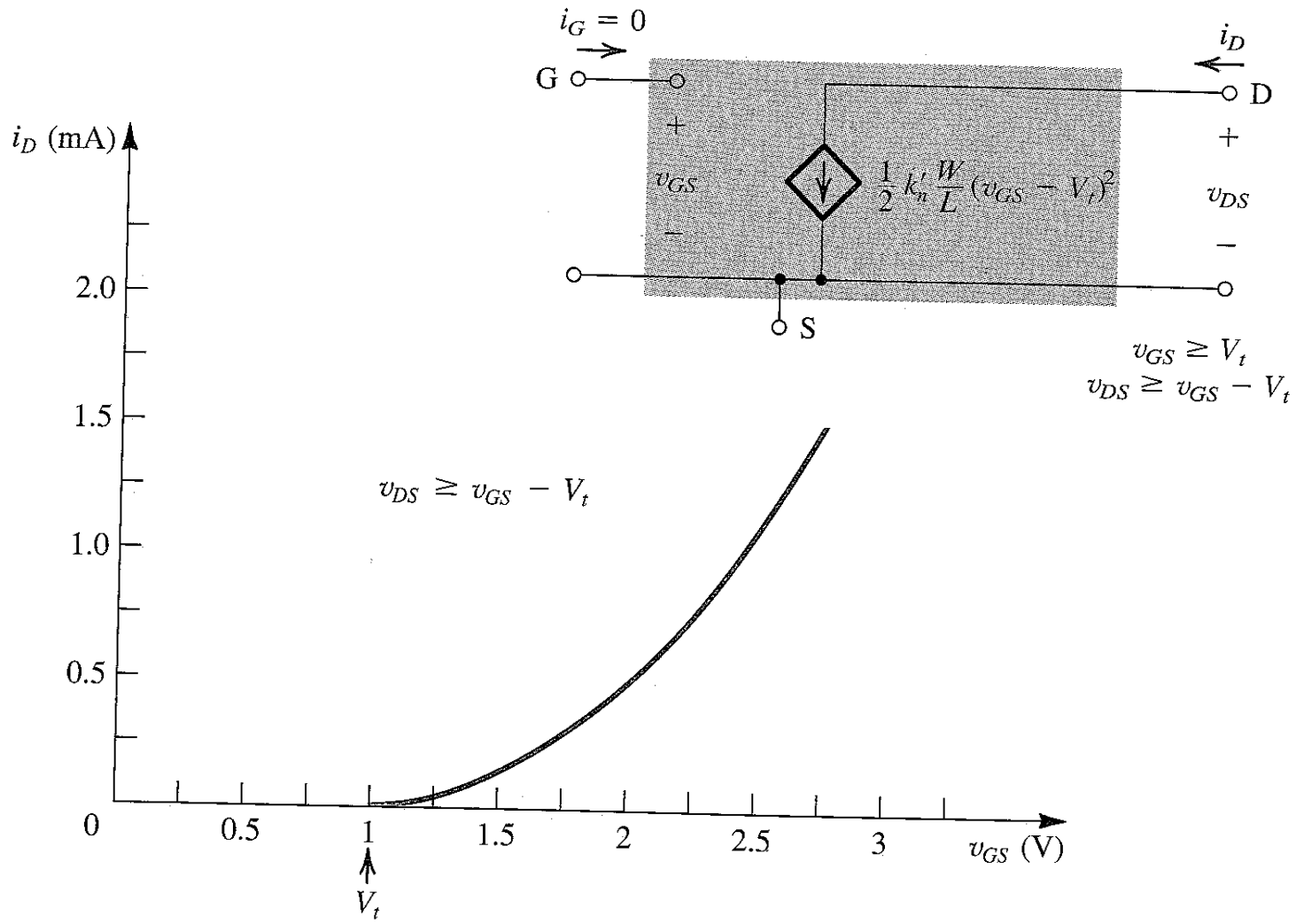
(b)

Zonas de operación del MOSFET

Corte	$v_{GS} < V_t$. '	ID= 0
Triodo (VDS<VDSsat)	$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right]$ $v_{GS} \geq V_t$ (Induced channel) $v_{DS} < v_{GS} - V_t$ (Continuous channel)	
Saturación (VDS>VDSsat)	$v_{GS} \geq V_t$ (Induced channel) $v_{DS} \geq v_{GS} - V_t$ (Pinched-off channel) $i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2$	

$$k_n' = \mu_n C_{ox}$$

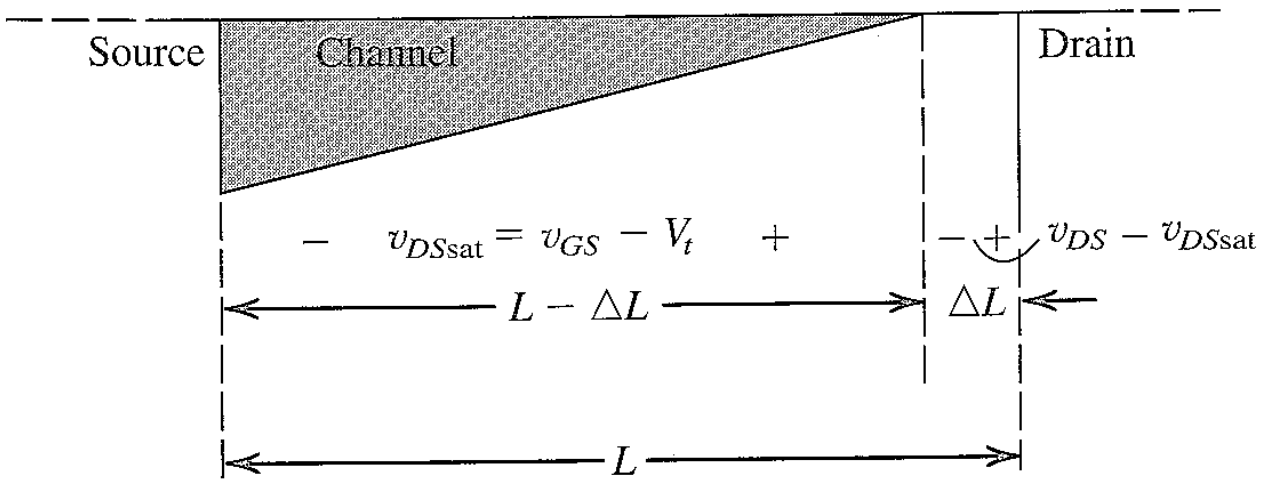
ID vrs VGS


$i_G = 0$
i_D
G
D
S
+
v_{GS}
−
+
v_{DS}
−
$\frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2$
$v_{GS} \geq V_t$
$v_{DS} \geq v_{GS} - V_t$
i_D (mA)
2.0
1.5
1.0
0.5
0
0.5
1
1.5
2
2.5
3
v_{GS} (V)
V_t
$v_{DS} \geq v_{GS} - V_t$

Efecto de la Temperatura en el MOSFET

- Con el incremento de la temperatura I_D baja
  - Vt → aumenta (2mV x 1Celcius de incremento)
  - K'n→ disminuye (* efecto dominante)

Modulación del largo de canal



Idealmente no cuando VDS alcanza VDSsat; ID se vuelve independiente de VDS

En la practica esto no ocurre así: la longitud del canal se modifica creando una nueva longitud L'

Efecto en la corriente de Drain

$$i_D = \frac{1}{2}k_n'\frac{W}{L-\Delta L}(v_{GS}-V_t)^2$$

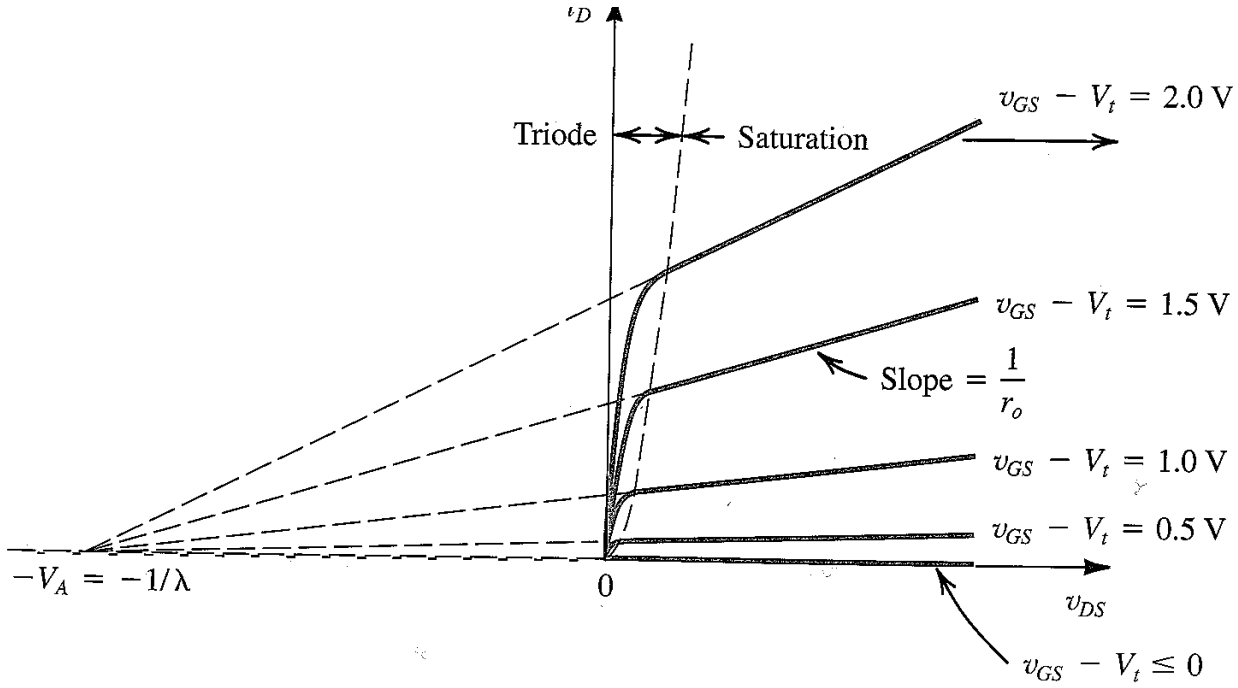
$$= \frac{1}{2}k_n'\frac{W}{L}\frac{1}{1-(\Delta L/L)}(v_{GS}-V_t)^2$$

$$\cong \frac{1}{2}k_n'\frac{W}{L}\left(1+\frac{\Delta L}{L}\right)(v_{GS}-V_t)^2$$

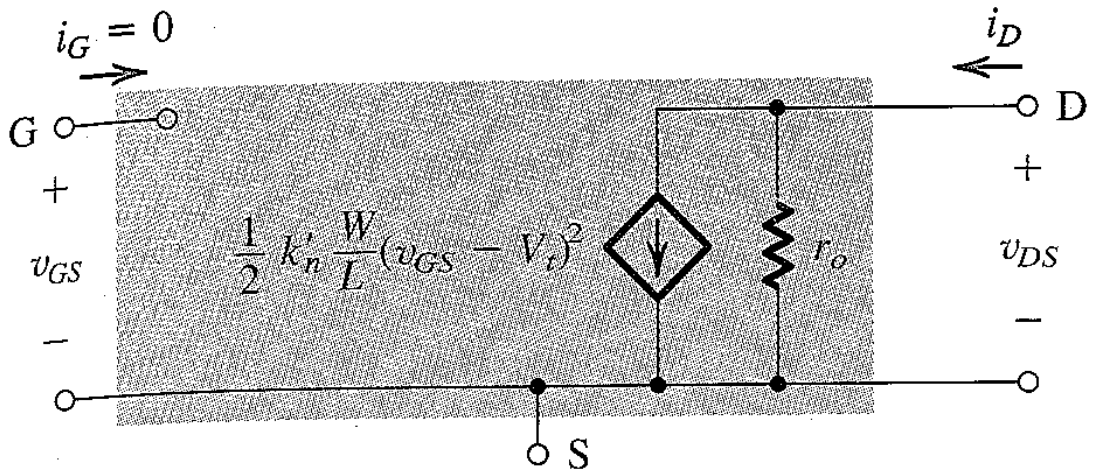
$$\Delta L = \lambda' v_{DS} \qquad \lambda = \frac{\lambda'}{L}$$

$$i_D = \frac{1}{2}k_n'\frac{W}{L}\left(1+\frac{\lambda'}{L}v_{DS}\right)(v_{GS}-V_t)^2$$

Efecto de la Modulación del Longitud del canal en la característica ID-VDS



Circuito equivalente incluyendo efecto de modulación de la longitud del canal



$$r_o \equiv \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}_{v_{GS}\ \text{constant}}$$

$$r_o = \left[\lambda \frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_t)^2\right]^{-1}$$

$$r_o = \frac{1}{\lambda I_D}$$

$$r_o = \frac{V_A}{I_D}$$

ID sin tomar en cuanta Modulación de la longitud de Canal

Efecto del Sustrato en un MOSFET

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_s}}{C_{ox}}$$

Parámetro de efecto cuerpo

$$V_t = V_{t0} + \gamma\left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right]$$

Zonas de operación del MOSFET

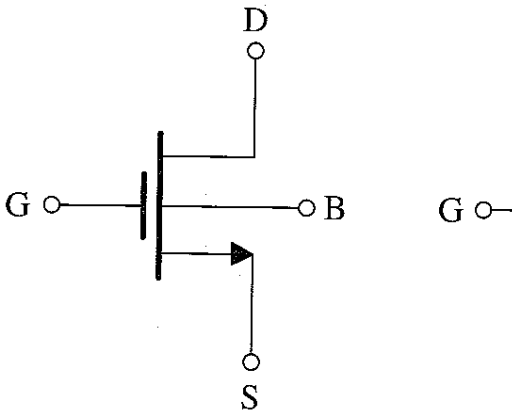
Corte	$v_{GS} < V_t$	ID= 0
Triodo (VDS<VDSsat)	$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right]$ $v_{GS} \geq V_t$ (Induced channel) $v_{DS} < v_{GS} - V_t$ (Continuous channel)	
Saturación (VDS>VDSsat)	$v_{GS} \geq V_t$ (Induced channel) $v_{DS} \geq v_{GS} - V_t$ (Pinched-off channel) $i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2$	

$$k_n' = \mu_n C_{ox}$$

Relaciones adicionales

NMOS Transistor

Symbol:



Overdrive voltage:

$$v_{OV} = v_{GS} - V_t$$

$$v_{GS} = V_t + v_{OV}$$

Operation in the *triode* region:

- Conditions:

  (1) $v_{GS} \geq V_t \quad \Leftrightarrow \quad v_{OV} \geq 0$

  (2) $v_{GD} \geq V_t \quad \Leftrightarrow \quad v_{DS} \leq v_{GS} - V_t \quad \Leftrightarrow \quad v_{DS} \leq v_{OV}$

- i-v Characteristics:

$$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

- For $v_{DS} \ll 2(v_{GS} - V_t) \quad \Leftrightarrow \quad v_{DS} \ll 2v_{OV}$

$$r_{DS} \equiv \frac{v_{DS}}{i_D} = 1\Big/\left[\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)\right]$$

Operation in the *saturation* region:

- Conditions:

  (1) $v_{GS} \geq V_t \quad \Leftrightarrow \quad v_{OV} \geq 0$

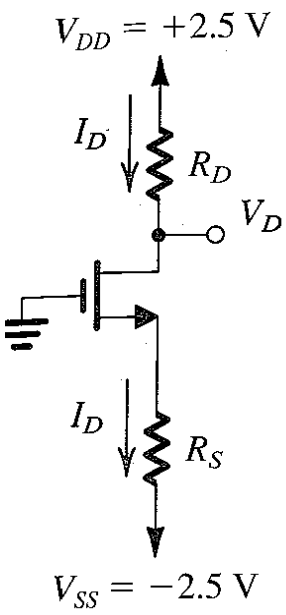
  (2) $v_{GD} \leq V_t \quad \Leftrightarrow \quad v_{DS} \geq v_{GS} - V_t \quad \Leftrightarrow \quad v_{DS} \geq v_{OV}$

- i-v Characteristics:

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS})$$

Análisis de MOSFET en CD

- Se desestima el efecto de la modulación del largo del canal



Características del Diseño

$$I_D = 0.4 \text{ mA}$$

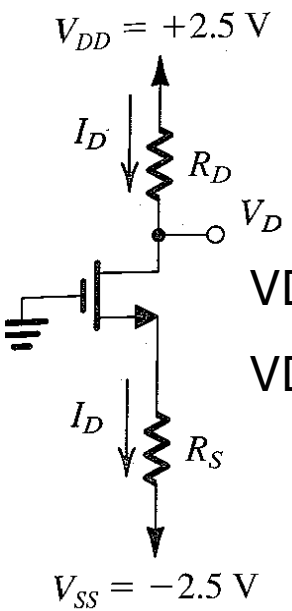
$$V_D = +0.5 \text{ V}.$$

Datos que provee el problema

$V_t = 0.7$ V, $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, $L = 1\ \mu$m, and $W = 32\ \mu$m.

Dimensionar RD y RS para cumplir características de operación dadas

Análisis del Circuito



VDG = VD – VG

VDG = +0.5 V

$$R_D = \frac{V_{DD} - V_D}{I_D}$$

$$= \frac{2.5 - 0.5}{0.4} = 5\ \text{k}\Omega$$

$$v_{GD} \leq V_t$$

<u>MOSFET operando en región de saturación</u>

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

$$R_S = \frac{V_S - V_{SS}}{I_D}$$

$$R_S = \frac{-1.2 - (-2.5)}{0.4} = 3.25\ \text{k}\Omega$$

<u>VGS = VG – VS</u>

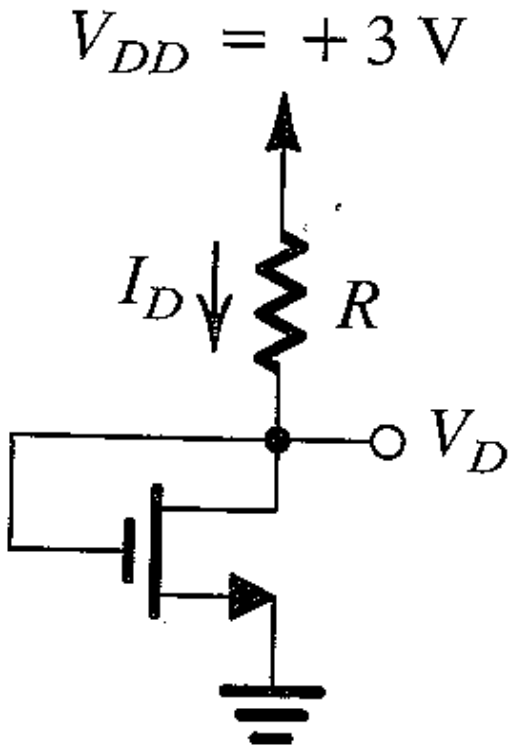
<u>VGS = 0 – VS = -VS</u>

$$V_{GS} = V_t + V_{OV} = 0.7 + 0.5 = 1.2\ \text{V}$$

Problema 2

$$V_t = 0.6 \text{ V}, \ \mu_n C_{ox} = 200 \ \mu\text{A/V}^2.$$

$$L = 0.8 \ \mu\text{m, and } W = 4 \ \mu\text{m.}$$



Calcule R y VD para ID =80 uA

A- Identifique los valores conocidos
B- Ubique el punto de operación del Transistor
C- Utilice las relaciones I-V del MOSFET para calcular los parámetros pedidos

A- Valores conocidos

VGD = 0

VGS = VDS

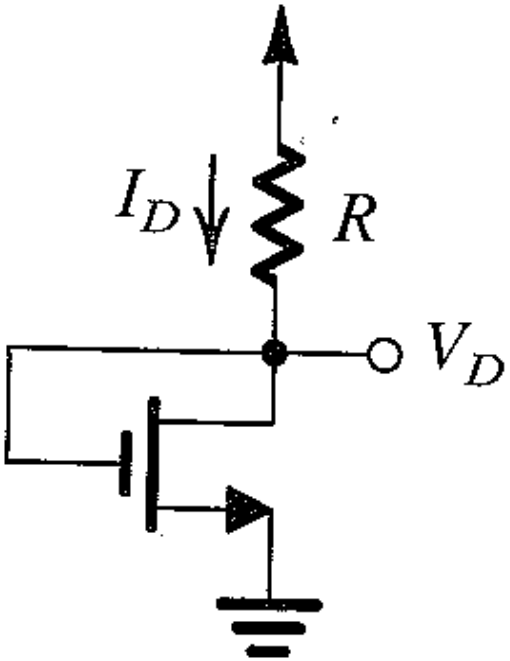
ID = 80 uA

Problema 2

$v_{GD} \leq V_t$ MOSFET operando en región de saturación

$V_{DD} = +3\ \text{V}$

0 < 0.6



VGS = VGS = VD

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

$$V_{GS} = V_t + V_{OV}$$

$$V_{OV} = \sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)}}$$

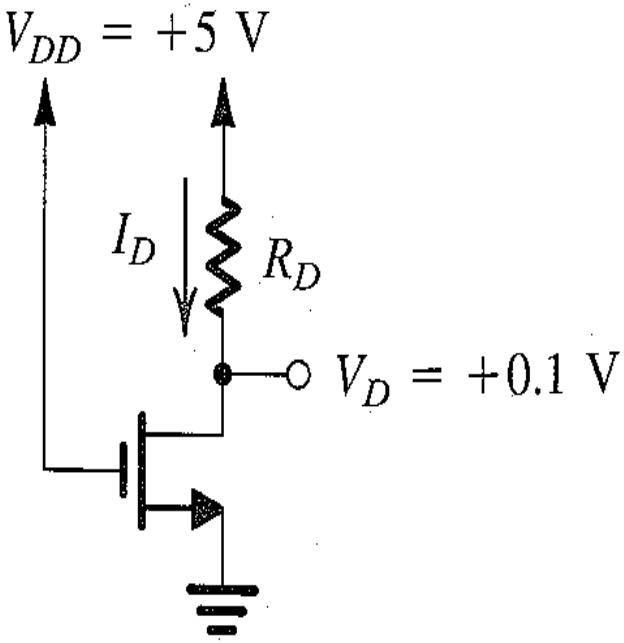
$$R = \frac{V_{DD} - V_D}{I_D}$$

$$= \frac{3-1}{0.080} = 25\ \text{k}\Omega$$

Problema 3

Calcule los valores de los componentes para obtener VD = 0.1

Calcule el valor de la resistencia para el dispositivo en este punto de operación



$k'_n(W/L) = 1$ mA/V^2.

$V_t = 1$

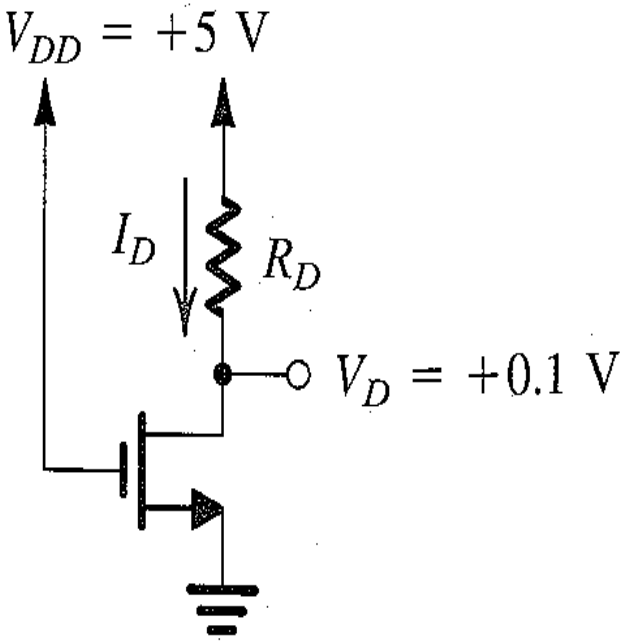
Datos del Circuito
VGS =5V
VDS = 0.1 V

Ubicación del punto de operación del transistor

$v_{GD} \geq V_t$ VGD = VGS – VDS = 4.9 V

4.9 V >1 V → Región de triodo

Problema 3



Calculo de los parámetros del circuito

$$I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$I_D = 1 \times \left[(5-1)\times 0.1 - \frac{1}{2}\times 0.01\right]$$

$$= 0.395 \text{ mA}$$

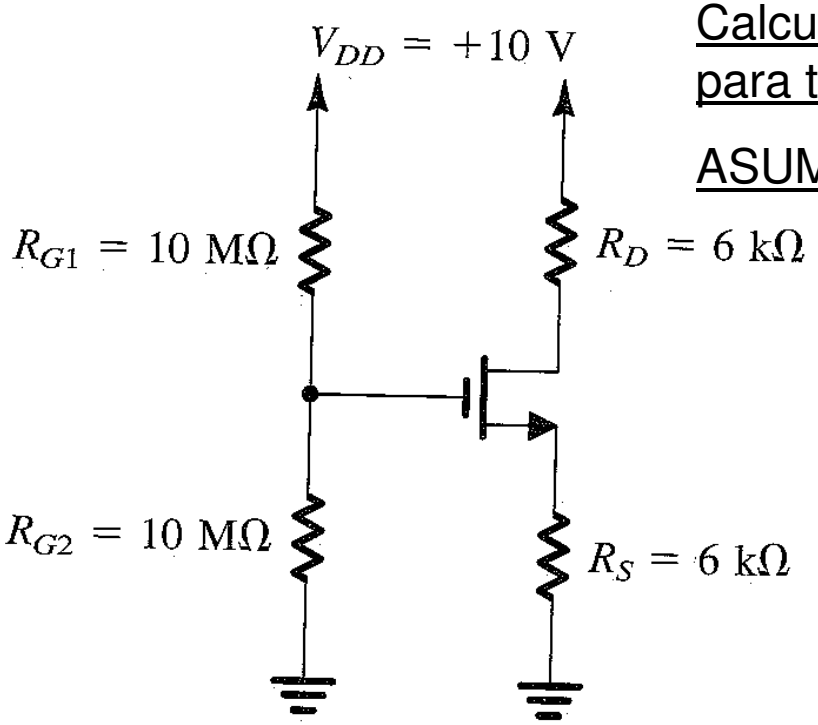
$$R_D = \frac{V_{DD} - V_D}{I_D}$$

$$= \frac{5 - 0.1}{0.395} = 12.4 \text{ k}\Omega$$

$$r_{DS} = \frac{V_{DS}}{I_D}$$

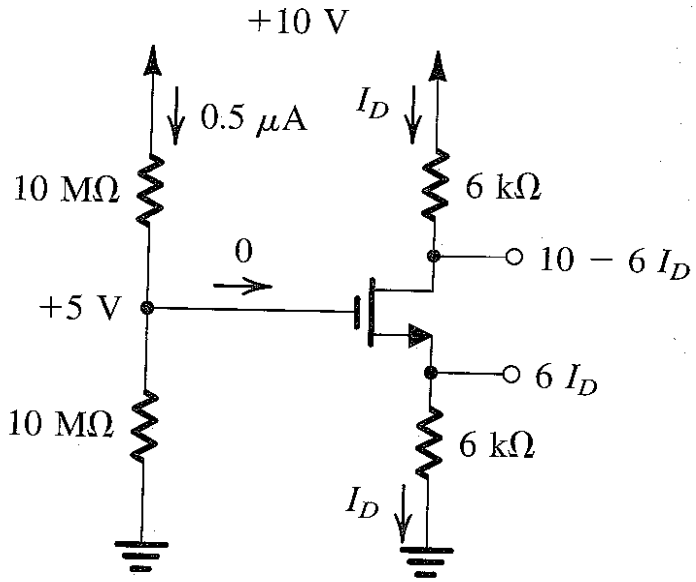
$$= \frac{0.1}{0.395} = 253\ \Omega$$

Problema 4

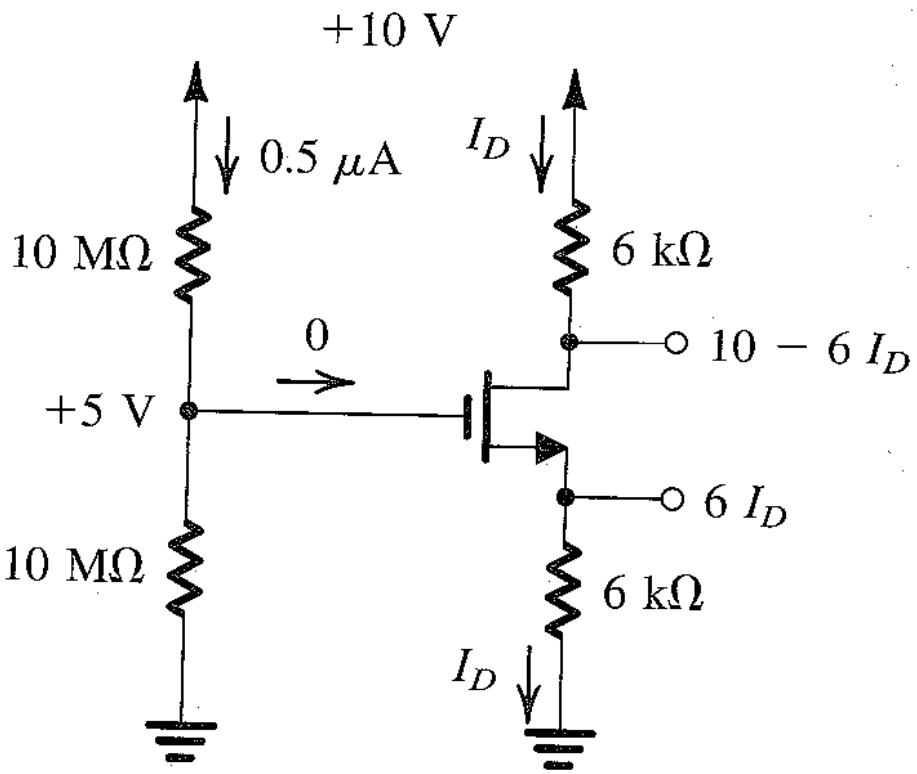


Calcule los valores de las corrientes y los voltaje para todos los nodos

ASUMA: $V_t = 1$ V and $k_n'(W/L) = 1$ mA/V^2



Problema 4



$$V_G = V_{DD}\frac{R_{G2}}{R_{G2}+R_{G1}} = 10\times\frac{10}{10+10} = +5\text{ V}$$

$$I_D = \frac{1}{2}k_n'\frac{W}{L}(V_{GS}-V_t)^2$$

$$= \frac{1}{2}\times 1\times(5-6I_D-1)^2$$

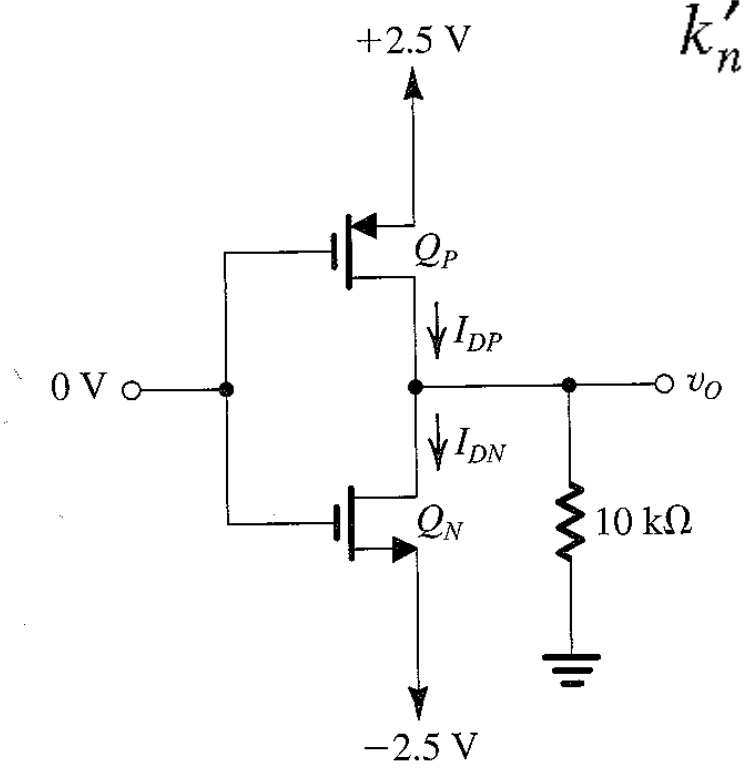
$$18I_D^2 - 25I_D + 8 = 0$$

$$V_D > V_G - V_t,$$

Problema 5

$$V_{tn} = -V_{tp} = 1\ \text{V}.$$

$$k_n'(W_n/L_n) = k_p'(W_p/L_p) = 1\ \text{mA/V}^2$$



Encuentre IDN IDP y Vo?

A- Valores deducibles del circuito

$$|V_{DG}| = 0$$