Single Event Upset Error Propagation Between Interconnected VLSI Logic Devices

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Abstract

This work presents experimental and analytical results of single event upset error propagation between interconnected VLSI logic devices representative of a spaceborne system. The results show that up to 50% of the time a single transistor upset internal to a logic device can result in system failure.

I. INTRODUCTION

To date, the majority of single event upset (SEU) testing has been performed at the device level. However, devices are rarely flown in spacecraft as single entities, rather, they are combined into memory units, processors and so on as subsystems within the spacecraft. Therefore, it is necessary to understand how upsets that occur in individual devices are propagated, multiplied or mitigated as they (the upset) move from one device to another interconnected device and eventually to the system output.

Previous results of cyclotron testing of individual VLSI logic devices have shown that errors can be observed at multiple output pads of the device (ref 1). Analysis of the cyclotron results show that errors occurring at multiple output pads can be due to a single transistor upset internal to the logic device. Note that a 1 to 1 (or 1 to 0) relation between internal transistor upset and device output errors may also occur. The devices tested and analyzed were CMOS/SOS VLSI logic devices. Each device is packaged in a 172 pin package.

The impetus of the current effort is to determine the system level impact of the error "multiplication" internal to the logic device and the effects of error propagation between interconnected devices which can eventually result in a system upset.

II. MULTICHIP ASSESSMENT/ANALYTICAL

The interconnected VLSI logic devices, designated by a "V", which were evaluated are shown in the block diagram of Figure 1. The 5 device types are all CMOS/SOS and comprise a portion of a Control Data 1750A space computer. This chip set was simulated while running diagnostic and functional software which included error detection and correction, parity checks on buses, microcode and internal registers and a fault handling routine. In general, when a fault is detected the fault handling routine is entered and if necessary the command is reissued.

A single event upset was simulated by changing the state on one of the known upsettable output pins of the V3 device for one clock cycle. The V3 device was chosen because it was the most extensively evaluated as an individual device. The results of the analyses show that the impact of the single upset injected ranged from no impact to system failure. The upset, and subsequent propagation was monitored by interrogating the data buses between the chips at each clock cycle and comparing the state to the expected (correct) state. In this manner the induced error was observed to have no impact on the data and functionality of the system in some cases and in other cases to propagate to the interconnected device, be multiplied in that device and eventually produce such a high density of bus errors that the system could not recover. Approximately 50% of the runs result in an error for one or two clock cycles which was corrected by the fault handling routine and system functionality was maintained. The remaining runs resulted in a system fault. These system faults are due to the error multiplication and propagation through the interconnected devices. These analytical results were verified by the Brookhaven test as discussed in the following paragraphs.

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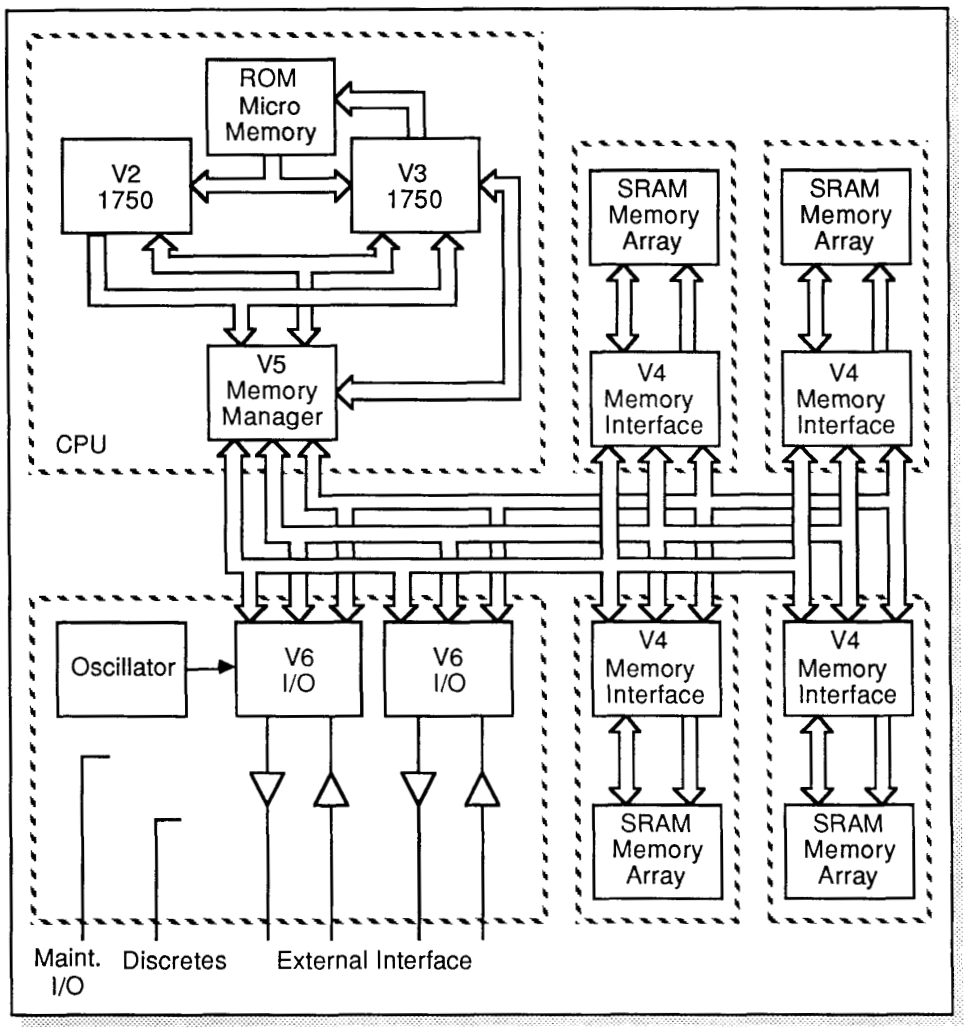

Figure 1. Block Diagram of Interconnected VLSI Devices

III. MULTICHIP ASSESSMENT/EXPERIMENTAL

Testing was performed at the Brookhaven Van de Graaff generator. The unit tested was a brassboard configuration of the system shown in figure 1. The brassboard set consists of 3 boards: Central Processing Unit (CPU), Memory and I/O. The CPU VLSI devices were tested. The CPU board faced the beam and the three VLSI devices delidded. The memory and I/O boards were located behind the CPU board and not exposed during this test. The entire brassboard configuration was placed in the vacuum chamber for the irradiation. The brassboard set was connected to a PC with tailored I/O boards and a frequency generator located adjacent to the vacuum chamber.

The ions required to induce upsets in the CMOS/SOS devices were Au ions with a minimum linear energy transfer (LET) of 123.7 MeV/mg/cm^2 which were used to induce upsets incident on the device. All of the system test data presented are for Gold ions, with a 32MHz base clock (devices at 8MHz) and an operating voltage of 4.5V. The software running during the irradiation for the data set presented in this summary was a register to register multiply function which exercised the entire system.

IV. RESULTS AND DISCUSSION

Overall, during the irradiation, one device could be hit, one device could be monitored "in situ" and the entire system output monitored. The data discussed in this paper are for the

case where the V3 chip was in the beam the V2 device was monitored in situ and the system output was monitored. This data is included in table 1. The V2 static bias condition (row 1 in table 1) consisted of loading the V2 registers with a known data pattern, irradiating the device and comparing the post irradiation data files with the known data. This test is identical to testing generally performed when only a single device is tested. The dynamic condition, on the other hand, exercises the entire system with the data presented here for the system running a multiplies function (MR). The MR test multiples identical paired values and compares them. If the values are not equal a system breakpoint (failure) is flagged. If an upset is observed in a register other than those being compared, a bit flip is flagged. Therefore, in the MR dynamic situation one device (V3) was "hit", a second interconnected device (V2) was monitored to evaluate error propagation between the V3 and V2 devices and the system output was monitored to determine errors propagating from V3/V2 through all other interconnected devices to the system output.

Several important factors are to be noted from the data in table 1. First, the cross section for the dynamic situation is slightly higher than the static situation. This is expected since in the dynamic situation SETS (Single Event Transients) will also contribute to the "error count". Second, the observance of breakpoints or catastrophic failures only occurs under dynamic bias, again as expected since errors will only propagate to the system output with clocking which occurs under the dynamic situation only.

The most significant results are contained in the evaluation of the data presented in the last row of table 1. The V3 device is the beam and based on testing performed on V3 in the static mode a cross section of 1.6×10^{-6} cm^2/V3 device was determined. Since the cross section is upsets per ion fluence (ions/cm^2), we would expect that hitting the V3 device with 1×10^6 ions/cm^2 would result in 1.6 upsets observed at the V3 device output pins. During the dynamic test, errors were observed in the interconnected (but nonirradiated) V2 device on the order of 0.9 errors per 1×10^6 ions/cm^2 hitting the V3 device.

These results not only imply that single particle induced upsets occurring in the irradiated V3 device are propagated to the V2, resulting in observed errors in the registers but also that the percentage of upsets propagated is approximately 56%. That is, slightly over half of the upsets occurring in V3 are propagated to and observed in the V2 device.

The significance of this result is understood when considering the methodology employed to calculate a system level upset. Traditionally, upset rates for individual devices are simply added to determine a system level upset rate. For this example, units of upsets per million ions per cm^2 will be used to maintain consistency with the previous discussion. Note that upsets/ions/cm^2 can be translated to upsets/device-day given device parameters, i.e. critical charge, and a specific environment.

So, for our simple example of a 2 device system, as shown in Figure 2, the number of upsets calculated per 1×10^6 ions/cm^2 using the traditional addition method would result in 3.2 upsets /10^6 ions/cm^2 (1.6 + 1.6) at the system level. However, taking into account error propagation between the V3 and V2 devices results in a rate of 4.1 upsets per million ions/cm^2 (1.6 + 1.6 + 0.9) as shown in the lower portion of Figure 2. This implies that by simply adding individual device upset rates, a lower system level upset rate will be obtained than when error propagation is considered.

Table 1. System Results

Softwrae: MR
System Freq: 32 MH_z
Voltage: 4.5V
All Data: Au, LET= 123 MeV/mg/cm2

Test Condition "Hit"	Monitor	Bias	Total ions/cm^2	VLSI Device Cross Section	System Breakpoints
V2	V2	static	10.5×10^6	1.5×10^{-6}	0
V2	V2+system	dynamic	10.0×10^6	1.6×10^{-6}	2
V3	V2+system	dynamic	10.0×10^6	8.99×10^{-7}	12

Note: Device cross section in cm^2/VLSI device. This value is calculated using bit upsets only and does not include the contribution of breakpoint (catastrophic) failures.

Another aspect of the data is the catastrophic errors are only observed under dynamic bias conditions and that the number of breakpoints observed can vary significantly due to the probabilistic nature of the exact time and location of an SEU hit. Returning again to the data represented by the lowest row of table 1, it is noted that for the ion fluence shown, 10 million ions/cm^2, that 12 system breakpoints or failures were observed. That is 12 "upsets" were observed at the total system output. In this run, for 10 million ions/cm^2 we predict 16 upsets occurring in V3 (the irradiated device) with approximately 9 of those upsets being propagated to the V2 device. Since V2 is not irradiated, we could expect only those 9 errors as a maximum to be propagated to the system output. However 12 breakpoints are observed. This observation implies one or a combination of 2 phenomenon. First, the 9 errors observed in the V2 registers may be being multiplied within the V2 device before the signals proceed through interconnected devices and to the system output. Or, second 9 errors may indeed be output from the V2 device however, those 9 errors are multiplied as they pass through interconnected devices as they progress through the system to the output. The actual observation of 12 upsets may be a result of either of these phenomena or combination of the two. Additional testing is required to investigate this effect.

IV. CONCLUSION

Experimental testing has verified error propagation between interconnected VLSI devices. The data show that by neglecting the propagated errors an overly conservative (low) combined error rate may be calculated at the system level. Catastrophic system level failures were observed with occurrence frequencies between 0.2 failures/million ions/cm^2 and 1.2 failures/million ions/cm^2 verifying upset propagation to system output with implications of error multiplication either within individual devices or as an error propagates through the system.

V. REFERENCE

[1] D. M. Newberry, Single Event Upsets in VLSI Logic Devices - Experimental and Analytical Assessment, DNA-TR-87-228, October, 1987.

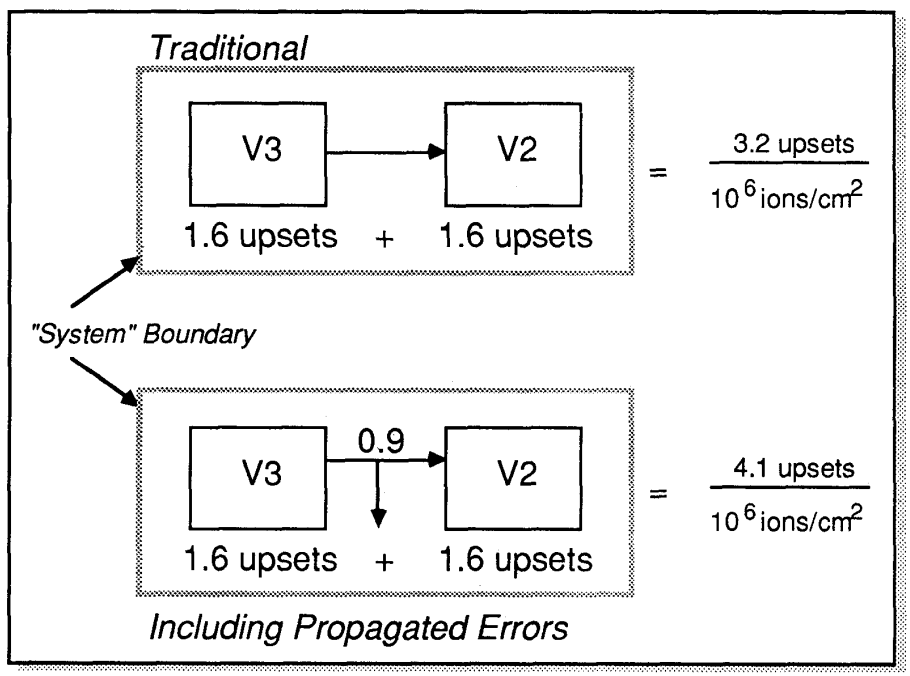

Figure 2. Approaches for Calculating System Error Rates