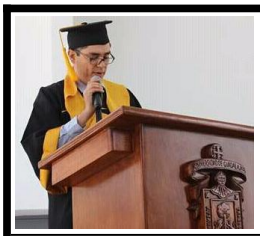

FRANCISCO FLORES

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I am a technology enthusiast; I like to integrate technology with all kinds of applications. I am fascinated by creating hardware designs with specialized firmware to interfaces to integrate computing technologies such as: hardware design for pcb and also firmware development with development modules and also cloud applications, artificial intelligence, machine learning, mixed with the internet of things (IoT) and industry 4.0

EXPERIENCE

JUN 2019 – NOV 2021

IT MANAGER AND TECHNOLOGY INTEGRATION ENGINEER, GALEX GAME

Management of technological projects derived from the design of hardware and software applied for the company, support, follow up of the same, implementation of development phases

- Creation of an internet of things platform to connect electronic cards (Team leader and integration engineer)
- Implementation of serial protocols (I2c,Uart,Spi) to interconnect IoT electronic devices to arcade machines (Owner, Integration engineer)
- Management of Galex system, internal and external programs configuration for implementation on internal servers or servers in the cloud (IT Manager)
- Galex network management with firewall for remote access with VPN management switches, routers and other network systems (IT Manager)
- Progress management of internal software and hardware development project using scrum with Monday (Team leader, metting with stackeholder and team)

JUN 2016 – JUL 2019

SOFTWARE AND HARDWARE DEVELOPMENT ENGINEER, INTRALIX

Development of web services, comparisons, port information replicator, ip tcp port communication between servers, custom electronic design, integration, firmware updates, remote VPN connections

- Creation of design pcb versions for multiple purpose with gps to secure assets using 8 bits micro-controllers (Project leader, design hardware and firmware developer)
- Creation of interface to communicate with databases of gps platforms and crm systems (Collaboration, backend developer)
- Creation monitoring system for the analysis of fuel consumption vs kilometers traveled (Team support bugs, backend developer)
- Interface synchrony for gps 4G device data replication for multiple gps platforms (Owner, Integration engineer and backend developer) https://www.intralix.com/plataformas.html

EDUCATION

JULY 2017 – (PROFESSIONAL LICENSE #12231563)

GRADUATE IN COMPUTER SCIENCE ENGINEERING,

UNIVERSITY OF GUADALAJARA

DEC 2021 – (PROFESSIONAL LICENSE IN PROGRESS)

GRADUATE OF MASTER´S DEGREE IN MULTIMEDIA INTELLIGENT SYSTEMS,

POSTGRADUATE STUDIES CIATEQ

JULY 2022

SPECIALIZED TALENT DEVELOPMENT PROGRAM: PRE-SILICON VERIFICATION,

INSTITUTO NACIONAL DE ASTROFÍSICA, ÓPTICA Y ELECTRÓNICA

COLLABORATIVE TEAMWORKS (4):

1. Documentation for system verilog code (Collaboration)
2. Creating diagrams to interpret circuit design logic in system verilog (Collaboration)
3. Creation of reports and presentation for project presentation (Collaboration)
4. Automation with script in python and c++ to elaborate test bench for modules in system verilog (Collaboration)
5. Create verilog code for ALU, MemReg and DataMemory modules for unicycle mips architecture (Collaboration)

TECHNICAL SKILLS

- Verilog for Digital Systems HW Description (intermediate level)
- SystemVerilog for Verification (intermediate level)
- UVM (intermediate level)
- C/C++ programming (high level)
- Python programming (high level)
- Protocols: CAN, I2C, UART, SPI, RS232, Wifi, Web-Sockets, Mqtt, Tcp Ip and Https (high level)
- IoT technology integrations with Web-Service/Api-Rest platforms for electronics modules 32 bits (high level)
- Pcb Design: Eagle and Fritzing design of custom components for new modules, diagrams and schematics (intermediate level)
- Test and Measurement Equipment: Oscilloscope and Logic Analyzer (high level)
- Linux Systems (high level)
- Intel processors Microarchitectures (intermediate level)
- Digital Systems Verification (intermediate level)
- Web Projects: frameworks with php, python and net-core(high level)
- Setup cloud services: VPS configurations for linux and windows with apache and nginx (high level)
- Databases: SqlServer, Mysql-Maria triggers and stored procedure management (intermediate level)
- Version control software: Github, Gitlab and Bitbucket (high level)
- Agile Methodologies: Scrum, Kanvas (trello and monday), Jenkins principles (intermediate level)

LANGUAGES

- ENGLISH: median level (Toefl Itps score: 490)
- SPANISH: Native

CERTIFICATIONS AND PUBLICATIONS

- **Tesis:** Improvement proposal to develop an application model for IoT services in entertainment machines (https://ciateq.repositorioinstitucional.mx/jspui/handle/1020/569)
- **Article:** Internet of Things (IoT) applications, approaches and trends: systematic literature review (https://ciateq.repositorioinstitucional.mx/jspui/handle/1020/543)
- **Article:** Intelligent IoT Platform to Predict Failures in the Reception of Equipment Telemetry Requests (in progress)
- **Article:** Implementation of Interface for Device and Smart IoT Platform Integration (in progress)

EXTRA INFORMATION

- **Personal Project:** IoT-Hotspot is a simple platform that applies Internet of Things (IoT) technology, strengthening it with a bit of statistics and an algorithm for machine learning (AI) focused on failure prediction and telemetry analysis of the devices.
  Link Web: https://hotspot.fjlic.com
  Link GiHub: https://github.com/fjlic/IoT-Hotspot-Laravel
  Link Documentation: https://hotspot.fjlic.com/docs/1.0/overview
- **Personal Project:** Design modular prototype with modules Arduino Nano, ESP32 and A9G GPRS with GPS + SD Card that allowed us to send telemetry to the IoT platform, this was a two-layer design to validate the sending of telemetry.
  Link Web: https://hotspot.fjlic.com/docs/1.0/firmware-erb
  Link GiHub: https://github.com/fjlic/IoT-Hotspot-Laravel/tree/master/electronics_boards/erb_board/fritzing/SensorIOT
- **Personal Project:** web project to create your own portfolio of projects in the purest cms style.
  Link Web: https://fjlic.com
  Link GiHub: https://github.com/fjlic/Fjlic-Cms
  Link Documentation: https://fjlic.com/docs/1.0/overview
- **Project Documentation Link (workgroup of four):** practices for understanding verification tests with system verilog and uvm applied to mips architecture.
  Mips monocycle with system verilog: https://www.edaplayground.com/x/WCm9
  Mips multicycle with system verilog : https://www.edaplayground.com/x/tNJ5
  Mips monocycle with uvm: https://www.edaplayground.com/x/UG33
  Mips multicycle with uvm: https://www.edaplayground.com/x/f4bk