

# Lab Notebook

## FPGA Capstone Project

### Academic Integrity

*By signing below you acknowledge the CU Honor Code, "On my honor, as a University of Colorado Boulder student I have neither given nor received unauthorized assistance" applies to this assignment.*

Signed: \_\_\_\_\_

## Module 1

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### Setup

Author:

Date:

Procedure/Description of Test:

Observations:

Data:

Images/Drawings:

Results:

DE10_LITE_Small	
Fmax	
Logic Utilization %	
# Flip-Flops	

DE10_LITE_Default	
Fmax	
Logic Utilization %	
# Flip-Flops	

Questions:

1. Record your observations of the board behavior once the FPGA is programmed. Does it behave as you might expect?

Conclusions:

Lessons Learned (What did you learn?):

## Part 1

Author:

Date:

Procedure/Description of Test:

Observations:

Data:

Images/Drawings:

Results:

Fmax	
Logic Utilization %	
# Flip-Flops	

Questions:

1. Based on your observations of the board behavior once the FPGA is programmed, does it behave as you might expect?

2. Explain the reason for the number of flip-flops used in the design.

Conclusions:

Lessons Learned (What did you learn?):

## Part 2

Date:

Procedure/Description of Test:

Observations:

Data:

Images/Drawings:

Results:

Fmax	
Logic Utilization %	
# Flip-Flops	
With V = 0, z	
With V = 0, A	
With V = F, z	
With V = F, A	

Questions:

1. Based on your observations of the board behavior once the FPGA is programmed, does it behave as you might expect?
2. Does this design use more or less logic than the design in Part 1? Why?

Conclusions:

Lessons Learned (What did you learn?):

### Part 3

Date:

Procedure/Description of Test:

Observations:

Data:

Images/Drawings:

Results:

Fmax	
Logic Utilization %	
#Flip-Flops	

Questions:

1. Based on your observations of the board behavior once the FPGA is programmed, does it behave as you might expect?

Conclusions:

Lessons Learned (What did you learn?):

### Part 4

Date:

Procedure/Description of Test:

Observations:

Data:

Images/Drawings:

Results:

# Logic Cells	
Logic Utilization %	

Questions:

1. Based on your observations of the board behavior once the FPGA is programmed, does it behave as you might expect?

Conclusions:

Lessons Learned (What did you learn?):

## Part 5

Date:

Procedure/Description of Test:

Observations:

Data:

Images/Drawings:

Results:

# Logic Cells	
Logic Utilization %	

Questions:

1. Based on your observations of the board behavior once the FPGA is programmed, does it behave as you might expect?
2. How does this compare to the number of Logic Cells in Part 4?

Conclusions:

Lessons Learned (What did you learn?):

## Module 2

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### PWM

Author:

Date:

Procedure/Description of Test:

Observations:

Data:

Images/Drawings:

Results:

Fmax	
% Logic Utilization	
Total registers	

Questions:

1. Did the LED change brightness depending on the setting of the first 3 switches?

Conclusions:

Lessons Learned (What did you learn?):

## ADC

Author:

Date:

Procedure/Description of Test:

Observations:

Data:

Images/Drawings:

Results:

Fmax	
%Logic Utilization	

Questions:

1. Does the board behave as you expected?
2. Is this a good voltmeter as is?
3. What could you change in either the board hardware or FPGA logic to make it perform better?

Conclusions:

Lessons Learned (What did you learn?):

## Module 3

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### NIOS II Hardware Design

Author:

Date:

Procedure/Description of Test:

Observations:

Data:

Images/Drawings:

Results:

Fmax	
Logic Utilization	

Questions:

1. What is the purpose of the Avalon Memory-Mapped Clock-Crossing Bridge?

Conclusions:

Lessons Learned (What did you learn?):



## Module 4

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### NIOS II Software Design and System Test

Author:

Date:

Procedure/Description of Test:

Observations:

Data:

Images/Drawings:

Results:

Fmax	
Logic Utilization	

Questions:

1. Is the control of the 10 LEDs implemented in hardware or in software?
2. Is the control of the 7-segment LEDs done by hardware or by software?
3. How much memory is required to run your Nios II program? Can you fit it into the onchip RAM if you redesign the onchip RAM block?
4. Your Nios II processor is running at what clock speed? How much faster can it run in your MAX10 design?

Conclusions:

Lessons Learned (What did you learn?):