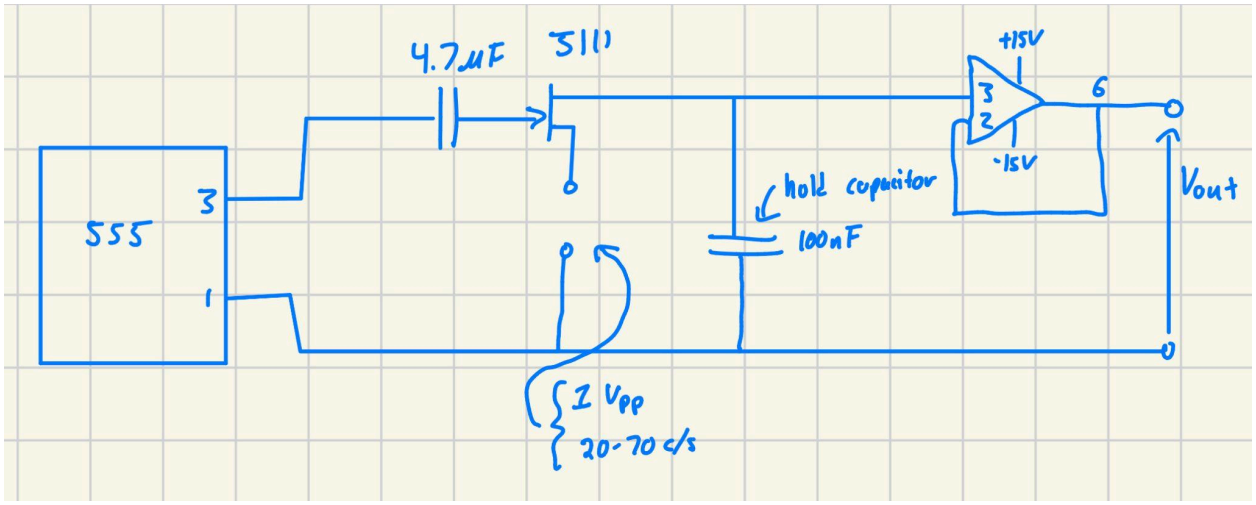
ECE 182 Lab #7 Sample and Hold Circuit
Day of Submission: 10/17/2025
Name of student: Frank Tamburro

Circuit and Schematic

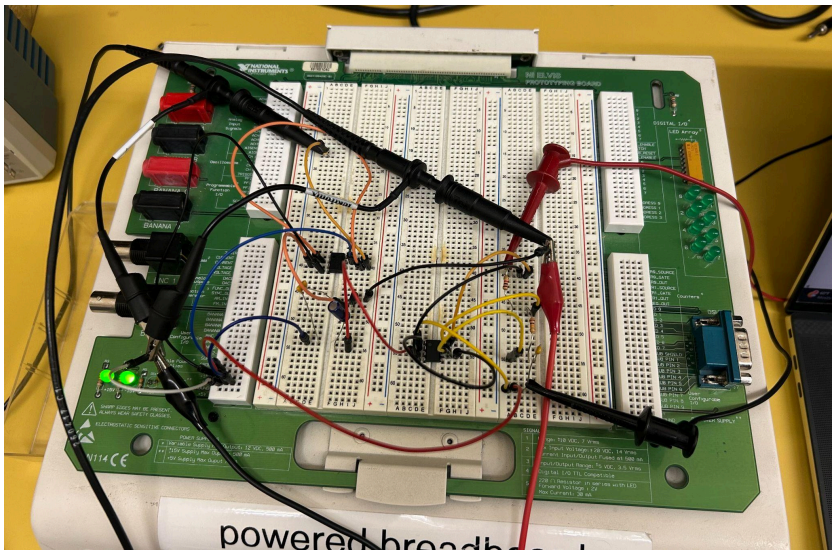


- Theoretical vs Experimental
- Hold Capacitor: 100nF vs 100.9 nF
- 4.7 microFarad vs 4.733 microfarad

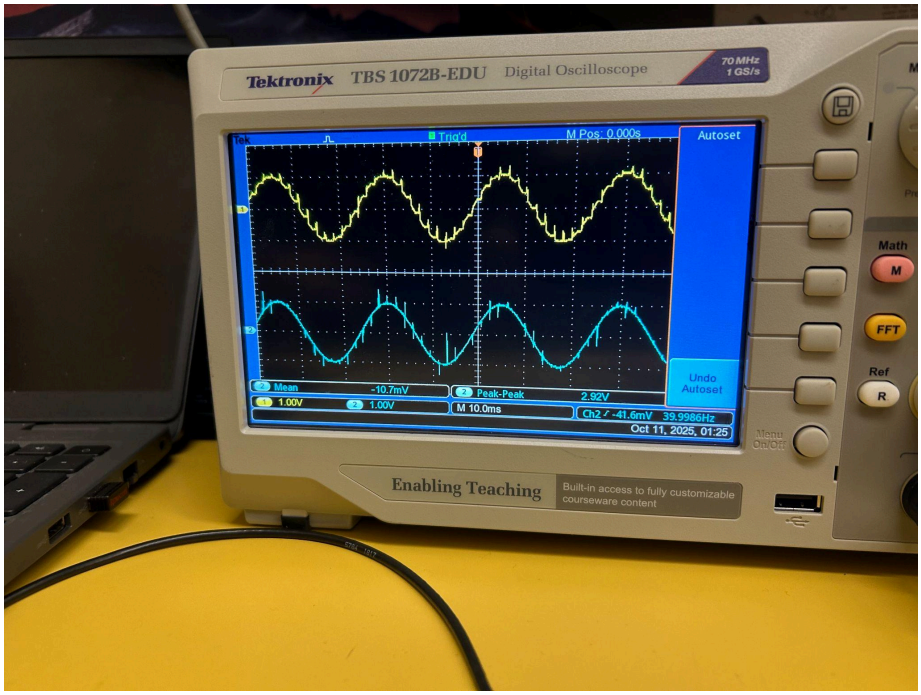
Equations for Theoretical Basis

Results and Calculations

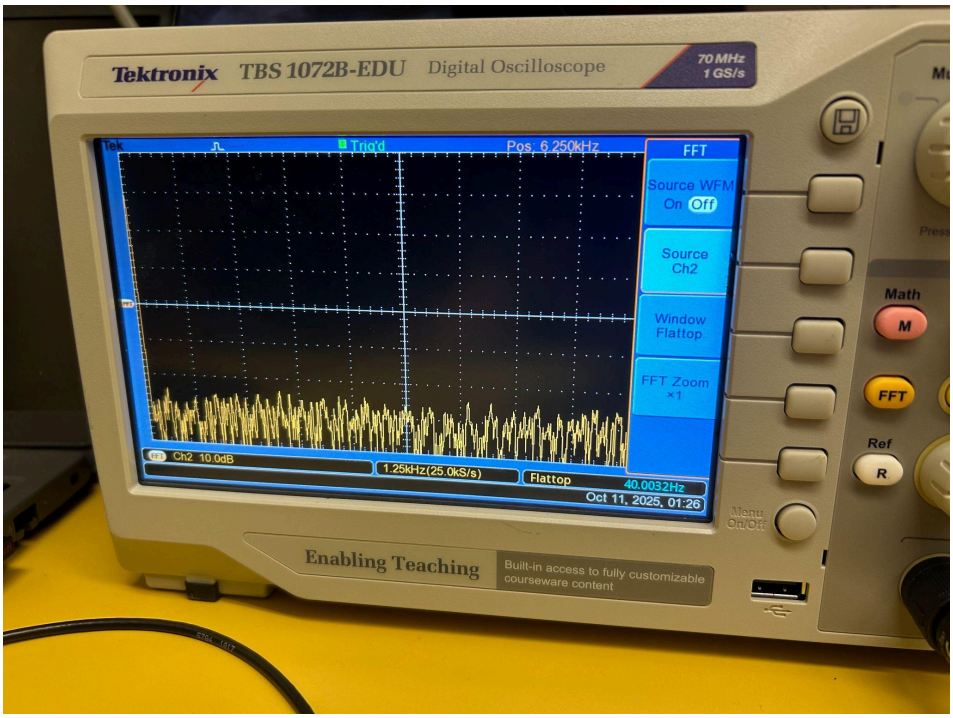
Circuit on Breadboard



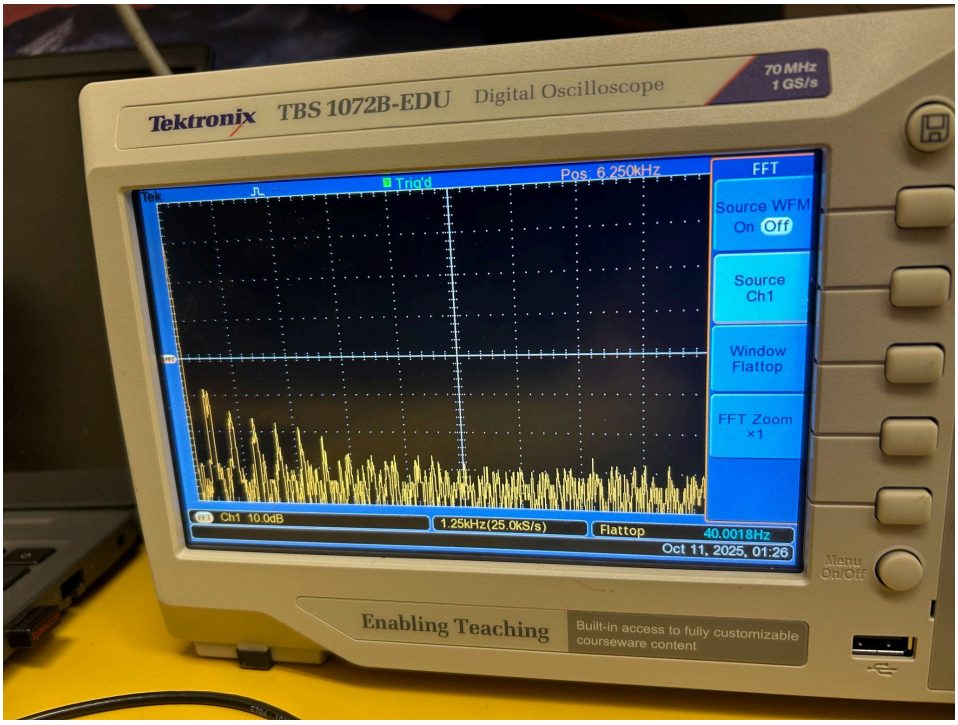
Input (Blue) and Output (Yellow) Waveforms



FFT Input



FFT Output



Calculations

$$\text{Voltage Droop Rate} = \frac{\Delta V}{\Delta I} = \frac{2.92 - 2V}{3mA - 0mA} = 0.64$$

Summary

In this lab, a sample and hold circuit was designed and tested to understand how it captures and maintains an analog signal for a short duration. Using a J111 JFET, 1N4001 diode, and a 100 nF hold capacitor, the circuit successfully sampled a 30 Hz sinusoidal input driven by a 555-timer pulse at 600 Hz. The output waveform displayed the expected staircase shape, with each step corresponding to a held sample. FFT analysis showed that the output contained the input frequency along with higher order harmonics introduced by the sampling process. Minor voltage droop was observed during the hold period, caused by leakage and component tolerances. Overall, the results verified that the circuit functioned as intended, demonstrating key concepts of sampling, signal retention, and the importance of capacitor quality and switch behavior in analog systems.