Mini Frost32 CPU

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Table of Contents

Registers

There are 16 general purpose registers: `r0` (always zero), `r1`, `r2`, `r3`, `r4`, `r5`, `r6`, `r7`, `r8`, `r9`, `r10`, `r11`, `r12`, `lr`, `fp`, `sp`

One last register is the program counter, `pc`.

Instructions and Encoding

- **`add rA, rB, rC`**
  - Encoding: `0000 aaaa bbbb cccc 0000 0000 0000 0000`
  - Encoding Note: `rC != 0`
- **`addi rA, rB, simm16`**
  - Encoding: `0000 aaaa bbbb 0000 iiii iiii iiii iiii`
- **`sub rA, rB, rC`**
  - Encoding: `0001 aaaa bbbb cccc 0000 0000 0000 0000`
  - Encoding Note: `rC != 0`
- **`subi rA, rB, simm16`**
  - Encoding: `0001 aaaa bbbb 0000 iiii iiii iiii iiii`
- **`sltu rA, rB, rC`**
  - Encoding: `0010 aaaa bbbb cccc 0000 0000 0000 0000`
  - Encoding Note: `rC != 0`
- **`sltui rA, rB, simm16`**
  - Encoding: `0010 aaaa bbbb 0000 iiii iiii iiii iiii`
- **`slts rA, rB, rC`**
  - Encoding: `0011 aaaa bbbb cccc 0000 0000 0000 0000`
  - Encoding Note: `rC != 0`
- **`sltsi rA, rB, simm16`**
  - Encoding: `0011 aaaa bbbb 0000 iiii iiii iiii iiii`
- **`add rA, pc, rC`**
  - Encoding: `0100 aaaa 0000 cccc 0000 0000 0000 0000`
  - Encoding Note: `rC != 0`

- **addi** rA, pc, simm16
  - Encoding: 0100 aaaa 0000 0000 iiii iiii iiii iiii
- **lui** rA, simm16
  - Encoding: 0101 aaaa 0000 0000 iiii iiii iiii iiii
- **lsl** rA, rB, rC
  - Encoding: 0110 aaaa bbbb cccc 0000 0000 0000 0000
  - Encoding Note: rC != 0
- **lsli** rA, rB, simm16
  - Encoding: 0110 aaaa bbbb 0000 iiii iiii iiii iiii
- **lsr** rA, rB, rC
  - Encoding: 0111 aaaa bbbb cccc 0000 0000 0000 0000
  - Encoding Note: rC != 0
- **lsri** rA, rB, simm16
  - Encoding: 0111 aaaa bbbb 0000 iiii iiii iiii iiii
- **asr** rA, rB, rC
  - Encoding: 1000 aaaa bbbb cccc 0000 0000 0000 0000
  - Encoding Note: rC != 0
- **asri** rA, rB, simm16
  - Encoding: 1000 aaaa bbbb 0000 iiii iiii iiii iiii
- **jmp** rA
  - Encoding: 1001 aaaa 0000 0000 0000 0000 0000 0000
- **beq** rA, rB, simm16
  - Encoding: 1010 aaaa bbbb 0000 iiii iiii iiii iiii
- **bne** rA, rB, simm16
  - Encoding: 1011 aaaa bbbb 0000 iiii iiii iiii iiii
- **ldr** rA, [rB, rC]
  - Encoding: 1100 aaaa bbbb cccc 0000 0000 0000 0000
  - Encoding Note: rC != 0
- **ldri** rA, [rB, simm16]

  - Encoding: `1100 aaaa bbbb 0000 iiii iiii iiii iiii`

- **`str rA, [rB, rC]`**
  - Encoding: `1101 aaaa bbbb cccc 0000 0000 0000 0000`
  - Encoding Note: `rC != 0`

- **`stri rA, [rB, simm16]`**
  - Encoding: `1101 aaaa bbbb 0000 iiii iiii iiii iiii`