

Volt32 CPU

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Registers, Main Widths, etc.

- The main width of the processor is 32-bit, and addresses are 32-bit. Some 64-bit operations exist.
- The machine is an implementation of Line Associative Registers (LARs). Both instruction LARs (ILARs) and data LARs (DLARs) are included in the design. There are a grand total of 128 ILARs and 128 DLARs, but they are split between the LARs owned by the supervisor mode and the LARs owned by the user mode. There are 64 supervisor mode ILARs, 64 supervisor mode DLARs, 64 user mode ILARs, and 64 user mode DLARs.
- The machine boots in supervisor mode. The processor jumps to address 0x0 when it enters supervisor mode, which includes when the machine boots.
- ILARs
 - In user mode, ILARs 0 to 63 are referred to as `i0`, `i1`, `i2`, ..., `i61`, `i62`, `ipc`.
 - In supervisor mode, ILARs 64 to 127 are referred to as `i0`, `i1`, `i2`, ..., `i61`, `i62`, `ipc`.
 - The two ILARs called "`i0`" have all their fields set to zero, and when written to, the contents of the ILAR does not change.
 - The two ILARs called "`ipc`" are the program counters for the two operating modes of the processor.
 - An ILAR's data field is 128 bytes long. It is composed of 32-bit instructions aligned to 32 bits.
 - An ILAR's scalar offset field is 5-bit due to instructions being 32-bit and the data field being 128 bytes long.
 - The base address field of an ILAR is $(32 - 7 = 25)$ -bit.
 - An ILAR's tag field is 6-bit.
- DLARs
 - In user mode, DLARs 0 to 63 are referred to as `d0`, `d1`, `d2`, ..., `d59`, `d60`, `dcp`, `dfp`, `dsp`.
 - In supervisor mode, DLARs 64 to 127 are referred to as `d0`, `d1`, `d2`, ..., `d59`, `d60`, `dcp`, `dfp`, `dsp`.
 - The two DLARs called "`d0`" have all their fields set to zero, and when written to, the contents of the DLAR does not change.
 - A DLAR's data field is 128 bytes long. It is composed of the scalar data elements of the 128 byte vectors, where the type of the scalar data elements is determined by the type tag field of the DLAR.
 - A DLAR's scalar offset field is 7-bit due to the data field being 128 bytes long.

- The base address field of a DLAR is $(32 - 7 = 25)$ -bit.
 - DLARs can take on the following types (3-bit enum):
 - * 8-bit, unsigned (`u8`)
 - * 8-bit, signed (`i8`)
 - * 16-bit, unsigned (`u16`)
 - * 16-bit, signed (`i16`)
 - * 32-bit, unsigned (`u32`)
 - * 32-bit, signed (`i32`)
 - * 64-bit, unsigned (`u64`); only usable for some operations
 - * 64-bit, signed (`i64`); only usable for some operations
 - A DLAR's tag field is 6-bit.
- The `ie` register
 - "interrupt enable"
 - This register is 1-bit.
 - This register is a flag indicating whether or not an interrupt can be serviced. It can be read from/written to using `cpy` instructions.
 - The `reti` instruction sets `ie` to `0b1` and returns to user mode from supervisor mode.
 - The `xct` register
 - "exception type"
 - This register is 32-bit.
 - This register is set to the numerical value of an exception's type upon the machine entering supervisor mode. It can be read from/written to using `cpy` instructions.
 - The `swiarg0` register
 - This register is 32-bit.
 - This register indicates argument 0 to `swi`. It can be read from/written to with `cpy` instructions.
 - The `swiarg1` register
 - This register is 32-bit.
 - This register indicates argument 1 to `swi`. It can be read from/written to with `cpy` instructions.
 - The `swiarg2` register
 - This register is 32-bit.

- This register indicates argument 2 to `swi`. It can be read from/written to with `cpy` instructions.
- The `swiarg3` register
 - This register is 32-bit.
 - This register indicates argument 3 to `swi`. It can be read from/written to with `cpy` instructions.

Exceptions

Some instructions may cause an exception to occur, putting the processor in supervisor mode.

The following exceptions may occur during normal execution of a program. `xct` is set to a numerical value representing these upon the processor encountering an exception.

- Taking an interrupt, which also sets `ie` to `0b0`.
- Division by zero.
- Undefined instruction.
- Instructions where 64-bit ops are not defined.
- `swi`.
 - Note that this instruction always causes an exception to occur.
- `reti` when in user mode.
- `retx` when in user mode.
- `cpy` that reads from `ie` in user mode.
- `cpy` that writes to `ie` in user mode.
- `cpy` that reads from `xct` in user mode.
- `cpy` that writes to `xct` in user mode.
- `cpy` that reads from `swiarg0` when in user mode.
- `cpy` that writes to `swiarg0` when in user mode.
- `cpy` that reads from `swiarg1` when in user mode.
- `cpy` that writes to `swiarg1` when in user mode.
- `cpy` that reads from `swiarg2` when in user mode.
- `cpy` that writes to `swiarg2` when in user mode.
- `cpy` that reads from `swiarg3` when in user mode.
- `cpy` that writes to `swiarg3` when in user mode.
- Instructions that read from supervisor mode ILARs or DLARs when in user mode.
- Instructions that write to supervisor mode ILARs or DLARs when in user mode.

Instructions

4.1 Group 0 Instructions

- Encoding: 0000 aaaa aabb bbbb cccc cddv dddv oooo
 - a: DLAR a
 - b: DLAR b
 - c: DLAR c
 - d: DLAR d (d0 to d31)
 - v:
 - * when 0b0: scalar operation. The assembly syntax indicating a scalar operation simply adds ".s" to the instruction's name.
 - * when 0b1: vector operation. The assembly syntax indicating a vector operation simply adds ".v" to the instruction's name.
 - o: Opcode
- Instruction List:
 1. add dA, dB, dC
 - This instruction causes an exception if dA is of the following types: u64, i64.
 2. sub dA, dB, dC
 - This instruction causes an exception if dA is of the following types: u64, i64.
 3. slt dA, dB, dC
 - This instruction causes an exception if dA is of the following types: u64, i64.
 4. mul dA, dB, dC
 - This instruction causes an exception if dB or dC is of the following types: u64, i64.
 5. div dA, dB, dC, dD
 - This instruction causes an exception if dB, dC, or dD is of the following types: u64, i64.
 - This instruction writes the quotient into dA, and the remainder into dD.
 6. and dA, dB, dC
 7. or dA, dB, dC
 8. xor dA, dB, dC
 9. shl dA, dB, dC
 - Logical shift left.

- This instruction causes an exception if dA, dB, or dC is of the following types: u64, i64.
 - This instruction casts a temporary copy of dC to the unsigned type that is the same size as dA's type and uses that instead of dC.
10. `shr dA, dB, dC`
- Logical shift right if dA is unsigned, or arithmetic shift right if dA is signed.
 - This instruction causes an exception if dA, dB, or dC is of the following types: u64, i64.
 - This instruction casts a temporary copy of dC to the unsigned type that is the same size as dA's type and uses that instead of dC.
11. `rol dA, dB, dC`
- Rotate left.
 - This instruction causes an exception if dA, dB, or dC is of the following types: u64, i64.
 - This instruction casts a temporary copy of dC to the unsigned type that is the same size as dA's type and uses that instead of dC.
12. `ror dA, dB, dC`
- Rotate right.
 - This instruction causes an exception if dA, dB, or dC is of the following types: u64, i64.
 - This instruction casts a temporary copy of dC to the unsigned type that is the same size as dA's type and uses that instead of dC.
13. `add dA, dB.addr, dC`
- This instruction causes an exception if dA or dC is of the following types: u64, i64.
 - For `add.v dA, dB.addr, dC`, this instruction duplicates `cast(dA.type, dB.addr)` (a scalar) into a temporary (128 bytes long) vector of element type `dA.type`.
14. `shl dA, dB.addr, dC`
- This instruction causes an exception if dA or dC is of the following types: u64, i64.
 - For `shl.v dA, dB.addr, dC`, this instruction duplicates `cast(dA.type, dB.addr)` (a scalar) into a temporary (128 bytes long) vector of element type `dA.type`.
 - This instruction casts a temporary copy of dC to the unsigned type that is the same size as dA's type and uses that instead of dC.
15. *Reserved for future expansion.*
16. *Reserved for future expansion.*

4.2 Group 1 Instructions

- Encoding: 0001 aaaa aabb bbbb cccc ccii iiiii iooo
 - a: DLAR a
 - b: DLAR b
 - c: DLAR c
 - i: `simm7` (sign-extended 7-bit immediate)
 - o: Opcode
- For these instructions, the `dB` register's scalar data field (temporarily casted to the `u32` type) and the `dC` register's address field are used.
- Instruction List:
 1. `ldu8 dA, dB, dC, simm7`
 2. `ldi8 dA, dB, dC, simm7`
 3. `ldu16 dA, dB, dC, simm7`
 4. `ldi16 dA, dB, dC, simm7`
 5. `ldu32 dA, dB, dC, simm7`
 6. `ldi32 dA, dB, dC, simm7`
 7. `ldu64 dA, dB, dC, simm7`
 8. `ldi64 dA, dB, dC, simm7`

4.3 Group 2 Instructions

- Encoding: 0010 aaaa aabb bbbb cccc ccii iiii iooo
 - a: DLAR a
 - b: DLAR b
 - c: DLAR c
 - i: `simm7` (sign-extended 7-bit immediate)
 - o: Opcode
- For these instructions, the `dB` register's scalar data field (temporarily casted to the `u32` type) and the `dC` register's address field are used.
- Instruction List:
 1. `stu8 dA, dB, dC, simm7`
 2. `sti8 dA, dB, dC, simm7`
 3. `stu16 dA, dB, dC, simm7`
 4. `sti16 dA, dB, dC, simm7`
 5. `stu32 dA, dB, dC, simm7`
 6. `sti32 dA, dB, dC, simm7`
 7. `stu64 dA, dB, dC, simm7`
 8. `sti64 dA, dB, dC, simm7`

4.4 Group 3 Instructions

- Encoding: 0011 aaaa aabb bbbb 0000 0000 0000 0000
 - a: DLAR a
 - b: DLAR b
 - o: Opcode
- For these instructions, the dB register's scalar data field is used.
- Instruction List:
 1. dpu8 dA, dB
 - This instruction casts (a temporary copy of) the scalar data of dB to the u8 type. The casted scalar data is then stored into every u8 vector element of dA. The type of dA is then changed to u8.
 2. dpi8 dA, dB
 - This instruction casts (a temporary copy of) the scalar data of dB to the i8 type. The casted scalar data is then stored into every i8 vector element of dA. The type of dA is then changed to i8.
 3. dpu16 dA, dB
 - This instruction casts (a temporary copy of) the scalar data of dB to the u16 type. The casted scalar data is then stored into every u16 vector element of dA. The type of dA is then changed to u16.
 4. dpi16 dA, dB
 - This instruction casts (a temporary copy of) the scalar data of dB to the i16 type. The casted scalar data is then stored into every i16 vector element of dA. The type of dA is then changed to i16.
 5. dpu32 dA, dB
 - This instruction casts (a temporary copy of) the scalar data of dB to the u32 type. The casted scalar data is then stored into every u32 vector element of dA. The type of dA is then changed to u32.
 6. dpi32 dA, dB
 - This instruction casts (a temporary copy of) the scalar data of dB to the i32 type. The casted scalar data is then stored into every i32 vector element of dA. The type of dA is then changed to i32.
 7. dpu64 dA, dB
 - This instruction casts (a temporary copy of) the scalar data of dB to the u64 type. The casted scalar data is then stored into every u64 vector element of dA. The type of dA is then changed to u64.
 8. dpi64 dA, dB
 - This instruction casts (a temporary copy of) the scalar data of dB to the i64 type. The casted scalar data is then stored into every i64 vector element of dA. The type of dA is then changed to i64.

4.5 Group 4 Instructions

- Encoding: 0100 aaaa aabb bbbb cccc iiii iiii jjjj
 - a: ILAR a
 - b: ILAR b
 - c: DLAR c (d0 to d15)
 - i: isimm8 (sign-extended 8-bit immediate)
 - j: jimm4 (zero-extended 4-bit immediate), the number of consecutive ILARs past iA to fetch into.
- This instruction uses the address field of iB and the scalar data field (temporarily casted to the u32 type) of the dC register.
- Instruction List:
 1. fetch iA, iB, dC, isimm8, jimm4

4.6 Group 5 Instructions

- Encoding: 0101 aaaa aabb bbbb iiii ij j0v oooo
 - a: DLAR a
 - b: ILAR b
 - i: iimm5 (zero-extended 5-bit immediate i)
 - j: jimm5 (zero-extended 5-bit immediate j)
 - v:
 - * when 0b0: scalar operation (uses the scalar data of dA). The assembly syntax indicating a scalar operation simply adds ".s" to the instruction's name.
 - * when 0b1: vector operation (uses the vector data of dA). The assembly syntax indicating a vector operation simply adds ".v" to the instruction's name.
 - o: Opcode
- These instructions use the scalar or vector data field of dA.
- Instruction List:
 1. sel dA, iB, iimm5, jimm5
 - This instruction jumps to iB[iimm5 << 2] if the particular data field of dA is non-zero, otherwise to the address iB[jimm5 << 2].
 2. jz dA, iB, iimm5
 - This instruction jumps to iB[iimm5 << 2] if the particular data field of dA is zero.
 3. jnz dA, iB, iimm5
 - This instruction jumps to iB[iimm5 << 2] if the particular data field of dA is non-zero.
 4. reti dA
 - This instruction returns from an interrupt if dA is non-zero, setting ie to 0b1.
 - This instruction causes an exception if the processor is in user mode.
 5. retx dA
 - This instruction returns from supervisor mode to user mode if dA is non-zero.
 - This instruction causes an exception if the processor is in user mode.
 6. *Reserved for future expansion.*
 7. *Reserved for future expansion.*
 8. *Reserved for future expansion.*

9. *Reserved for future expansion.*
10. *Reserved for future expansion.*
11. *Reserved for future expansion.*
12. *Reserved for future expansion.*
13. *Reserved for future expansion.*
14. *Reserved for future expansion.*
15. *Reserved for future expansion.*
16. *Reserved for future expansion.*

4.7 Group 6 Instructions

- Encoding: 0110 aaaa aabb bbbb cccc ccii iiiii sooo
 - a: ILAR a or DLAR a
 - b: ILAR b or DLAR b
 - c: DLAR c
 - i: imm6 (zero-extended 6-bit immediate), amount of LAR contents to use
 - s:
 - * when 0b0: Destination LARs (the ones starting with iA or dA) or source LARs (the ones starting with iB or dB) are user mode LARs. An example of the syntax for `getaddr` in this case is `getaddr.u`. The ".u" suffix indicates this instruction will have the s bit set to 0b0.
 - * when 0b1: Destination LARs (the ones starting with iA or dA) or source LARs (the ones starting with iB or dB) are supervisor mode LARs. An example of the syntax for `getaddr` in this case is `getaddr.s`. The ".s" suffix indicates this instruction will have the s bit set to 0b1.
 - o: Opcode
- Instruction List:
 1. `getaddr dA, dB, imm6`
 - This instruction uses the s bit to indicate which mode the source DLARs belong to.
 - This instruction grabs the addresses of source DLARs starting with dB and then also the following `imm6 - 1` source DLARs. The grabbed addresses are then written into consecutive scalar data elements of destination DLARs (starting with dA and continuing into the following destination DLARs as necessary).
 - When supervisor mode LARs are used for the source(s), this instruction causes an exception if used in user mode.
 2. `getaddr dA, iB, imm6`
 - This instruction uses the s bit to indicate which mode the source ILARs belong to.
 - This instruction grabs the addresses of source ILARs starting with dB and then also the following `imm6 - 1` source DLARs. The grabbed addresses are then written into consecutive scalar data elements of destination DLARs (starting with dA and continuing into the following destination DLARs as necessary).
 - When supervisor mode LARs are used for the source(s), this instruction causes an exception if used in user mode.
 3. `gettype dA, dB, imm6`
 - This instruction uses the s bit to indicate which mode the source DLARs belong to.

- This instruction grabs the types of source DLARs starting with `dB` and then also the following `imm6 - 1` source DLARs. The grabbed types are then written into consecutive scalar data elements of destination DLARs (starting with `dA` and continuing into the following destination DLARs as necessary).
 - When supervisor mode LARs are used for the source(s), this instruction causes an exception if used in user mode.
4. `ldm dA, dB, dC, imm6`
- This instruction's name is short for "load multiple".
 - This instruction uses the `s` bit to indicate to which mode the destination DLARs belong.
 - This instruction uses addresses stored in the `imm6` scalar data elements of consecutive DLARs (starting with `dB`) and types stored in the `imm6` scalar data elements of consecutive DLARs (starting with `dC`). Multiple loads from memory are performed into the `imm6` destination DLARs (starting with `dA`).
 - When supervisor mode LARs are used for the destination(s), this instruction causes an exception if used in user mode.
5. `fetchm iA, dB, imm6`
- This instruction's name is short for "fetch multiple".
 - This instruction uses the `s` bit to indicate to which mode the destination DLARs belong.
 - This instruction uses addresses stored in the `imm6` scalar data elements of consecutive DLARs (starting with `dB`). Multiple fetches from memory are performed into the `imm6` destination ILARs (starting with `iA`).
 - When supervisor mode LARs are used for the destination(s), this instruction causes an exception if used in user mode.
6. *Reserved for future expansion.*
7. *Reserved for future expansion.*
8. *Reserved for future expansion.*

4.8 Group 7 Instructions

- Encoding: 0111 aaaa aabb bbbb cccc ccdd dddd oooo
 - a: DLAR a
 - b: DLAR b
 - c: DLAR c
 - d: DLAR d
 - o: Opcode
- Instruction List:
 1. cpy dA, ie
 2. cpy ie, dA
 3. cpy dA, xct
 4. cpy xct, dA
 5. cpy dA, swiarg0
 6. cpy swiarg0, dA
 7. cpy dA, swiarg1
 8. cpy swiarg1, dA
 9. cpy dA, swiarg2
 10. cpy swiarg2, dA
 11. cpy dA, swiarg3
 12. cpy swiarg3, dA
 13. swi dA, dB, dC, dD
 14. *Reserved for future expansion.*
 15. *Reserved for future expansion.*
 16. *Reserved for future expansion.*