Volt32 CPU

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Registers, Main Widths, etc.

- The main width of the processor is 32-bit, and addresses are 32-bit. Some 64-bit operations exist.
- The machine is an implementation of Line Associative Registers (LARs). Both instruction LARs (ILARs) and data LARs (DLARs) are included in the design. There are a grand total of 128 ILARs and 128 DLARs, but they are split between the LARs owned by the supervisor mode and the LARs owned by the user mode. There are 64 supervisor mode ILARs, 64 supervisor mode DLARs, 64 user mode ILARs, and 64 user mode DLARs.
- The machine boots in supervisor mode. The processor jumps to address `0x0` when it enters supervisor mode, which includes when the machine boots.
- ILARs
  - In user mode, ILARs 0 to 63 are referred to as `i0`, `i1`, `i2`, ..., `i61`, `i62`, `ipc`.
  - In supervisor mode, ILARs 64 to 127 are referred to as `i0`, `i1`, `i2`, ..., `i61`, `i62`, `ipc`.
  - The two ILARs called "`i0`" have all their fields set to zero, and when written to, the contents of the ILAR does not change.
  - The two ILARs called "`ipc`" are the program counters for the two operating modes of the processor.
  - An ILAR's data field is 128 bytes long. It is composed of 32-bit instructions aligned to 32 bits.
  - An ILAR's scalar offset field is 5-bit due to instructions being 32-bit and the data field being 128 bytes long.
  - The base address field of an ILAR is (32 - 7 = 25)-bit.
  - An ILAR's tag field is 6-bit.
- DLARs
  - In user mode, DLARs 0 to 63 are referred to as `d0`, `d1`, `d2`, ..., `d61`, `d62`, `d63`.
  - In supervisor mode, DLARs 64 to 127 are referred to as `d0`, `d1`, `d2`, ..., `d61`, `d62`, `d63`.
  - The two DLARs called "`d0`" have all their fields set to zero, and when written to, the contents of the DLAR does not change.
  - A DLAR's data field is 128 bytes long. It is composed of the scalar data elements of the 128 byte vectors, where the type of the scalar data elements is determined by the type tag field of the DLAR.
  - A DLAR's scalar offset field is 7-bit due to the data field being 128 bytes long.

  - The base address field of a DLAR is (32 - 7 = 25)-bit.
  - DLARs can take on the following types (3-bit enum):
    * 8-bit, unsigned (`u8`)
    * 8-bit, signed (`i8`)
    * 16-bit, unsigned (`u16`)
    * 16-bit, signed (`i16`)
    * 32-bit, unsigned (`u32`)
    * 32-bit, signed (`i32`)
    * 64-bit, unsigned (`u64`); only usable for some operations, if not usable gets treated like `u32`
    * 64-bit, signed (`i64`); only usable for some operations, if not usable gets treated like `i32`
  - A DLAR's tag field is 6-bit.

- The `ie` register
  - This register is 1-bit.
  - This register is a flag indicating whether or not an exception can be serviced. It can be written to with the `cpy` (with `ie` as the destination operand) instruction, and it can be read from with the `cpy` (with `ie` as a source operand) instruction.
  - The `reti` instruction sets `ie` to `0b1` and returns from supervisor mode to user mode.

Exceptions

Some instructions may cause an exception to occur, putting the processor in supervisor mode.

The following exceptions may occur during normal execution of a program.

- Taking an interrupt, which also sets `ie` to `0b0`.
- Division by zero.
- `swi`.
  - Note that this instruction always causes an exception to occur.
- `reti` in user mode.
- `cpy` that writes to `ie` when in user mode.
- Instructions that read from/write to supervisor mode ILARs or DLARs when in user mode.