

# Volt32 CPU

Andrew Clark

June 20, 2022

## Table of Contents

<b>Table of Contents</b>	<b>1</b>
<b>Registers, Main Widths, etc.</b>	<b>2</b>
<b>Exceptions</b>	<b>5</b>
<b>Instructions</b>	<b>6</b>
4.1 Group 0 Instructions . . . . .	6
4.2 Group 1 Instructions . . . . .	8
4.3 Group 2 Instructions . . . . .	10
4.4 Group 3 Instructions . . . . .	11
4.5 Group 4 Instructions . . . . .	12
4.6 Group 5 Instructions . . . . .	13
4.7 Group 6 Instructions . . . . .	14
4.8 Group 7 Instructions . . . . .	16
4.9 Group 8 Instructions . . . . .	18
4.10 Group 9 Instructions . . . . .	19
4.11 Group 10 Instructions . . . . .	22

## Registers, Main Widths, etc.

- The main width of the processor is 32-bit, and addresses are 32-bit. Some 64-bit operations exist.
- The machine is an implementation of Line Associative Registers (LARs). Both instruction LARs (ILARs) and data LARs (DLARs) are included in the design. There are a grand total of 128 ILARs and 128 DLARs, but they are split between the LARs owned by the supervisor mode and the LARs owned by the user mode. There are 64 supervisor mode ILARs, 64 supervisor mode DLARs, 64 user mode ILARs, and 64 user mode DLARs.
- The machine boots in supervisor mode. The processor jumps to address `0x0` when it enters supervisor mode, which includes when the machine boots.
- ILARs
  - In user mode, ILARs 0 to 63 are referred to as `i0`, `i1`, `i2`, ..., `i61`, `i62`, `ipc`.
  - In supervisor mode, ILARs 64 to 127 are referred to as `i0`, `i1`, `i2`, ..., `i61`, `i62`, `ipc`.
  - The two ILARs called "`i0`" have all their fields set to zero, and when written to, the contents of the ILAR does not change.
  - The two ILARs called "`ipc`" are the program counters for the two operating modes of the processor. The location within the `ipc` ILARs can be computed by taking the low 6 bits (6 because 128 bytes long ILARs) of their addresses.
  - An ILAR's data field is 128 bytes long. It is composed of 32-bit instructions aligned to 32 bits.
  - An ILAR's scalar offset field is  $(7 - 2 = 5)$ -bit due to instructions being 32-bit and the data field being 128 bytes long.
  - The base address field of an ILAR is  $(32 - 6 = 26)$ -bit.
  - An ILAR's tag field is 7-bit because there are 128 total ILARs.
- DLARs
  - In user mode, DLARs 0 to 63 are referred to as `d0`, `d1`, `d2`, ..., `d59`, `d60`, `dcp`, `dfp`, `dsp`.
  - In supervisor mode, DLARs 64 to 127 are referred to as `d0`, `d1`, `d2`, ..., `d59`, `d60`, `dcp`, `dfp`, `dsp`.
  - The two DLARs called "`d0`" have all their fields set to zero, and when written to, the contents of the DLAR does not change.
  - A DLAR's data field is 128 bytes long. It is composed of the scalar data elements of the 128 byte vectors, where the type of the scalar data elements is determined by the type tag field of the DLAR.

- A DLAR's scalar offset field is 7-bit due to the data field being 128 bytes long.
  - The base address field of a DLAR is  $(32 - 6 = 26)$ -bit.
  - DLARs can take on the following types (3-bit enum):
    - \* 8-bit, unsigned (`u8`)
    - \* 8-bit, signed (`s8`)
    - \* 16-bit, unsigned (`u16`)
    - \* 16-bit, signed (`s16`)
    - \* 32-bit, unsigned (`u32`)
    - \* 32-bit, signed (`s32`)
    - \* 64-bit, unsigned (`u64`); only usable for some operations
    - \* 64-bit, signed (`s64`); only usable for some operations
  - A DLAR's tag field is 7-bit because there are 128 total DLARs.
  - Similarly, a DLAR's reference count field is 7-bit because there are 128 total DLARs.
  - A DLAR's dirty field is 1-bit.
- The `ie` register
    - "ie" is short for "interrupt enable".
    - This register is 1-bit.
    - This register is a flag indicating whether or not an interrupt can be serviced. It can be read from/written to using `cpy` instructions.
    - The `reti` instruction sets `ie` to `0b1` and returns to user mode from supervisor mode.
  - The `xct` register
    - "exception type"
    - This register is 32-bit.
    - This register is set to the numerical value of an exception's type upon the machine entering supervisor mode. It can be read from/written to using `cpy` instructions.
  - The `swiarg0` register
    - This register is 32-bit.
    - This register indicates argument 0 to `swi`. It can be read from/written to with `cpy` instructions.
  - The `swiarg1` register
    - This register is 32-bit.

- This register indicates argument 1 to `swi`. It can be read from/written to with `cpy` instructions.
- The `swiarg2` register
  - This register is 32-bit.
  - This register indicates argument 2 to `swi`. It can be read from/written to with `cpy` instructions.
- The `swiarg3` register
  - This register is 32-bit.
  - This register indicates argument 3 to `swi`. It can be read from/written to with `cpy` instructions.

## Exceptions

Some instructions may cause an exception to occur, putting the processor in supervisor mode.

The following exceptions may occur during normal execution of a program. `xct` is set to a numerical value representing these upon the processor encountering an exception.

- When `xct == 0x0`: Taking a non-software interrupt (which would also set `ie` to `0b0`).
- When `xct == 0x1`: Division by zero.
- When `xct == 0x2`: Undefined instruction.
- When `xct == 0x3`: Instructions where 64-bit ops are not defined.
- When `xct == 0x4`: `swi`.
- When `xct == 0x5`: `reti` when in user mode.
- When `xct == 0x6`: `retx` when in user mode.
- When `xct == 0x7`: `cpy` that reads from `ie` in user mode.
- When `xct == 0x8`: `cpy` that writes to `ie` in user mode.
- When `xct == 0x9`: `cpy` that reads from `xct` in user mode.
- When `xct == 0xa`: `cpy` that writes to `xct` in user mode.
- When `xct == 0xb`: Instructions that read from supervisor mode ILARs or DLARs when in user mode.
- When `xct == 0xc`: Instructions that write to supervisor mode ILARs or DLARs when in user mode.

## Instructions

### 4.1 Group 0 Instructions

- Encoding: 0000 aaaa aabb bbbb cccc cdd dddv oooo
  - a: DLAR a
  - b: DLAR b
  - c: DLAR c
  - d: DLAR d (d0 to d31)
  - v:
    - \* when 0b0: scalar operation. The assembly syntax indicating a scalar operation simply adds ".s" to the instruction's name.
    - \* when 0b1: vector operation. The assembly syntax indicating a vector operation simply adds ".v" to the instruction's name.
  - o: Opcode
- Instruction List:
  1. add dA, dB, dC
  2. sub dA, dB, dC
  3. slt dA, dB, dC
  4. mul dA, dB, dC
    - This instruction causes an exception if dB or dC is of the following types: u64, s64.
  5. div dA, dB, dC, dD
    - This instruction causes an exception if dB, dC, or dD is of the following types: u64, s64.
    - This instruction writes the quotient into dA, and the remainder into dD.
  6. and dA, dB, dC
  7. or dA, dB, dC
  8. xor dA, dB, dC
  9. shl dA, dB, dC
    - Logical shift left.
    - This instruction causes an exception if dA, dB, or dC is of the following types: u64, s64.
    - This instruction casts a temporary copy of dC to the unsigned type that is the same size as dA's type and uses that instead of dC.
  10. shr dA, dB, dC
    - Logical shift right if dA is unsigned, or arithmetic shift right if dA is signed.

- This instruction causes an exception if `dA`, `dB`, or `dC` is of the following types: `u64`, `s64`.
  - This instruction casts a temporary copy of `dC` to the unsigned type that is the same size as `dA`'s type and uses that instead of `dC`.
11. `rol dA, dB, dC`
- Rotate left.
  - This instruction causes an exception if `dA`, `dB`, or `dC` is of the following types: `u64`, `s64`.
  - This instruction casts a temporary copy of `dC` to the unsigned type that is the same size as `dA`'s type and uses that instead of `dC`.
12. `ror dA, dB, dC`
- Rotate right.
  - This instruction causes an exception if `dA`, `dB`, or `dC` is of the following types: `u64`, `s64`.
  - This instruction casts a temporary copy of `dC` to the unsigned type that is the same size as `dA`'s type and uses that instead of `dC`.
13. `add dA, dB.addr, dC`
- This instruction causes an exception if `dA` or `dC` is of the following types: `u64`, `s64`.
  - For `add.v dA, dB.addr, dC`, this instruction duplicates the value of `cast(dA.type, dB.addr)` (a scalar) into a temporary (64 bytes long) vector of element type `dA.type`.
14. `shl dA, dB.addr, dC`
- This instruction causes an exception if `dA` or `dC` is of the following types: `u64`, `s64`.
  - For `shl.v dA, dB.addr, dC`, this instruction duplicates `cast(dA.type, dB.addr)` (a scalar) into a temporary (64 bytes long) vector of element type `dA.type`.
  - This instruction casts a temporary copy of `dC` to the unsigned type that is the same size as `dA`'s type and uses that instead of `dC`.
15. *Reserved for future expansion.*
16. *Reserved for future expansion.*



## 4.2 Group 1 Instructions

- Encoding: 0001 aaaa aabb bbbb 0000 0000 0000 0000
  - a: DLAR a
  - b: DLAR b
  - o: Opcode
- Instruction List:
  1. `add.r dA, dB`
    - This instruction casts a temporary copy of `dB` to the `dA`'s type and performs a sum of all the scalar data elements of the temporary copy of `dB`, then stores the result in `dA`'s scalar data.
    - This instruction causes an exception if `dA` is of the following types: `u64, s64`.
  2. `mul.r dA, dB`
    - This instruction casts a temporary copy of `dB` to the `dA`'s type and performs a product of all the scalar data elements of the temporary copy of `dB`, then stores the result in `dA`'s scalar data.
    - This instruction causes an exception if `dA` is of the following types: `u64, s64`.
  3. `max.r dA, dB`
    - This instruction casts a temporary copy of `dB` to the `dA`'s type and finds the scalar data element of the temporary copy of `dB` that is the maximum, then stores the result in `dA`'s scalar data.
    - This instruction causes an exception if `dA` is of the following types: `u64, s64`.
  4. `min.r dA, dB`
    - This instruction casts a temporary copy of `dB` to the `dA`'s type and finds the scalar data element of the temporary copy of `dB` that is the minimum, then stores the result in `dA`'s scalar data.
    - This instruction causes an exception if `dA` is of the following types: `u64, s64`.
  5. `and.r dA, dB`
    - This instruction casts a temporary copy of `dB` to the `dA`'s type and performs a bitwise AND reduction of all the scalar data elements of the temporary copy of `dB`, then stores the result in `dA`'s scalar data.
    - This instruction causes an exception if `dA` is of the following types: `u64, s64`.
  6. `or.r dA, dB`

- This instruction casts a temporary copy of `dB` to the `dA`'s type and performs a bitwise OR reduction of all the scalar data elements of the temporary copy of `dB`, then stores the result in `dA`'s scalar data.
- This instruction causes an exception if `dA` is of the following types: `u64`, `s64`.

7. `xor.r dA, dB`

- This instruction casts a temporary copy of `dB` to the `dA`'s type and performs a bitwise XOR reduction of all the scalar data elements of the temporary copy of `dB`, then stores the result in `dA`'s scalar data.
- This instruction causes an exception if `dA` is of the following types: `u64`, `s64`.

8. *Reserved for future expansion.*

9. *Reserved for future expansion.*

10. *Reserved for future expansion.*

11. *Reserved for future expansion.*

12. *Reserved for future expansion.*

13. *Reserved for future expansion.*

14. *Reserved for future expansion.*

15. *Reserved for future expansion.*

16. *Reserved for future expansion.*

### 4.3 Group 2 Instructions

- Encoding: 0010 aaaa aabb bbbb cccc ccii iiii iooo
  - a: DLAR a
  - b: DLAR b
  - c: DLAR c
  - i: `simm7` (sign-extended 7-bit immediate)
  - o: Opcode
- For these instructions, the `dB` register's scalar data field (temporarily casted to the `u32` type) and the `dC` register's address field are used.
- Also, the type that a DLAR is set to is indicated in the instruction name, with, for example, `ldu8` setting `dA`'s type to `u8`.
- Instruction List:
  1. `ldu8 dA, dB, dC, simm7`
  2. `lds8 dA, dB, dC, simm7`
  3. `ldu16 dA, dB, dC, simm7`
  4. `lds16 dA, dB, dC, simm7`
  5. `ldu32 dA, dB, dC, simm7`
  6. `lds32 dA, dB, dC, simm7`
  7. `ldu64 dA, dB, dC, simm7`
  8. `lds64 dA, dB, dC, simm7`

## 4.4 Group 3 Instructions

- Encoding: 0011 aaaa aabb bbbb cccc ccii iiii iooo
  - a: DLAR a
  - b: DLAR b
  - c: DLAR c
  - i: `simm7` (sign-extended 7-bit immediate)
  - o: Opcode
- For these instructions, the `dB` register's scalar data field (temporarily casted to the `u32` type) and the `dC` register's address field are used.
- Also, the type that a DLAR is set to is indicated in the instruction name, with, for example, `stu8` setting `dA`'s type to `u8`.
- Instruction List:
  1. `stu8 dA, dB, dC, simm7`
  2. `sts8 dA, dB, dC, simm7`
  3. `stu16 dA, dB, dC, simm7`
  4. `sts16 dA, dB, dC, simm7`
  5. `stu32 dA, dB, dC, simm7`
  6. `sts32 dA, dB, dC, simm7`
  7. `stu64 dA, dB, dC, simm7`
  8. `sts64 dA, dB, dC, simm7`

## 4.5 Group 4 Instructions

- Encoding: 0100 aaaa aabb bbbb 0000 0000 0000 0000
  - a: DLAR a
  - b: DLAR b
  - o: Opcode
- For these instructions, the dB register's scalar data field is used.
- Instruction List:
  1. dpu8 dA, dB
    - This instruction casts (a temporary copy of) the scalar data of dB to the u8 type. The casted scalar data is then stored into every u8 vector element of dA. The type of dA is then changed to u8.
  2. dps8 dA, dB
    - This instruction casts (a temporary copy of) the scalar data of dB to the s8 type. The casted scalar data is then stored into every s8 vector element of dA. The type of dA is then changed to s8.
  3. dpu16 dA, dB
    - This instruction casts (a temporary copy of) the scalar data of dB to the u16 type. The casted scalar data is then stored into every u16 vector element of dA. The type of dA is then changed to u16.
  4. dps16 dA, dB
    - This instruction casts (a temporary copy of) the scalar data of dB to the s16 type. The casted scalar data is then stored into every s16 vector element of dA. The type of dA is then changed to s16.
  5. dpu32 dA, dB
    - This instruction casts (a temporary copy of) the scalar data of dB to the u32 type. The casted scalar data is then stored into every u32 vector element of dA. The type of dA is then changed to u32.
  6. dps32 dA, dB
    - This instruction casts (a temporary copy of) the scalar data of dB to the s32 type. The casted scalar data is then stored into every s32 vector element of dA. The type of dA is then changed to s32.
  7. dpu64 dA, dB
    - This instruction casts (a temporary copy of) the scalar data of dB to the u64 type. The casted scalar data is then stored into every u64 vector element of dA. The type of dA is then changed to u64.
  8. dps64 dA, dB
    - This instruction casts (a temporary copy of) the scalar data of dB to the s64 type. The casted scalar data is then stored into every s64 vector element of dA. The type of dA is then changed to s64.

## 4.6 Group 5 Instructions

- Encoding: 0101 aaaa aabb bbbb cccc ccii iiii jjjj
  - a: ILAR a
  - b: ILAR b
  - c: DLAR c
  - i: `isimm6` (sign-extended 6-bit immediate)
  - j: `jimm4` (zero-extended 4-bit immediate), the number of consecutive ILARs past `iA` to `fetch` into.
- This instruction uses the address field of `iB` and the scalar data field (temporarily casted to the `u32` type) of the `dC` DLAR.
- Also, the address to `fetch` from is computed by adding these two temporary values to a temporary value equivalent to the sign extended value of `isimm6`.
- Instruction List:
  1. `fetch iA, iB, dC, isimm6, jimm4`

## 4.7 Group 6 Instructions

- Encoding: 0110 aaaa aabb bbbb 0iii iijj jjjv oooo
  - a: DLAR a
  - b: ILAR b
  - i: iimm5 (zero-extended 5-bit immediate i)
  - j: jimm5 (zero-extended 5-bit immediate j)
  - v:
    - \* when 0b0: scalar operation (uses the scalar data of dA). The assembly syntax indicating a scalar operation simply adds ".s" to the instruction's name.
    - \* when 0b1: vector operation (uses the vector data of dA). The assembly syntax indicating a vector operation simply adds ".v" to the instruction's name.
  - o: Opcode
- These instructions use the scalar or vector data field of dA.
- Instruction List:
  1. sel dA, iB, iimm5, jimm5
    - This instruction jumps to iB[iimm5 << 2] if the particular data field of dA is non-zero, otherwise to the address iB[jimm5 << 2].
  2. jz dA, iB, iimm5
    - This instruction jumps to iB[iimm5 << 2] if the particular data field of dA is zero.
  3. jnz dA, iB, iimm5
    - This instruction jumps to iB[iimm5 << 2] if the particular data field of dA is non-zero.
  4. reti dA
    - This instruction returns from an interrupt if dA is non-zero, setting ie to 0b1.
    - This instruction causes an exception if the processor is in user mode.
  5. retx dA
    - This instruction returns from supervisor mode to user mode if dA is non-zero.
    - This instruction causes an exception if the processor is in user mode.
  6. *Reserved for future expansion.*
  7. *Reserved for future expansion.*
  8. *Reserved for future expansion.*

9. *Reserved for future expansion.*
10. *Reserved for future expansion.*
11. *Reserved for future expansion.*
12. *Reserved for future expansion.*
13. *Reserved for future expansion.*
14. *Reserved for future expansion.*
15. *Reserved for future expansion.*
16. *Reserved for future expansion.*



## 4.8 Group 7 Instructions

- Encoding: 0111 aaaa aabb bbbb cccc ccii iiii Sooo
  - a: ILAR a or DLAR a
  - b: ILAR b or DLAR b
  - c: DLAR c
  - i: imm6 (zero-extended 6-bit immediate), amount of LAR contents to use
  - S:
    - \* when 0b0: Destination LARs (the ones starting with iA or dA) or source LARs (the ones starting with iB or dB) are user mode LARs. An example of the syntax for `getaddrs` in this case is `getaddrs.U`. The ".U" suffix indicates this instruction will have the S bit set to 0b0.
    - \* when 0b1: Destination LARs (the ones starting with iA or dA) or source LARs (the ones starting with iB or dB) are supervisor mode LARs. An example of the syntax for `getaddrs` in this case is `getaddrs.S`. The ".S" suffix indicates this instruction will have the S bit set to 0b1.
  - o: Opcode
- Instruction List:
  1. `getaddrs dA, dB, imm6`
    - This instruction uses the S bit to indicate which mode the source DLARs belong to.
    - This instruction grabs the addresses of source DLARs starting with dB and then also the following `imm6 - 1` source DLARs. The grabbed addresses are then written into consecutive scalar data elements of destination DLARs (starting with dA and continuing into the following destination DLARs as necessary).
    - When supervisor mode LARs are used for the source(s), this instruction causes an exception if used in user mode.
  2. `getaddrs dA, iB, imm6`
    - This instruction uses the S bit to indicate which mode the source ILARs belong to.
    - This instruction grabs the addresses of source ILARs starting with dB and then also the following `imm6 - 1` source DLARs. The grabbed addresses are then written into consecutive scalar data elements of destination DLARs (starting with dA and continuing into the following destination DLARs as necessary).
    - When supervisor mode LARs are used for the source(s), this instruction causes an exception if used in user mode.
  3. `gettypes dA, dB, imm6`
    - This instruction uses the S bit to indicate which mode the source DLARs belong to.

- This instruction grabs the types of source DLARs starting with `dB` and then also the following `imm6 - 1` source DLARs. The grabbed types are then written into consecutive scalar data elements of destination DLARs (starting with `dA` and continuing into the following destination DLARs as necessary).
  - When supervisor mode LARs are used for the source(s), this instruction causes an exception if used in user mode.
4. `ldm dA, dB, dC, imm6`
- This instruction's name is short for "load multiple".
  - This instruction uses the `S` bit to indicate to which mode the destination DLARs belong.
  - This instruction uses addresses stored in the `imm6` scalar data elements of consecutive DLARs (starting with `dB`) and types stored in the `imm6` scalar data elements of consecutive DLARs (starting with `dC`). Multiple loads from memory are performed into the `imm6` destination DLARs (starting with `dA`).
  - When supervisor mode LARs are used for the destination(s), this instruction causes an exception if used in user mode.
5. `fetchm iA, dB, imm6`
- This instruction's name is short for "fetch multiple".
  - This instruction uses the `S` bit to indicate to which mode the destination DLARs belong.
  - This instruction uses addresses stored in the `imm6` scalar data elements of consecutive DLARs (starting with `dB`). Multiple fetches from memory are performed into the `imm6` destination ILARs (starting with `iA`).
  - When supervisor mode LARs are used for the destination(s), this instruction causes an exception if used in user mode.
6. *Reserved for future expansion.*
7. *Reserved for future expansion.*
8. *Reserved for future expansion.*

## 4.9 Group 8 Instructions

- Encoding: 1000 aaaa aabb bbbb cccc ccdd dddd oooo
  - a: DLAR a
  - b: DLAR b
  - c: DLAR c
  - d: DLAR d
  - o: Opcode
- Instruction List:
  1. cpy dA, ie
  2. cpy ie, dA
  3. cpy dA, xct
  4. cpy xct, dA
  5. cpy dA, swiarg0
  6. cpy swiarg0, dA
  7. cpy dA, swiarg1
  8. cpy swiarg1, dA
  9. cpy dA, swiarg2
  10. cpy swiarg2, dA
  11. cpy dA, swiarg3
  12. cpy swiarg3, dA
  13. swi dA, dB, dC, dD
    - Note that this instruction always causes an exception to occur.
  14. *Reserved for future expansion.*
  15. *Reserved for future expansion.*
  16. *Reserved for future expansion.*

## 4.10 Group 9 Instructions

- Encoding: 1001 aaaa aabb bbbb cccc cc00 000v oooo
  - a: DLAR a
  - b: DLAR b
  - c: DLAR c
  - v:
    - \* when 0b0: scalar operation. The assembly syntax indicating a scalar operation simply adds ".s" to the instruction's name.
    - \* when 0b1: vector operation. The assembly syntax indicating a vector operation simply adds ".v" to the instruction's name.
  - o: Opcode
- These instructions perform a read from/write to the IO address calculated by adding the scalar data of dB and dC, or (in other words)  $dB + dC$ . The types of dB and dC are temporarily casted to u32 for this calculation.
- When a scalar operation is being performed, only the scalar data of dA is read into from/written out to IO space.
- When a vector operation is being performed, the entire vector data of dA is read into from/written out to IO space.
- Instruction List:
  1. `inu8 dA, dB, dC`
    - This instruction sets the type of dA to u8 before performing anything else of the operation.
    - This instruction reads from IO space and writes to dA.
  2. `ins8 dA, dB, dC`
    - This instruction sets the type of dA to s8 before performing anything else of the operation.
    - This instruction reads from IO space and writes to dA.
  3. `inu16 dA, dB, dC`
    - This instruction sets the type of dA to u16 before performing anything else of the operation.
    - This instruction reads from IO space and writes to dA.
  4. `ins16 dA, dB, dC`
    - This instruction sets the type of dA to s16 before performing anything else of the operation.
    - This instruction reads from IO space and writes to dA.
  5. `inu32 dA, dB, dC`

- This instruction sets the type of dA to u32 before performing anything else of the operation.
  - This instruction reads from IO space and writes to dA.
6. `ins32 dA, dB, dC`
- This instruction sets the type of dA to s32 before performing anything else of the operation.
  - This instruction reads from IO space and writes to dA.
7. `inu64 dA, dB, dC`
- This instruction sets the type of dA to u64 before performing anything else of the operation.
  - This instruction reads from IO space and writes to dA.
8. `ins64 dA, dB, dC`
- This instruction sets the type of dA to s64 before performing anything else of the operation.
  - This instruction reads from IO space and writes to dA.
9. `outu8 dA, dB, dC`
- This instruction sets the type of dA to u8 before performing anything else of the operation.
  - This instruction writes to IO space and reads from dA.
10. `outs8 dA, dB, dC`
- This instruction sets the type of dA to s8 before performing anything else of the operation.
  - This instruction writes to IO space and reads from dA.
11. `outu16 dA, dB, dC`
- This instruction sets the type of dA to u16 before performing anything else of the operation.
  - This instruction writes to IO space and reads from dA.
12. `outs16 dA, dB, dC`
- This instruction sets the type of dA to s16 before performing anything else of the operation.
  - This instruction writes to IO space and reads from dA.
13. `outu32 dA, dB, dC`
- This instruction sets the type of dA to u32 before performing anything else of the operation.
  - This instruction writes to IO space and reads from dA.
14. `outs32 dA, dB, dC`
- This instruction sets the type of dA to s32 before performing anything else of the operation.

- This instruction writes to IO space and reads from dA.
15. `outu64 dA, dB, dC`
- This instruction sets the type of dA to `u64` before performing anything else of the operation.
  - This instruction writes to IO space and reads from dA.
16. `outs64 dA, dB, dC`
- This instruction sets the type of dA to `s64` before performing anything else of the operation.
  - This instruction writes to IO space and reads from dA.

## 4.11 Group 10 Instructions

- Encoding: 1010 aaaa aabb bbbbbb iiii iiii iiii iiii
  - a: DLAR a
  - b: DLAR b
  - i: `simm16` (sign-extended 16-bit immediate)
- Instruction List:
  1. `add.s dA, dB, ipc.addr, simm16`
    - Note: this is a scalar operation.