Volt32 CPU

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March 7, 2021

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Registers, Main Widths, etc.

1. The main width of the processor is 32-bit. Addresses are 32-bit, and some operations forcibly treat the operands as 32-bit.

2. The machine is an implementation of Line Associative Registers (LARs). Both instruction LARs (ILARs) and data LARs (DLARs) are included in the design. There are a grand total of 128 ILARs and 128 DLARs, but they are split between the LARs owned by the supervisor mode and the LARs owned by the user mode. There are 64 supervisor mode ILARs and 64 supervisor mode DLARs, and there are 64 user mode ILARs and 64 user mode DLARs.

3.