# AN 22.3
# USB334x USB Transceiver Layout Guidelines

## 1 Introduction

The USB334x provides the physical layer interface (PHY) in systems using Hi-Speed USB 2.0. Proper design techniques must be used in the printed circuit board (PCB) layout to maintain the signal integrity required for 480 Mbps operation. The USB334x is available in both 24-pin and 32-pin QFN packages; layout guidelines for general QFN packages are provided in this application note.

### 1.1 Audience

This document is written for a reader that is familiar with hardware design and the USB 2.0 specification. The goal of this application note is to provide guidance on sensitive areas of the PCB layout.

### 1.2 Overview

The following recommendations are for a four layer PCB layout with an SMSC part. Our recommendations are not the only way to layout our 24-pin and 32-pin QFN packages. PCB design engineers will have his/her own preference, and the implementation will be dependent on complexity and density of layout, PCB real estate, number and types of devices in circuit and the environment that the final product will reside in. For example, the PCB described in this application note has components on both sides of the board. A four layer board could be realized with components on one side only.

### 1.3 References

The following documents should be referenced when using this application note:

- SMSC USB334x Datasheets
- Universal Serial Bus Specification Revision 2.0

## 2 General Design Guidelines

This chapter provides guidelines for the sensitive circuits associated with the system application of the USB334x.

### 2.1 ULPI Bus

The layout of the ULPI interface should be analyzed with the timing requirements of the USB Link controller to ensure that the proper timing is met. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system. For more information on ULPI timing and system design, refer to the SMSC Application Note 19.17 - “ULPI Design Guide”.

## 2.2 Controlled Impedance for USB Traces

The USB 2.0 specification requires that the USB DP/DM traces maintain a nominal 90 Ohms differential impedance +/- 15% (see USB specification Rev 2.0, paragraph 7.1.1.3 for more details). In this design example, the traces are 7 mil (0.178mm) wide with line spacing of 7 mils (0.178mm). These numbers are derived for 5 mil (0.127mm) distance from ground reference plane. For different dielectric thickness, copper weight or board stack-up, trace width and spacing will need to be recalculated. A continuous ground plane is required directly beneath the DP/DM traces and extending at least 5 times the spacing width to either side of DP/DM lines.

Maintain symmetry between DP/DM lines in regards to shape and length.

Single ended impedance is not as critical as the differential impedance. A range of 42 Ohms to 78 Ohms is acceptable (equivalently, common mode impedance must be between 21 Ohms and 39 Ohms).

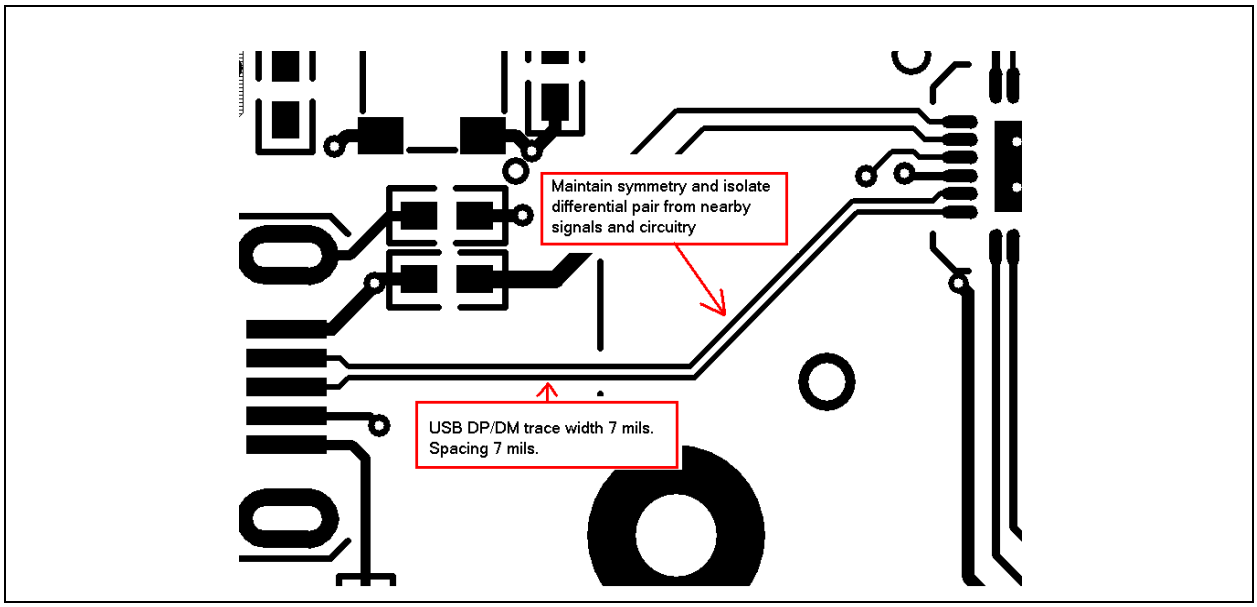


**Figure 2.1 Example of Routing DP/DM from QFN Pkg to Type B Connector**

Figure 2.1 shows DP/DM traces with approximately equal trace length and symmetry. It is important to maintain a conductor width and spacing that provides differential and common mode impedances compliant with the USB specification. Use 45 degree turns to minimize impedance discontinuities.

## 2.3 Isolation of DP/DM Traces

The DP/DM traces must be isolated from nearby circuitry and signals. Maintain a distance of components to lines that is greater than or equal to 5 times the distance of the 7 mil (0.178mm) spacing between the traces. For example, if DP/DM have a 5 mil (0.127mm) gap between them, it is recommended that no other traces be routed within 25mils (0.635mm) of each trace.

Whenever possible, it is best to avoid:

- Routing differential pairs under components.
- Routing DP/DM lines over the top of other PCB traces on adjacent layers.

For more information on USB 2.0 High Speed system design, refer to the SMSC Application Note 20.2 -“Optimizing USB 2.0 High Speed Physical Layer Design”.

## 2.4 Isolated Shielding on the USB Connector

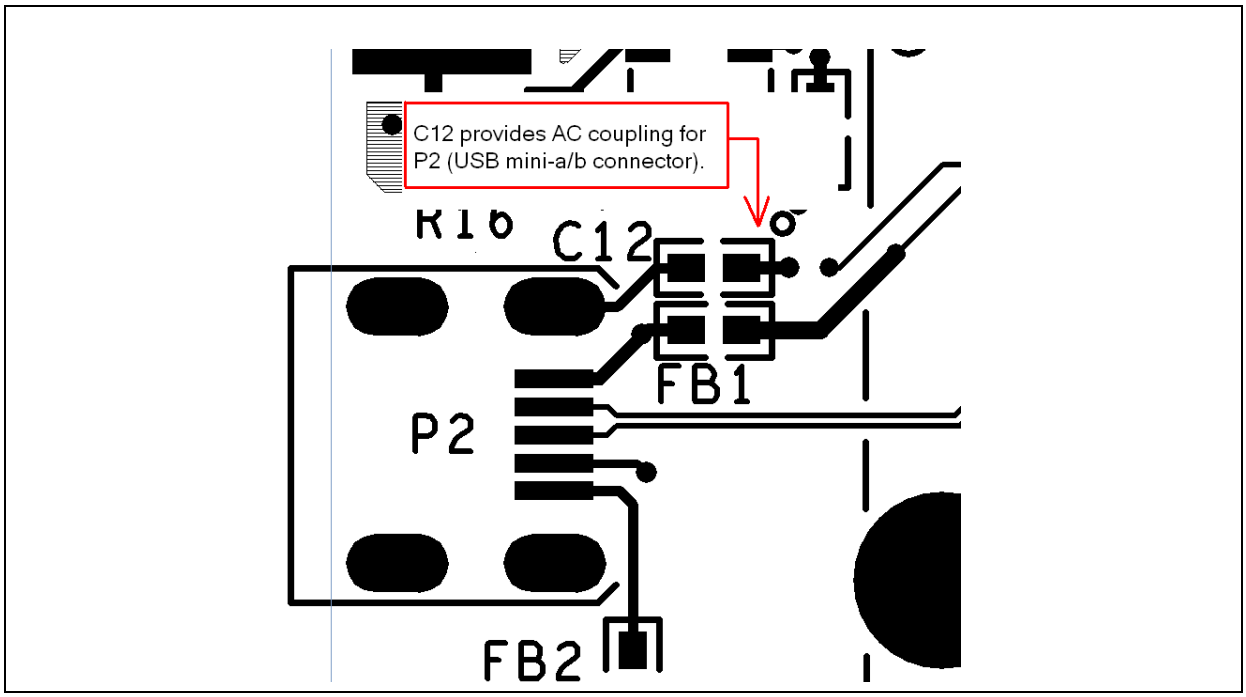


**Figure 2.2 Connections to Shield of USB Connector**

The USB334x fully supports USB On-the-Go (OTG). Figure 2.2 shows the Mini-AB connector housing is DC isolated but AC coupled to the device ground. Industry convention is to ground only the host side of the cable shield. This is done to provide cable shielding while preventing possible ground currents from flowing in the USB cable if there happens to be a potential difference between the host and device grounds. If DC grounding is required replace C12 with a zero Ohm resistor.

In OTG applications the shield may be DC grounded at both ends of the cable.

## 2.5 SPK_L and SPK_R

In USB audio mode, internal analog switches connect the DP pin to the SPK_R pin and the DM pin to the SPK_L pin. The system will then accommodate stereo/mono audio signaling over the USB cable. The internal analog switches can also be used to mux other USB traffic to the USB connector. Rules applied to DP/DM should also be applied to SPK_L and SPK_R traces. Refer to Section 2.3, "Isolation of DP/DM Traces".

Because the SPK_L and SPK_R pins can be used to carry audio signals to the user's audio components, the traces to these pins should follow the layout guidelines illustrated below to prevent noise from nearby circuitry and other signals.

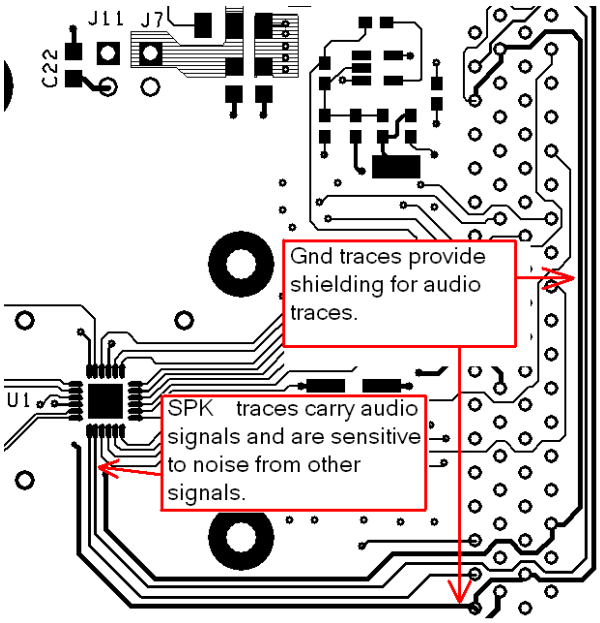


**Figure 2.3 Example of Routing SPK Traces from QFN Package**

## 2.6 RBIAS

The RBIAS resistor sets an internal current source reference. Thus, the RBIAS pin is a high impedance node and any noise induced on the RBIAS traces will directly impact internal current references and degrade eye-diagram quality. The RBIAS resistor should be placed close to the RBIAS pin and the ground return should be short and direct to VSS. Traces for the resistor should be very short and isolated from nearby traces if possible.

## 2.7 Power Supply Bypass Capacitors

Bypass capacitors should be placed close to respective supply pins of the USB334x for optimum power supply decoupling, and connected with short, wide traces. In Figure 2.4, the top (dark) and bottom (red) circuit layers show bypass cap placement with respect to the USB334x's GND pin. The USB334x evaluation board has bypassing directly under part, with return current paths tied to internal ground plane. Refer to datasheet for bypass cap values and ESR requirements.

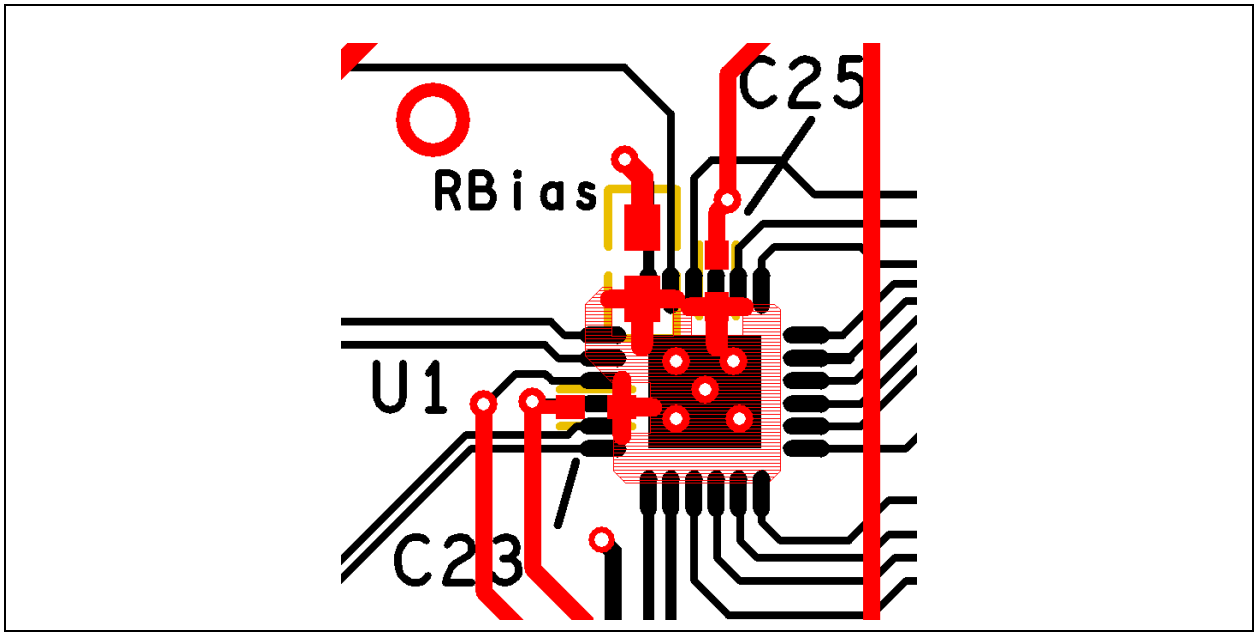


**Figure 2.4 C25 and C23 are the Decoupling for Supply Pins for QFN Pkg.**

## 2.8 VIAS in Ground Flag

The die pad (flag) in the QFN package is 98 mils (2.49mm) square. An 8 mil (0.203mm) drilled via in a pattern of 2-1-2 has been provided adequate grounding for the USB334x. Ideally these vias would be plugged so that no solder will flow through which would result in less than ideal solder connection to flag.

## 2.9 Crystal Placement and Routing

In addition to the general guidelines for the USB334x family of USB transceivers, the USB3340 and USB3343 require some additional guidelines for the crystal placement and routing.

- The crystal should be placed as close as possible to the USB334x.
- The lengths of signals XO and XI should be kept as short as possible (<1in (2.54cm), if possible).
- Capacitors on XI and XO should be placed as close as possible to the crystal. (For applications using a ceramic resonator, capacitors are not required.)

# 3 Application Note Revision History

**Table 3.1 Customer Revision History**

| REVISION LEVEL & DATE | SECTION/FIGURE/ENTRY | CORRECTION |
|---|---|---|
| Rev. 1.0 (11-26-12) | Document co-branded: Microchip logo added; modification to legal disclaimer | |
| Rev. 1.0 (12-13-10) | Initial Document | |