MachXO2 sysIO Usage Guide

February 2012 **Technical Note TN1202**

Introduction

The MachXO2™ PLD family sysIO™ buffers are designed to meet the needs of flexible I/O standards in today's fast-paced design world. The supported I/O standards range from single-ended I/O standards to differential I/O standards so that users can easily interface their designs to standard buses, memory devices, video applications and emerging standards. This technical note provides a description of the supported I/O standards and the banking scheme for the MachXO2 PLD family. The sysIO architecture and the software usage are also discussed to provide a better understanding of the I/O functionality and placement rules.

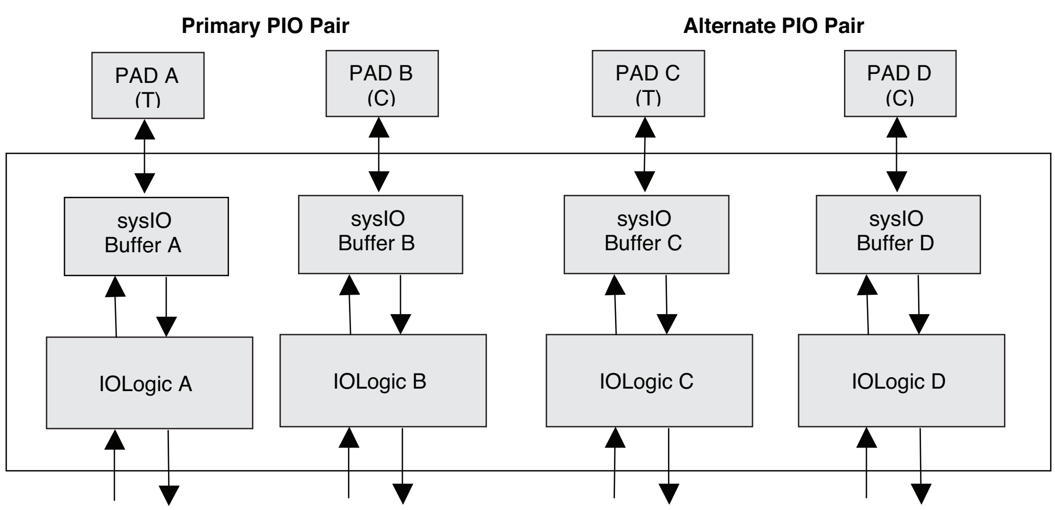
sysIO Buffer Overview

The basic building block of the MachXO2 sysIO is the Programmable I/O Cell (PIC) block. There are four types of PIC blocks in the MachXO2 device architecture. These include the basic PIC block, the memory PIC block for DDR memory support, the receiving PIC block with gearing, and the transmitting PIC block with gearing. The PIC blocks with gearing are used for video and high-speed applications. The PIC blocks with gearing have a built-in control module for word alignment. The memory PIC block has additional logic to manage DQS strobe signals and clock phase shift. The details of the memory PIC block and the gearing PIC block can be found in TN1203, MachXO2 High-Speed Source Synchronous and Memory Interfaces.

A common feature of all four types of PIC blocks is that each PIC block consists of four programmable I/Os (PIOs). Each PIO includes a sysIO buffer and an I/O logic block. A simplified sysIO block diagram is shown in Figure 10-1. The I/O logic block consists of an input block, an output block, and a tri-state block. These blocks have registers, input delay cells, and the necessary control logic to support various operational modes. The sysIO buffer determines the compliance to the supported I/O standards. It also supports features like hysteresis to meet common design needs. The I/O logic block and the sysIO buffer are designed with a minimal use of die area; providing easy bus interfacing, and pin out efficiency.

Two adjacent PIOs can form a pair of complementary output drivers. In addition, PIOA and PIOB of the PIC block form the primary pair of the buffer, while PIOC and PIOD form the alternate pair of the buffer. The primary pairs have additional capability that is not available on the alternate pair. The sysIO buffers of the PIC block are equivalent when implemented as the single-ended I/O standards.

Figure 10-1. PIC Block Diagram



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Supported sysIO Standards

The Lattice MachXO2 sysIO buffer supports both single-ended and differential standards. The single-ended standard can be further divided into internally ratioed standards such as LVCMOS, and externally referenced standards such as SSTL. The internally ratioed standards support individually configurable drive strength and bus maintenance circuits (weak pull-up, weak pull-down, or bus keeper).

There are two types of ratioed input buffers. One is connected to V_{CCIO} and the other is connected to V_{CC} (1.2V). Each sysIO buffer supports both buffers in parallel, and therefore provides an option to program any input buffer to be a 1.2V ratioed input buffer regardless of the V_{CCIO} voltage.

All banks of the MachXO2 devices support true differential inputs, and emulated differential outputs using external resistors and the complementary LVCMOS outputs. The true-LVDS differential outputs and LVDS input termination are supported in specific banks as described in the sysIO Banking Scheme section of this document.

Table 10-1. Supported Input Standards

Input Standard	V_{REF} (Nominal)	V_{CCIO}[1] (Nominal)
Single-Ended Interfaces		
LVTTL33	—	—
LVCMOS33	—	—
LVCMOS25	—	—
LVCMOS18	—	—
LVCMOS15	—	—
LVCMOS12	—	—
SSTL25 Class I, II	1.25	—
SSTL18 Class I, II	0.9	—
HSTL18 Class I, II	0.9	—
PCI33	-	3.3
Differential Interfaces		
LVDS25	—	—
LVPECL33	—	—
MLVDS25	—	—
BLVDS25	—	—
RSDS25	—	—
SSTL25 Differential	—	—
SSTL18D Differential	—	—
HSTL18D Differential	—	—
LVTTL / LVCMOS Differential	—	—

1. If not specified, refer to mixed voltage support in the VCCIO Requirement section.

Table 10-2. Supported Output Standards

Output Standards	Drive (mA)	V_{CCIO} (Nominal)
Single-Ended Interfaces		
LVTTL33	4, 8, 12, 16, 24	3.3
LVCMOS33	4, 8, 12, 16, 24	3.3
LVCMOS25	4, 8, 12, 16	2.5
LVCMOS18	4, 8, 12	1.8
LVCMOS15	4, 8	1.5
LVCMOS12	2, 6	1.2
SSTL25 Class I	8	2.5
SSTL18 Class I	8	1.8
HSTL18 Class I	8	1.8
PCI33	24	3.3
Differential Interfaces		
LVDS25	3.5, 2.5, 2.0, 1.25	2.5, 3,3
LVPECL33	16	3.3
MLVDS25	16	2.5
BLVDS25	16	2.5
RSDS25	8	2.5
SSTL25 Differential	8	2.5
SSTL18D Differential	8	1.8
HSTL18D Differential	8	1.8
LVTTL33 Differential	4, 8, 12, 16, 24	3.3
LVCMOS33 Differential	4, 8, 12, 16, 24	3.3
LVCMOS25 Differential	4, 8, 12, 16	2.5
LVCMOS18 Differential	4, 8, 12	1.8
LVCMOS15 Differential	4, 8	1.5
LVCMOS12 Differential	2, 6	1.2

sysIO Banking Scheme

The MachXO2 family has a non-homogeneous I/O banking structure. MachXO2-256, MachXO2-640/U and MachXO2-1200 have four I/O banks each with one I/O bank per side. MachXO2-1200U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices have six I/O banks each, with one I/O bank on each of the top, bottom and right sides, and three banks on the left side.

The MachXO-640U, MachXO-1200/U and higher density devices support true LVDS differential outputs through the primary pairs on the top bank (bank 0). Devices with the same LUT densities support 100 ohm differential input termination on every I/O pair on the bottom I/O bank. There is also a programmable PCI clamp available on the bottom I/O bank for these devices. For the “R1” version of the MachXO2 devices, the 100 ohm differential input termination is approximately 200 ohms. The “R1” versions of the MachXO2 devices have an “R1” suffix at the end of the part number (e.g., LCMXO2-1200ZE-1TG144CR1). For more details on the R1 to Standard migration refer to AN8086, Designing for Migration from MachXO2-1200-R1 to Standard (Non-R1) Devices.

MachXO2-256 and MachXO2-640 do not support true LVDS differential outputs, differential input termination, and PCI clamps in any banks (MachXO2-640U I/O architecture is similar to the larger devices and supports the aforementioned features). Each of the I/O pins on all MachXO2 PLDs has a clamp feature which can be disabled or enabled. This clamp is similar to the PCI clamp but it is not PCI compliant except in the bottom bank of the MachXO2-640U, MachXO2-1200/U and higher density devices. The arrangements of the I/O banks are shown in Figures 10-2, 10-3, and 10-4. DDR memory support in bank 1 is not available for devices in wafer level chip scale packages (WLCSP).

Figure 10-2. MachXO2-256 and MachXO2-640 I/O Banking Arrangement

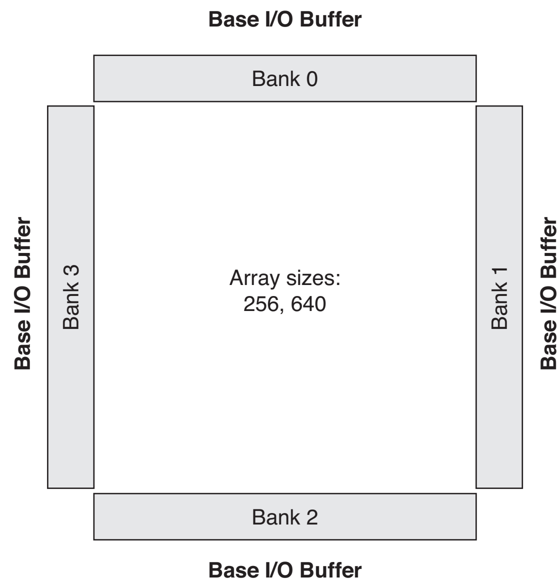


Figure 10-3. MachXO2-640U and MachXO2-1200 I/O Banking Arrangement

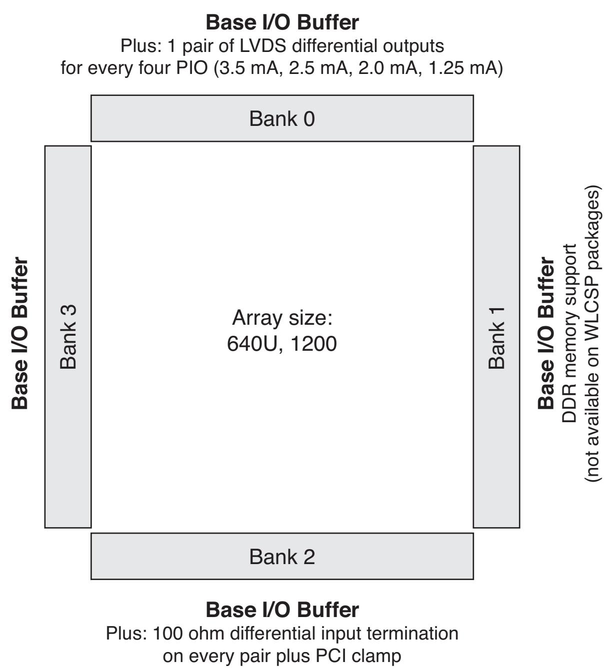
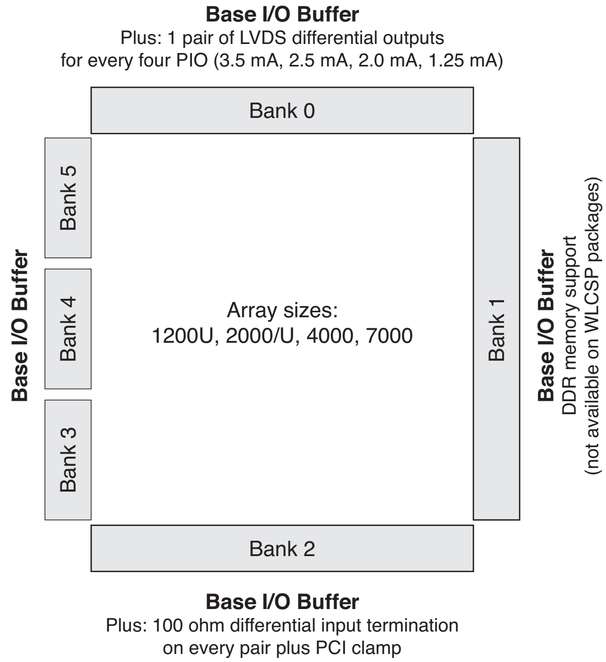


Figure 10-4. MachXO2-1200U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 I/O Banking Arrangement



sysIO Standards Supported by I/O Banks

All banks can support multiple I/O standards under the V_{CCIO} rules discussed above. Tables 10-3 and 10-4 summarize the I/O standards supported on various sides of the MachXO2 device.

Table 10-3. Single-Ended I/O Standards Supported on Various Sides

Standard	Top	Bottom	Left	Right
PCI33	—	Yes[1]	—	—
LVTTL33	Yes	Yes	Yes	Yes
LVCMOS33	Yes	Yes	Yes	Yes
LVCMOS25	Yes	Yes	Yes	Yes
LVCMOS18	Yes	Yes	Yes	Yes
LVCMOS15	Yes	Yes	Yes	Yes
LVCMOS12	Yes	Yes	Yes	Yes
SSTL25[2]	Yes	Yes	Yes	Yes
SSTL18[2]	Yes	Yes	Yes	Yes
HSTL18[2]	Yes	Yes	Yes	Yes

1. PCI33 is supported at the bottom bank of MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices.
2. SSTL Class II and HSTL Class II are supported as input only.

Table 10-4. Differential I/O Standards Supported on Various Sides

Standard	Top	Bottom	Left	Right
LVDS output	Yes[1]	—	—	—
LVPECL33E[2]	Yes	Yes	Yes	Yes
MLVDS25E[2]	Yes	Yes	Yes	Yes
BLVDS25E[2]	Yes	Yes	Yes	Yes
RSDS25E[2]	Yes	Yes	Yes	Yes
LVDS25E[2]	Yes	Yes	Yes	Yes
SSTL25D output	Yes	Yes	Yes	Yes
SSTL18D output	Yes	Yes	Yes	Yes
HSTL18D output	Yes	Yes	Yes	Yes
LVTTL33D output	Yes	Yes	Yes	Yes
LVCMOS33D output	Yes	Yes	Yes	Yes
LVCMOS25D output	Yes	Yes	Yes	Yes
LVCMOS18D output	Yes	Yes	Yes	Yes
LVCMOS15D output	Yes	Yes	Yes	Yes
LVCMOS12D output	Yes	Yes	Yes	Yes
LVDS input	Yes	Yes	Yes	Yes
LVPECL33 input	Yes	Yes	Yes	Yes
MLVDS25 input	Yes	Yes	Yes	Yes
BLVDS25 input	Yes	Yes	Yes	Yes
RSDS25 input	Yes	Yes	Yes	Yes
SSTL25D input	Yes	Yes	Yes	Yes
SSTL18D input	Yes	Yes	Yes	Yes
HSTL18D input	Yes	Yes	Yes	Yes
LVTTL33D input	Yes	Yes	Yes	Yes
LVCMOS33D input	Yes	Yes	Yes	Yes
LVCMOS25D input	Yes	Yes	Yes	Yes
LVCMOS18D input	Yes	Yes	Yes	Yes
LVCMOS15D input	Yes	Yes	Yes	Yes
LVCMOS12D input	Yes	Yes	Yes	Yes

1. True LVDS output is supported at the top bank of MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices.
2. Emulated output standards are denoted with a trailing “E” in the name of the standard.

Power Supply Requirements

The MachXO2 device family has a simplified power supply scheme for sysIO buffers. The core power V_{CC} and the bank power V_{CCIO} are the two main power supplies. A MachXO2 device can be powered and operated with a single power supply by connecting V_{CC} and V_{CCIO} to nominal voltages of 1.2V. The JTAG programming pins are powered by V_{CCIO} in bank 0 where the JTAG pins reside. All the user sysIOs have a weak pull-down after power-up is complete and before the device configuration is done.

V_{CCIO} Requirement for I/O Standards

Each I/O bank of a MachXO2 device has a separate V_{CCIO} supply pin that can be connected to 1.2V, 1.5V, 1.8V, 2.5V or 3.3V. This voltage is used to power the output I/O standard and source the drive strength for the output. In addition to this, V_{CCIO} also powers the ratioed input buffers such as LVTTL, LVCMOS and PCI. This ensures that the threshold of the input buffers tracking the V_{CCIO} voltage level.

For LVCMOS I/O types, mixed input voltage support is allowed in each I/O bank as long as the V_{CCIO} requirement for the input or output I/O standard is the same, or when all inputs in the bank are within the over-drive or under-drive range as specified in Tables 10-5 and 10-6. Two other options exist to further increase the input receiver flexibility. One is to configure an I/O to be a 1.2V ratioed input buffer, regardless of the bank V_{CCIO} voltage. This is possible because the MachXO2 sysIO buffer has two ratioed input buffers connected to V_{CCIO} and V_{CC} in parallel. The other option is to use the input reference voltage pin to set the input threshold for LVCMOS standards that are not covered by the V_{CCIO} of the bank.

Table 10-5. V_{CCIO} for Same Bank LVCMOS/LVTTL Input/Output Requirements[1]

I/O Type	Bank Restrictions
LVCMOS12	Outputs require V_{CCIO} = 1.2V Inputs available in all V_{CCIO} levels
LVCMOS15	Outputs require V_{CCIO} = 1.5V Inputs available in all V_{CCIO} levels.
LVCMOS15R33[2, 3]	Inputs only, require V_{CCIO} = 3.3V and V_{REF} = 0.75V
LVCMOS15R25[2, 3]	Inputs only, require V_{CCIO} = 2.5V and V_{REF} = 0.75V
LVCMOS18	Outputs require V_{CCIO}= 1.8V Inputs require V_{CCIO} = 1.5V, 1.8V, 2.5V, or 3.3V
LVCMOS18R33[2, 3]	Inputs only, require V_{CCIO} = 3.3V and V_{REF} = 0.9V
LVCMOS18R25[2, 3]	Inputs only, require V_{CCIO} = 2.5V and V_{REF} = 0.9V
LVCMOS25	Outputs require V_{CCIO} = 2.5V Inputs require V_{CCIO} = 1.5V, 1.8V, 2.5V, or 3.3V.
LVCMOS25R33[2, 3]	Inputs only, require V_{CCIO} = 3.3V and V_{REF} = 1.25V
LVCMOS33	Outputs require V_{CCIO} = 3.3V Inputs require V_{CCIO} = 1.5V, 1.8V, 2.5V, or 3.3V
LVTTL33	Outputs require V_{CCIO} = 3.3V Inputs require V_{CCIO} = 1.5V, 1.8V, 2.5V, or 3.3V
PCI33	Inputs and outputs both require V_{CCIO}= 3.3V

1. Certain I/O type and bank V_{CCIO} combinations may cause higher DC current. For more details refer to Table 10-6. Use Power Calculator to get power estimation for I/O types.
2. The HYSTERESIS option and BUS KEEPER option are not available for these I/O types.
3. Since only one V_{REF} signal can be supported in each I/O bank, only one of these I/O standards can be used in each I/O bank.

Table 10-6. Mixed Voltage Support for LVCMOS and LVTTL I/O Types

V_{CCIO}	Inputs					Outputs				
	1.2V	**1.5V**	**1.8V**	**2.5V**	**3.3V**	**1.2V**	**1.5V**	**1.8V**	**2.5V**	**3.3V**
1.2V	YES	YES[6]				YES				
1.5V	YES[1]	YES	YES[6]	YES[6]	YES[6]		YES			
1.8V	YES[1]	YES[5]	YES	YES[6]	YES[6]			YES		
2.5V	YES[1]	YES[2, 5, 7]	YES[3, 5, 7]	YES	YES[6]				YES	
3.3V	YES[1]	YES[2, 5, 7]	YES[3, 5, 7]	YES[4, 5, 7]	YES					YES

1. Leakage will occur if bus hold or weak pull-up is turned on.
2. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O types LVCMOS15R25 or LVCMOS15R33 with the referenced input buffer.
3. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O type LVCMOS18R25 or LVCMOS18R33 with the referenced input buffer.
4. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O type LVCMOS25R33 with the referenced input buffer.
5. Under-drive condition when using the ratioed input buffer. Under-drive causes higher DC current when the IO is at logic high. It is recommended to use Power Calculator to estimate the power consumption under such condition.
6. Over-drive condition when using the ratioed input buffer.
7. Ratioed input buffer in under-drive conditions is preferred over referenced input buffer due to lower power requirement for the ratioed input buffer.
8. When using the ratioed input buffers in under-drive or over-drive conditions, the HYSTERESIS setting shall be NA, the CLAMP setting shall be OFF, and the UP and KEEPER PULLMODE settings are not supported.

For differential input standards, certain mixed voltage support is allowed in the architecture as shown in Table 10-7.

Table 10-7. Mixed Voltage Support for Differential Input Standards

V_{CCIO}	Differential Inputs					
	LVDS, LVPECL33, MLVDS25, BLVDS25, RSDS25	**SSTL25D**	**SSTD18D, HSTL18D**	**LVTTL33D, LVCMOS33D**	**LVCMOS25D, LVCMOS15D, LVCMOS12D**	**LVCMOS18D**
1.2V						
1.5V						
1.8V			YES			YES
2.5V	YES	YES	YES		YES	YES
3.3V	YES	YES	YES	YES	YES	YES

Input Reference Voltage

Each I/O bank supports one reference voltage (V_{REF}). Any I/O in the bank can be configured as the input reference voltage pin. This pin is a regular I/O if it is not used as reference voltage input. To support SSTL and HSTL inputs, the reference voltage is set to half of the V_{CCIO} level. The input reference voltage can also be generated internally from the V_{REF} generator. Again, there is one V_{REF} generator per bank and its programmable settings include OFF, 45% of V_{CCIO}, 50% of V_{CCIO}, and 55% of V_{CCIO}. Programming of the internal V_{REF} generator and the external V_{REF} pin cannot be set at the same time for a particular bank because there is only one V_{REF} bus per bank.

sysIO Buffer Configuration

MachXO2 devices have three types of general-purpose sysIO buffer pairs to support a variety of single-ended and differential standards. Each sysIO buffer pair is made of two PIO buffers. PIO A and B pads form the primary pair, and PIO C and D pads form the alternate pair. Pads A and C of the pair are considered the “true” pad, while pads B and D are considered the “comp” pad. The “true” pad is associated with the positive side of the differential signal, while the “comp” pad is associated with the negative side of the differential signal.

All the PIOs support programmable clamp and bus maintenance circuitry to allow a weak pull-up, or a weak pull-down, or a weak bus keeper. The base sysIO buffer pair is used on all sides of the smaller devices, and on the left and right sides of MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices. The LVDS sysIO buffer pairs have additional LVDS output drivers in the primary PIO pairs. They are used on the top bank of the MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices. The bottom sysIO buffer pairs have additional 100ohm termination resistors between the “true” and “comp” pads. The bottom sysIO buffer pairs also support PCI clamp. They are supported on the bottom I/O bank of the MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices.

LVCMOS Buffer Configurations

The LVCMOS buffers are built on the base sysIO buffer pairs. These LVCMOS buffers can be configured in a variety of modes to support common circuit design needs.

Bus Maintenance circuit

Each pad has a weak pull-up, weak pull-down, and weak bus-keeper capability. These are selected with ON and OFF programmability. The pull-up and pull-down settings offer a fixed characteristic, which is useful in creating wired logic such as wired ORs. The bus-keeper option latches the signal in the last driven state, holding it at a valid level with minimal power dissipation. Input leakage can be minimized by turning off the bus maintenance circuitry. However, it is important to ensure that inputs are driven to a known state to avoid unnecessary power dissipation in the input buffer. The bus maintenance circuit is available for single-ended ratioed I/O standards.

Programmable Drive Strength

All single-ended drivers have programmable drive strength. This option can be set for each I/O independently. The drive strengths available for each I/O standard can be found in the MachXO2 Family Data Sheet. The MachXO2 programmable drive architecture is guaranteed with minimum drive strength for each drive setting. The V/I curves in the data sheet provide details of output driving capability versus the output load. This information, together with the current per bank and the package thermal limit current, should be taken into consideration when selecting the drive strength.

Input Hysteresis

All ratioed input receivers, except LVCMOS12, support input hysteresis. The input hysteresis for the LVCMOS33, LVCMOS25, LVCMOS18 and LVCMOS15 have two settings for flexibility. The ratioed input receivers have no input hysteresis when they are operated in under-drive or over-drive input conditions as shown in Tables 10-5 and 10-6.

Programmable Slew Rate

The single-ended output buffer for each device I/O pin has programmable output slew rate control that can be configured for either low noise (SLEWRATE=SLOW) or high speed (SLEWRATE=FAST) performance. Each I/O pin has an individual slew rate control. This slew rate control affects both the rising edge and the falling edges.

Tri-state and Open Drain Control

Each single-ended output driver has a separate tri-state control in addition to the global tri-state control for the device. The single-ended output drivers also support open drain operation on each I/O independently. The open drain output is typically pulled up externally and only the sink current specification is maintained.

PCI Support with PCI Clamp

The bottom sysIO buffer pair supports an optional PCI clamp diode that may be programmed individually.

This is only supported at the bottom edge of MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices. The PCI clamp supports a larger clamping current than the programmable clamp available on all other sides of the devices.

Complementary Outputs

Each sysIO buffer pair has built-in complementary circuit that can optionally be driven by the complement of the data that drives the single-ended driver associated with the true pad. This allows a pair of single-ended drivers to be used to drive complementary outputs with the lowest possible skew between the signals.

Differential Buffer Configurations

The base sysIO buffer pair supports differential input standards. Its complementary outputs support SSTL and HSTL differential output standards. The top and bottom edges of MachXO2-640U, MachXO2-1200/U and higher density devices support some additional functions over those supported by the base sysIO buffer pairs.

Differential Receivers

All the sysIO buffer pairs support differential input on all edges of the device. When a sysIO buffer pair is configured as differential receiver, the input hysteresis and the bus maintenance capabilities will be disabled for the buffer.

On-Chip Input Termination

The MachXO2 device supports on-chip 100 ohm (nominal) input differential termination on the bottom edge of MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices. The termination is available on all input PIO pairs of the bottom edge and is programmable.

Emulated Differential Outputs

All sysIO buffer pairs support complementary outputs as described above. This feature can be used to drive complementary SSTL or HSTL signals as required for differential SSTL and HSTL standards. It can also be used together with off-chip resistor networks for emulating the differential output standards such as LVPECL, MLVDS, BLVDS, and RSDS differential standards. When a sysIO buffer pair is configured as differential transmitter, the bus maintenance and open drain capabilities will be disabled. All single-ended sysIO buffers pairs in the MachXO2 family can support emulated differential output standards.

True Differential Output And Output Drive

MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices support true differential output drivers on the top edge of these devices. These true differential outputs are only available on the primary PIO pairs. The output driver has a fixed common mode of 1.2V and a programmable drive current of 1.25 mA, 2.5 mA, 2.0 mA or 3.5 mA. Only one true LVDS differential drive setting is available at a time. All true LVDS differential drivers on the top edge must be programmed to have the same drive strength. The bank V_{CCIO} for true differential output can be 2.5V or 3.3V.

Software sysIO Attributes

The sysIO attributes or primitives must be used in the Lattice development software to control the functions and capabilities of the sysIO buffers. sysIO attributes or primitives can be specified in the HDL source code, in the Lattice Diamond™ Spreadsheet View GUI, or in the ASCII preference file (.lpf) file directly. Appendices A, B and C list examples of using such attributes in different environments. This section describes each of these attributes in detail.

HDL Attributes

All the attributes discussed in this section, except two, can be used in the HDL source code to direct the sysIO buffer functionality.

I/O_TYPE

This attribute is used to set the sysIO standard for an I/O. The V_{CCIO} required to set these I/O standards are embedded in the attribute names. The BANK VCCIO attribute is used to specify allowed V_{CCIO} combinations for each I/O type. Table shows the valid I/O types for the MachXO2 family.

Table 10-8. Supported I/O Types

sysIO Signaling Standard	I/O_TYPE
LVDS 2.5V	LVDS25
Emulated LVDS 2.5V[1]	LVDS25E
RSDS	RSDS25
Emulated RSDS[1]	RSDS25E
Bus LVDS 2.5V	BLVDS25
Emulated Bus LVDS 2.5V[1]	BLVDS25E
MLVDS 2.5V	MLVDS25
Emulated MLVDS 2.5V[1]	MLVDS25E
LVPECL 3.3V	LVPECL33
Emulated LVPECL 3.3V[1]	LVPECL33E
SSTL 25 Class I	SSTL25_I
SSTL 25 Class II[2]	SSTL25_II
SSTL 25 Class I differential[3]	SSTL25D_I
SSTL 25 Class II differential[2, 3]	SSTL25D_II
SSTL 18 Class I	SSTL18_I
SSTL 18 Class II[2]	SSTL18_II
SSTL 18 Class I differential[3]	SSTL18D_I
SSTL 18 Class II differential[2, 3]	SSTL18D_II
HSTL 18 Class I	HSTL18_I
HSTL 18 Class II[2]	HSTL18_II
HSTL 18 Class I differential[3]	HSTL18D_I
HSTL 18 Class II differential[2,3]	HSTL18D_II
PCI 3.3V	PCI33
LVTTL 3.3V	LVTTL33
LVTTL 3.3V differential[3]	LVTTL33D
LVCMOS 3.3V	LVCMOS33
LVCMOS 3.3V differential[3]	LVCMOS33D
LVCMOS 2.5V (default)	LVCMOS25
LVCMOS 2.5V differential[3]	LVCMOS25D
LVCMOS 2.5V in a 3.3V VCCIO bank[4]	LVCMOS25R33
LVCMOS 1.8V	LVCMOS18
LVCMOS 1.8V differential[3]	LVCMOS18D
LVCMOS 1.8V in 3.3V VCCIO bank[4]	LVCMOS18R33
LVCMOS 1.8V in 2.5V VCCIO bank[4]	LVCMOS18R25
LVCMOS 1.5V	LVCMOS15
LVCMOS 1.5V differential[3]	LVCMOS15D
LVCMOS 1.5V in 3.3V VCCIO bank[4]	LVCMOS15R33
LVCMOS 1.5V in 2.5V VCCIO bank[4]	LVCMOS15R25
LVCMOS 1.2V	LVCMOS12
LVCMOS 1.2V differential[3]	LVCMOS12D

1. These differential output standards are emulated by using a complementary LVCMOS driver pair together with an external resistor pack.
2. Only input mode is supported. Output or bidirectional modes are not supported for these I/O types.
3. These differential standards are implemented by using a complementary LVCMOS driver pair.
4. These are input only and require V_{REF} to be set to certain value to allow the specified I/O types to be used.

DRIVE

The DRIVE strength attribute is available for the output and bidirectional I/O standards. The default drive value depends on the I/O standard used. Table 10-9 shows the supported drive strength for the single-ended I/O types under designated V_{CCIO} conditions.

Table 10-9. Output Drive Capability for Ratioed sysIO Standards

Drive Strength (mA)	I/O Type					
	LVCMOS12	LVCMOS15	LVCMOS18	LVCMOS25	LVCMOS33	LVTTL33
2	YES					
4		YES	YES	YES	YES	YES
6	YES					
8		YES	YES	YES	YES	YES
12			YES	YES	YES	YES
16				YES	YES	YES
24					YES	YES

DIFFDRIVE

The DIFFDRIVE strength attribute is available for the true LVDS output standard. All true LVDS differential drivers on the top edge must be programmed to have the same drive strength. The DIFFDRIVE value will be listed in the DRIVE column of Design Planner since this value is only valid for LVDS25 outputs.

Values: 1.25, 2.0, 2.5, 3.5, NA
Default: 3.5

PULLMODE

The PULLMODE option can be enabled or disabled independently for each I/O. When the user selects OPENDRAIN=ON, the PULLMODE for the output standard is default to NONE. If using LVCMOS I/O type in an under-drive or over-drive mode, the UP and KEEPER settings are not supported The FAILSAFE option is available for MLVDS25E bi-directional mode only.

Values: UP, DOWN, NONE, KEEPER, FAILSAFE
Default: DOWN for LVTTL, LVCMOS, and PCI; all others NONE

CLAMP

The CLAMP option can be enabled or disabled independently for each I/O. The available settings on the bottom edge of MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices is PCI or OFF. All other I/O have ON or OFF settings for this attribute.

Values: OFF, ON, PCI
Default: OFF

HYSTERESIS

The ratioed input buffers have two input hysteresis settings. The HYSTERESIS option can be used to change the amount of hysteresis for the LVTTL and LVCMOS input and bidirectional I/O standards, except for the LVCMOS12 inputs. The LVCMOS12 inputs do not support HYSTERESIS.

The LVCMOS25R33, LVCMOS18R25, LVCMOS18R33, LVCMOS15R25, and LVCMOS15R33 input types do not support HYSTERESIS. The HYSTERESIS option for each of the input pins can be set independently when it is supported for the I/O type.

Values: SMALL, LARGE, NA
Default: SMALL

VREF

The VREF option is enabled for single-ended SSTL and HSTL inputs and the referenced LVMCOS input buffers. The referenced LVMCOS input buffers are specified by choosing the I/O type as LVCMOS25R33, LVCMOS18R25, LVCMOS18R33, LVCMOS15R25, or LVCMOS15R33. The default value of NA will apply for all I/O types that do not use a VREF signal.

The VREF will default to external VREF pin for the single-ended SSTL/HSTL inputs, LVCMOS25R33, LVCMOS18R25, LVCMOS18R33, LVCMOS15R25, or LVCMOS15R33 inputs. The user may enter a VREF_NAME value in the “VREF Location(s)” pop-up window of the Spreadsheet View of the Diamond software. In doing so, the software will present the VREF_NAME as an available value in additional to the I45, I50 and I55 values in the VREF column of the Port Assignments tab of the Diamond Spreadsheet View. A pin location specified by the VREF_NAME value will be used as the VREF driver for that I/O bank. VREF_NAME is only necessary if the user wants to specify a pin to be used as an external VREF pin. Otherwise, the software will automatically assign a pin for the VREF signal.

There is only one VREF pin or internal VREF driver per I/O bank. Only one of the VREF driver settings chosen from I45, I50, I55 or VREF1_LOAD can be used in each I/O bank. This attribute can be set in the software GUI or in the ASCII preference file.

Values: OFF, I45, I50, I55, VREF_NAME
Default: NA

OPENDRAIN

The OPENDRAIN option is available for all LVTTL and LVCMOS output and bidirectional I/O standards. Each sysIO can be assigned independently to be open drain. When the OPENDRAIN attribute is used, the PULLMODE must be NONE and the CLAMP must be OFF.

Values: OFF, ON
Default: OFF

SLEWRATE

Each I/O pin has an individual slew rate control. This allows the designer to specify slew rate control on a pin-by-pin basis for outputs and bidirectional I/O pins. This is not a valid attribute for inputs or true differential outputs.

Values: FAST, SLOW, NA
Default: SLOW

DIFFRESISTOR

The bottom side I/O pins support on-chip differential input termination resistors on the MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices. The termination resistor is available for both the primary pair and the alternate pair of a sysIO. The values supported are zero (OFF) or 100 ohms.

Values: OFF, 100
Default: OFF

DIN/DOUT

The DIN/DOUT option is available for each I/O and can be configured independently. An input register is used for the input if the DIN attribute is assigned. Similarly, the software assigns an output register when the DOUT attribute is specified. By default, the software automatically assigns DIN or DOUT to input or output registers if possible.

LOC

This attribute specifies the site location for the component after the mapping process. When attached to multiple components, it indicates that these blocks are to be mapped together in the specified site. It specifies the PIC site for the pad when it is assigned to a pad. The LOC attribute can be attached to components that will end up on an I/O cell, clocks, and internal flip-flops, but it should not be attached to combinational logic that will end up on a logic cell; doing so could fail to generate a locate preference. The LOC attribute overrides register ordering.

Bank VCCIO

This attribute is necessary to verify the valid I/O types for a bank, to determine which input buffer to use, and to set the correct drive strength for the applicable I/O types. Since the I/O bank information is not required at the HDL level, this attribute is available through either the Diamond software's Spreadsheet View or in the ASCII preference file. Values: AUTO, 3.3, 2.5, 1.8, 1.5, 1.2. Default: AUTO.

sysIO Primitives

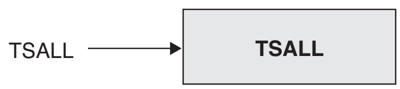
There are many sysIO primitives in the software library. A few are selected to be discussed in this section because some sysIO capabilities can only be utilized through instantiating the primitives in the HDL source code.

Tri-State All (TSALL)

The MachXO2 device supports the TSALL function that is used to enable or disable the tristate control to all the output buffers. The user can choose to assign any general purpose I/O pin to control the TSALL function since there is no dedicated TSALL pin. The TSALL primitive must be instantiated in the source code in order to enable the TSALL function. The input of the primitive can be assigned to an input pin or to an internal signal.

A value of TSALL=1 will tri-state all outputs but the outputs will be under individual OE control when TSALL=0.

Figure 10-5. TSALL Primitive



Fixed Data Delay (DELAYE)

This primitive supports up to 32 steps of static delay for all sysIO buffers in all banks of a MachXO2 device. Refer to the MachXO2 Family Data Sheet for delay step values. Although users can choose USER_DEFINED mode to set input delay, this primitive is primarily used by pre-defined source synchronous interfaces as described in TN1203, MachXO2 High-Speed Source Synchronous and Memory Interfaces.

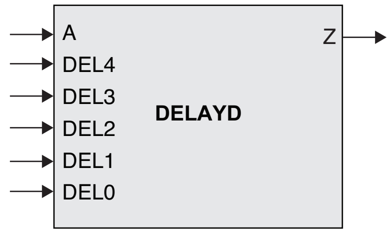
Figure 10-6. DELAYE Primitive and Associated Attributes

Attribute	Description	Value	Software Default
DEL_MODE	Fixed delay value depending on interface or user-defined delay values	SCLK_ZEROHOLD ECLK_ALIGNED ECLK_CENTERED SCLK_ALIGNED SCLK_CENTERED USER_DEFINED	USER_DEFINED
DEL_VALUE	User-defined value	DELAY0…DELAY31	DELAY0

Dynamic Data Delay (DELAYD)

This primitive supports dynamic delay for the sysIO buffers in the bottom bank (Bank 2) of MachXO2-640U, MachXO2-1200/U and larger devices. The 5-bit inputs can be controlled by user logic to modify the delay during the device operation.

Figure 10-7. DELAYD Primitive



Design Consideration and Usage

This section summarizes the MachXO2 designs rules and considerations that have been discussed in detail in previous sections. Table 10-6 lists the miscellaneous I/O features on each side of a MachXO2 device.

sysIO Buffer Features Common to All MachXO2 Devices

1. All banks support true differential inputs.
2. All banks support emulated differential outputs using external resistors and complementary LVCMOS outputs. Emulated differential output buffers are supported on both primary and alternate pairs.
3. All banks have programmable I/O clamps but they are not PCI compliant clamps.
4. All banks support weak pull-up, pull-down, and bus-keeper (bus hold latch) settings on each I/O independently.
5. V_{CCIO} voltage levels, together with the selected I/O types, determine the characteristics of an I/O, such as the pull mode, hysteresis, clamp behavior, and drive strength, supported in a bank. Multiple input standards can be supported in a bank through under-drive or over-drive conditions. Only one alternative input standard can be supported through the bank VREF setting (for example, LVCMOS25R33 requires V_{REF} to be 1.25V in a 3.3V V_{CCIO} bank). Each bank also supports 1.2V inputs regardless of the V_{CCIO} setting of the bank.
6. Each bank supports one V_{CCIO} signal.
7. Each bank supports one V_{REF} signal, whether it is from an external pin or from the internal V_{REF} generator.

sysIO Buffer Rules Specific to MachXO2-256 and MachXO2-640

1. Does not support true differential output buffers.
2. Does not support internal 100 ohm differential input terminations.
3. Does not support PCI clamps.

sysIO Buffer Rules Specific to MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000

1. Only Bank 0 (top side) supports true differential output buffers with programmable drive strengths. Only the primary pair supports true differential output buffers.
2. Only Bank 2 (bottom side) supports internal 100 ohm differential input terminations.
3. Only Bank 2 (bottom side) supports PCI compliant clamps.

Table 10-10. Miscellaneous I/O Features on Each Device Edge

Feature	Top	Bottom	Left	Right
100 Ohm Differential Resister	—	Yes[1]	—	—
Hot Socket	Yes	Yes	Yes	Yes
Clamp[3]	Yes	Yes	Yes	Yes
PCI Compliant Clamp	—	Yes[1]	—	—
Weak Pull-up[3]	Yes	Yes	Yes	Yes
Weak Pull-down[2]	Yes	Yes	Yes	Yes
Bus Keeper[3]	Yes	Yes	Yes	Yes
Input Hysteresis[3]	Yes	Yes	Yes	Yes
Slew Rate Control	Yes	Yes	Yes	Yes
Open Drain	Yes	Yes	Yes	Yes

1. Supported by MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices.
2. Software default setting
3. I/O characteristic under special conditions
    a. HYSTERESIS option is not available for LVCMOS12.
    b. HYSTERESIS option and BUS KEEPER option are not available for referenced input standards.
    c. When using the ratioed input buffers in under-drive or over-drive conditions, the HYSTERESIS setting shall be NA, the CLAMP setting shall be OFF, and the UP and KEEPER PULLMODE settings are not supported.
    d. HYSTERESIS and the bus maintenance capabilities are disabled for differential receivers.

Technical Support Assistance

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+1-503-268-8001 (Outside North America)
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Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
November 2010	01.0	Initial release.
January 2011	01.1	Updated for ultra-high I/O (“U”) devices.
April 2011	01.2	Updated for Lattice Diamond design software.
July 2011	01.3	Updated sysIO Banking Scheme text section with information on migrating from MachXO2-1200-R1 to Standard (non-R1) devices.
February 2012	01.4	Updated document with new corporate logo.
		Document status changed from Preliminary to Final.

Appendix A. sysIO HDL Attributes

The sysIO attributes can be used directly in the HDL source codes. This section provides a list of sysIO attributes supported by the MachXO2 PLD family. The correct syntax and examples for the Synplify® synthesis tool are provided here for reference.

Attributes in VHDL Language

Syntax

Table 10-11. VHDL Attribute Syntax

Attribute	Syntax
I/O_TYPE	attribute I/O_TYPE: string; attribute I/O_TYPE of Pinname: signal is "I/O_TYPE Value";
DRIVE	attribute DRIVE: string; attribute DRIVE of Pinname: signal is "Drive Value";
DIFFDRIVE	attribute DRIVE: string; attribute DRIVE of Pinname: signal is "Diffdrive Value";
DIFFRESISTOR	attribute DIFFRESISTOR: string; attribute DIFFRESISTOR of Pinname: signal is "DIFFRESISTOR Value";
CLAMP	attribute CLAMP: string; attribute CLAMP of Pinname: signal is "Clamp Value";
HYSTERESIS	attribute HYSTERESIS: string; attribute HYSTERESIS OF Pinname: signal is "Hysteresis Value";
VREF	NA
PULLMODE	attribute PULLMODE: string; attribute PULLMODE of Pinname: signal is "Pullmode Value";
OPENDRAIN	attribute OPENDRAIN: string; attribute OPENDRAIN of Pinname: signal is "OpenDrain Value";
SLOWSLEW	attribute PULLMODE: string; attribute PULLMODE of Pinname: signal is "Slewrate Value";
DIN	attribute DIN: string; attribute DIN of Pinname: signal is "value ";
DOUT	attribute DOUT: string; attribute DOUT of Pinname: signal is "value ";
LOC	attribute LOC: string; attribute LOC of Pinname: signal is "Pin locations";
BANK VCCIO	NA

Examples

I/O_TYPE

```
 --***Attribute Declaration***
ATTRIBUTE I/O_TYPE: string;
 --***I/O_TYPE assignment for I/O Pin***
ATTRIBUTE I/O_TYPE OF portA: SIGNAL IS "PCI33";
ATTRIBUTE I/O_TYPE OF portB: SIGNAL IS "LVCMOS33";
ATTRIBUTE I/O_TYPE OF portC: SIGNAL IS "SSTL18_I";
ATTRIBUTE I/O_TYPE OF portD: SIGNAL IS "LVDS25";
```

DRIVE

```
--***Attribute Declaration***
ATTRIBUTE DRIVE: string;
--***DRIVE assignment for I/O Pin***
ATTRIBUTE DRIVE OF portB: SIGNAL IS "8";
```

DIFFDRIVE

```
 --***Attribute Declaration***
ATTRIBUTE DIFFDRIVE: string;
--*** DIFFDRIVE assignment for I/O Pin***
ATTRIBUTE DIFFDRIVE OF portD: SIGNAL IS "2.0";
```

DIFFRESISTOR

```
 --***Attribute Declaration***
ATTRIBUTE DIFFRESISTOR: string;
--*** DIFFRESISTOR assignment for I/O Pin***
ATTRIBUTE DIFFRESISTOR OF portD: SIGNAL IS "100";
```

CLAMP

```
--***Attribute Declaration***
ATTRIBUTE CLAMP: string;
--*** CLAMP assignment for I/O Pin***
ATTRIBUTE CLAMP OF portA: SIGNAL IS "PCI33";
```

HYSTERESIS

```
--***Attribute Declaration***
ATTRIBUTE HYSTERESIS: string;
--*** HYSTERESIS assignment for Input Pin***
ATTRIBUTE HYSTERESIS OF portA: SIGNAL IS " LARGE ";
```

PULLMODE

```
--***Attribute Declaration***
ATTRIBUTE PULLMODE : string;
--***PULLMODE assignment for I/O Pin***
ATTRIBUTE PULLMODE OF portA: SIGNAL IS "DOWN";
ATTRIBUTE PULLMODE OF portB: SIGNAL IS "UP";
```

OPENDRAIN

```
--***Attribute Declaration***
ATTRIBUTE OPENDRAIN: string;
--***Open Drain assignment for I/O Pin***
ATTRIBUTE OPENDRAIN OF portB: SIGNAL IS "ON";
```

SLEWRATE

```
 --***Attribute Declaration***
ATTRIBUTE SLEWRATE : string;
--*** SLEWRATE assignment for I/O Pin***
ATTRIBUTE SLEWRATE OF portB: SIGNAL IS "FAST";
```

DIN/DOUT

```
--***Attribute Declaration***
ATTRIBUTE din : string; ATTRIBUTE dout : string;
--*** din/dout assignment for I/O Pin***
ATTRIBUTE din OF input_vector: SIGNAL IS "TRUE ";
ATTRIBUTE dout OF output_vector: SIGNAL IS "TRUE ";
```

LOC

```
--***Attribute Declaration***
ATTRIBUTE LOC : string;
 --*** LOC assignment for I/O Pin***
ATTRIBUTE LOC OF input_vector: SIGNAL IS "E3,B3,C3 ";
```

Attributes in Verilog Language

Syntax

Table 10-12. Verilog Attribute Syntax

Attribute	Syntax
I/O_TYPE	PinType PinName /* synthesis I/O_TYPE="I/O_Type Value"*/;
DRIVE	PinType PinName /* synthesis DRIVE="Drive Value"*/;
DIFFDRIVE	PinType PinName /* synthesis DIFFDRIVE =" DIFFDRIVE Value"*/;
DIFFRESISTOR	PinType PinName /* synthesis DIFFRESISTOR =" DIFFRESISTOR Value"*/;
CLAMP	PinType PinName /* synthesis CLAMP =" Clamp Value"*/;
HYSTERESIS	PinType PinName /*synthesis HYSTERESIS = "Hysteresis Value" */;
VREF	N/A
PULLMODE	PinType PinName /* synthesis PULLMODE="Pullmode Value"*/;
OPENDRAIN	PinType PinName /* synthesis OPENDRAIN ="OpenDrain Value"*/;
SLOWSLEW	PinType PinName /* synthesis SLEWRATE="Slewrate Value"*/;
DIN	PinType PinName /* synthesis DIN= "value" */;
DOUT	PinType PinName /* synthesis DOUT= "value" */;
LOC	PinType PinName /* synthesis LOC="pin_locations "*/;
Bank VCCIO	N/A

Examples

//I/O_TYPE, PULLMODE, SLEWRATE and DRIVE assignment

```
output portB /*synthesis I/O_TYPE="LVCMOS33"
PULLMODE ="UP" SLEWRATE ="FAST" DRIVE ="20"*/;
output portC /*synthesis I/O_TYPE="LVDS25" */;
```

//DIFFDRIVE

```
output portD /* synthesis I/O_TYPE="LVDS25" DIFFDRIVE="2.0"*/;
```

//DIFFRESISTOR

```
output [4:0] portA /* synthesis I/O_TYPE="LVDS25" DIFFRESISTOR ="100"*/;
```

//CLAMP

```
output portA /*synthesis I/O_TYPE="PCI33" CLAMP ="PCI" */;
```

//HYSTERESIS

```
input mypin /* synthesis HYSTERESIS = "LARGE" */;
```

//OPENDRAIN

```
output portA /*synthesis OPENDRAIN ="ON"*/;
```

// DIN Place the flip-flops near the load input

```
 input load /* synthesis din="" TRUE */;
```

// DOUT Place the flip-flops near the outload output

```
 output outload /* synthesis dout="TRUE" */;
```

//LOC pin location

```
input [3:0] DATA0 /* synthesis loc="E3,B1,F3"*/;
```

//LOC Register pin location

```
reg data_in_ch1_buf_reg3 /* synthesis loc="R10C16" */;
```

//LOC Vectored internal bus

```
reg [3:0] data_in_ch1_reg /*synthesis loc ="R10C16,R10C15,R10C14,R10C9" */;
```

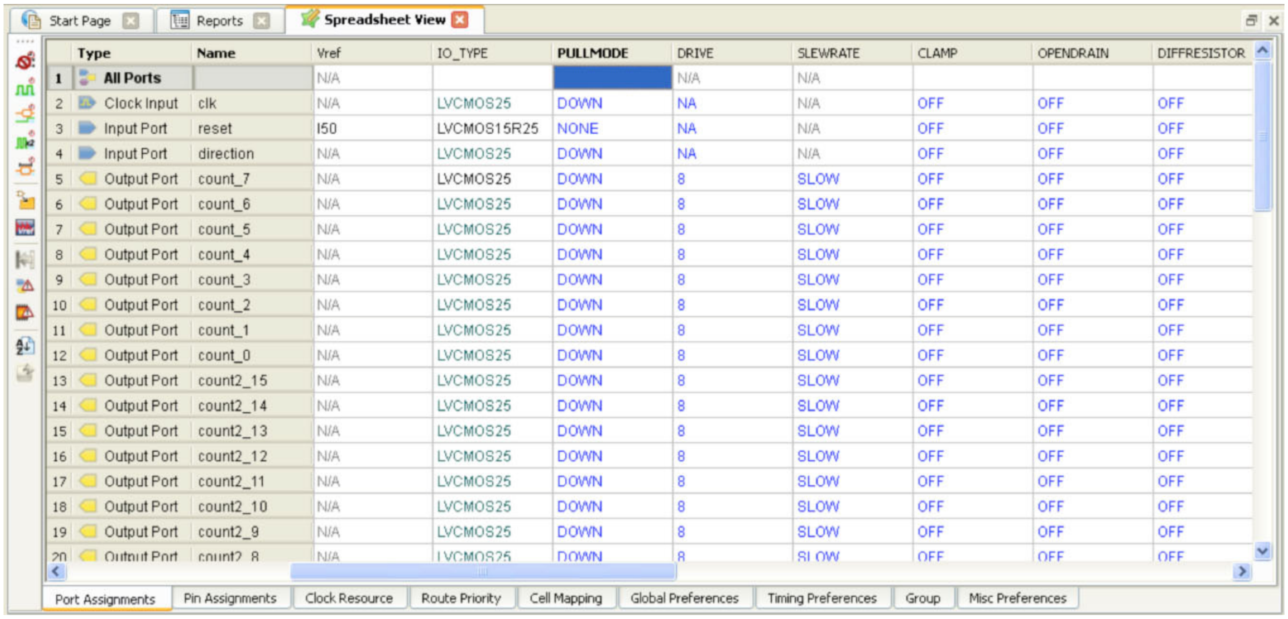
Appendix B. sysIO Attributes Using the Spreadsheet View

The sysIO buffer attributes can be assigned using the Spreadsheet View available in the Diamond design tool. The attributes that are not available as HDL attributes, such as VREF and Bank VCCIO, are available in the Spreadsheet View GUI.

The Port Assignment tab lists all the ports in a design and all the available sysIO attributes as preferences. Click on each of these cells for a list of all the valid I/O preferences for that port. Each column takes precedence over the next. Therefore, when a particular I/O_TYPE is chosen, the columns for the DRIVE, PULL-MODE, SLEW-RATE and other attributes will list the valid combinations for that I/O_TYPE. Pin locations can be locked using the Pin column of the Port Assignment tab. Right-clicking on a cell will list all the available pin locations. The Spreadsheet View can run a DRC check to check for incorrect sysIO attribute assignments.

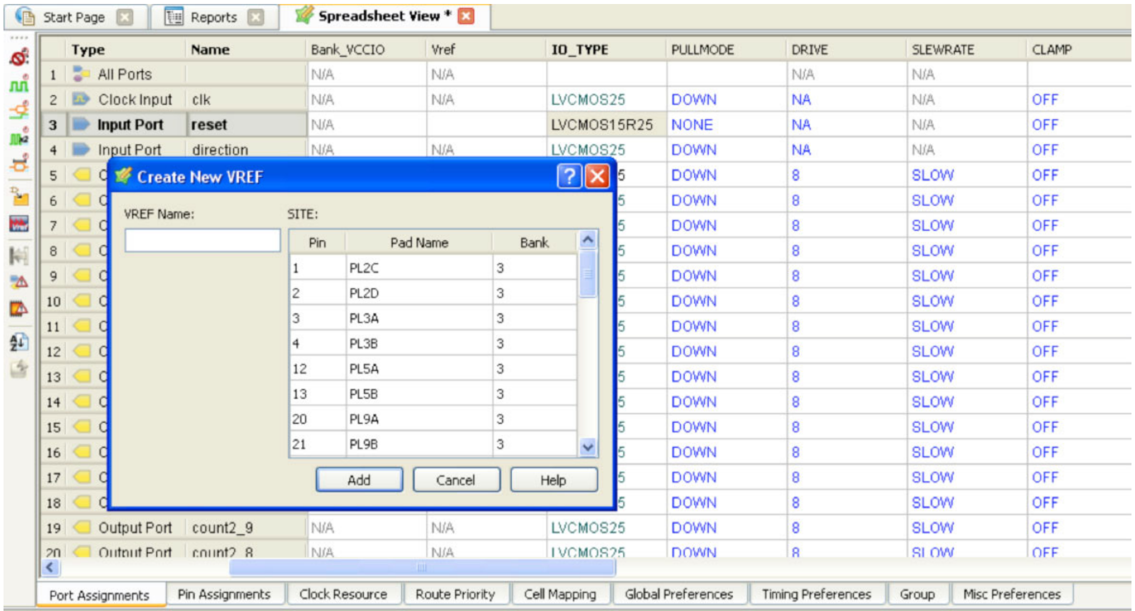
All the preferences assigned using the Spreadsheet View are written into the logical preference file (.lpf).

Figure 10-8. Port Assignment Tab of Spreadsheet View



	Type	Name	Vref	IO_TYPE	PULLMODE	DRIVE	SLEWRATE	CLAMP	OPENDRAIN	DIFFRESISTOR
1	All Ports		N/A			N/A	N/A			
2	Clock Input	clk	N/A	LVCMOS25	DOWN	NA	N/A	OFF	OFF	OFF
3	Input Port	reset	I50	LVCMOS15R25	NONE	NA	N/A	OFF	OFF	OFF
4	Input Port	direction	N/A	LVCMOS25	DOWN	NA	N/A	OFF	OFF	OFF
5	Output Port	count_7	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
6	Output Port	count_6	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
7	Output Port	count_5	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
8	Output Port	count_4	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
9	Output Port	count_3	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
10	Output Port	count_2	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
11	Output Port	count_1	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
12	Output Port	count_0	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
13	Output Port	count2_15	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
14	Output Port	count2_14	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
15	Output Port	count2_13	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
16	Output Port	count2_12	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
17	Output Port	count2_11	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
18	Output Port	count2_10	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
19	Output Port	count2_9	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF
20	Output Port	count2_8	N/A	LVCMOS25	DOWN	8	SLOW	OFF	OFF	OFF

Figure 10-9. VREF Name and Location Pop-up Window of the Spreadsheet View



V_{REF} Assignment in the Spreadsheet View

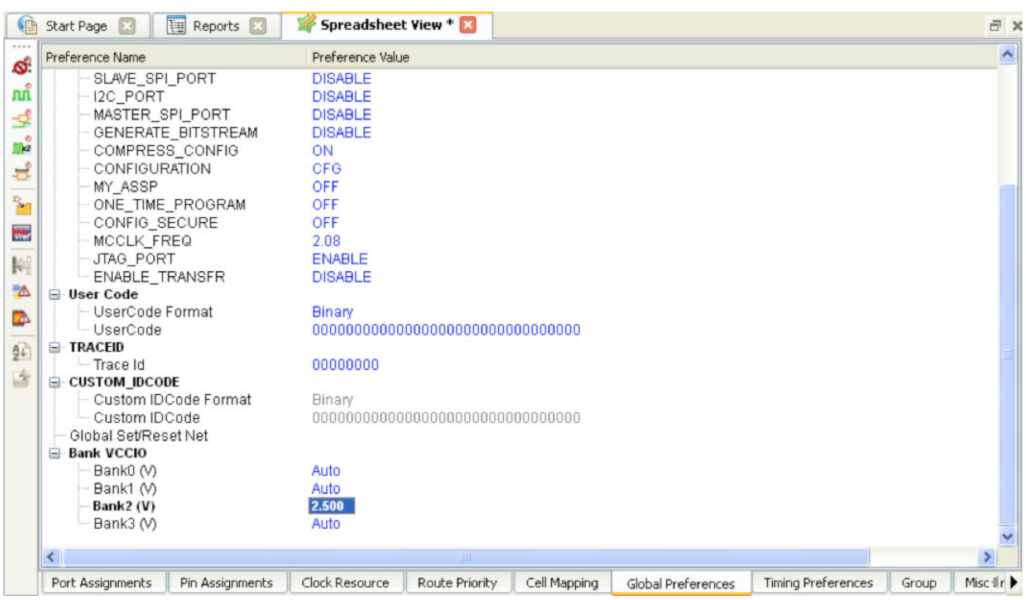
The VREF attribute can be assigned in the Spreadsheet View by clicking on the Vref Locations(s) button on the left hand side. It is required to use this button only if a specific location for the VREF driver is desired. Otherwise the software will assign the VREF driver signal to any location that does not violate the sysIO bank rules.

When the VREF_NAME is assigned to a specific pin, the software will list VREF_NAME in the VREF column of the Port Assignments tab. Both VREF_NAME and pin location will be reflected in the VREF column of the Pin Attribute sheet.

Bank V_{CCIO} Setting in the Spreadsheet View

Bank VCCIO is editable in the Global tab of the Spreadsheet View. The value of the Bank VCCIO can be chosen by the users to determine the value of VCCIO of a specific bank.

Figure 10-10. Bank VCCIO in Global Preference Tab



Appendix C. sysIO Attributes Using Preference File (ASCII File)

Designers can enter sysIO attributes directly in the preference (.lpf) file as sysIO buffer preferences. The LPF file is a post-synthesis FPGA constraint file that stores logical preferences that have been created or modified in the Spreasheet View or directly in a text editor. It also contains logical preferences originating in the HDL source. Modifying the Speadsheet View in the Diamond software will automatically update the content of the LPF file and vice versa. The settings in the Spreadsheet View are reflected in the preference file once they are saved. Details of the supported preferences and their corresponding syntax can be found in the Diamond Help System.