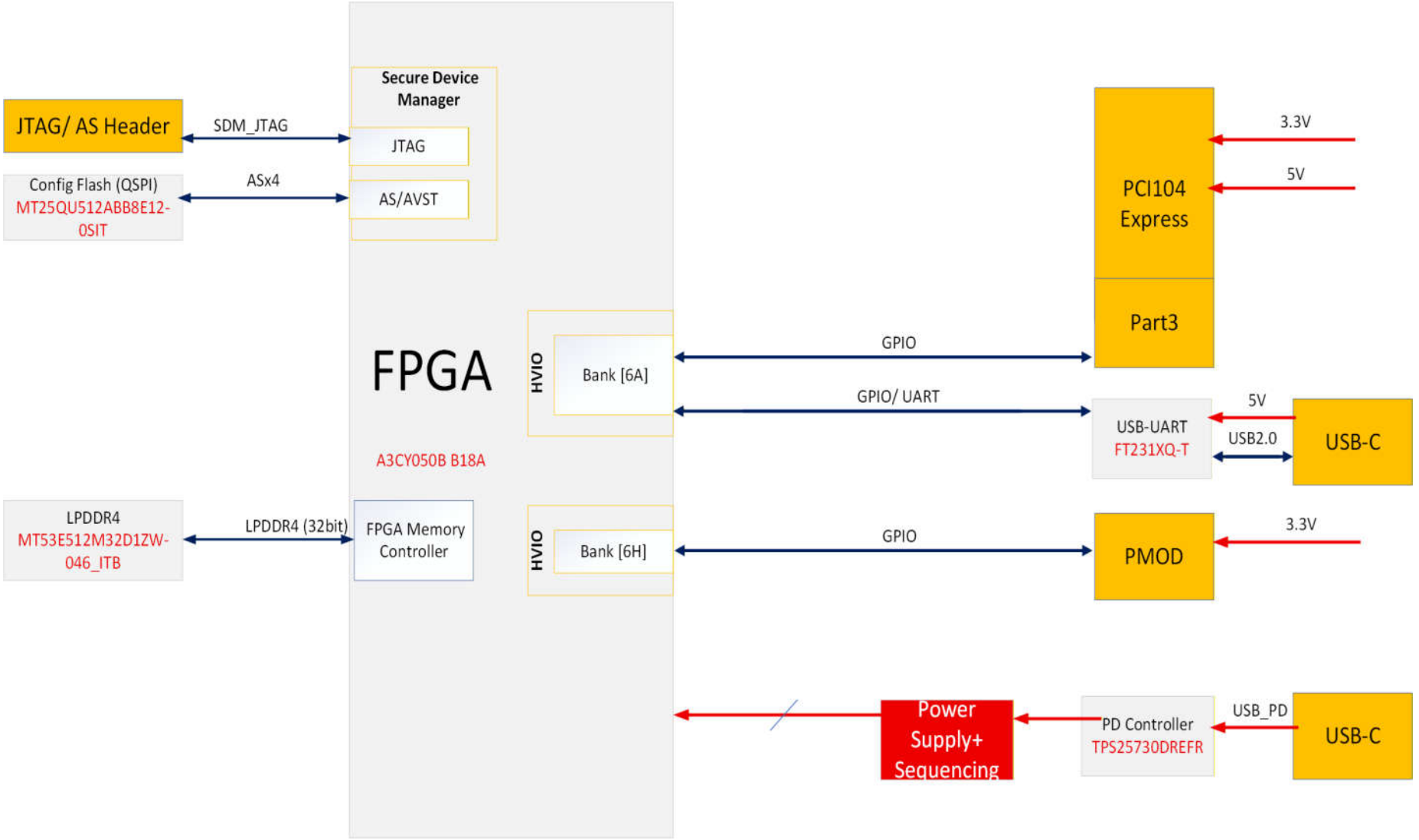
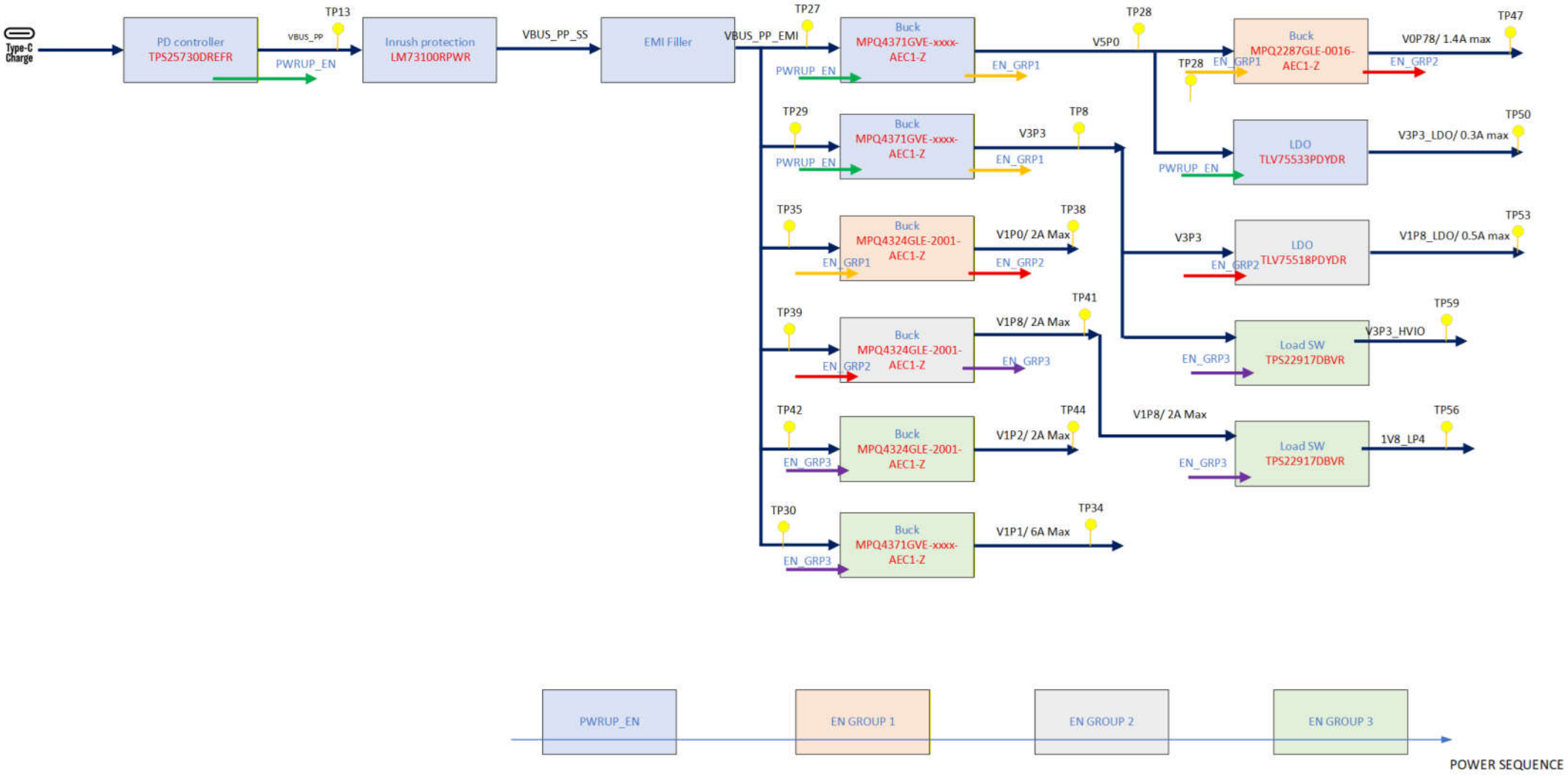
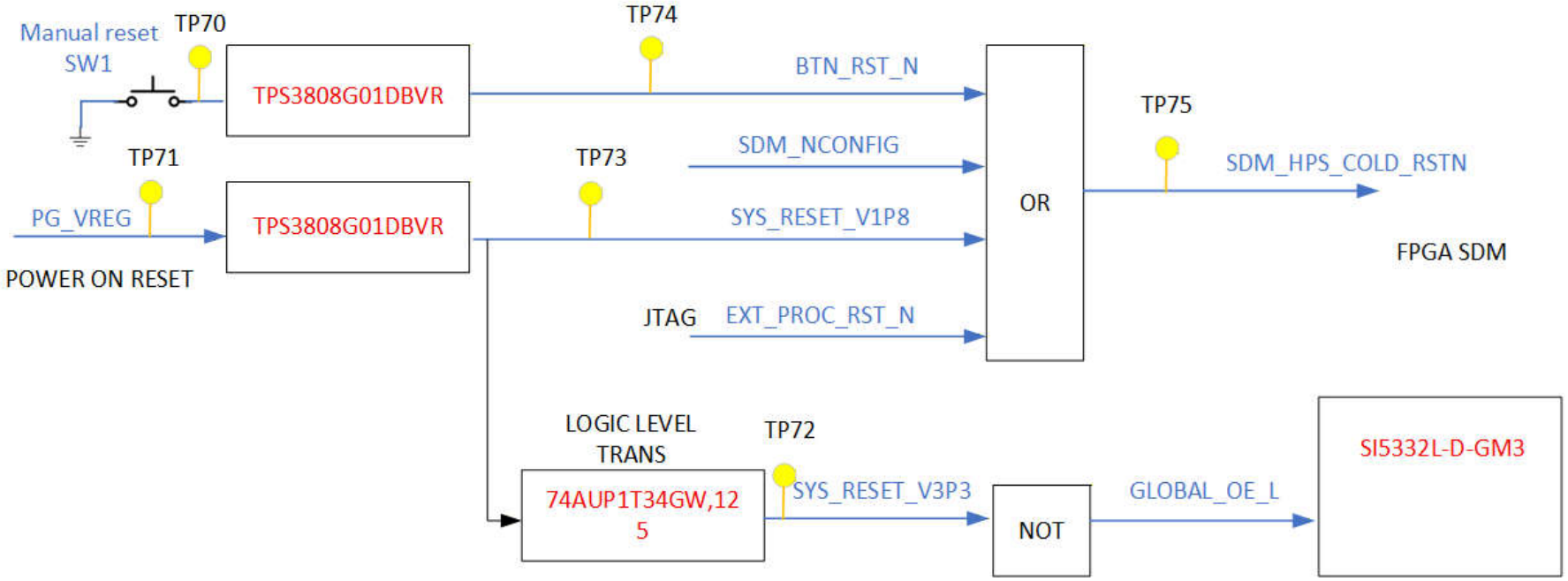


<OrgName> <OrgAddr1>		Title: Block Diagram		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	B	01
Review	<Engineer Name>	Sheet 1	Number of Sheets	25



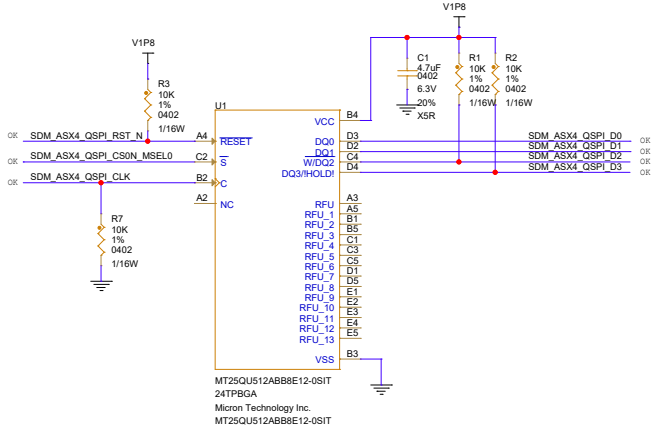
<*OrgName*> <OrgAddr1>		Title: Power tree+ sequence		
Responsible	**Name**	**Date**	**Size**	**Rev**
Design	<Checker>	Saturday, December 06, 2025	B	01
Review	<Engineer Name>	**Sheet** 2	**Number of Sheets**	25

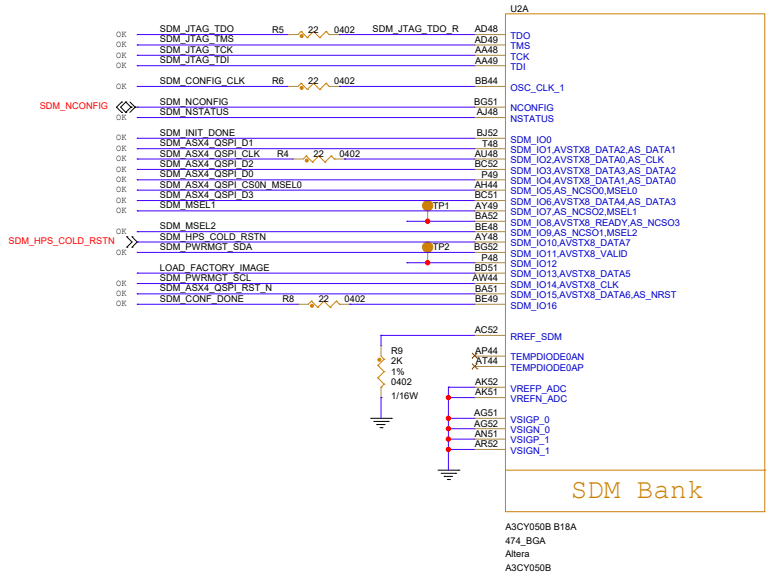


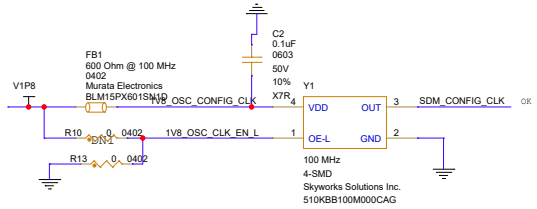
<OrgName> <OrgAddr1>		Title: Reset Diagram		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	B	01
Review	<Engineer Name>	Sheet 3	Number of Sheets	25

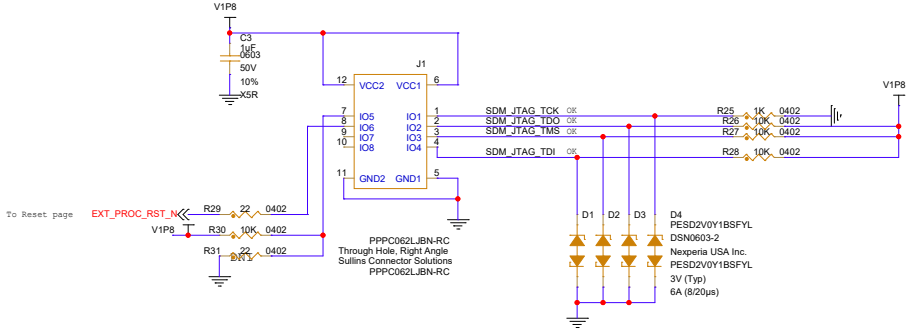
Reference	Note
TP1	FPGA SDM_IO8 pin
TP2	FPGA SDM_IO12 pin
TP3	V1P8_VCCADC
TP4	V1P8_VCCPLL_SDM
TP5	V0P78F
TP9	USB Type C PD controller, ADC 1 input
TP10	USB Type C PD controller, ADC 2 input
TP11	USB Type C PD controller, ADC 3 input
TP12	USB Type C PD controller, ADC 4 input
TP13	VBUS_PP (15-20V) input
TP14	GND
TP18	VIN_3V3 (External)
TP19	USB Type C PD controller, LDO_3V3
TP20	USB Type C PD controller, LDO_1V5
TP21	U5, SYN
TP22	U6, SYN
TP23	U7, SYN
TP24	U11, SYNOUT

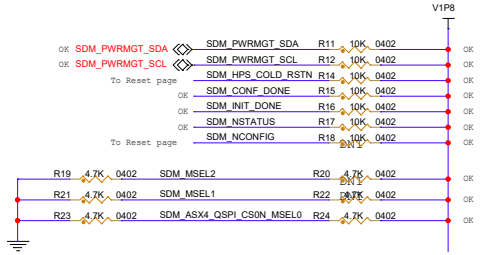
<OrgName> <OrgAddr1>		Title: Configuration table		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	B	01
Review	<Engineer Name>	Sheet 4	Number of Sheets	25



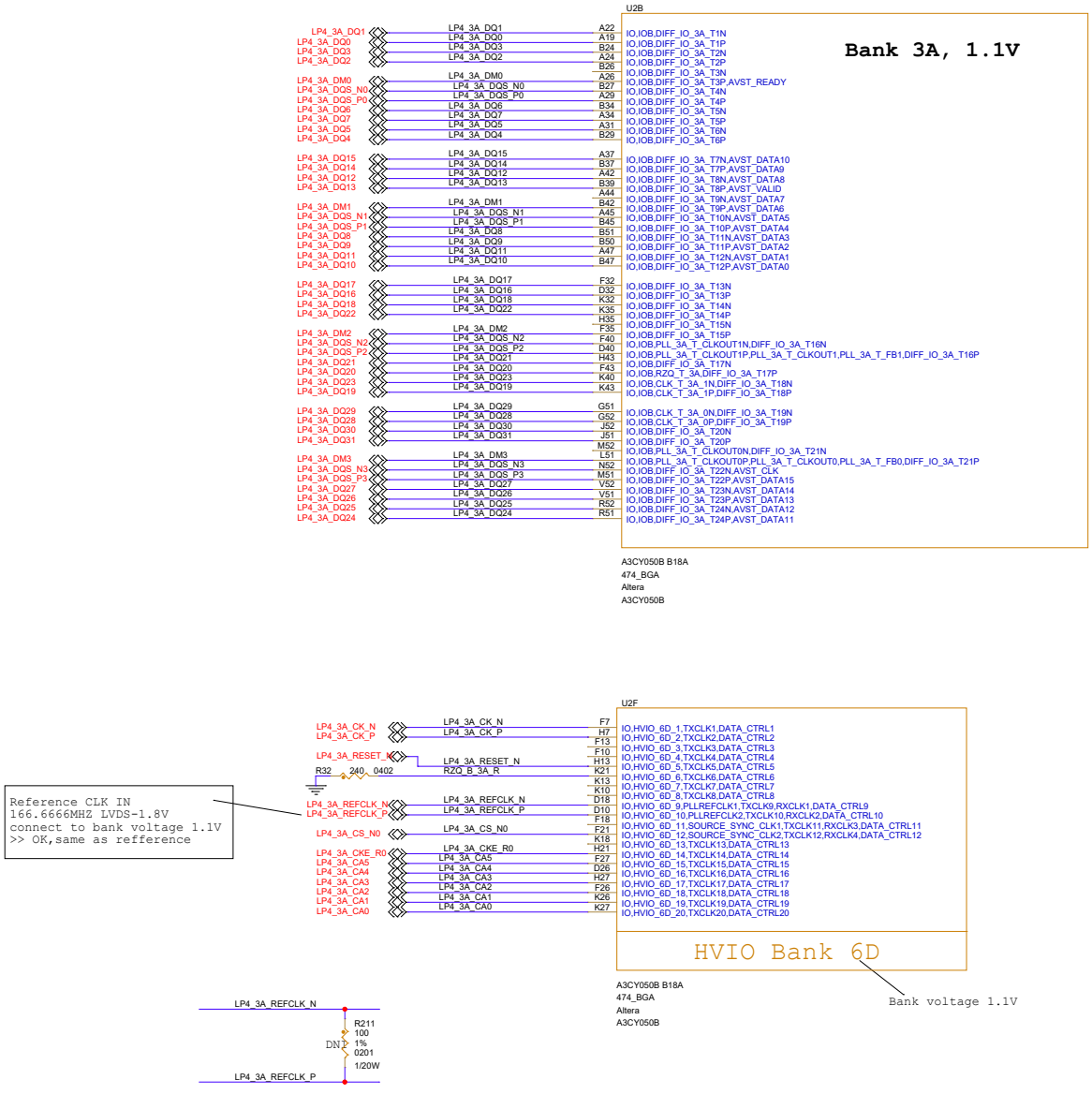




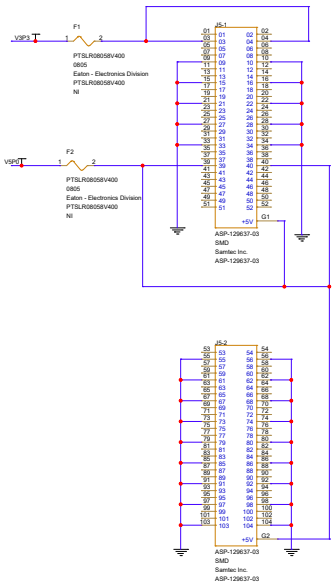




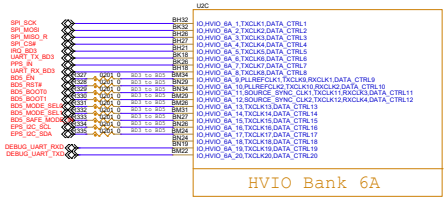
<OrgName> <OrgAddr1>		Title: QSPI, SDM Configuration		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	C	01
Review	<Engineer Name>	Sheet 5	Number of Sheets	25

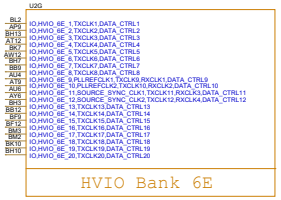


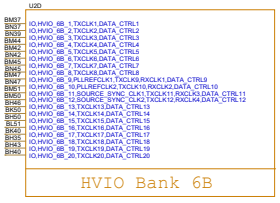
<OrgName> <OrgAddr1>		Title: FPGA LPDDR4 IO		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	C	01
Review	<Engineer Name>	Sheet 6	Number of Sheets	25

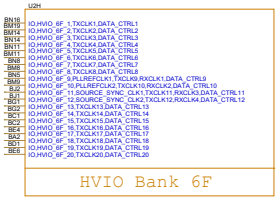


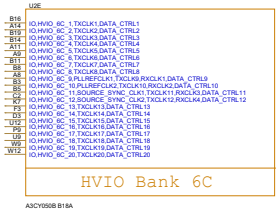
[PCIe-Connector Mechanical Stack Only]

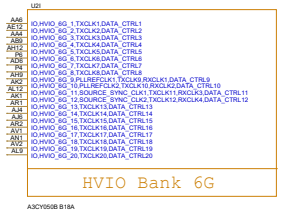




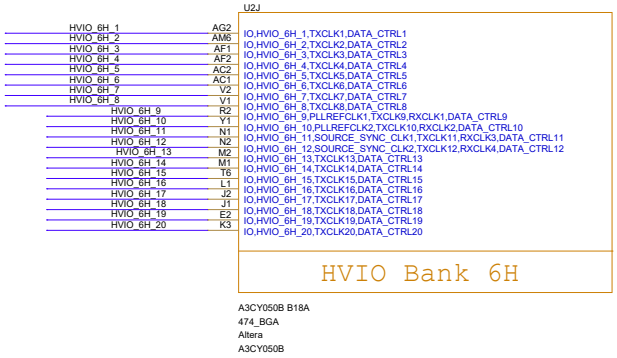


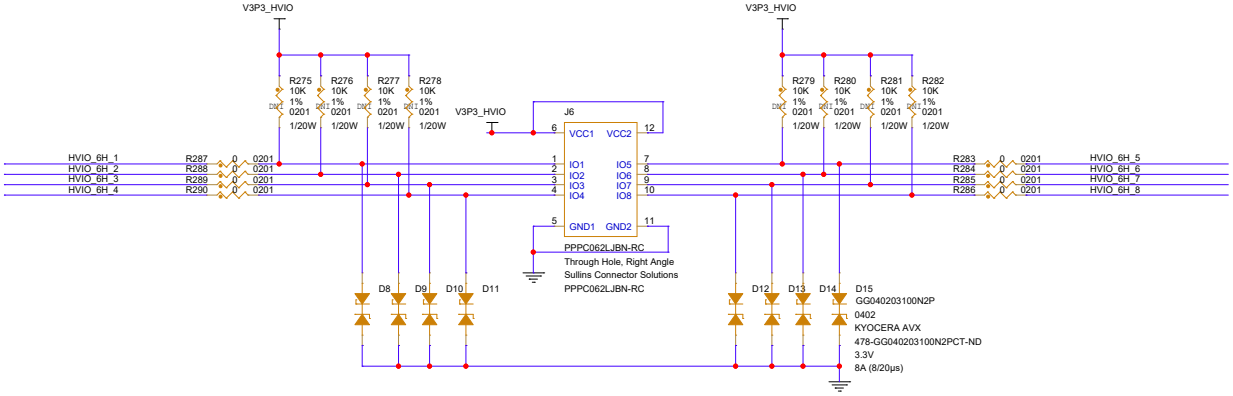




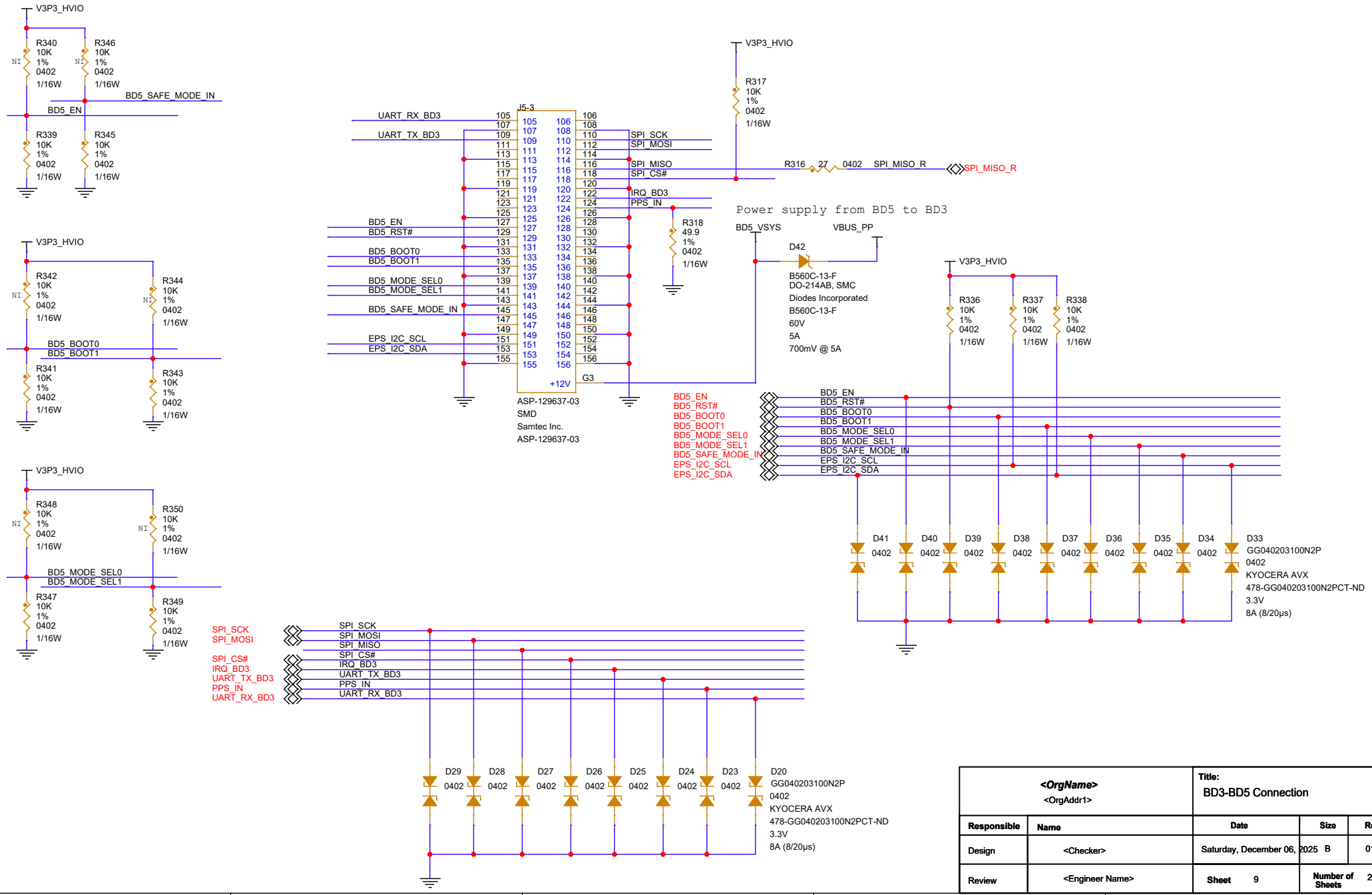


<OrgName> <OrgAddr1>		Title: PCI104, BD3-BDS IO	
Responsible	Name	Date	Size / Rev
Design	<Checker>	Saturday, December 06, 2025	D / 01
Review	<Engineer Name>	Sheet 7	Number of Sheets 25

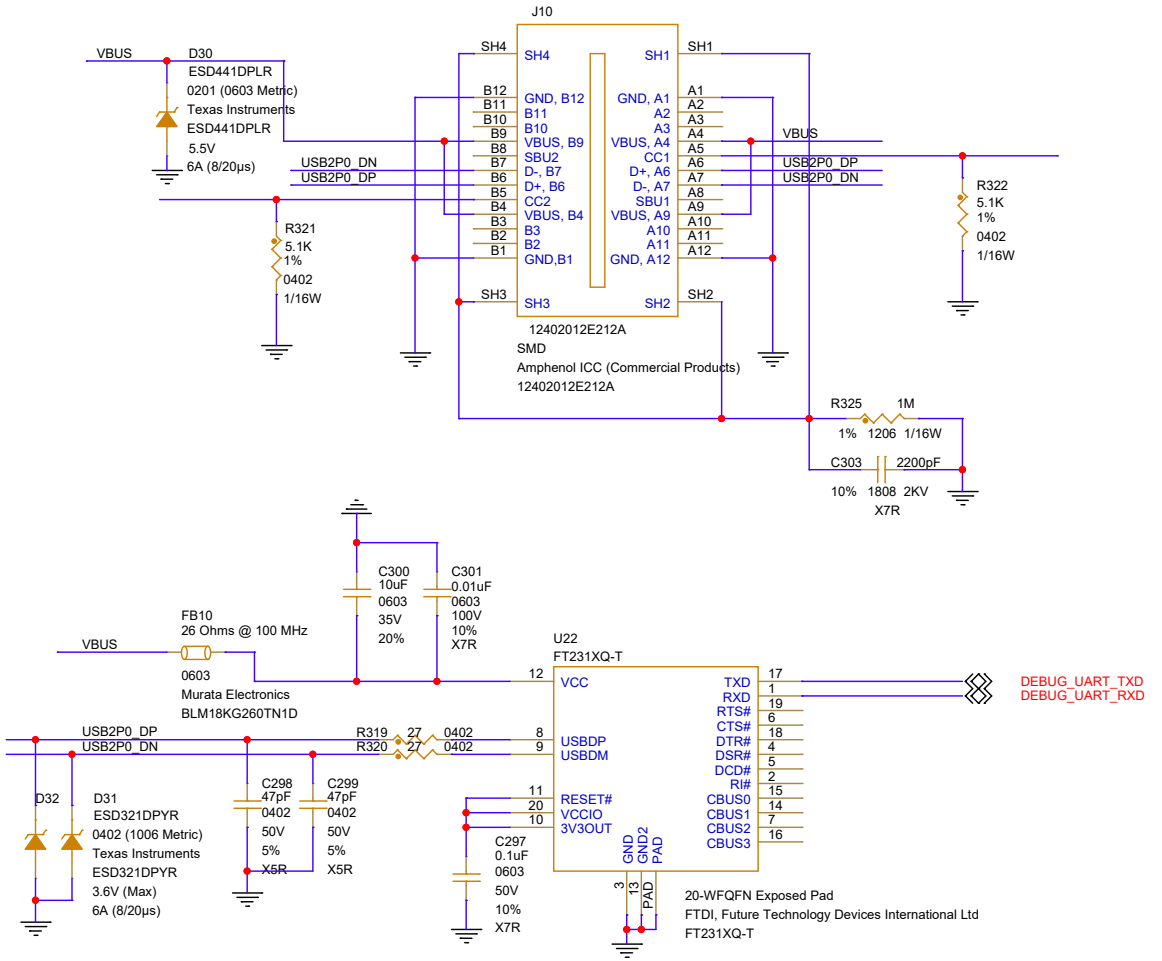




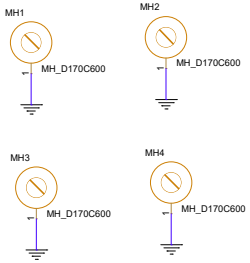
<OrgName> <OrgAddr1>		Title: PMOD		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	C	01
Review	<Engineer Name>	Sheet 8	Number of Sheets	25



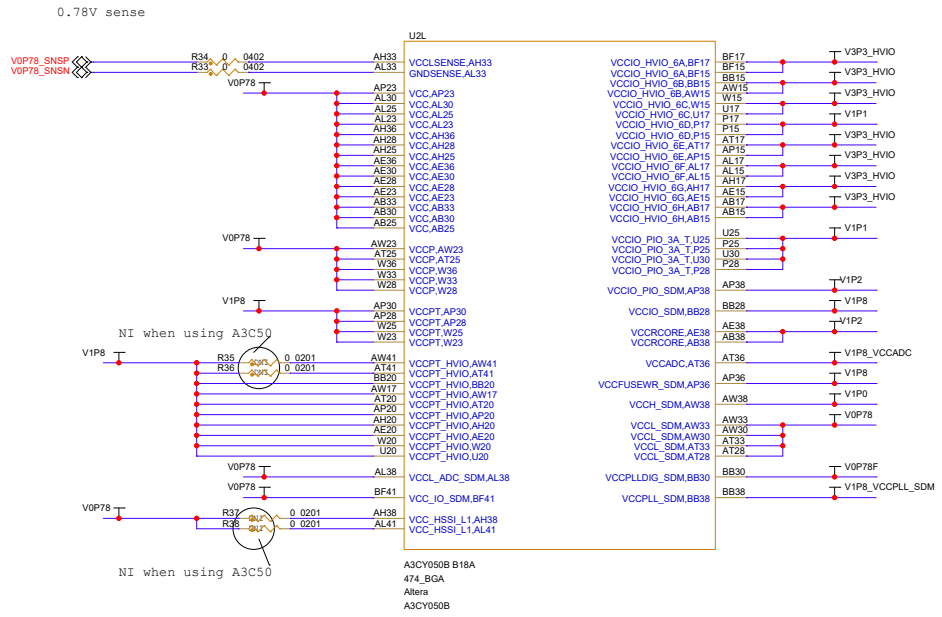
<OrgName> <OrgAddr1>		Title: BD3-BD5 Connection		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	B	01
Review	<Engineer Name>	Sheet 9	Number of Sheets	25

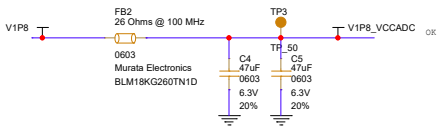


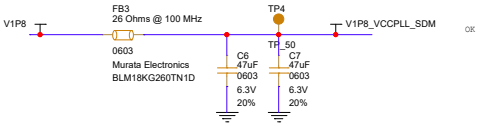
<OrgName> <OrgAddr1>		Title: USBC-UART Debug		
Responsible	**Name**	**Date**	**Size**	**Rev**
Design	<Checker>	Saturday, December 06, 2025	B	01
Review	<Engineer Name>	**Sheet** 10	**Number of Sheets**	25

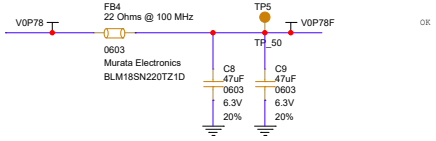


<OrgName> <OrgAddr1>		**Title:** Mechanical		
Responsible	**Name**	**Date**	**Size**	**Rev**
Design	<Checker>	Saturday, December 06, 2025	C	01
Review	<Engineer Name>	**Sheet** 11	**Number of Sheets**	25

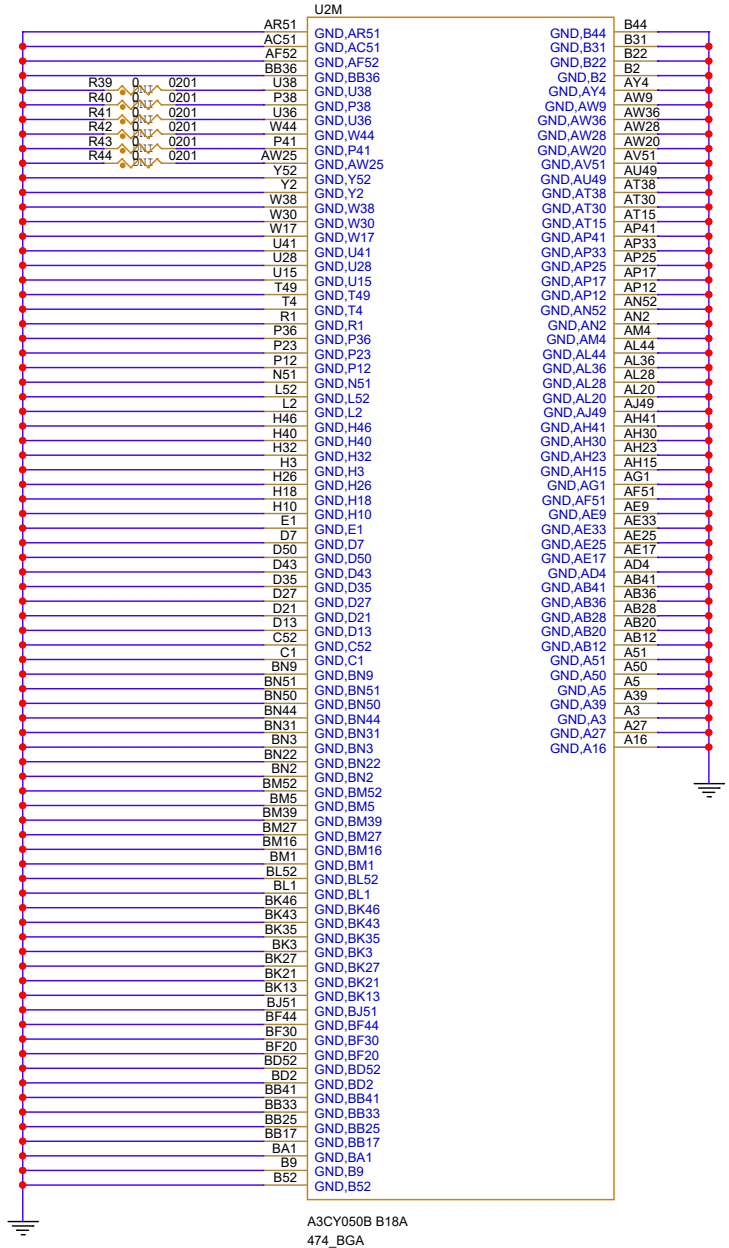


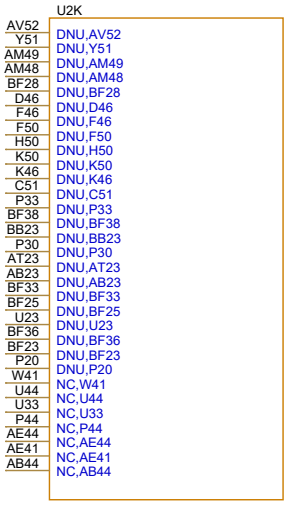






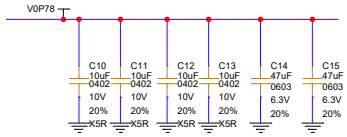
<OrgName> <OrgAddr1>		Title: FPGA POWER SUPPLY TEST POINT		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	C	01
Review	<Engineer Name>	Sheet 12	Number of Sheets	25



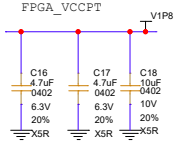


<OrgName> <OrgAddr1>		Title: FPGA Ground & NC		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	B	01
Review	<Engineer Name>	Sheet 13	Number of Sheets	25

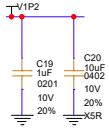
FPGA_VCC_VCCP



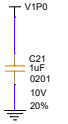
FPGA_VCCPT



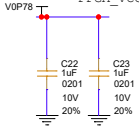
FPGA_VCCRCORE



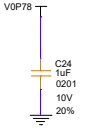
FPGA_VCCH_SDM



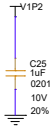
FPGA_VCCL_SDM



FPGA_VCC_IO_SDM



FPGA_VCCIO_PIO_SDM



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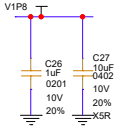
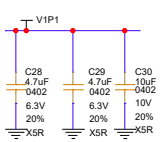
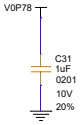


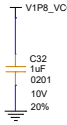
FPGA_VCCIO_PIO_3A



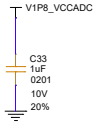
FPGA_VCCPLLDIG_SDM



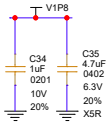
V1P8_VCCADC



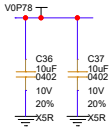
V1P8_VCCADC



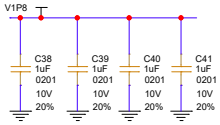
FPGA_VCCFUSEWR_SDM



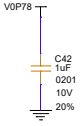
FPGA_VCC_HSSI_L1



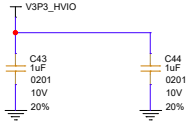
FPGA_VCCPT_HVIO



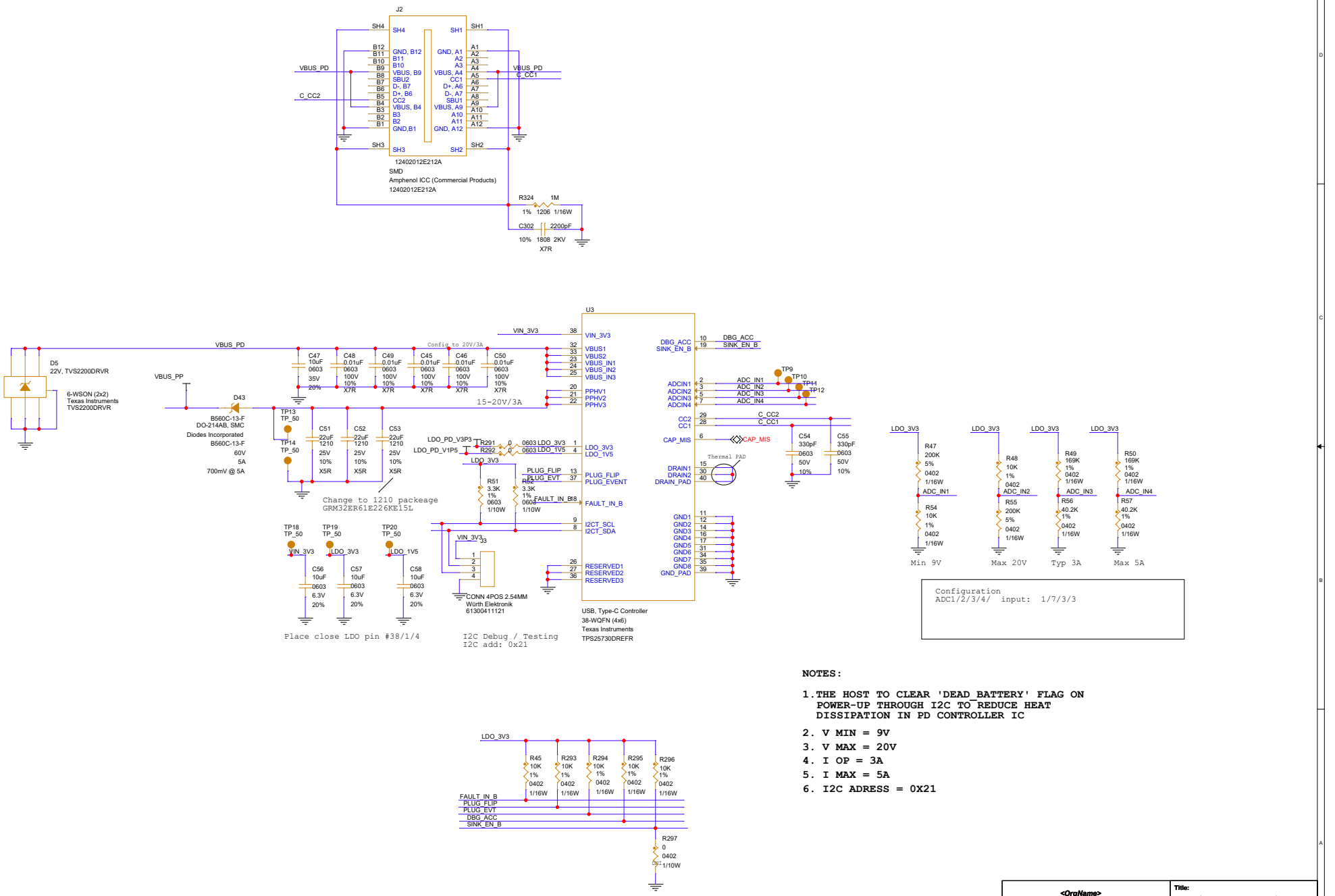
FPGA_VCCL_SDM



FPGA_VCCIO_HVIO



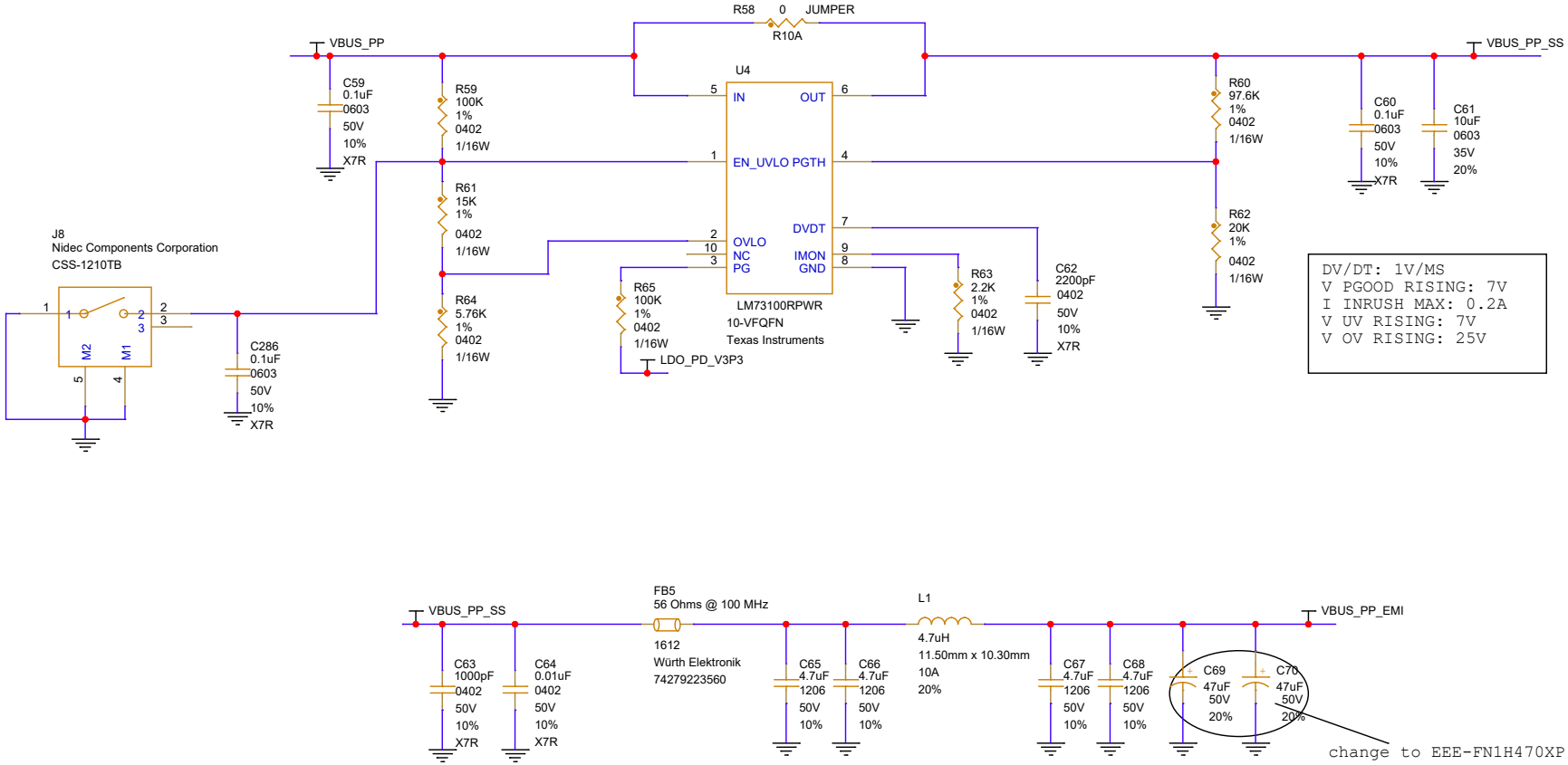
<OrgName> <OrgAddr1>		Title: FPGA DECAP		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	C	01
Review	<Engineer Name>	Sheet 14	Number of Sheets	25



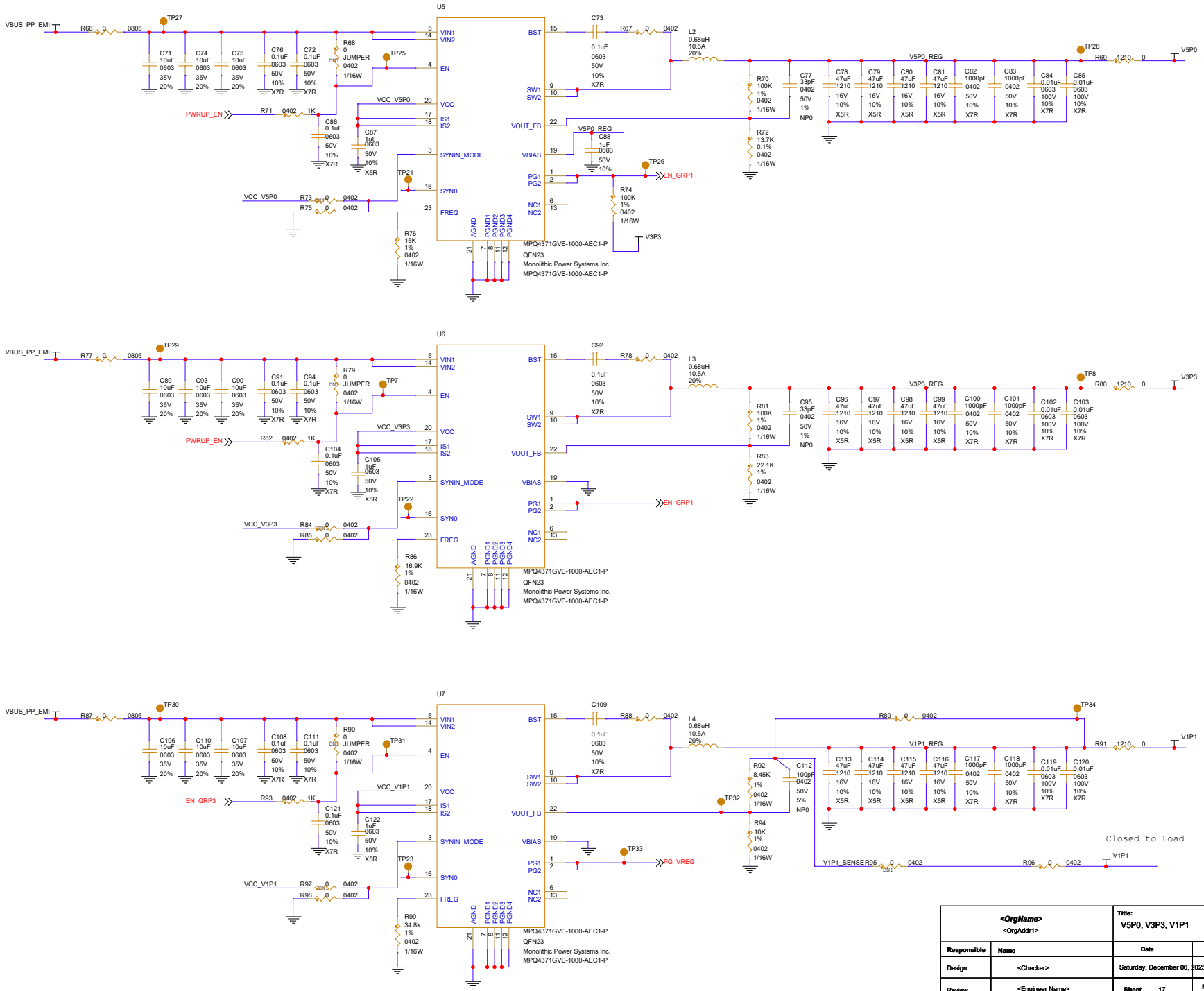
NOTES:

1. THE HOST TO CLEAR 'DEAD_BATTERY' FLAG ON POWER-UP THROUGH I2C TO REDUCE HEAT DISSIPATION IN PD CONTROLLER IC
2. V MIN = 9V
3. V MAX = 20V
4. I OP = 3A
5. I MAX = 5A
6. I2C ADRESS = 0X21

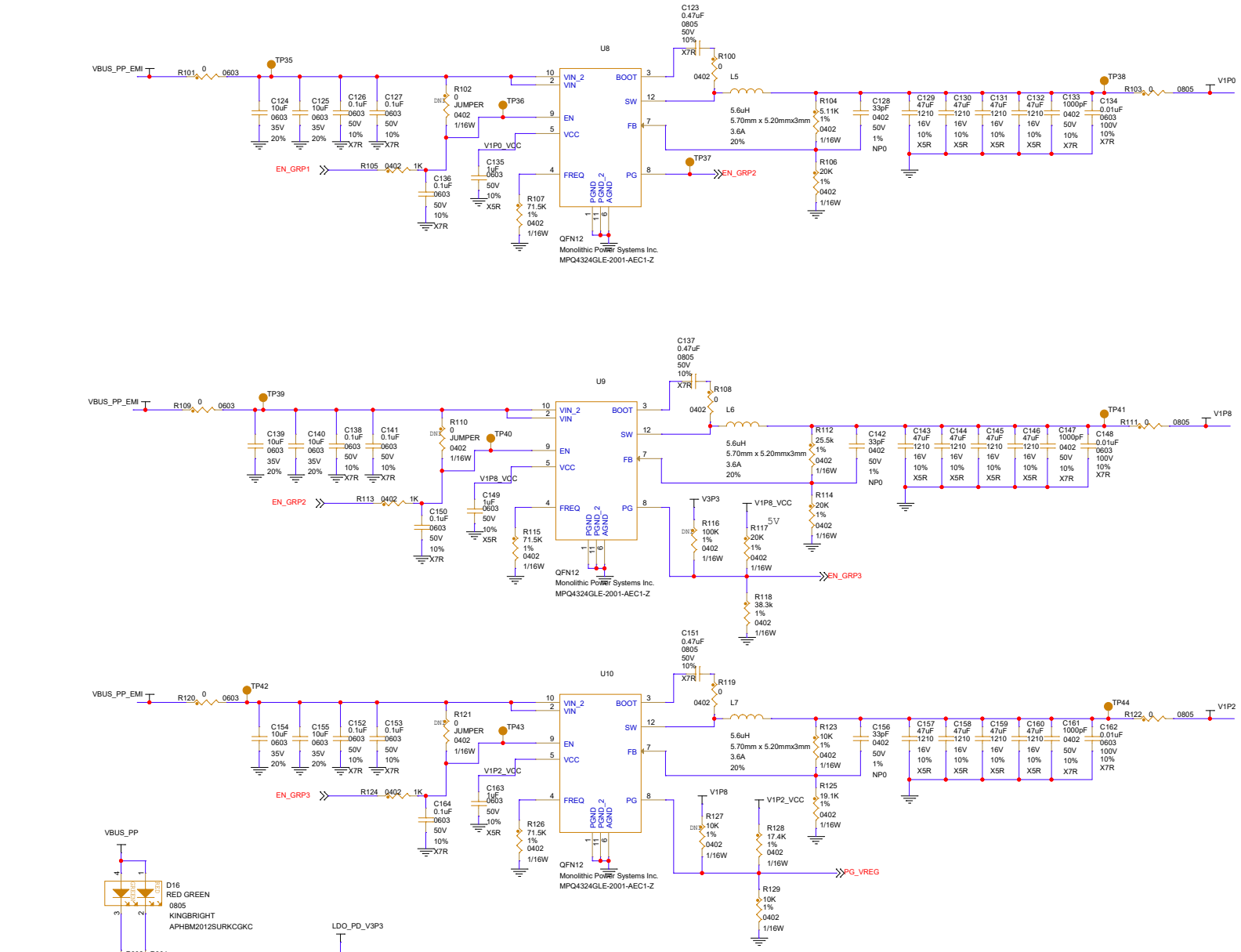
<OrgName> <OrgAddr1>		Title: Type C, PD controller, VBUS_PP		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	C	01
Review	<Engineer Name>	Sheet 15	Number of Sheets	25



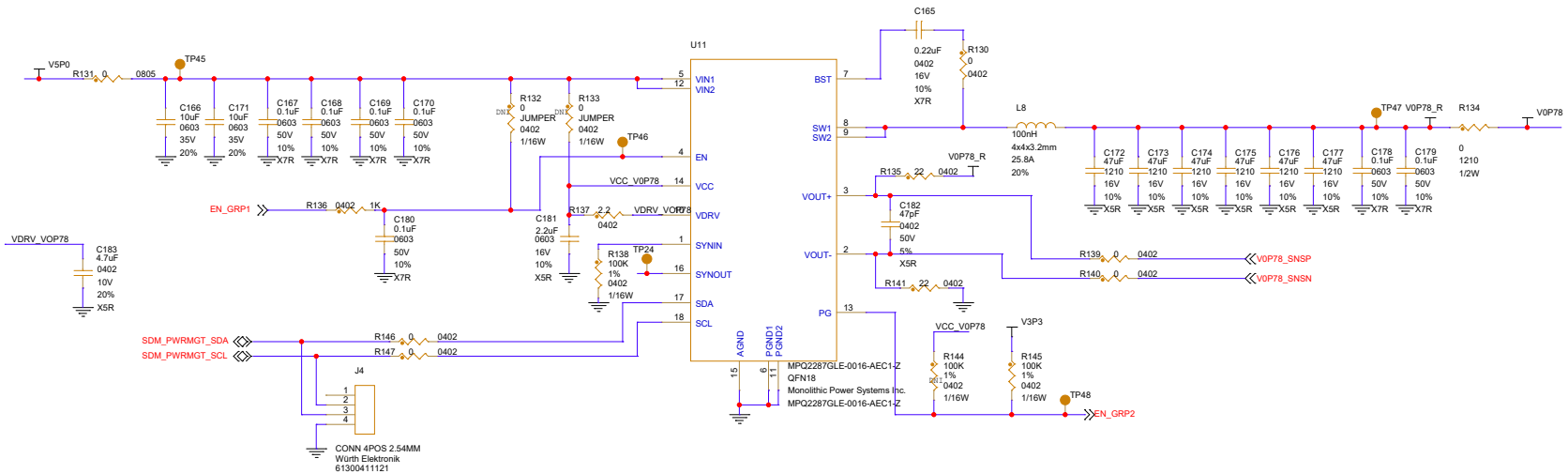
<OrgName> <OrgAddr1>		Title: Irush Protection, EMI Fillter		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	B	01
Review	<Engineer Name>	Sheet 16	Number of Sheets	25



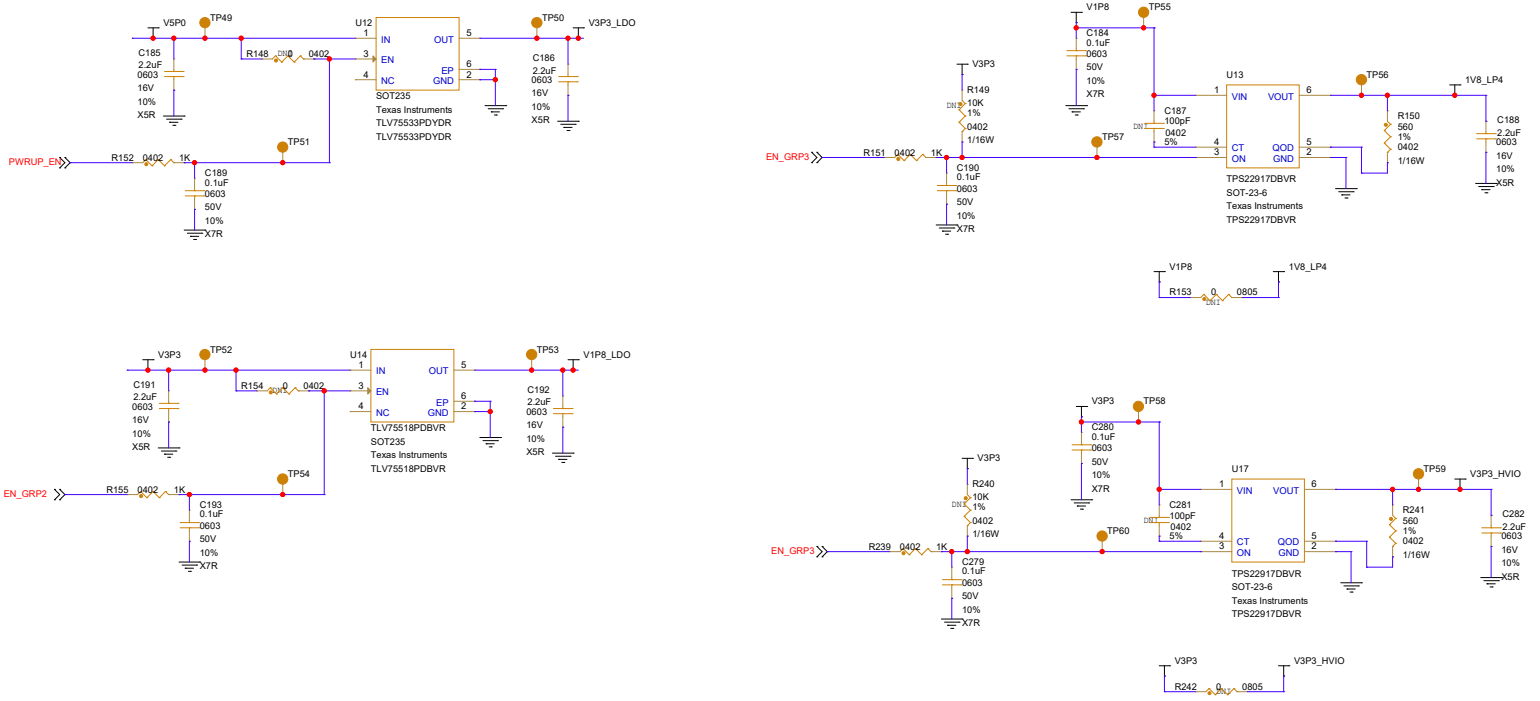
<OrgName> <OrgAddr1>		Title: V5P0, V3P3, V1P1		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	C	01
Review	<Engineer Name>	Sheet 17	Number of Sheets	25



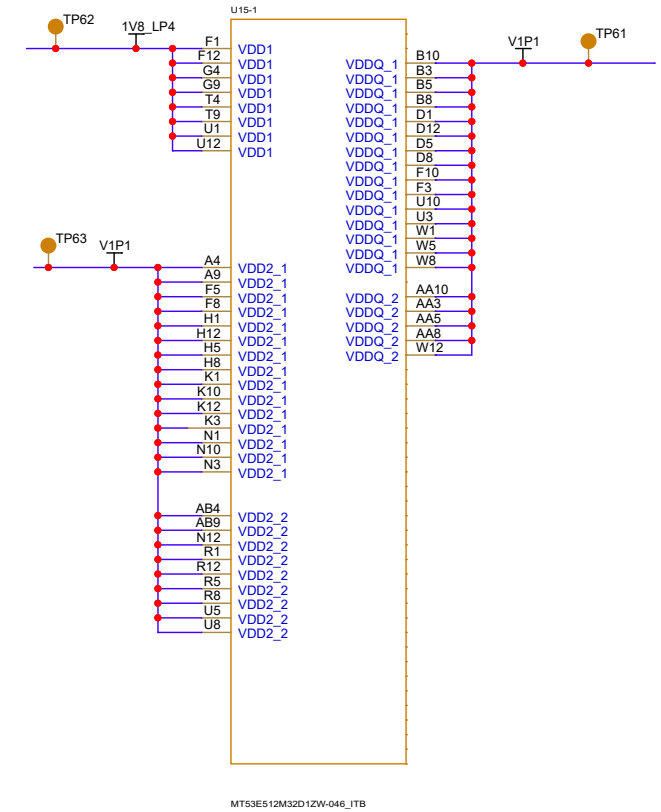
<OrgName> <OrgAddr1>		Title: V1P0, V1P2, V1P8		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	C	01
Review	<Engineer Name>	Sheet 18	Number of Sheets	25

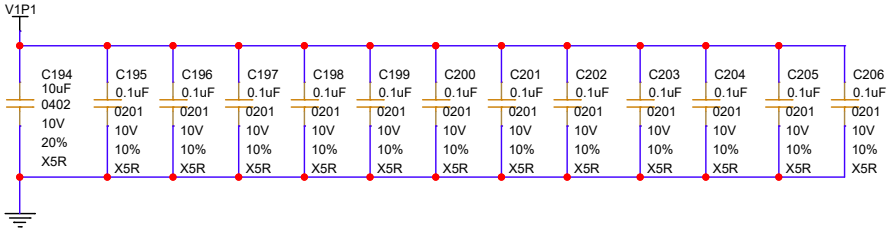


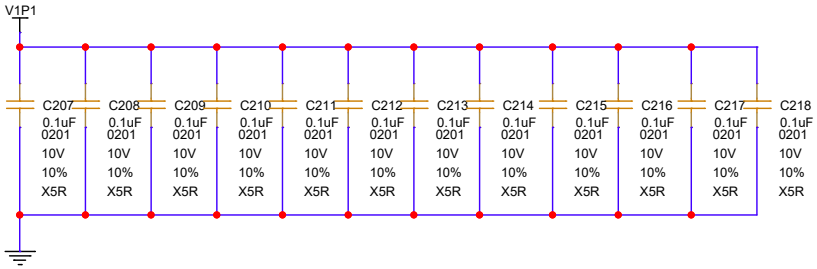
<OrgName> <OrgAddr1>		Title: V0P78		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	C	01
Review	<Engineer Name>	Sheet 19	Number of Sheets	25

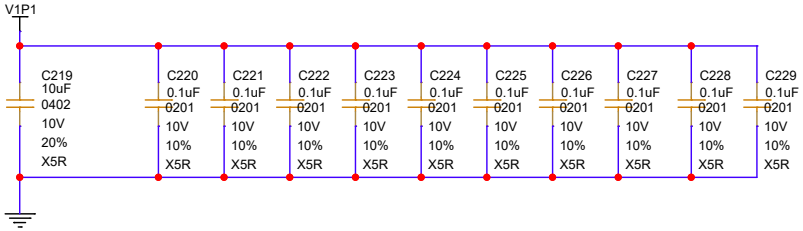


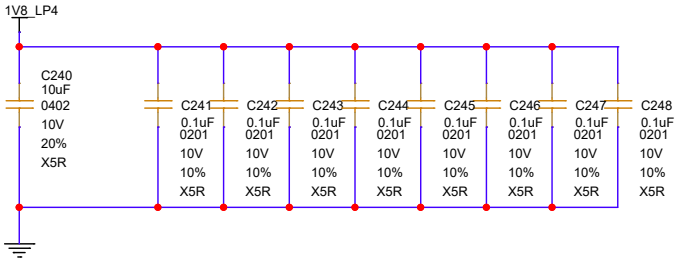
<OrgName> <OrgAddr1>		Title: LDO, Load SW		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	C	01
Review	<Engineer Name>	Sheet 20	Number of Sheets	25

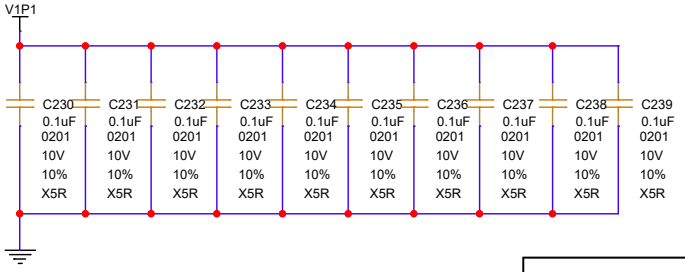




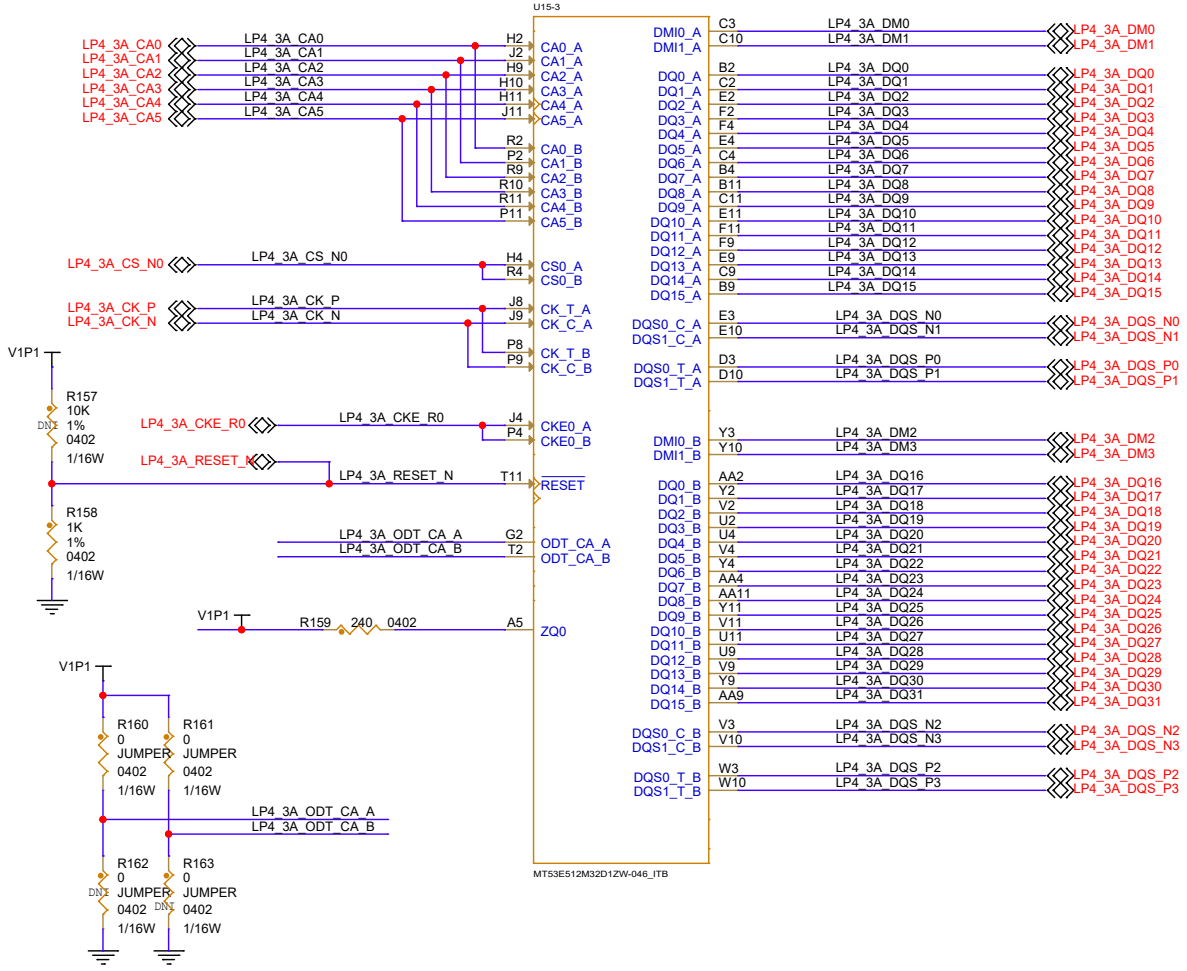


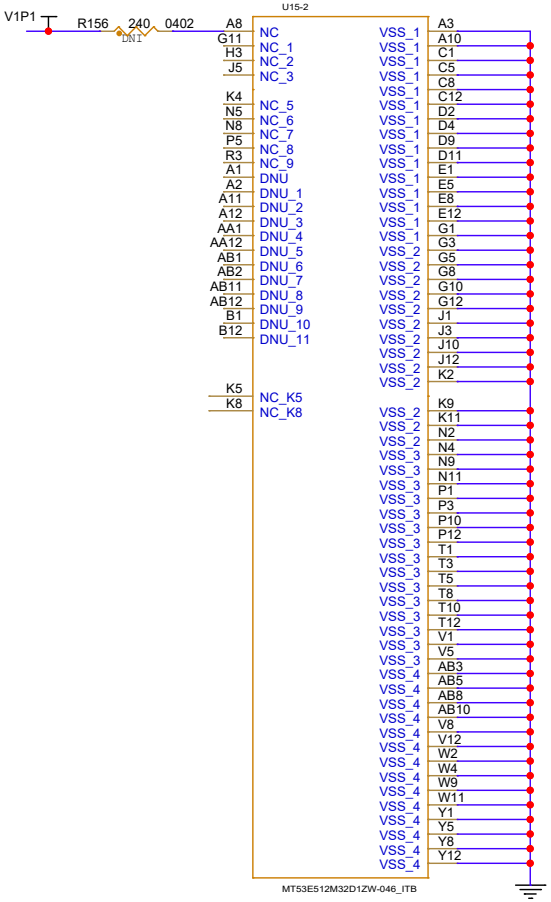




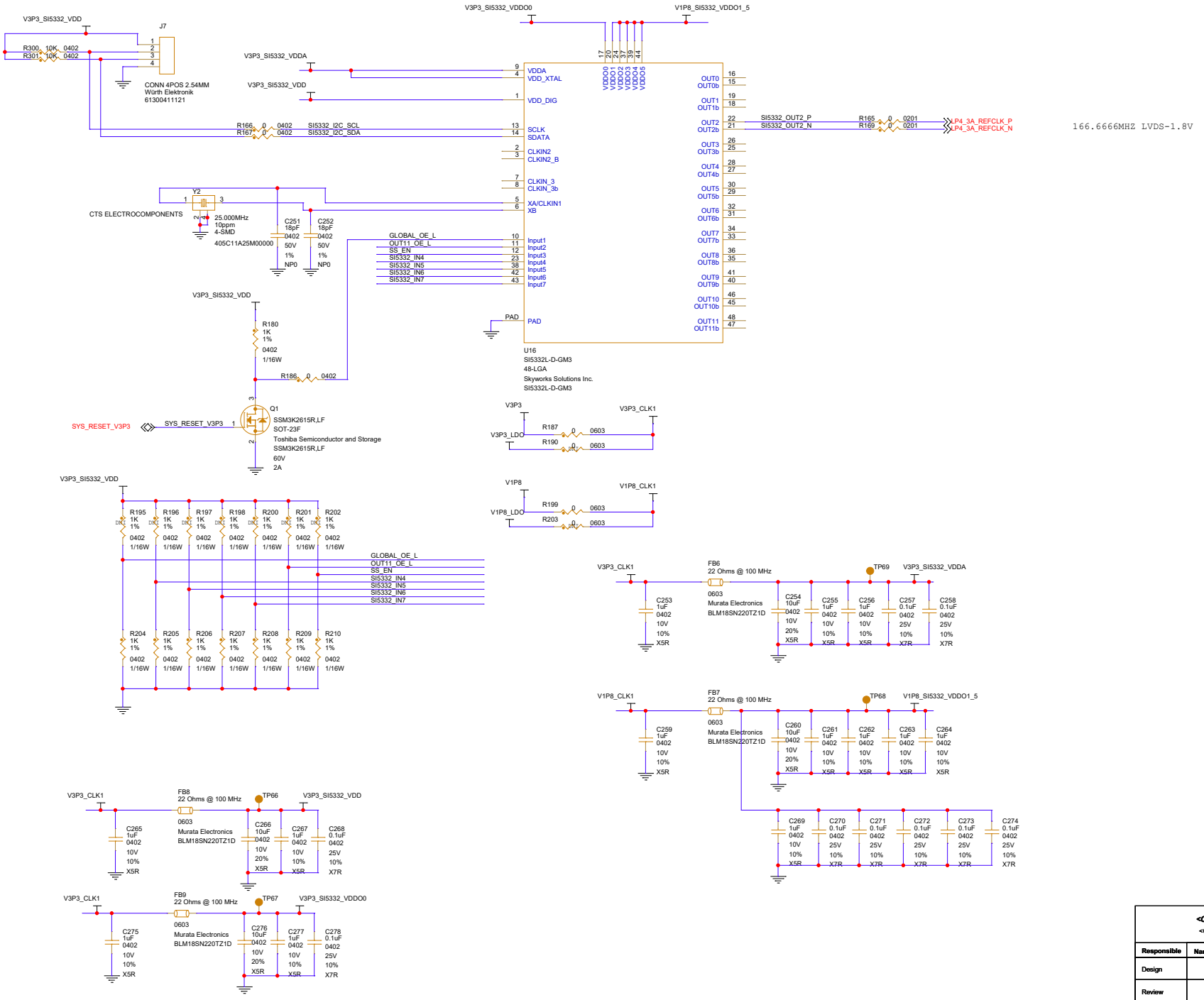


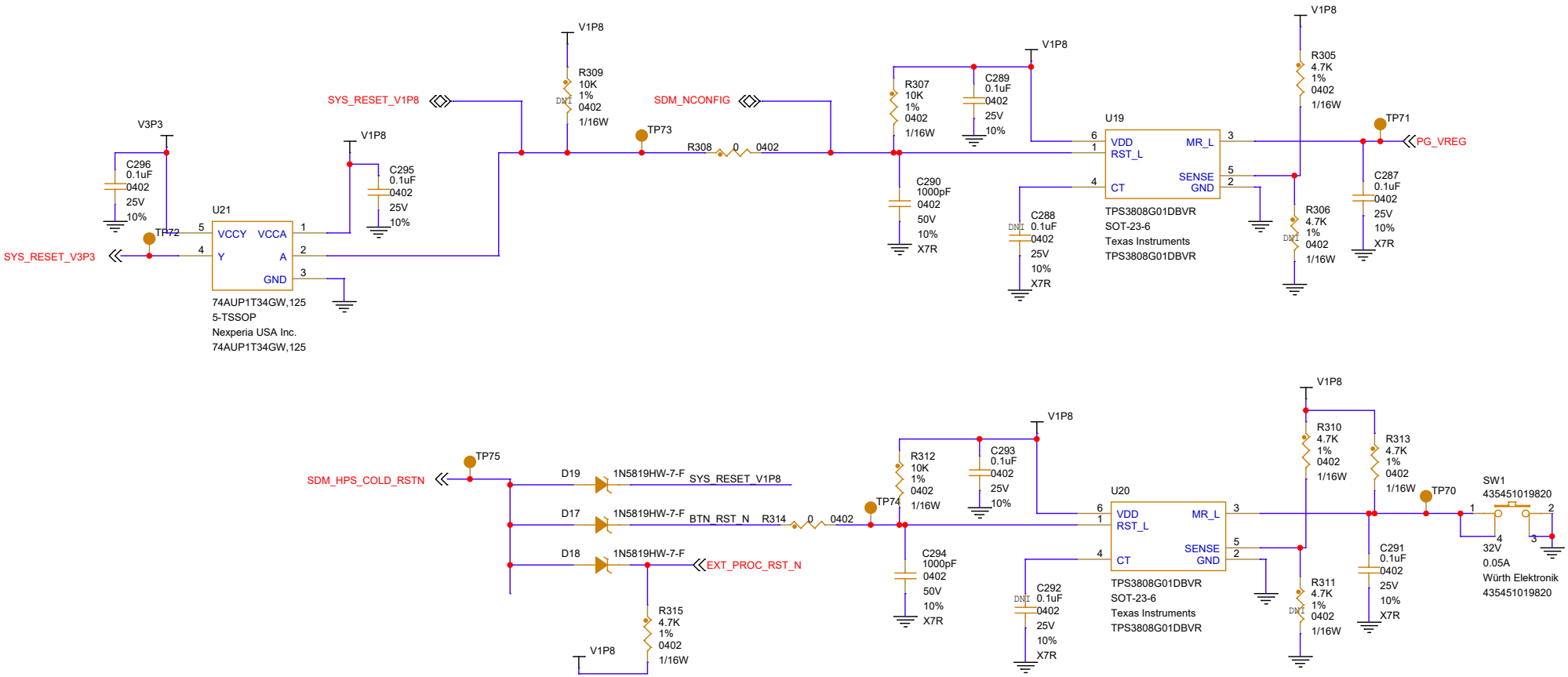
<OrgName> <OrgAddr1>		Title: LPDDR4_ Power		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	B	01
Review	<Engineer Name>	Sheet 21	Number of Sheets	25



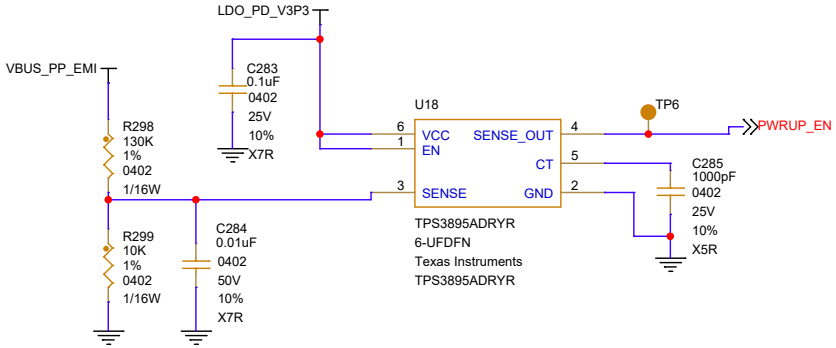


<OrgName> <OrgAddr1>		Title: LPDDR4 IO		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	B	01
Review	<Engineer Name>	Sheet 22	Number of Sheets	25


V3P3_SI5332_VDD
J7
R300 10K 0402
R301 10K 0402
CONN 4POS 2.54MM
Würth Elektronik
61300411121
V3P3_SI5332_VDDO0
V1P8_SI5332_VDDO1_5
V3P3_SI5332_VDDA
V3P3_SI5332_VDD
R166 0 0402 SI5332_I2C_SCL
R167 0 0402 SI5332_I2C_SDA
VDDA
VDD_XTAL
VDD_DIG
SCLK
SDATA
CLKIN2
CLKIN2_B
CLKIN_3
CLKIN_3b
XA/CLKIN1
XB
PAD
OUT0 OUT0b
OUT1 OUT1b
OUT2 OUT2b
OUT3 OUT3b
OUT4 OUT4b
OUT5 OUT5b
OUT6 OUT6b
OUT7 OUT7b
OUT8 OUT8b
OUT9 OUT9b
OUT10 OUT10b
OUT11 OUT11b
SI5332_OUT2_P
SI5332_OUT2_N
R165 0 0201
R169 0 0201
LP4_3A_REFCLK_P
LP4_3A_REFCLK_N
166.6666MHZ LVDS-1.8V
Y2
CTS ELECTROCOMPONENTS
25.000MHz
10ppm
4-SMD
405C11A25M00000
C251 18pF 0402 50V 1% NP0
C252 18pF 0402 50V 1% NP0
GLOBAL_OE_L
OUT11_OE_L
SS_EN
SI5332_IN4
SI5332_IN5
SI5332_IN6
SI5332_IN7
Input1
Input2
Input3
Input4
Input5
Input6
Input7
U16
SI5332L-D-GM3
48-LGA
Skyworks Solutions Inc.
SI5332L-D-GM3
R180 1K 1% 0402 1/16W
R186 0 0402
Q1
SSM3K2615R_LF
SOT-23F
Toshiba Semiconductor and Storage
SSM3K2615R_LF
60V
2A
SYS_RESET_V3P3
V3P3
V3P3_LDO
V3P3_CLK1
R187 0 0603
R190 0 0603
V1P8
V1P8_LDO
V1P8_CLK1
R199 0 0603
R203 0 0603
R195 R196 R197 R198 R200 R201 R202 1K 1% 0402 1/16W
R204 R205 R206 R207 R208 R209 R210 1K 1% 0402 1/16W
FB6
22 Ohms @ 100 MHz
0603
Murata Electronics
BLM18SN220TZ1D
TP69
C253 1uF 0402 10V 10% X5R
C254 10uF 0402 10V 20% X5R
C255 1uF 0402 10V 10% X5R
C256 1uF 0402 10V 10% X5R
C257 0.1uF 0402 25V 10% X7R
C258 0.1uF 0402 25V 10% X7R
FB7
22 Ohms @ 100 MHz
TP68
C259 1uF 0402 10V 10% X5R
C260 10uF 0402 10V 20% X5R
C261 1uF 0402 10V 10% X5R
C262 1uF 0402 10V 10% X5R
C263 1uF 0402 10V 10% X5R
C264 1uF 0402 10V 10% X5R
C269 1uF 0402 10V 10% X5R
C270 0.1uF 0402 25V 10% X7R
C271 0.1uF 0402 25V 10% X7R
C272 0.1uF 0402 25V 10% X7R
C273 0.1uF 0402 25V 10% X7R
C274 0.1uF 0402 25V 10% X7R
FB8
22 Ohms @ 100 MHz
TP66
C265 1uF 0402 10V 10% X5R
C266 10uF 0402 10V 20% X5R
C267 1uF 0402 10V 10% X5R
C268 0.1uF 0402 25V 10% X7R
FB9
22 Ohms @ 100 MHz
TP67
C275 1uF 0402 10V 10% X5R
C276 10uF 0402 10V 20% X5R
C277 1uF 0402 10V 10% X5R
C278 0.1uF 0402 25V 10% X7R
<OrgName>
<OrgAddr1>
Title:
CLock
Responsible
Name
Date
Size
Rev
Design
<Checker>
Saturday, December 06, 2025
C
01
Review
<Engineer Name>
Sheet 23
Number of Sheets 25



<OrgName> <OrgAddr1>		Title: RESET		
Responsible	Name	Date	Size	Rev
Design	<Checker>	Saturday, December 06, 2025	B	01
Review	<Engineer Name>	Sheet 24	Number of Sheets	25



<OrgName> <OrgAddr1>		Title: Power sequence		
Responsible	**Name**	**Date**	**Size**	**Rev**
Design	<Checker>	Saturday, December 06, 2025	B	01
Review	<Engineer Name>	**Sheet** 25	**Number of Sheets**	25