variant_NUCLEO_F446ZE.cpp  const PinName digitalPin[] = {		Do Not Use		IX SPI/other		En Flt 10 Signal	ıke		Track A	Track B	Track C	Frack D	Track E	Track F	Track G	Track H	Track 9	Track 10	D0/D1 UART6	D52/D53 U-2	D47/D48 U-5	Nrf24	Ethernet	SDA SCL	na	
•				SPI,	S			notes	Tra	Tra	Tra	8	D23	D4,	Ž,	Eth	SD/	Open								
F446ZE		128	64 3	2 16	8	4 2	2 1	2023-09-23								_				4						
PG_9, //D0	0		1			_										-			0	-						
PG_14, //D1	1			1			-									_			1	-						
PF_15, //D2	2					1		4/2								-	_			-					2	
PE_13, //D3	3				_	1		pwm1/3								_	3			-						
PF_14, //D4	4					1				-						_		4		4						
PE_11, //D5	5					_	1	pwm1/2		5						4		_		4						
PE_9, //D6	6						1	pwm1/1								_	_	6		4						
PF_13, //D7	7					1	-	no pwm								_	7	_		-						
PF_12, //D8	8					1		no pwm								-		8		-						
PD_15, //D9	9						1	pwm4/4									9			_						
PD_14, //D10	10						1	pwm4/3	10							_				4						
PA_7, //D11/A10	11				1	_		F429ZI Ethernet conflict								_		118		_			11			
PA_6, //D12/A11	12				1	_ 1		pwm2/1								_	12			4						
PA_5, //D13/A12	13				1	1		pwm3/1								_		13		4						
PB_9, //D14	14	1			_		-	SDA	_							_				4				14		
PB_8, //D15	15	1				1	+	SCL	1			_		_		$\dashv$				_				15		
PC_6, //D16	16					1	+	CDIO ACCO	16			_		_		$\dashv$				_						
PB_15, //D17	17			1			+	SPI2_MOSI				_		_		$\dashv$				_		17		Щ		
PB_13, //D18	18					1	+	CDIO CC	-					_		_		-		_			PB13	5		
PB_12, //D19	19			1		_	$\perp \downarrow$	SPI2_CS								_				_		19				
PA_15, //D20	20					1	$\square$		20							_				_						
PC_7, //D21	21					1		pwm3/2	21							_		_		_						
PB_5, //D22	22					1				22						_				_						
PB_3, //D23	23					1		pwm2/2		23																
PA_4, //D24/A13	24				1		$\perp \perp$		24 A1											_[						
PB_4, //D25	25					1	$\perp \downarrow$			25																
PB_6, //D26	26					1	$\perp \downarrow$				26															
PB_2, //D27	27					1					27															
PD_13, //D28	28						1	pwm4/2			28															
PD_12, //D29	29						1	pwm4/1				29														
PD_11, //D30	30					1						30														
PE_2, //D31	31					x																	?			31 change for v2
PA_0, //D32/A14	32				1										F	۱14										
PB_0, //D33/A18 - LED_GREEN	33							??																	33	LED
PE_0, //D34	34					1								34		П				П						
PB_11, //D35	35					1	L	pwm2/4						35												
PB_10, //D36	36					1	L	pwm2/3					36													
PE_15, //D37	37					1								37												
PE_14, //D38	38						1	pwm1/4					38													
PE_12, //D39	39					1							39													
PE_10, //D40	40					1							40													
PE_7, //D41	41		1																						41	Tx7or5
PE_8, //D42	42			1																					42	Rx7or5
PC_8, //D43	43					1		pwm3/3			43															
PC_9, //D44	44					1	L	pwm3/4				44														
PC_10, //D45	45			1																					45	Tx4
PC_11, //D46	46		1																						46	Rx4
PC_12, //D47	47			1			$\Box$													_	47					- RS485
PD_2, //D48	48		1				$\sqcap$													1	48					- RS485
PG_2, //D49	49					1	$\sqcap$					49								1						49 use instead
PG_3, //D50	50					1	П													1		50				50 of PE2
PD_7, //D51	51					1	$\sqcap$													1	51					- RS485
PD_6, //D52	52		1				$\sqcap$													52						
PD_5, //D53	53			1			П												_	53						
PD_4, //D54	54					1	П													1		54				
PD_3, //D55	55			1			П	SPI2_SCK												1		55				
PE_2, //D56	56	1					$\Box$									1				1						also D31 - fix in v2
PE_4, //D57	57				$\Box$	1	$\Box$		1						57	_				1						
PE_5, //D58	58				$\Box$		1	pwm9/1	1					58		_				1						
PE_6, //D59	59						1	pwm9/2	1					_	59	$\neg$				1						
PE_3, //D60	60					1		· ·	1						60	1				1						
PF_8, //D61/A15	61				1	+	1	pwm13/1	1						_	61				1						
PF_7, //D62/A16	62	1					П	pwm11/1 - DCC signal								$\neg$				1						
PF_9, //D63/A17	63	_			1	+	1	pwm14/1	1							1				1		t	im14	4		
PG_1, //D64	64					1		not pwm	1					_	64	$\dashv$				1						
	65				+	_ 1		not pwm	1			1		_		65		_		$\dashv$						
PG 0. //D65	66					1	$\forall$		1							66				1						
PG_0, //D65 PD 1. //D66		-				1	+		1							67				1						
PD_1, //D66			$\perp$	-	+	-	+	Clock ?	1			-		-		~′		+		$\dashv$						
PD_1, //D66 PD_0, //D67	67	1					1		_	-					_	-				_						
PD_1, //D66 PD_0, //D67 PF_0, //D68	67 68	1					1 1	Clock ?												- 1						
PD_1, //D66 PD_0, //D67 PF_0, //D68 PF_1, //D69	67 68 69	1				1	+	Clock ?				_				$\dashv$				$\dashv$						
PD_1, //D66 PD_0, //D67 PF_0, //D68 PF_1, //D69 PF_2, //D70	67 68 69 70	1				1																				also D11
PD_1, //D66 PD_0, //D67 PF_0, //D68 PF_1, //D69 PF_2, //D70 PA_7, //D71	67 68 69 70 71	1				1		NC																		also D11
PD_1, //D66 PD_0, //D67 PF_0, //D68 PF_1, //D69 PF_2, //D70 PA_7, //D71 NC, //D72	67 68 69 70 71 72	1				1																				also D11
PD_1, //D66 PD_0, //D67 PF_0, //D68 PF_1, //D69 PF_2, //D70 PA_7, //D71	67 68 69 70 71	1				1		NC																		also D11

variant_NUCLEO_F446ZE.cpp  const PinName digitalPin[] = {		Do Not Use			SPI/other	CS CI #1.0	lal la	ke			Track A	Frack B	Track C	Track D	Track E	Track F	Track G	Frack H	Track 9	Track 10	D0/D1 UART6	D52/D53 U-2	D47/D48 U-5	24	Ethernet	SDA SCL	C C	
<b>.</b>		۵	ž	ř	SPI/	S F	Signal	Brake	notes	i	Tra	9	D27	D47	Nrf24	EH	SDA	Open										
PD_9, //D76 - Serial Rx	76																											
PD_8, //D77 - Serial Tx	77																											
PA_3, //D78/A0	78					1													A0									
PC_0, //D79/A1	79					1														A1								
PC_3, //D80/A2	80					1							A2															
PF_3, //D81/A3	81					1									А3													
PF_5, //D82/A4	82					1										A4						T						
PF_10, //D83/A5	83					1											A5					1						
PB_1, //D84/A6	84					1						A6										T						
PC_2, //D85/A7	85				1	1			SPI2_	MISO												1		Α7				
PF_4, //D86/A8	86					1								A8								1						
PF_6, //D87/A9	87					1																1						
PA_1, //D88/A19	88					1																T			PA1			
PA_2, //D89/A20	89					1																T			PA2			
PA 8, //D90	90																											
PA_9, //D91	91																					T						
PA 10, //D92	92																											
PA_11, //D93	93								RMII	pins Table 11												1						
PA_12, //D94	94								PA1	RMII Reference Clock		-		7								1						
PA_13, //D95	95								PA2	RMII MDIO				1								7						
PA 14, //D96	96				1				PC1	RMII MDC		-										7						
PC_1, //D97/A21	97					1			PA7	RMII RX Data Valid		D11										_			PC1			
PC_4, //D98/A22	98					1			PC4	RMII RXD0		-										_		_	PC4			
PC 5, //D99/A23	99					1			PC5	RMII RXD1		-		1								7			PC5			
PC 14, //D100	100					Ī			PG11	RMII TX Enable		-										1			-			
PC_15, //D101	101								PG13	RXII TXD0		-		+								_						
PD_10, //D102	102				$\dashv$	+	+		PB13	RMII TXD1	12	S_A_	CK	+								$\dashv$						
PE_1, //D103	103				$\dashv$	+			1013	KWIII TADT	12	.~_^_'										$\dashv$						_
PF_11, //D104	104				1	+																$\dashv$						
PG 4, //D105	105				1	+	+															$\dashv$						
PG_5, //D106	106				$\dashv$	+																$\dashv$						
PG 6, //D107	107				$\dashv$	+	+															+						
PG_7, //D108	108				1	+																$\dashv$						
PG_8, //D109	109					+																$\dashv$						
PG_10, //D110	110				+	+	+											-				$\dashv$				$\dashv$		
PG 11, //D111	111				+	+	+											-				$\dashv$			G11	$\dashv$		
PG 12, //D112	112				$\dashv$	+																$\dashv$		- 1	511			
PG_13, //D113	113				+	+	+															$\dashv$		С	G13			
PG_15, //D114	114					+	+															$\dashv$			213			
PH_0, //D115	115				+	+	+															$\dashv$						
PH_0, //D115 PH 1 //D116	116	-			+	+	+	-										-	-			$\dashv$		-	-	_		
LII_T \\DIIO	110				4	_						5								6		2		6				