# Analog Circuits, Sensor Readout and Conversion

### Design of a 2-stage OPAMP

Design bias voltages, currents and W/L values of the 2-stage OPAMP depicted in Fig. 1 in order to satisfy the provided specifications.

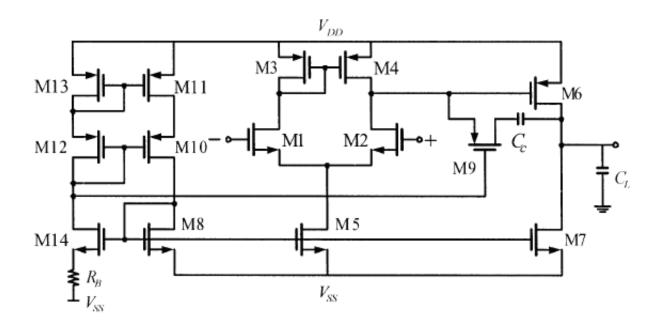


Figure 1: Op-Amp CMOS 2 stadi

• Use the following MOSFET models:

```
.model NMOD1CAP
                 NMOS LEVEL=1
                                           .model PMOD1CAP
                                                            PMOS LEVEL=1
+ vto = 0.71
                 gamma = 0.01
                                           + vto = -0.901
                                                             gamma = 0.01
                                           + phi = 0.6
+ phi = 0.6
                kp = 182e - 6
                                                             kp = 41.5e - 6
+ lambda = 0.01
                                           + lambda = 0.01
+ tox = 9.6e-9
                                           + tox = 9.6e-9
+ cj = 350e-6 cjsw = 120e-12
                                           + cj = 350e-6 cjsw = 120e-12
+ pb = 0.8 mj = 0.33 mjsw = 0.33
                                          + pb = 0.8 mj = 0.33 mjsw = 0.33
+ cgso = 0.046e-9 cgdo = 0.046e-9
                                           + cgso = 0.046e-9 cgdo = 0.046e-9
```

#### SPECS

$V_{DD}/V_{SS}$	2.5/-2.5 V
Slew Rate	$+5/$ -5 V $/\mu$ s
Load Capacitor $C_L$	5pF
max Vin Common Mode	2.1V
min Vin Common Mode	-1.3V
max Vout	2.2V
min Vout	-2.2V
Gain Bandwidth	5MHz
Differential Gain	>80dB
Phase Margin	>60°

ullet The specification related to Noise is student-dependent. Find the value of the input-referred noise voltage (Sn(f)) specification by looking at the following table, where N is the last digit of the student badge number

E.g. Mr. James Bond (badge number 007) will select  $\sqrt{Sn(f)}=\sqrt{\overline{v_{iN}^2}/\Delta f}<36~{\rm nV}/\sqrt{Hz}.$ 

### Noise

N	0	1	2	3	4
$\sqrt{Sn(f)} \; [{ m nV}/\sqrt{Hz}]$	22	24	26	28	30
	_	_	_	_	_
N	5	6	1	8	9

• in addition, try to minimize power consumption.

## Additional instructions and report template

- The report should be prepared with the following template:
  - 1. Page 1: Name, badge number, related specs, circuit schematic and table with with the transistors' sizing defined in the design process by the student.
  - 2. Pages 2 and 3: description of the design procedure.
  - 3. Page 4 and following: SPICE plots (Bode plots, transient analysis, etc. . . ).
  - 4. Last page: table which compares the requested specs with the achieved circuit performance.
- Drop an email to: "I.demarchi@unibo.it" attaching the report (pdf), and all the SPICE files (schematics, netlists, libraries) which have been used in the simulations.
- The project task should be done autonomously.
- The project report should be delivered to the instructor one week before the scheduled oral examination.