# HIGH-VOLTAGE MIXED-SIGNAL IC

# UC1611s

160COM x 256SEG Matrix LCD Controller-Driver w/ 16-shade per pixel



MP Specifications Revision 1.0

June 11, 2008





# **TABLE OF CONTENT**

INTRODUCTION	3
ORDERING INFORMATION	4
BLOCK DIAGRAM	5
PIN DESCRIPTION	6
RECOMMENDED COG LAYOUT	10
CONTROL REGISTERS	11
COMMAND TABLE	14
COMMAND DESCRIPTIONS	16
LCD VOLTAGE SETTING	28
V <sub>LCD</sub> QUICK REFERENCE	29
LCD DISPLAY CONTROLS	31
HOST INTERFACE	34
DISPLAY DATA RAM	45
WINDOW PROGRAM	46
RESET & POWER MANAGEMENT	49
MULTI-TIME PROGRAM NV MEMORY	51
MTP OPERATION FOR LCM MAKERS	52
SAMPLE COMMAND SEQUENCES	56
ESD CONSIDERATION	57
ABSOLUTE MAXIMUM RATINGS	58
SPECIFICATIONS	59
AC CHARACTERISTICS	60
PHYSICAL DIMENSIONS	68
ALIGNMENT MARK INFORMATION	69
PAD COORDINATES	70
TRAY INFORMATION	76
REVISION HISTORY	77

# **UC1611s**

Single-Chip, Ultra-Low Power 160COM x 256SEG Matrix Passive LCD Controller-Driver

#### INTRODUCTION

UC1611s is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

UC1611s employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture and LRM (Line Rate Modulation) gray-shade modulation scheme to achieve near crosstalk free images, with well balanced gray shades.

In addition to low power SEG and COM drivers, UC1611s contains all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation, and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

#### MAIN APPLICATIONS

 Cellular Phones, Smart Phones, PDA, and other battery-operated palmtop devices and/or portable instruments.

#### **FEATURE HIGHLIGHTS**

- Single-chip controller-driver supports 160x256 STN LCD, 16-shade-per-pixel with gamma compensated modulation.
- Soft-ICON: Partial scroll function to support programmable graphics ICON or scroll bar.
- Support both row ordered and column ordered display buffer RAM access

- Support industry standard 4-wire, 3-wire, and 2-wire serial buses (S8, S9, I<sup>2</sup>C), and 16- /8- /4-bit parallel buses (8080 or 6800).
- Special driver structure and gray shade modulation scheme produce near crosstalk free image, with low power consumption for all display patterns.
- Fully programmable Mux Rate, partial display window, Bias Ratio, and Line Rate allow many flexible power management options.
- 4 software programmable frame rates (25Hz, 30Hz, 35Hz, and 40Hz). Support the use of fast Liquid Crystal material for speedy LCD response.
- 4 software-programmable temperature compensation coefficients.
- On-chip Power-ON Reset and Software RESET command make RST pin optional.
- Self-configuring 11x charge pump with on-chip pumping capacitor requires only 5 external capacitors to operate.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.

V<sub>DD</sub> (digital) range (Typ.): 1.8 V ~ 3.3V
 V<sub>DD</sub> (analog) range (Typ.): 2.8 V ~ 3.3V
 LCD V<sub>OP</sub> range: 5.65V ~ 17.5V

Available in gold bump dies

Bump pitch: 38 μM (Typ.) Bump gap: 13 μM (Typ.) Bump surface: 1887.5 μM<sup>2</sup>



#### **ORDERING INFORMATION**

High-Voltage Mixed-Signal IC

Product ID	Description
UC1611sGAA	Gold bumped die.

#### **General Notes**

#### **APPLICATION INFORMATION**

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

#### BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers. UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and quality their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

#### USE OF I2C

The implementation of I<sup>2</sup>C is already included and tested in all silicon.

#### MTP LIGHT & ESD SENSITIVITY

The MTP memory cell is sensitive to photon excitation and ESD. Under extended exposure to strong ambient light, or when TST4 pin is exposed to ESD strikes, the MTP cells can lose its content before the specified memory retention time span. The system designer is advised to provide proper light & ESD shields to realize full MTP content retention performance.

#### LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

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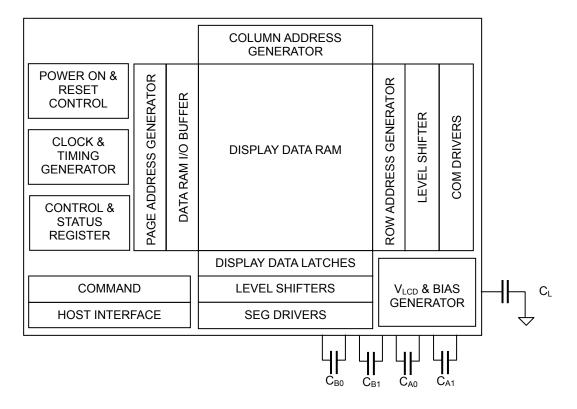
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#### **BLOCK DIAGRAM**





## **PIN DESCRIPTION**

Name	Туре	Pins	Description
			Main Power Supply
V <sub>DD</sub> V <sub>DD2</sub> V <sub>DD3</sub>	PWR	11 10 4	$V_{DD2}/V_{DD3}$ is the analog power supply and it should be connected to the same power source. $V_{DD}$ is the digital power supply and it should be connected to a voltage source that is no higher than $V_{DD2}/V_{DD3}$ . Please maintain the following relationship: $V_{DD}+1.5~V~\geqslant~V_{DD2/3}~\geqslant~V_{DD}$ Minimize the trace resistance for $V_{DD}$ and $V_{DD2}/V_{DD3}$ .
V <sub>SS</sub> V <sub>SS2</sub>	GND	11 11	Ground. Connect $V_{SS}$ and $V_{SS2}$ to the shared GND pin. Minimize the trace resistance for $V_{SS}$ and $V_{SS2}$ .
			LCD Power Supply
V <sub>A0+</sub> , V <sub>A0-</sub> V <sub>A1+</sub> , V <sub>A1-</sub> V <sub>B0+</sub> , V <sub>B0-</sub> V <sub>B1+</sub> , V <sub>B1-</sub>	$V_{A1+, V_{B1-}}$ PWR 4		LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of $C_{AX}$ / $C_{BX}$ value between $V_{AX+}$ / $V_{BX+}$ and $V_{AX-}$ / $V_{BX-}$ , respectively. The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace
			resistance is critical in achieving high quality image.
V <sub>LCD-IN</sub> V <sub>LCD-OUT</sub>	PWR	2 2	High voltage LCD Power Supply. Connect these pins together. A bypass capacitor $C_L$ should be connected between $V_{LCD}$ and $V_{SS}$ . Keep the trace resistance under 30 $\Omega$ ~ 50 $\Omega$ .

#### Note:

Recommended capacitor values:

C<sub>B</sub>:  $100\sim250$  x LCD load capacitance or 5  $\mu$ F (5V), whichever is higher. C<sub>L</sub>:  $0.1\mu$ F  $\sim0.5$   $\mu$ F (25V) is appropriate for most applications.

Name	Туре	Pins		D	escription	_								
			Ho	ST INTERFACE										
				Bus Mode: The interface bus mode is determined by BM[1:0] and D[15, 13] with the following relationship:										
			BM[1:0]	DB15, DB13	Mode									
				00	Data	8080/16-bit								
			01	Data	6800/16-bit									
5144 6			10	00	8080/8-bit									
BM1~0	I	2	11	00	6800/8-bit									
			10	01	8080/4-bit									
			11	01	6800/4-bit									
			10	10	4-wire SPI (S8)									
			11	10	3-wire SPI (S9)									
			11	11	2-wire SPI (I <sup>2</sup> C)									
CS1/A3 CS0/A2	Ι	2			when CS1="H" and CS0 = "L". be high impedance.	When the								
DOT			When RST="L", states.	all control registe	ers are re-initialized with their o	default								
RST	I	1			n-chip. There is no need for $\epsilon$ d, connect the pin to $V_{\text{DD}}$ .	external RC								
CD	I	1		odes, CD pin is n	ection for read/write operation. not used, connect CD pin to $V_S$ ": Display data	s.								
WR0		1	WR[1:0] controls Interface section		peration of the host interface.	See Host								
WR1	I	l 1 1		080 mode. In ser	ng depends on whether the int ial interface modes, these two									



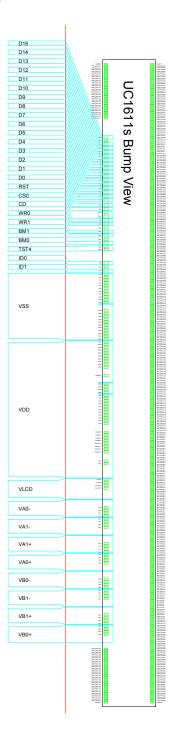
Name	Туре	Pins						De	scri	ptic	on						
			Bi-directional bus for parallel host interface. In serial modes, connect D[0] to SCK, D[3] to SDA, and D[15, 13] to $V_{DD}$ or $V_{SS}$ .												D[0]		
			D15	D14	D13	D12	D11	D10	D9	D8 C	7 D6	D5 D4	D3	D2 [	D1	D0	
			16-bit (BM=0x)	DB[15:0]													
	D15~D0 I/O 16		8-bit (BM=1x)	0	-	0	-	_	-	_	-		Γ	DB[7:0	)]		
D15~D0		4-bit (BM=1x)	0	-	1	-	_	-	_		-   -			DB[3	3:0]		
				S8/S9 (BM=1x)	1	-	0	-	-	-	-		-   -		SDA	. –	- S
			I <sup>2</sup> C (BM=11)	1	-	1	-	_	-	-		-   -		SDA	. –	- S	CK
			Connect unused pins to $V_{SS}$ or $V_{DD}$ . For connection details, refer to the table in the <i>Host Interface</i> section.														
ID0	I	1	Production cor the Get Stat													ien ι	using
ID1	1	1		EG selection. Window commands will adjust its upper bound of column													

Name	Туре	Pins	Description
			HIGH VOLTAGE LCD DRIVER OUTPUT
SEG1 ~ SEG256	HV	256	SEG (column) driver outputs. Support up to 256 columns. Leave unused drivers open-circuit.
COM1~ COM160	HV	160	COM (row) driver outputs. Support up to 160 rows. Leave unused drivers open-circuit.
			Misc. Pins
V <sub>DDX</sub>	0	5	Auxiliary $V_{DD}$ . These pins are connected to the main $V_{DD}$ bus on chip. They are provided to facilitate chip configurations in COG application. These pins should not be used to provide $V_{DD}$ power to the chip. It is not necessary to connect $V_{DDX}$ to main $V_{DD}$ externally.
TST4	I/HV	2	TST4 controls test mode and is also used to supply one of the high voltage required for MTP Program operation. Leave TST4 open during normal LCD operation. In COG applications keep TST4 trace resistance between 30 $\Omega$ ~ 50 $\Omega$ .
TST2 TST1	I/O	1 1	Test I/O pins. Leave these pins open during normal use.
Dummy		13	Dummy pins are <u>NOT</u> connected inside the IC.

**Note:** Several control registers will specify "0-based index" for COM and SEG electrodes. In those situations,  $COM_{\underline{X}}$  or  $SEG_{\underline{X}}$  will correspond to index  $\underline{X}$ -1, and the value ranges for those index registers will be 0~159 for COM and 0~255 for SEG.



## RECOMMENDED COG LAYOUT



#### Note for $V_{DD}$ and $V_{SS}$ with COG:

The operation condition,  $V_{DD}$ =1.8V (typical), should be satisfied under all operating conditions. UC1611s' peak current ( $I_{DD}$ ) can be up to ~15mA during high speed data-write to UC1611s' on-chip SRAM. Such high pulsing current mandates very careful design of  $V_{DD}$  and  $V_{SS}$  ITO trances in COG modules. When  $V_{DD}$  and  $V_{SS}$  trace resistance is not low enough, the pulsing  $I_{DD}$  current can cause the actual on-chip  $V_{DD}$  to drop to below 1.65V and cause the IC to malfunction.

#### **CONTROL REGISTERS**

UC1611s contains registers that control the chip operation. These registers can be modified by commands. The following table is a summary of the control registers, their meaning and their default value. Commands supported by UC1611s will be described in the next two sections. A summary table comes first and then followed by a detailed instruction-by-instruction description.

Name: The symbolic reference of the register.

Note that, some symbol names refer to bits (flags) within another register.

Default: Numbers shown in Bold font are default values after Power-Up-Reset and System-Reset.

Name	Bits	Default	Description
SL	8	00H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value are between 0 (for no scrolling) and (159 – FL). Setting SL outside of this range causes undefined effect on the displayed image.
FL	4	OH	Fixed lines. The first (FLx2) lines of each frame are fixed and are not affected by scrolling (SL). When FL is non-zero, the screen is effectively separated into two regions: one scrollable, one non-scrollable.
CA	8	00H	Display Data RAM Column Address (Used in Host to Display Data RAM access)
PA	7	00H	Display Data RAM Page Address (Used in Host for Display Data RAM access)  When DC[5:3] = 100b, PA[6:5] : used to select Write Pattern 0~3. PA[4:0] : set SRAM page address
BR	2	2H	Bias Ratio. The ratio between V <sub>LCD</sub> and V <sub>BIAS</sub> . 00b: 5 01b: 10 10b: 11 11b: 12
TC	2	0H	Temperature Compensation (per °C). <b>00b: -0.05%</b> 01b: -0.10% 10b: -0.15% 11b: 0.00%
PM	8	EAH	Electronic Potentiometer to fine tune V <sub>BIAS</sub> and V <sub>LCD</sub>
РМО	6	00H	PM offset. the effective PM value, PMV = PM - PMO[4:0] when PMO[5]=1 the effective PM value, PMV = PM + PMO[4:0] when PMO[5]=0
PC	4	FH	Pump Control.  PC[1:0]: Panel Loading  00b: LCD: ≤33nF  11b: 33nF ≤ LCD≤55nF  PC[3:2]: Pump Control  00b: External V <sub>LCD</sub> 11b: Internal V <sub>LCD</sub> (11x charge pump)  (Setting to 01 or 10 will be invalid and default value will be used instead.)
AC	4	1H	Address Control:  AC[0]: WA: Automatic column/page Wrap Around (Default 1:ON)  AC[1]: Auto-Increment order  0: Column (CA) first  1: Page (PA) first  AC[2]: PID: PA (page address) auto increment direction (0:+1, 1:-1)  AC[3]: Window Program Mode  0: Inside Mode: Write to SRAM within the window defined by (WPC0,WPP0), (WPC1,WPP1)  1: Outside Mode: Write to SRAM but skip the window defined by (WPC0,WPP0), (WPC1,WPP1)



Name	Bits	Default		Descript	ion									
DC	8	18H	Display Control: DC[0]: PXV: Pixels Inver DC[1]: APO: All Pixels O DC[2]: Display ON/OFF DC[4:3]: Gray-shade Mo 00: On/Off mode 10: 4-shade Mode DC[5]: Input Type of On/ 0: 4-bit per 1-pixe DC[7:6]: Display Pattern 00: Pattern0 10: Pattern2	N (Default 0:OFI (Default 0:OFF) dulation mode. 01: 8 11: 1 Off Mode (enable 1 1: 1- Selection (enable 01: F	B-shade Moo B-shade me e only when bit per 1-pix	de <b>ode</b> DC[4:3]=0 <sup>i</sup> el	0b)							
LC	10	020H	LCD Control:  LC[0]: MSF: MSB First mapping Option (Default: 0:0FF)  LC[1]: MX, Mirror X. SEG/Column sequence inversion (Default: 0:0FF)  LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: 0:0FF)  LC[3]: Enable FL lines in partial display mode.(Default: 0:0FF)  LC[5:4]: Line Rate (= Frame-Rate x Mux-Rate)											
				LC[5:4]=00b	01b	10b	11b							
			16-shade	20.0 Klps	24.0	28.0	32.0							
			8-shade	14.1	16.9	19.7	22.5							
			4-shade	13.3	16.0	18.7	21.4							
			On/Off mode	5.9	7.1	8.2	9.4							
			LC[7:6] : Reserved (Det LC[9:8] : Partial Display <b>0xb: Disable</b> 11b: Enabled		+1 (DST a	nd DEN are	er-second ) e not used.)							
NIV	7	00H	N-Line Inversion NIV[5:0] : <b>000000b : Di</b> NIV[6] : <b>0b: no-XOR</b>	sable N-line Inv										
CEN DST DEN	8 8 8	9FH 00H 9FH	COM scanning ENd (the Display STart (the first Display EDd (the last CC Please maintain the follo CEN = (the actual n CEN ≥ DEN ≥ DS	COM with active so wing relationship umber of pixel ro	scan pulse, an pulse, 0- o:	0-based ir based inde	idex)							
ISOF	4	1H	Set the ISOlation clock in	r Front of COM p	oulse.									
ISOB	4	0H	Set the ISOlation clock in	n Back of COM p	ulse.									
WPC0	8	00H	Window program starting	g column address	s. Value ran	ge: 0 ~255.								
WPP0	6	00H	Window program starting When DC[5:3]=100b, val	•	alue range:	0~79.								
WPC1	8	FFH	Window program ending	column address	. Value rang	je: 0~255.								
WPP1	6	4FH	Window program ending When DC[5:3]=100b, val		llue range: (	)~79.								

Name	Bits	Default	Description
MTPC	5	10H	MTP Programming Control:  MTPC[2:0]: MTP command  000: Idle 001: Read 010: Erase 011: Program 1xx: For UltraChip debug use only  MTPC[3]: MTP Enable (automatically cleared after each MTP command)  MTPC[4]: Ignore/Use MTP. 0: Ignore 1: Use
MTPM	6	00H	MTP Write Mask
			0: no action 1: program
APC	1	N/A	Advanced Product Configuration. For UltraChip only. Please do not use.
			Status Registers
ОМ	2	1	Operating Modes (Read Only) 00b: Reset 01b: (Not used) 10b: Sleep 11b: Normal
MD	1	. 1	MTP option flag. 0 : for non-MTP version. 1 : for MTP version
MS	1	-	MTP programming in-progress
WS	1	_	MTP Operation Succeeded



# **COMMAND TABLE**

The following list of host commands is supported by UC1611s

0: Control 1: Data 0: Write cycle 1: Read cycle W/R:

Effective Data bits

Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default	
1.	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A	
2.	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A	
				Ver	MX	MY	WA	DE	WS	MD	MS	•		
3.	Get Status	0	1	ID[′	[0:1			PMO[5:0]				Get Status	N/A	
				Product Code				0 0 0 EF			EF			
4.	Set Column Addr. LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0	
4.	Set Column Addr. MSB	0	0	0	0	0	1	#	#	#	#	Set CA[7:4]	0	
5.	Temp. Compensation.	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b: -0.05%/°C	
6.	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC [1:0]	11b: 33~55 nF	
7.	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC [3:2]	11b	
8.	Set Adv. Program Control	0	0	0	0	1	1	0	0	R	R	Set APC[R][7:0]	N/A	
0.	(double-byte command)	Ů	U	#	#	#	#	#	#	#	#	R = 0~3	IN/A	
9.	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0	
٥.	Set Scroll Line MSB	Ŭ	U	0	1	0	1	#	#	#	#	Set SL[7:4]	0	
10.	Set Page Address LSB	0	0	0	1	1	0	#	#	#	#	Set PA[3:0]	0	
10.	Set Page Address MSB	Ľ	Ů	0	1	1	1	0	#	#	#	Set PA[6:4]	0	
11.	Set Potentiometer	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	PM=EAH	
ļ	(double-byte command)	Ľ		#	#	#	#	#	#	#	#		=,	
				1	0	0	0	0	0	1	0			
12.	Set Isolation Clock Front	0	0	0	0	0	1	0	0	1	1	Set ISOF[3:0]	1H	
				-	-	-	-	#	#	#	#			
				1	0	0	0	0	0	1	0			
13.	Set Isolation Clock Back	0	0	0	0	0	1	0	1	0	0	Set ISOB[3:0]	0H	
				-	-	-	-	#	#	#	#			
	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[9:8]	00b: Disable	
15.	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b	
16.	Set Fixed Lines	0	0	1	0	0	1	#	#	#	#	Set FL[3:0]	0	
17.	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[5:4]	10b:28klps	
18.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0	
19.	. ,	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0	
20.	. ,	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b	
21.	Set LCD Mapping Control	0	0	1	1	0	0	0	0	0	0	Set LC[3:0]	0	
-	(double-byte command)			0	0	0	0	#	#	#	#			
22.	Set N-line Inversion (double-byte command)	0	0	1	1	0	0	1	0	0	0	Set NIV[6:0]	00H	
00	• •	_	_	-	#	#	#	#	#	#	#	0-4-0017-51	0001-	
23.	. ,	0	0	1	1	0	1	0	#	#	#	Set DC[7:5]	000b	
24.	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A	
25.	NOP	0	0	1	1	1	0	0	0	1 -	1 T	No operation	N/A	
26.	Set test control	0	0	1 4	1 4	1 4	0	0	1 4	T		For testing only.	N/A	
27	(double-byte command)	0	0	#	#	#	#	#	#	#	#	Do not use.	10h: 44	
27.	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	10b: 11	
28.	Set COM End	0	0	1 #	1 #	1 #	1 #	0 #	0 #	0 #	1 #	Set CEN[7:0]	159	
-	0 ( 0 ( 10 )	0	0	1	1	1	1	0	0	1	0	0.100777.63		
29.	Set Partial Display Start	ő	ő	#	#	#	#	#	#	#	#	Set DST[7:0]	0	
30	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[7:0]	159	
50.	Cott artial Display Life	0	0	#	#	#	#	#	#	#	#	OCC DENT.0]	100	

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Actio	n	Default
31.	Set Window Program Starting Column Address	0	0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	0 #		Set WPC0	0
32.	Set Window Program Starting Row Address	0	0	1 -	1 -	1 #	1 #	0 #	1 #	0 #	1 #	Shared with MTP	Set WPP0	0
33.	Set Window Program Ending Column Address	0	0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	0 #	Commands	Set WPC1	255
34.	Set Window Program Ending Column Address	0	0	1 -	1 -	1 #	1 #	0 #	1 #	1 #	1 #		Set WPP1	79
35.	Window Program Mode	0	0	1	1	1	1	1	0	0	#	Set AC	[3]	0:Inside
36.	Set MTP Operation Control	0	0	1 -	0	1 #	1 #	1 #	0 #	0 #	0 #	Set MTP	C[5:0]	10H
37.	Set MTP Write Mask	0	0	1 -	0	1 #	1 #	1 #	0 #	0 #	1 #	Set MTPI	M[5:0]	0
38.	Set V <sub>MTP1</sub> Potentiometer	0	0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	0 #		Set MTP1	N/A
39.	Set V <sub>MTP2</sub> Potentiometer	0	0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #	Shared with Window	Set MTP2	N/A
40.	Set MTP Write Timer	0	0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	0 #	Program Commands	Set MTP3	N/A
41.	Set MTP Read Timer	0	0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set MTP4	N/A
	9	ERIAL	REAL	Сом	MAND	(ENA	BLE IN	<b>S8</b> 0	R <b>S9</b> I	Bus N	IODES	ONLY)		
		0	0	1	1	1	1	1	1	1	0			
42.	2. Get Status		1	Ver MX MY WA ID[1:0]				DE WS MD MS PMO[5:0]			Get Status Disab		N/A	
$\bot$				Р	roduc	t Cod	е	0	0	0	EF			

#### Notes:

- All bit patterns other than commands listed above may result in undefined behavior.
- Commands (38)~(41) are shared with commands (31)~(34), and have exactly the same code.
   When MTPC[3]=0, commands (37)~(41) are interpreted as Window Programming commands.
   When MTPC[3]=1, they are MTP Control commands.
- MTPM and PM are actually the same register. Only one of the commands (36) is valid at any time, and it is determined by MTPC[3].
- After MTP-ERASE or MTP-PROGRAM operation, please always perform the following steps,
  - a) Disconnect TST4 power source.
  - b) Do a full  $V_{DD}$  ON-OFF cycle (make sure  $V_{DD}$  drops below 50mV). before resuming normal operation.



#### **COMMAND DESCRIPTIONS**

#### (1) WRITE DATA TO DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1 0 8-bit Data-Write to SRAM							M		

#### (2) READ DATA FROM DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1		8-b	it Dat	a-Rea	ad fro	m SR	AM	

Write/Read Data Byte (command 1, 2) operation accesses display buffer RAM based on Page Address (PA) register and Column Address (CA) register. To minimize bus interface cycles, PA and CA will increase or decrease automatically after each bus cycle, depending on the setting of Access Control (AC) register. PA and CA can also be programmed directly by issuing Set Page Address and Set Column Address commands.

If  $\underline{W}$ rap- $\underline{A}$ round (WA) is OFF (AC[0] = 0), CA will stop increasing after reaching the end of page, and system programmers need to set the values of PA and CA explicitly. If WA is ON (AC[0]=1), when CA reaches end of page, CA will be reset to 0 and PA will be increased or decreased by 1, depending on the setting of  $\underline{P}$  age  $\underline{I}$  increment  $\underline{D}$  irection (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 79), PA will be wrapped around to the other end of RAM and continue.

For both 8-bit and 16-bit interfaces, the first 1 byte and 2 bytes Read respectively is a dummy Read. Please ignore the data read out.

#### (3) GET STATUS SUMMARY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
			Ver	MX	MY	WA	DE	WS	MD	MS
Get Status	0	1	ID[´	1:0]			PMC	[5:0]		
			Р	roduc	t Coc	le	0	0	0	EF

#### Status 1 definitions:

Ver: Version Code. 1

MX: Status of register LC[1], mirror X.MY: Status of register LC[2], mirror Y.

WA: Status of register AC[0]. Automatic column/row wrap around.

DE: Display enable flag. DE=1 when display is enabled

WS: MTP Command Succeeded

MD: MTP Option (Yes/No)
MS: MTP action status

#### Status 2 definitions:

ID: Connection Status of the ID pin, could be used for production identifying.

PMO[5:0]: PM offset value

#### Status 3 definitions:

Product Code: 1h

EF: ESD Flag. EF=1 when ESD strikes.

If multiple Get Status commands are issued consecutively within one single CD 1\$0\$1 transaction, the Get Status command will return {Status1, Status2, Status3, Status1, Status2, Status3, Status1..} alternately.

#### (4) SET COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	0	0	0	0	CA3	CA2	CA1	CA0
Set Column Address MSB CA[4:7]	0	0	0	0	0	1	CA7	CA6	CA5	CA4

Set the SRAM column address for read/write access.

CA possible value: 0 ~ 255

#### (5) SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Compensation TC[1:0]	0	0	0	0	1	0	0	1	TC1	TC0

Set  $V_{\text{BIAS}}$  Temperature compensation coefficient (%-per-degree-C) for all 4 temperature compensation curves.

Temperature compensation curve definition:

#### (6) SET PANEL LOADING

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	0	0	1	0	1	0	PC1	PC0

Set PC[1:0] according to the capacitance loading of LCD panel.

Panel loading definition:  $00b : LCD \le 33nF$   $11b : 33 nF \le LCD \le 55 nF$ 

#### (7) SET PUMP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC[3:2]	0	0	0	0	1	0	1	1	PC3	PC2

Set PC[3:2] to program the build-in charge pump stages.

00b=External V<sub>LCD</sub> 11b= Internal V<sub>LCD</sub> (11x charge pump)

#### (8) SET ADVANCED PROGRAM CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[R][7:0]	0	0	0	0	1	1	0	0	0	R
(Double byte command)	0	0		AF	C[R]	regis	ter pa	rame	ter	

For UltraChip only. Please do NOT use.



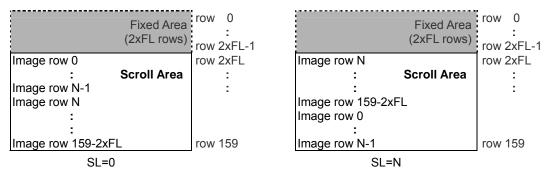
#### (9) SET SCROLL LINE

High-Voltage Mixed-Signal IC

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	0	1	0	0	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[7:4]	0	0	0	1	0	1	SL7	SL6	SL5	SL4

Set the number of lines for scroll area.

The scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and 159-2x(FL) (full scrolling). FL is the register value programmed by the Set Fixed Lines command.



#### (10) SET PAGE ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address LSB PA [3:0]	0	0	0	1	1	0	PA3	PA2	PA1	PA0
Set Page Address MSB PA [6:4]	0	0	0	1	1	1	0	PA6	PA5	PA4

Set SRAM page address for read/write access. UC1611s can store 4 B/W mode pictures in SRAM. Set PA[6:5] to specify which one to store. (Also refer to command "Set Display Mode".)

Possible value = 0 ~ 79

When On/Off mode and DC[5]=1

PA[6:5]: select Write Pattern0(00b) ~ Write Pattern3(11b)

PA[4:0]: set SRAM page address

#### (11) SET POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Potentiometer PM [7:0]	0	0	1	0	0	0	0	0	0	1
(Double-byte command)	0	0				PM[	7:0]			

Program V<sub>BIAS</sub> Potentiometer (PM[7:0]). See section *LCD Voltage Setting* for more detail.

Effective range of PM value = 0 ~ 255 (Default : 234)

#### (12) SET ISOLATION CLOCK FRONT

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
0.11.12.00.15.20.10.05.10.05	0	0	1	0	0	0	0	0	1	0
Set Isolation Clock Front ISOF [3:0] (Triple-byte command)	0	0	0	0	0	1	0	0	1	1
(mple byte comment)	0	0	-	,	,	,		ISOF	[3:0]	

Program isolation clock in front of COM pulse.

Effective range of ISOF value =  $0 \sim 15$  (Default : 1)

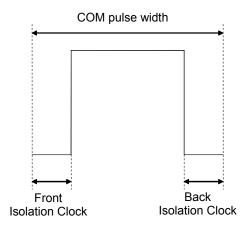
#### (13) SET ISOLATION CLOCK BACK

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Out to dath of our Object Double 100D to 01	0	0	1	0	0	0	0	0	1	0
Set Isolation Clock Back ISOB [3:0] (Triple-byte command)	0	0	0	0	0	1	0	1	0	0
(Triple byte command)	0	0	-	-	•	•		ISOE	3[3:0]	

Program isolation clock in back of COM pulse.

Effective range of ISOB value = 0 ~ 15 (Default : 0)

Note: Use higher V<sub>LCD</sub> when increase isolation clock.



#### (14) SET PARTIAL DISPLAY CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Control LC [9:8]	0	0	1	0	0	0	0	1	LC9	LC8

This command is used to control partial display function.

LC[9:8] : **0xb: Disable Partial Display**, Mux-Rate = CEN+1 (DST and DEN are not used.) 11b: Enable Partial Display, Mux-Rate = DEN-DST+1+LC[3]xFLx2

#### (15) SET RAM ADDRESS CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	1	0	0	0	1	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic column/page wrap around.

- 0: CA or PA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary
- 1: CA or PA (depends on AC[1]= 0 or 1) will restart, and PA or CA will increment by one step.

AC[1]: Auto-Increment order

- 0: column (CA) increases (+1) first until CA reach CA boundary, then PA will increase by (+/-1).
- 1 : page (PA) increases (+/-1) first until PA reach PA boundary, then CA will increase by (+1).

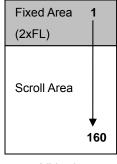
AC[2]: PID, page address (PA) auto increment direction ( $\mathbf{0}/1 = +/-1$ )

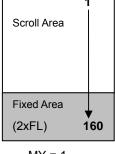
When WA=1 and CA reaches CA boundary(CA=MC), PID controls whether page address will be adjusted by increasing +1 or -1. If WA is 0, the column address will stay in MC value and the page address will stay unchanged.

#### (16) SET FIXED LINES

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines FL [3:0]	0	0	1	0	0	1	FL3	FL2	FL1	FL0

The Fixed Lines function is used to implement the partial scroll function by dividing the screen into scroll and fixed area. The Set Fixed Lines command will define the fixed area, which will not be affected by the SL scroll function. When MY=0, the fixed area covers the top 2xFL rows; when MY=1, the bottom 2xFL rows. One example of the visual effect on LCD is illustrated in the figure below. Default: 0.





MY = 0

MY = 1

#### (17) SET LINE RATE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [5:4]	0	0	1	0	1	0	0	0	LC5	LC4

Program LC [5:4] for line rate setting (Line-Rate = Frame-Rate x Mux-Rate)

In 16-shade mode:	00b : 20.0 Klps	01b : 24.0 Klps	10b : 28.0 Klps	11b : 32.0 Klps
In 8-shade mode:	00b : 14.1 Klps	01b : 16.9 Klps	10b : 19.7 Klps	11b : 22.5 Klps
In 4-shade mode:	00b : 13.3 Klps	01b : 16.0 Klps	10b : 18.7 Klps	11b : 21.4 Klps
In On/Off mode:	00b: 5.9 Klps	01b: 7.1 Klps	10b: 8.2 Klps	11b: 9.4 Klps
(Klps: Kilo-line per se	econd)			

#### (18) SET ALL PIXEL ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	1	0	1	0	0	1	0	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM. Default: **0**.

#### (19) SET INVERSE DISPLAY (PXV)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	1	0	1	0	0	1	1	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM. Default: **0**.

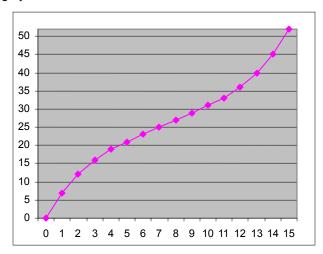
#### (20) SET DISPLAY ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC[4:2]	0	0	1	0	1	0	1	DC4	DC3	DC2

This command is for programming register DC[4:2]. Default: 110b.

When DC[2] is set to **0**, the IC will put itself into Sleep mode. All drivers, voltage generation circuit and timing circuit will be halted to conserve power. When DC[2] is set to 1, UC1611s will first exit from Sleep mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

DC[4:3] controls the gray shade modulation modes. UC1611s has four gray shade modulation modes: an On/Off mode 8-shade mode, 4-shade mode and a 16-shade mode. The modulation curves are shown below. Horizontal axes are the gray shade data. The vertical axes are the ON-OFF ratio.



Effective range:

ive range.										
DC[4:3]		Gray-Scale	D7	D6	D5	D4	D3	D2	D1	D0
00	C[5]=1	B/W Mode	1	0	1	0	1	0	1	0
	C[5]=0	D/W Wode	1				0	-	-	-
			1	1	1		0	0	0	-
01		8-shade	1	1	0		0	0	1	-
01		o-snaue	1	0	1	-	0	1	0	-
			1	0	0	-	0	1	1	-
10		4-shade	1	1			0	0	-	-
10		4-511aue	1	0	-	-	0	1	ı	ı
			1	1	1	1	0	0	0	0
			1	1	1	0	0	0	0	1
			1	1	0	1	0	0	1	0
11		16-shade	1	1	0	0	0	0	1	1
		10-Silaue	1	0	1	1	0	1	0	0
			1	0	1	0	0	1	0	1
			1	0	0	1	0	1	1	0
			1	0	0	0	0	1	1	1
MACE A . DAM	DIE 41 DIE	AL DAMA DIO.OI	חוח	^-						

MSF=0 : RAM\_D[7:4] = B[7:4], RAM\_D[3:0] = B[3:0] MSF=1 : RAM\_D[7:4] = B[3:0], RAM\_D[3:0] = B[7:4]

#### (21) SET LCD MAPPING CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC[3:0]	0	0	1	1	0	0	0	0	0	0
(Double-byte command)	J	U	0	0	0	0	LC3	MY	MX	MSF

Set LC[2:0] for COM (row) mirror (MY), SEG (column) mirror (MX) and MSB first or LSB first options (MSF).

MY is implemented by reversing the mapping order between RAM and COM (row) electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

MX is implemented by selecting the CA or 255-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

MSF is implemented by MSB-LSB swapping. The operation is determined by DC[4:3], as described in Set Gray Scale Mode command below.

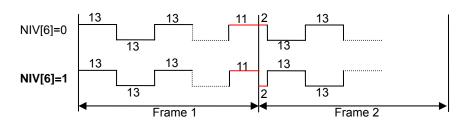
LC[3] controls whether the soft icon section (FL on the top) will be displayed during partial display mode.

#### (22) SET N-LINE INVERSION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set N-line Inversion NIV [6:0]	0	0	1	1	0	0	1	0	0	0
(Double-byte command)	U	U	-			N	IV [6:	0]		

Set N-Line inversion:

NIV[6]: **0b: non-XOR** 1b: XO



#### (23) SET DISPLAY PATTERN

Action	C/D	W/R	D7	D6	D5	D4	D3	D3 D2 D1		D0
Set Display Pattern	0	0	1	1	0	1	0		DC[7:5]	

Set Display Pattern Selection: (enabled only when DC[4:3]=00b)

DC[5]: Input type for On/Off mode

**0 : 4 bits for 1 pixel** 1 : 1 bit for 1 pixel

DC[7:6]: Select Display Pattern (Only enable when On/Off mode and DC[5:3] =100b)

**00 : Pattern0** 01 : Pattern1 10 : Pattern2 11 : Pattern3

UC1611s can store 4 different patterns in SRAM when DC[5:3]=100. Set PA[6:5] and DC[7:6] to select which pattern to store / display, respectively.

#### (24) SYSTEM RESET

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	1	1	1	0	0	0	1	0

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

#### (25) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No operation	0	0	1	1	1	0	0	0	1	1

This command is used for "no operation".

#### (26) SET TEST CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	1	1	1	0	0	1	Т	T
(Double byte command)	0	0			Tes	ting p	aram	eter		

This command is used for UltraChip production testing. For UltraChip only. Please do NOT use.

#### (27) SET LCD BIAS RATIO

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	1	1	1	0	1	0	BR1	BR0

Bias ratio definition: 00b= 5 01b=10 **10b**=11 11b=12

#### (28) SET COM END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN [7:0]	0	0	1	1	1	1	0	0	0	1
(Double byte command)	0	0		C	EN r	egiste	r para	amete	er	

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD.

#### (29) SET DISPLAY START

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST [7:0]	0	0	1	1	1	1	0	0	1	0
(Double byte command)	0	0			OS <i>T</i> re	egiste	r para	amete	er	

This command programs the starting COM electrode, which has been assigned a full scanning period, and which will output active COM scanning pulses.



#### (30) SET DISPLAY END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN [7:0]	0	0	1	1	1	1	0	0	1	1
(Double-byte command)	U	U		E	DEN r	egiste	r para	amete	er	

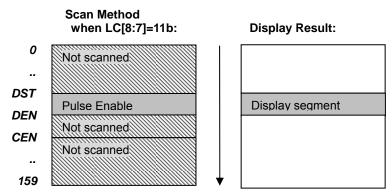
This command programs the ending COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse.

CEN, DST, and DEN are 0-based indexes of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

When LC[8:7]=11b, the Mux-Rate is narrowed down to DST-CEN+1+(LC[3]xFLx2). When MUS rate is reduced, reduce the line rate accordingly to reduce power. Changing MUX rate also require BR and VLCD to be reduced.

For minimum power consumption, set LC[8:7]=11b, set (DST, DEN, FL, CEN) to minimize MUX rate, use slowest line rate which satisfies the flicker requirement, use On/Off mode, set PC[1:0]=00b, disable N-line Inversion, and use lowest BR, lowest VLCD which satisfies the contrast requirement. When Mux-Rate is under 40, it is recommended to set BR=5 for optimum power saving.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



#### (31) SET WINDOW PROGRAM STARTING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC0 [7:0]	0	0	1	1	1	1	0	1	0	0
(Double-byte command)	0	0		W	PC0	regist	er pa	ramet	er	

This command is to program the starting column address of RAM program window.

#### (32) SET WINDOW PROGRAM STARTING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP0 [5:0]	0	0	1	1	1	1	0	1	0	1
(Double-byte command)	0	0	-	-	W	PP0	regist	er pai	ramet	er

This command is to program the starting row address of RAM program window.

#### (33) SET WINDOW PROGRAM ENDING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC1 [7:0]	0	0	1	1	1	1	0	1	1	0
(Double-byte command)	0	0		W	PC1	regist	er pai	ramet	er	

This command is to program the ending column address of RAM program window.

#### (34) SET WINDOW PROGRAM ENDING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP1 [5:0]	0	0	1	1	1	1	0	1	1	1
(Double-byte command)	0	0	-	-	W	PP1	regist	er pai	amet	er

This command is to program the ending row address of RAM program window.



#### (35) SET WINDOW PROGRAM ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Window Program Enable AC[3]	0	0	1	1	1	1	1	0	0	AC3

This command controls the Window Program function.

**0: Inside Mode** 1: Outside Mode

Setting or resetting AC[3] does not affect the values of CA and RA. So, always remember to reposition CA and RA properly after changing the setting of AC[3].

When using Outside mode, the data inside window will be ignored, that is, users can send data of full screen.

Display Data		Setting	Image in Display Data RAM
Direction	MX, LC[1]	RID, AC[2]	(Physical origin: upper left corner)
Normal	0	0	
Y-mirror	0	1	
X-mirror	1	0	
X-mirror Y-mirror	1	1	120

#### (36) SET MTP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPC[5:0]	0	0	1	0	1	1	1	0	0	0
(Double-byte command)	0	0	-	-	M	TPC	regist	er pai	ramet	er

This command is for MTP operation control:

MTPC[2:0] : MTP command

 000 : Idle
 001 : MTP Read

 010 : MTP Erase
 011 : MTP Program

1xx: For UltraChip use only.

MTPC[3]: MTP Enable (Automatically cleared each time after MTP command is done)

MTPC[4]: MTP value valid (Ignore MTP value when L) MTPC[5]: For testing only. Set to 0 for normal operation

#### The following commands (34)~(38) are only valid when MTPC[3]=1.

DC[2] and MTPC[3] are mutually exclusive. Only one of these two control flags can be set to ON at any time. In other words, when DC[2] is ON, all MTP operations will be blocked, and, when MTP operation is active, set DC[2] to 1 will be blocked.

#### (37) SET MTP WRITE MASK

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPM[5:0]	0	0	1	0	1	1	1	0	0	1
(Double-byte command)	0	0	-	•	M	TPM	regist	er pa	ramet	er

This command enables Write to each individual MTP bits.

When MTPM[x]=1, the x-th bit of the MTP memory will be programmed to "1". MTPM[x]=0 means no write action for x-th bit. And the content of this bit will not change.

The amount of "programming current" increases with the number of 1's in MTPM. If the "programming current" appears to be too high for the LCM design (e.g. TST4 ITO trace is not wide enough to supply the current), use multiple write cycles and distribute the 1's evenly into these cycles.

MTPM[5:0]: Set PMO value

#### (38) SET V<sub>MTP1</sub> POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP1	0	0	1 1 1 1 1 0 1 0					0	0	
(Double-byte command)	0	0	Shared register parameter							

This command is for fine tuning V<sub>OPT1</sub> setting (use with BR=00) and is valid only when MTPC[3]=1.

#### (39) SET V<sub>MTP2</sub> POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP2	0	0	1	1	1	1	0	1	0	1
(Double-byte command)		0	Shared register parameter							

This command is for fine tuning V<sub>MTP2</sub> PM setting (use with BR=11) and is valid only when MTPC[3]=1.

#### (40) SET MTP WRITE TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP3	0	0	1	1	1	1	0	1	1	0
(Double-byte command)	0	0		Sh	ared	regist	ter pa	rame	ter	

#### (41) SET MTP READ TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP4	0	0	1	1	1	1	0	1	1	1
(Double-byte command)	0	0	Shared register parameter							

Serial Read Commands (for S8 or S9 Bus mode only):

#### (42) GET STATUS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0			
	0	0	1	1	1	1	1	1	1	0			
Get Status	ı		Ver	MX	MY	WA	DE	WS	MD	MS			
Get Status		-	-	-	1 1	ID[1:0]				PMC	[5:0]		
			Р	roduc	t Coc	le	0	0	0	EF			



#### LCD VOLTAGE SETTING

High-Voltage Mixed-Signal IC

#### **MULTIPLEX RATES**

Multiplex Rate (MR) is completely software programmable in UC1611s via the register CEN.

Combined with low power partial display mode and a low bias ratio of 5, UC1611s can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

#### **BIAS RATIO SELECTION**

Bias Ratio (BR) is defined as the ratio between V<sub>LCD</sub> and V<sub>REF</sub>, i.e.

$$BR = V_{LCD}/V_{REF}$$
,  
where  $V_{REF} = V_{A1P} - V_{A1N}$ 

The theoretical optimum Bias Ratio can be estimated by  $\sqrt{Mux+1}$ . BR of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

Due to the nature of STN operation, an LCD designed for good gray-shade performance at high Mux Rate (e.g. MR=160), can generally perform very well as a black and white display, at lower Mux Rate. However, it is also true that such technique generally cannot maintain LCD's quality of gray shade performance, since the contrast of the LCD will increase as Mux Rate decreases, and the shades near the two ends of the spectrum will start to lose visibility.

UC1611s supports four BR as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	5	10	11	12

Table 1: Bias Ratios

#### **TEMPERATURE COMPENSATION**

Four (4) different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per °C	-0.05	-0.10	-0.15	0.00

Table 2: Temperature Compensation

#### **V<sub>LCD</sub> GENERATION**

V<sub>I CD</sub> may be supplied either by internal charge pump or by external power supply. The source of V<sub>LCD</sub> is controlled by PC[3:2]. For good product reliability, it is recommended to keep V<sub>LCD</sub> under 17.5V over the entire operating range.

When V<sub>LCD</sub> is generated internally, the voltage level of V<sub>ICD</sub> is determined by three control registers: BR (Bias Ratio), PM (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{\tiny LCD} = (C_{\tiny V0} + C_{\tiny PM} \times PM) \times (1 + (T-25) \times C_{\tiny T} \%)$$
 where

 $C_{V0}$  and  $C_{PM}$  are two constants, whose value depends on the BR register setting. The values are provided in the table in the next page,

PM is the numerical value of PM register,

T is the ambient temperature in  ${}^{\circ}C$ , and

 $C_T$  is the temperature compensation coefficient as selected by TC register.

#### **V<sub>LCD</sub>** FINE TUNING

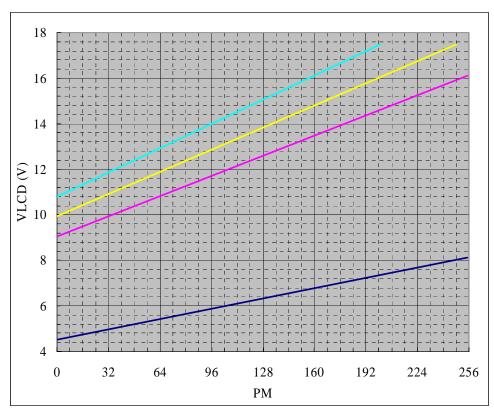
Gray shade and color STN LCD is sensitive to even a 1% mismatch between IC driving voltage and the Vop of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V<sub>LCD</sub> to match the actual V<sub>OP</sub> of the LCD.

For best result, software or MTP based V<sub>I CD</sub> adjustment is the recommended method for V<sub>LCD</sub> fine-tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LCM design.

#### LOAD DRIVING STRENGTH

The power supply circuits of UC1611s are designed to handle LCD panels with load capacitance up to 40nF at  $V_{LCD}$ =17V when  $V_{DD2}$  = 2.8V. For larger LCD panels or higher V<sub>LCD</sub>, use higher V<sub>DD2/3</sub>.

# **V<sub>LCD</sub> QUICK REFERENCE**



 $V_{\text{LCD}}\text{-PM}$  relationship for different BR setting at 25°C.

BR	C <sub>V0</sub> (V)	C <sub>PM</sub> (mV)	PM_reg	V <sub>LCD</sub> (V)
5	4.518	14.19	0	4.52
5	4.516 14.19 255		255	8.14
10	9.048 2		0	9.05
10	9.046	27.68	255	16.11
11	9.925	30.48	0	9.92
''	9.925	30.46	248	17.48
12	10.791	33.25	0	10.79
12	10.791	33.25	201	17.47

#### Note:

- For good product reliability, keep V<sub>LCD</sub> (max) under 17.5V under all operating temperature.
   The integer values of BR above are for reference only and may have slight shift.

#### HI-V GENERATOR AND BIAS REFERENCE CIRCUIT

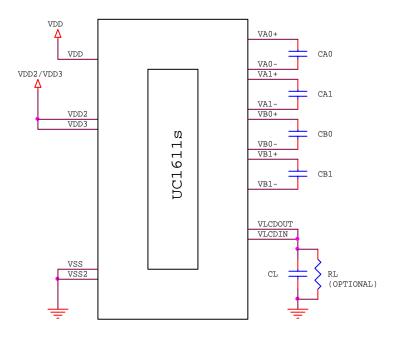


FIGURE 1: Reference circuit using internal Hi-V generator circuit

#### Note

Recommended component values:

 $100\sim250$  x LCD load capacitance or  $5\mu F$  (5V), whichever is higher.  $0.1\mu F\sim0.5\mu F$  (25V) is appropriate for most applications.

C<sub>L</sub>:

R<sub>L</sub>:  $3.3M \sim 10M\Omega$  Acts as a draining circuit when the power is abnormally shut down.

#### LCD DISPLAY CONTROLS

#### **CLOCK & TIMING GENERATOR**

UC1611s contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Eight different line rates are provided for system design flexibility. The line rate is controlled by register LC[5:4]. When Mux-Rate is above 108, frame rate is calculated as:

Frame rate = Line-Rate / Mux-Rate.

When Mux-Rate is under 107, 80, 53, 40, Line rate will automatically be scaled down by 1.5, 2, 3, 4 respectively to reduce power consumption.

Flicker-free frame rate is dependent on LC material and gray-shade modulation scheme. Frame rate ≥ 150Hz is recommended for 16-shade mode. Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

#### **DRIVER MODES**

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When SEG drivers are in idle mode, they will be connected together to ensure zero DC condition on the LCD.

#### **DRIVER ARRANGEMENTS**

The naming conventions are: COM(x), where  $x = 1\sim160$ , refers to the COM driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows is fixed and it is not affected by SL, CST, CEN, DST, DEN, MX or MY settings.

#### DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO), and Inverse (PXV). DE has the overriding effect over PXV and APO.

#### DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via *Set Display ON* command. When DC[2] is set to OFF (logic "0"), both COM and SEG drivers will become idle and UC1611s will put itself into Sleep mode to conserve power.

When DC[2] is set to ON, the DE flag will become "1", and UC1611s will first exit from Sleep mode, restore the power ( $V_{LCD}$ ,  $V_D$ , etc.) and then turn on COM and DEG drivers.

#### ALL PIXELS ON (APO)

When set, this flag will force all active SEG drivers to output On signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

#### INVERSE (PXV)

When this flag is set to ON, active SEG drivers will output the inverse of the value it received from the display buffer RAM. This flag has no impact on data stored in RAM.

#### PARTIAL SCROLL

The control register FL specifies a region of rows those are not affected by the SL register. Since SL register can be used to implement scroll function. The FL register can be used to implement fixed region when the other part of the display is scrolled by SL.

#### PARTIAL DISPLAY

UC1611s provides flexible control of Mux Rate and active display area. Please refer to command Set COM End, Set Partial Display Start, and Set Partial Display End for more detail.

#### GRAY-SHADE MODULATION MODE

UC1611s has two gray-shade modulation modes: 16-shade, 8-shade, 4-shade and On/Off mode.

The On/Off mode will consume roughly 40~45% less power than the 16-shade mode, and can be used for situations where power consumption is more critical than color fidelity.

Changing gray-shade modulation mode does not affect the content of SRAM display buffer, and the image data will remain the same after switching back and forth between On/Off mode and 16-shade mode.



#### LAYOUT CONSIDERATIONS FOR COM SIGNALS

Under 16-gray-shade mode, the COM scanning pulses of UC1611s can be as short as 17µs. Since COM distortion can lead to reduction of effective duty factor of the LCM, it is critical to control the RC delay of COM signal to minimize distortion of COM scanning pulse.

For the best image quality, limit the worst case RC delay of COM signal as calculated below.

$$RC_{COM} = (R_{ROW} / 3 + R_{COM} + R_{OUT}) \times C_{ROW}$$
  
 $RC_{COM-MAX} \le 1.2 \mu S$ 

where

LCD loading capacitance of one  $C_{ROW}$ :

row of pixels. It can be calculated by  $C_{LCD}$ /Mux-Rate, where  $C_{LCD}$  is

the LCD panel capacitance.  $R_{ROW}$ : ITO resistance over one row of

pixels within the active area

R<sub>COM</sub>: COM routing resistance from IC to

the active area (COF+ITO routing)

Rout: COM driver output impedance

In case RC<sub>COM-MAX</sub> exceed the above constraint significantly, please make sure

$$|RC_{COM-MAX} - RC_{COM-MIN}| < 0.6 \mu S$$

so that the COM scan pulse distortions from the top of the screen to the bottom of the screen are uniform.

For 8-gray-shade mode, the COM scanning pulse is about 35% slower than the 16-gray-shade mode. Therefore, the two constraints described above can be relaxed by 1/3 respectively to

$$RC_{COM} \le 1.6uS$$
  
 $|RC_{COM-MAX} - RC_{COM-MIN}| < 0.8\mu S$ 

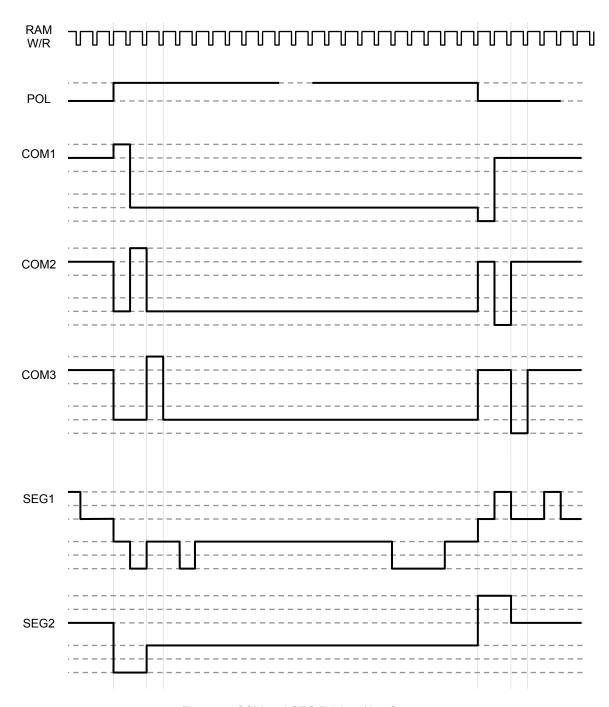


FIGURE 2: COM and SEG Driving Waveform



#### HOST INTERFACE

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As summarized in the table below, UC1611s supports 2 parallel bus protocols, 8080 and 6800 (in 16-bit, 8-bit, or 4-bit bus width), and 3 serial bus protocols (4-wire, 3-sire, and 2-wire).

Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules.

						Bus Type					
				Para	allel				Serial		
			8080			6800		S8	S9	I <sup>2</sup> C	
	Width	16-bit	8-bit	4-bit	16-bit	8-bit	4-bit	4-wire	3-wire	2-wire	
	Access		Read/Write								
	BM[1:0]	00	10	10	01	11	11	10	11	11	
S	D[15, 13]	Data	00	01	Data	00	01	10	10	11	
Pins	CS[1:0]				Chip S	Select				A[3:2]	
Data	CD			C	Control/Dat	а			-	-	
& D	WR0		WR			R/W			0		
	WR1		RD			EN			0		
Control	D[14, 12:8]	Data	1	_	Data	1	_		-		
0	D[7:4]	Da	ata	_	Da	Data –			-		
	D[3:0]	D[3:0] Data Data Data Data		Data Data		ta Data Data D3:			D3=SDA, D0=SCł		

<sup>\*</sup> Connect unused control pins and data bus pins to  $V_{\text{DD}}$  or  $V_{\text{SS}}$ 

Table 3: Host interfaces Choices

#### PARALLEL INTERFACE

The timing relationship between UC1611s' internal control signals, RD and WR, and their associated bus actions are shown in the figure below.

The Display RAM Read Interface is implemented as a two-stage pipe-line. This architecture requires a dummy read cycle to be performed before the actual data can propagate through the pipe-line and be read from data port D[7:0], every time memory address is modified (in 16-bit, 8-bit, or 4-bit mode) by either Set CA, or Set PA command.

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

#### 16-BIT, 8-BIT & 4-BIT BUS OPERATION

UC1611s supports 16-bit, 8-bit, and 4-bit bus widths. The bus width is determined by pins BM[1:0] and {D15, D13}.

UC1611s SARM read/write is based on 8-bit.

8-bit bus operation exactly doubles the clock cycles of 16-bit bus operation, while 4-bit doubles the clock cycles of 8-bit, MSB followed by LSB, including the dummy read, which also requires two clock cycles. For 16-bit bus operation, SRAM will perform read/write twice successively to finish a complete Read/Write.

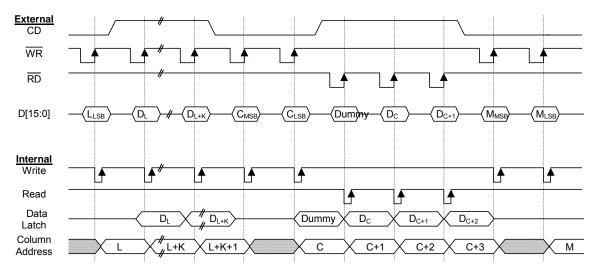


FIGURE 3.a: 16-bit Parallel Interface & Related Internal Signals

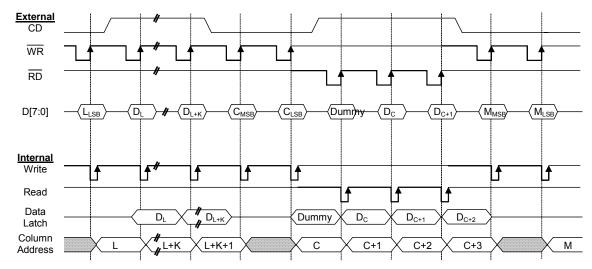


FIGURE 3.b: 8-bit Parallel Interface & Related Internal Signals

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#### SERIAL INTERFACE

UC1611s supports 3 serial modes, 4-wire SPI mode (S8), 3-wire SPI mode (S9), and 2-wire SPI mode (I<sup>2</sup>C). Bus interface mode is determined by the wiring of the BM[1:0] and D7. See configuration table in the beginning of this section for more detail.

#### 4-WIRE SERIAL INTERFACE (S8)

Pins CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

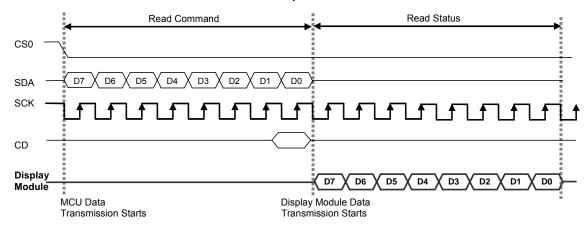


FIGURE 4.a: 4-wire Serial Interface (S8) - Read

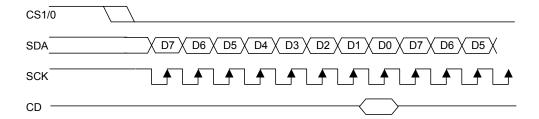


FIGURE 4.b: 4-wire Serial Interface (S8) - Write

## 3-WIER SERIAL INTERFACE (S9)

Pins CS[1:0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command or data bits are latched on rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command.

If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse. By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either  $V_{DD}$  or  $V_{SS}$ . The toggle of CS0 (or CS1) for each byte of data/command is recommended but optional.

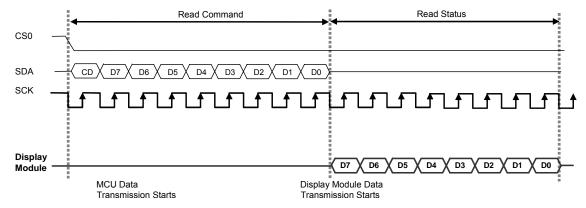


FIGURE 5.a: 3-wire Serial Interface (S9) - Read

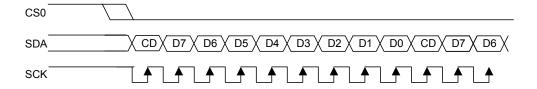


FIGURE 5.b: 3-wire Serial Interface (S9)

High-Voltage Mixed-Signal IC

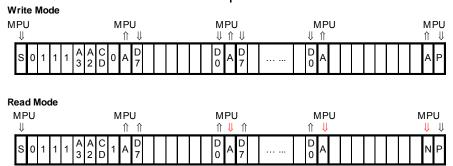
## I<sup>2</sup>C (2-WIRE) INTERFACE

When BM[1:0] is set to "LH" and D[7:6] is set to "HH", UC1611s is configured as an I<sup>2</sup>C bus signaling protocol compliant slave device. Please refer to I<sup>2</sup>C standard for details of the bus signaling protocol, and AC Characteristic section for timing parameters of UltraChip implementation.

In this mode, pins CS[1:0] become A[3:2] and are used to configure UC1611s' device address. Proper wiring to  $V_{\rm DD}$  or  $V_{\rm SS}$  is required for the IC to operate properly for I<sup>2</sup>C mode.

Each UC1611s I<sup>2</sup>C interface sequence starts with a "S" (Start) from the bus master, followed by a sequence header, containing a device address, the mode of transfer (CD, 0:Control, 1:Data), and the direction of the transfer (RW, 0:Write, 1:Read).

Since both WR and CD are expressed explicitly in the header byte, the control pins WR[1:0] and CD are not used in  $I^2C$  mode and should be connected to  $V_{SS}$ .



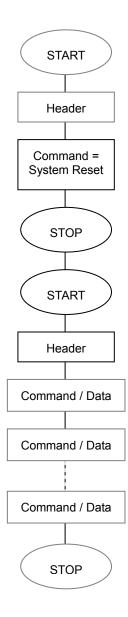
The direction (read or write) and content type (command or data) of the data bytes following each header byte are fixed for the sequence. To change the direction (R⇔W) or the content type (C⇔D), start a new sequence with a START (S) flag, followed by a new header.

After receiving the header, the UC1611s will send out a "A" (Acknowledge signal). Then, depends on the setting of the header, the transmitting device (either the bus master or UC1611s) will start placing data bits on SDA, MSB to LSB, and the sequence will repeat until a STOP signal (P, in WRITE mode), or an N (Not Acknowledged, in READ mode) is sent by the bus master.

160x256/16S Matrix LCD Controller-Driver

When using I<sup>2</sup>C serial mode, if command System Reset is to be written, the writing sequence must be finished (STOP) before succeeding data or commands start. The flow chart on the right shows a writing sequence with a "System Reset" command.

Note that, for data read (CD=1), the first byte of data transmitted will be dummy.





High-Voltage Mixed-Signal IC

## HOST INTERFACE REFERENCE CIRCUIT

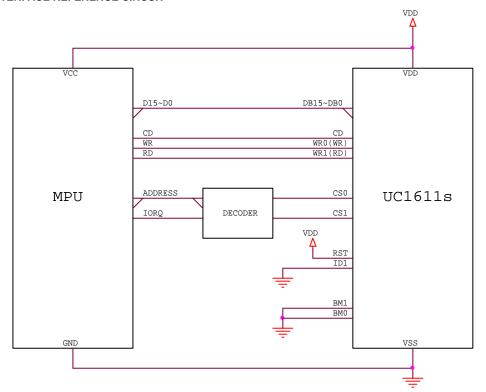


FIGURE 6: 8080/16-bit parallel mode reference circuit

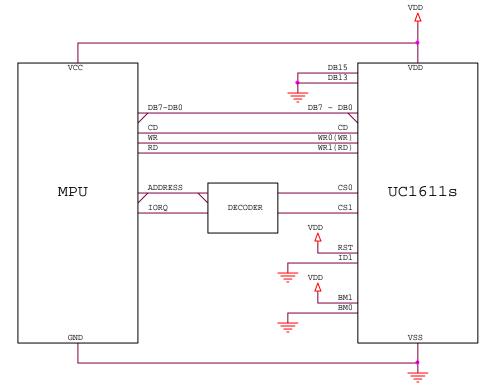
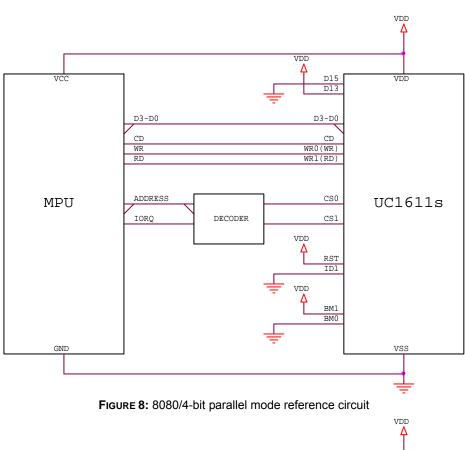


FIGURE 7: 8080/8-bit parallel mode reference circuit



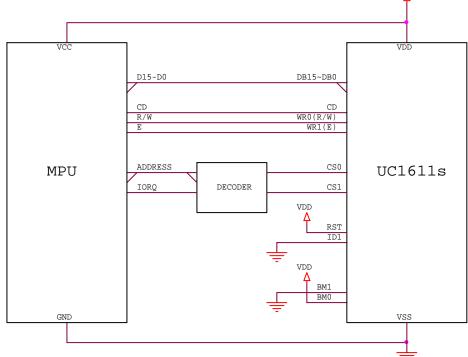


FIGURE 9: 6800/16-bit parallel mode reference circuit

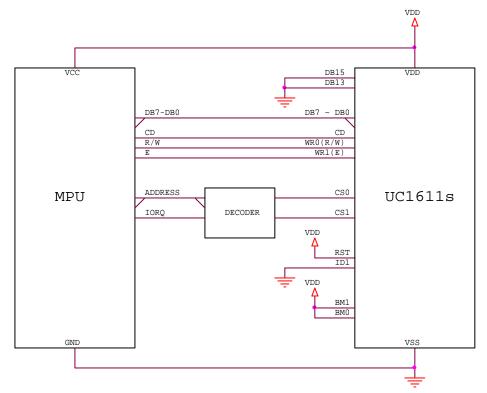


FIGURE 10: 6800/8-bit parallel mode reference circuit

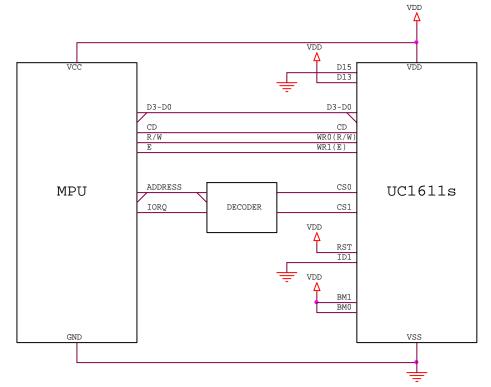


FIGURE 11: 6800/4-bit parallel mode reference circuit

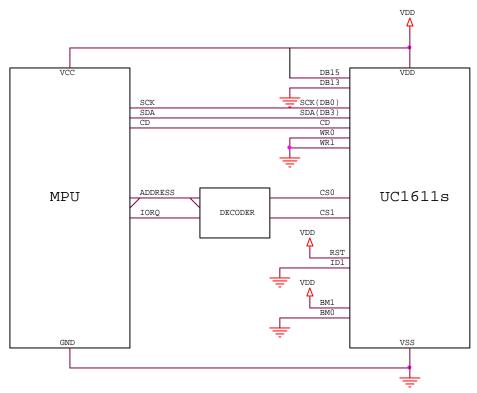


FIGURE 12: 4-Wire SPI (S8) serial mode reference circuit

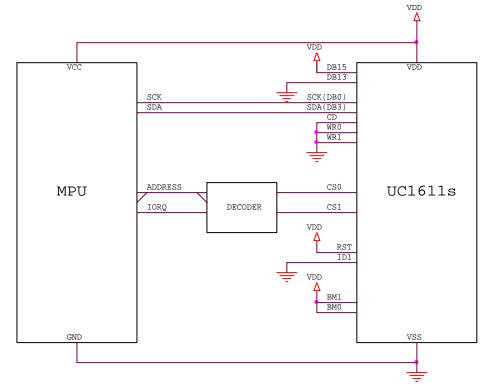


FIGURE 13: 3-Wire SPI (S9) serial mode reference circuit

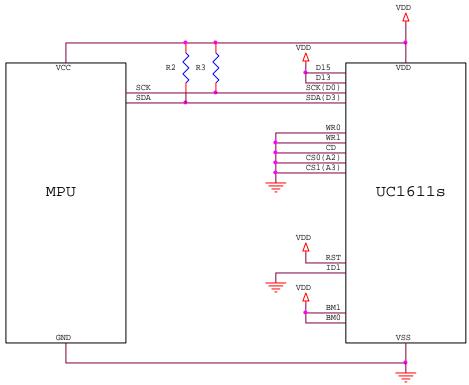


FIGURE 14: 2-Wire SPI (I<sup>2</sup>C) serial mode reference circuit

## Note:

- 1. RST pin is optional. When RST pin is not used, connect the pin to  $V_{DD}$ .
- 2. When using I<sup>2</sup>C serial mode, CS1/0 are user configurable and affect A[3:2] of device address.
- 3. R1, R2:  $2k \sim 10k \Omega$ . Use lower resistor for bus speed up to 3.6MHz; while use higher resistor for lower power.

## **DISPLAY DATA RAM**

### **DATA ORGANIZATION**

The display data is 4-bit per pixel and stored in a dual port SRAM. The SRAM is organized as 160x 256x4.

After setting CA and PA, the next data write cycle will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page for the relation between the COM, SEG, SRAM, and various memory control registers.

#### **DISPLAY DATA RAM ACCESS**

The Display RAM is a special purpose dual port RAM that allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

#### **DISPLAY DATA RAM ADDRESSING**

A Host Interface (HI) memory access operation starts with specifying Page Address (PA) and Column Address (CA) by issuing *Set Page Address* and *Set Column Address* commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of page (MC), and system programmers need to set the values of PA and CA explicitly.

If WA is ON (1), when CA reaches end of page, CA will be reset to 0 and PA will increment or decrement, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 79), PA will be wrapped around to the other end of RAM and continue.

## **MX** IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (255–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

### **RAM ADDRESS GENERATION**

The mapping of the data store in the display SRAM and the scanning electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

When FL=0, during the display operation, the RAM line address generation can be mathematically represented as following:

For the 1<sup>st</sup> line period of each field

Line = SL

Otherwise

Line = Mod (Line + 1, 160)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the "loop around" effect as it effectively resets *Line* to 0 when *Line*+1 reaches 160. Effects such as page scrolling and page swapping can be emulated by changing SL dynamically.

### **MY IMPLEMENTATION**

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1<sup>st</sup> line period of each field

Line = Mod(SL + MUX - 1, 160)

where MUX is the Mux rate

Otherwise

Line = Mod(Line - 1, 160)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.



# **WINDOW PROGRAM**

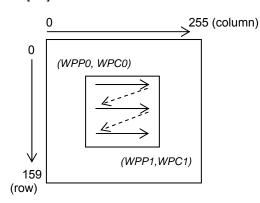
High-Voltage Mixed-Signal IC

Window program is designed for data write in a specified window range of SRAM address. The procedure should start with window boundary registers setting (WPP0, WPP1, WPC0 and WPC1) and then enable AC[3]. After AC[3] is set, data can be written to SRAM within the window address range which is specified by (WPPO, WPCO) and (WPP1, WPC1). AC[3] should be cleared after any modification of window boundary registers and then set again in order to initialize another window program.

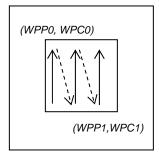
The data write direction will be determined by AC[2:0] and MX settings. When AC[0]=1, the data write can be consecutive within the range of the specified window. AC[1] will control the data write in either column or row direction. AC[2] will result the data write starting either from row WPP0 or WPP1. MX is for the initial column address either from WPC0 to WPC1 or from (MC-WPC0 to MC-WPC1).

# Example1:

AC[2:0] = 001 MX=0



## Example 2: AC[2:0] = 111 MX = 0



M	SF	Line	ı									RAM						MV	′=0	M	′=1
0	1	Adderss										NAW!						SL=0	SL=16	SL=0	SL=16
D3/0	D7/4	00H										Page 0						COM1	COM145	COM160	COM16
D7/4	D3/0	01H										rage 0						COM2	COM146	COM159	COM15
D3/0	D7/4	02H										Page 1						COM3	COM147	COM158	COM14
D7/4	D3/0	03H											_					COM4	COM148	COM157	COM13
D3/0	D7/4	04H										Page 2						COM5	COM149	COM156	COM12
D7/4	D3/0	05H		_									₩		_		Н	COM6	COM150	COM155	COM11
D3/0 D7/4	D7/4 D3/0	06H 07H				-						Page 3	-		-			COM7 COM8	COM151 COM152	COM154 COM153	COM10 COM9
D3/0	D7/4	07H											1				H	COM9	COM152 COM153	COM153	COM8
D7/4	D3/0	09H										Page 4						COM10	COM154	COM151	COM7
D3/0	D7/4	0AH										D 5						COM11	COM155	COM150	COM6
D7/4	D3/0	0BH										Page 5						COM12	COM156	COM149	COM5
D3/0	D7/4	0CH										Page 6						COM13	COM157	COM148	COM4
D7/4	D3/0	0DH										. ugc c						COM14	COM158	COM147	COM3
D3/0	D7/4	0EH										Page 7					Ш	COM15	COM159	COM146	COM2
D7/4	D3/0	0FH		_									_		_			COM16	COM160	COM145	COM1
D3/0	D7/4	10H				-						Page 8	-		H		$\vdash$	COM17	COM1	COM144	COM160
D7/4 D3/0	D3/0 D7/4	11H 12H		-	-			$\vdash$		$\vdash$			$\vdash$		$\vdash$		Н	COM18 COM19	COM2 COM3	COM143 COM142	COM159 COM158
D7/4	D3/0	12H		<del> </del>		$\vdash$		H	$\vdash$	Н		Page 9			$\vdash$		Н	COM19 COM20	COM4	COM142 COM141	COM158
D3/0	D7/4	14H			Н	Н		Н	Н	Н		<b>.</b>			Н	Н	Н	COM21	COM5	COM141	COM156
D7/4	D3/0	15H						П		П		Page 10			Т		П	COM22	COM6	COM139	COM155
D3/0	D7/4	16H										Page 11						COM23	COM7	COM138	COM154
D7/4	D3/0	17H										rage 11						COM24	COM8	COM137	COM153
D3/0	D7/4	18H										Page 12						COM25	COM9	COM136	COM152
D7/4	D3/0	19H										9	_				Ш	COM26	COM10	COM135	COM151
D3/0	D7/4	1AH				_						Page 13	_		_		Ш	COM27	COM11	COM134	COM150
D7/4	D3/0	1BH				-							┡		┝		Н	COM28	COM12	COM133	COM149
D3/0 D7/4	D7/4 D3/0	1CH 1DH		_		H						Page 14	-		H		Н	COM29 COM30	COM13 COM14	COM132 COM131	COM148 COM147
D3/0	D7/4	1EH						Н					+		H		Н	COM31	COM14 COM15	COM131	COM147 COM146
D7/4	D3/0	1FH										Page 15						COM32	COM16	COM129	COM145
D3/0	D7/4	8CH										Page 70	_					COM141	COM125	COM20	COM36
D7/4	D3/0	8DH				_											H	COM142	COM126	COM19	COM35
D3/0 D7/4	D7/4 D3/0	8EH 8FH		_		H						Page 71	-		H		Н	COM143 COM144	COM127 COM128	COM18 COM17	COM34 COM33
D3/0	D7/4	90H											-				Н	COM144 COM145	COM128	COM17	COM32
D7/4	D3/0	91H										Page 72	_					COM146	COM130	COM15	COM31
D3/0	D7/4	92H										Domo 72						COM147	COM131	COM14	COM30
D7/4	D3/0	93H										Page 73						COM148	COM132	COM13	COM29
D3/0	D7/4	94H										Page 74						COM149	COM133	COM12	COM28
D7/4	D3/0	95H		_	_			L		Ш			_		_		Ш	COM150	COM134	COM11	COM27
D3/0	D7/4	96H		_	<u> </u>	_		$\vdash$	H	H		Page 75	_		_		Н	COM151	COM135	COM10	COM26
D7/4	D3/0 D7/4	97H		<b>—</b>	├	-		$\vdash$	H	$\vdash$			$\vdash$		<u> </u>	Н	Н	COM152	COM136	COM9 COM8	COM25 COM24
D3/0 D7/4	_	98H 99H		_	$\vdash$			$\vdash$				Page 76			$\vdash$		Н	COM153 COM154	COM137 COM138	COM7	COM24 COM23
D3/0	D7/4	99H 9AH			$\vdash$	$\vdash$		Н		Н			$\vdash$		$\vdash$	$\vdash$	Н	COM154 COM155	COM138	COM6	COM23
D7/4	D3/0	9BH										Page 77			Т		H	COM156	COM140	COM5	COM21
D3/0	D7/4	9CH										Dage 70					П	COM157	COM141	COM4	COM20
D7/4	D3/0	9DH										Page 78						COM158	COM142	COM3	COM19
D3/0	D7/4	9EH				oxdot						Page 79			匚	Щ	Ш	COM159	COM143	COM2	COM18
D7/4	D3/0	9FH															Ш	COM160	COM144	COM1	COM17
		X	0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8		SEG236	SEG237	SEG238	SEG239	SEG240				
		2	-	SEG240	SEG239	SEG238	SEG237	SEG236	SEG235	SEG234	SEG233		SEG5	SEG4	SEG3	SEG2	SEG1				

# When DC[5:3] = 0xxb:

Example for memory mapping:

let MX = 0, MY = 0, SL = 0, MSF = 0, according to the data shown in the above table:

⇒ Page 0 SEG 1 : ( D[7:0] ) 0000 1111 b

⇒ Page 0 SEG 2 : ( D[7:0] ) 1111 0000 b



High-Voltage Mixed-Signal IC

	C.E.	1 :	1									D 444						3.00	/-0	3.65	/_1
	SF	Line										RAM							′=0		′=1
0	1	Adderss	1															SL=0	SL=16	SL=0	SL=16
D0	D4	00H																COM1	COM145	COM160	COM16
D1	D5	01H	1															COM2	COM146	COM159	COM15
D2	D6	02H	1												П		П	COM3	COM147	COM158	COM14
D3	D7	03H	t			-	<del>                                     </del>	$\vdash$	$\vdash$	$\vdash$	$\vdash$		$\vdash$	$\vdash$	$\vdash$	$\vdash$	Н	COM4	COM147 COM148	COM157	COM14
			ł	Ħ	F	$\vdash$		$\vdash$	-	$\vdash$	$\vdash$	Page 0	-	-	$\vdash$	$\vdash$	Н				
D4	D0	04H	ļ	<b>—</b>	_	$\vdash$	_	$\vdash$	<u> </u>	$\vdash$	ш	-	<u></u>		$\vdash$	<u> </u>	ш	COM5	COM149	COM156	COM12
D5	D1	05H	1	L				Ш		ш					$ldsymbol{ldsymbol{ldsymbol{eta}}}$		ш	COM6	COM150	COM155	COM11
D6	D2	06H		LĪ		L	L	LĪ	L	Ll	Ш		L	L	LĨ	L	<u>L</u> ]	COM7	COM151	COM154	COM10
D7	D3	07H																COM8	COM152	COM153	COM9
D0	D4	08H	1										T				М	COM9	COM153	COM152	COM8
D1	D5	09H	1	Н	Т	Т		Т					$\vdash$		Н	Т	М	COM10	COM154	COM151	COM7
	_		ł	$\vdash$	$\vdash$	$\vdash$		$\vdash$	-	$\vdash$	Н		$\vdash$	$\vdash$	$\vdash$	$\vdash$	Н				
D2	D6	0AH	ł	$\vdash$	$\vdash$	$\vdash$		$\vdash$	-	$\vdash$	$\vdash$		$\vdash$		$\vdash$	$\vdash$	Н	COM11	COM155	COM150	COM6
D3	D7	0BH	1	$\vdash$				Ш	<u> </u>	ш		Page 1	$\vdash$		$ldsymbol{\sqcup}$	<u> </u>	ш	COM12	COM156	COM149	COM5
D4	D0	0CH	1	$oldsymbol{oldsymbol{oldsymbol{eta}}}$	oxdot	$oxed{oxed}$		Ш				3.	$ldsymbol{le}}}}}}$		Ш	$oxed{oxed}$	Ш	COM13	COM157	COM148	COM4
D5	D1	0DH		L	L	L	L	LĪ	L	LĪ			L		LĪ	L		COM14	COM158	COM147	COM3
D6	D2	0EH	1															COM15	COM159	COM146	COM2
D7	D3	0FH	1												П		П	COM16	COM160	COM145	COM1
D0	D3	10H	t	$\vdash$	<del>                                     </del>		<b>-</b>	$\vdash$	<del>                                     </del>	H	H		+		$\vdash$		Н	COM17	COM1	COM144	COM160
			ł	$\vdash$	$\vdash$	$\vdash$		$\vdash$		$\vdash$	$\vdash$		$\vdash$		$\vdash$	$\vdash$	$\vdash$				
D1	D5	11H	ŀ	$\vdash$	_	Ь.		ш	<u> </u>	Н	Ш		$\vdash$		⊢	Ь.	Ш	COM18	COM2	COM143	COM159
D2	D6	12H	1	L		lacksquare		Ш		ш					$ldsymbol{ldsymbol{eta}}$		ш	COM19	COM3	COM142	COM158
D3	D7	13H	1	لــــــــــــــــــــــــــــــــــــــ								Page 2						COM20	COM4	COM141	COM157
D4	D0	14H	1									raye z						COM21	COM5	COM140	COM156
D5	D1	15H	1					П		П					П		П	COM22	COM6	COM139	COM155
D6	D2	16H	t	$\vdash$	$\vdash$	$\vdash$		$\vdash$			H		-	$\vdash$	Н		Н	COM23	COM7	COM138	COM153
			ł	$\vdash$	$\vdash$	$\vdash$		$\vdash$	-	$\vdash$	$\vdash$		$\vdash$	-	$\vdash$	$\vdash$	$\vdash$				
D7	D3	17H	ł	$\vdash$	<b>—</b>	┝	<b> </b>	$\vdash$	├	Н	ш		╄	_	⊢	<b>—</b>	ш	COM24	COM8	COM137	COM153
D0	D4	18H	1															COM25	COM9	COM136	COM152
D1	D5	19H	1	L	L	L	L	L	L	L			L	L	L	L		COM26	COM10	COM135	COM151
D2	D6	1AH	1															COM27	COM11	COM134	COM150
D3	D7	1BH	1					П										COM28	COM12	COM133	COM149
D4	D0	1CH	1	Н	$\vdash$			$\vdash$		Н	H	Page 3	$\vdash$		Н		Н	COM29	COM13	COM132	COM148
	_		ł	$\vdash$	$\vdash$	$\vdash$		$\vdash$	-	$\vdash$	H		$\vdash$	$\vdash$	$\vdash$	$\vdash$	Н		COM13		
D5	D1	1DH	ł	<b>—</b>	<u> </u>	<u> </u>		$\vdash$	<b>-</b>	$\vdash$			$\vdash$	<u> </u>	$\vdash$	<u> </u>	ш	COM30		COM131	COM147
D6	D2	1EH	1	Ь		Ь.		ш		ш	ш		$\vdash$		ш	Ь.	Ш	COM31	COM15	COM130	COM146
D7	D3	1FH	1	L									L					COM32	COM16	COM129	COM145
					l								1								
1	l	1		l	l	l							1			1					
1	l	1		l	l	l							1			1					
I				l					l				1								
I				l					l				1								
1	l	1		l	l	l							1			1	ı				
I				l					l				1								
1	l	1		l	l	l							1			1					
L	L		1	Щ.					<u></u>				<u>L</u>								
D0	D4	90H																COM145	COM129	COM16	COM32
D1	D5	91H	1															COM146	COM130	COM15	COM31
D2	D6	92H	1	Н	$\vdash$	$\vdash$	t	т	t	$\vdash$			$\vdash$		т	$\vdash$	М	COM147	COM131	COM14	COM30
D3	D7	93H	ł	$\vdash$	$\vdash$	$\vdash$	-	$\vdash$	$\vdash$	$\vdash$	$\vdash$		$\vdash$	<b>—</b>	$\vdash$	$\vdash$	Н	COM147 COM148		COM14 COM13	
			ł	$\vdash$	<b>—</b>	$\vdash$		$\vdash$	<b>—</b>	H	ш	Page 18	$\vdash$	-	$\vdash$	$\vdash$	Щ		COM132		COM29
D4	D0	94H		Ь		$\vdash$	<u> </u>	$\vdash$	<u> </u>	ш	ш	-	$\vdash$		╙	$\vdash$	ш	COM149	COM133	COM12	COM28
D5	D1	95H	1															COM150	COM134	COM11	COM27
D6	D2	96H			l	1							1			1	ıΠ	COM151	COM135	COM10	COM26
D7	D3	97H	1															COM152	COM136	COM9	COM25
D0	D4	98H	1					$\vdash$		Н			t		Н		М	COM153	COM137	COM8	COM24
D1	D5	99H	t	$\vdash$	<del> </del>	<del> </del>	-	$\vdash$	<b>—</b>	$\vdash$	H		$\vdash$	H	$\vdash$		Н	COM153		COM7	COM23
	_		ł	$\vdash$	<u> </u>	$\vdash$		$\vdash$	-	$\vdash$	$\vdash$		$\vdash$	<b>-</b>	$\vdash$	$\vdash$	Н		COM138		
D2	D6	9AH	1	lacksquare					<u> </u>	ш	ш		<u></u>		ш			COM155	COM139	COM6	COM22
D3	D7	9BH		L	L	L		L				Page 19				L		COM156	COM140	COM5	COM21
D4	D0	9CH										i age is						COM157	COM141	COM4	COM20
D5	D1	9DH	1					П		П					П		П	COM158	COM142	COM3	COM19
D6	D2	9EH	1	Н	Т	Т		Т		Н			<b>—</b>		Т			COM159	COM143	COM2	COM18
			ł	$\vdash$	$\vdash$	$\vdash$		$\vdash$	-	$\vdash$	H		$\vdash$	$\vdash$	$\vdash$	$\vdash$	Н				
D7	D3	9FH	ı	ш									1					COM160	COM144	COM1	COM17
				_																	
				<b>—</b>	2	က	4	2	ပ္ပ	_	တ		36	37	38	39	SEG240				
			0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8		SEG236	SEG237	SEG238	SEG239	32.				
				SE	SE	SE	SE	SE	SE	SE	SE		Ж	ΣĚ	Щ	ĕ	ЩI				
		×		-	$\vdash$	_		_		<u> </u>			(U)	3	()	(J)	(I)				
		2		9	39	38	37	36	35	34	33		2	4	က	2	_				
			~	SEG240	SEG239	SEG238	SEG237	SEG236	SEG235	SEG234	SEG233		SEG5	SEG4	SEG3	SEG2	SEG1				
				Щ	Щ	ĕ	Ж	Щ	Ж	Щ	ΞĚ		SE	SE	SE	SE	SE				
				U)	U)	U)	U)	U)	U)	0)	U)		1								

# When DC[5:3]=100b:

Example for memory mapping: Let MX = 0, MY = 0, SL = 0, MSF = 0, according to the data shown in the above table:

⇒ Page 0 SEG 1 : ( D[7:0] ) 0111 0000 b ⇒ Page 0 SEG 2 : ( D[7:0] ) 1011 0011 b

## **RESET & POWER MANAGEMENT**

#### Types of Reset

UC1611s has two different types of Reset: Power-ON-Reset and System-Reset.

Power-ON-Reset is performed right after  $V_{DD}$  is connected to power. Power-On-Reset will first wait for about 5~10mS, depending on the time required for  $V_{DD}$  to stabilize, and then trigger the System Reset.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means System Reset.

#### **RESET STATUS**

When UC1611s enters RESET sequence:

- Operation mode will be "Reset"
- All control registers are reset to default values.
   Refer to Control Registers for details of their default values.

#### **OPERATION MODES**

UC1611s has 3 operating modes (OM): Reset, Normal, Sleep.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

#### **CHANGING OPERATION MODE**

In addition to Power-ON-Reset, two commands will initiate OM transitions:

Set Display Enable, and System Reset.

When DC[2] is modified by Set Display Enable, OM will be updated automatically. There is no other action required to enter Sleep mode.

OM changes are synchronized with the edges of the IC's internal clock. To ensure consistent system states, wait at least  $10\mu S$  after Set Display Enable or System Reset command.

Action	Mode	OM
Reset command RST_ pin pulled "L" Power-ON-Reset	Reset	00
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11

Table 5: OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors  $C_{B0}$ ,  $C_{B1}$ , and  $C_L$ . When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that, Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as the IC consumes very little energy in Sleep mode (typically under  $1\mu$ A).

### **EXITING SLEEP MODE**

UC1611s contains internal logic to check whether  $V_{LCD}$  are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset Mode, COM and SEG drivers will not be activated until UC1611s' internal voltage sources are restored to their proper values.

### POWER-UP SEQUENCE

High-Voltage Mixed-Signal IC

UC1611s power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmers are only required to wait 150 mS before the CPU starting to issue commands to UC1611s. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands.

There's no delay needed while turning on  $V_{DD}$  and  $V_{DD2/3}$ , and either one can be turned on first.

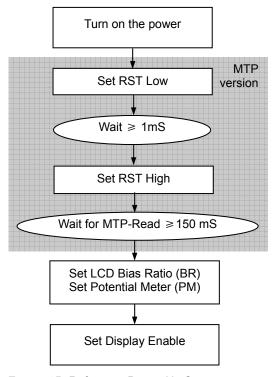


FIGURE 15: Reference Power-Up Sequence

#### POWER-DOWN SEQUENCE

To prevent the charge stored in capacitor  $C_L$  from causing abnoraml residue horizontal line on display when  $V_{DD}$  is switched off, use Reset mode to enable the built-in charge draining circuit to discharge the external capacitor.

When internal  $V_{LCD}$  is not used, UC1611s will *NOT* drain  $V_{LCD}$  during RESET. System designers need to make sure external  $V_{LCD}$  source is properly drained off before turning off  $V_{DD}$ .

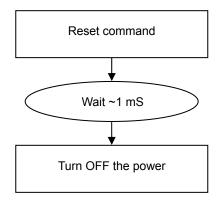


FIGURE 16: Reference Power-Down Sequence

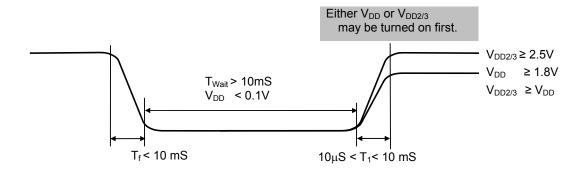


Figure 17: Delay allowance between  $V_{DD}$  and  $V_{DD2/3}$ 

## **MULTI-TIME PROGRAM NV MEMORY**

### **OVERVIEW**

MTP feature is available for UC1611s such that LCM maker can record an PM offset value in non-volatile memory cells, which can then be used to adjust the effective  $V_{\text{LCD}}$  value, in order to achieve high level of consistency for LCM contrast across all shipments.

To accomplish this purpose, three operations are supported by UC1611s:

MTP-Erase, MTP-Program, MTP-Read.

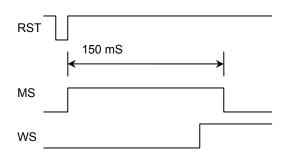
MTP-Program requires an external power source supplied to TST4 pin. MTP allows to program at least 10 times and should be performed only by the LCM makers.

MTP-Read is facilitated by the internal DC-DC converter built-in on UC1611s, no external power source is required, and it is performed automatically after hardware RESET (power-ON or pin RESET).

## **OPERATION FOR THE SYSTEM USERS**

For the MTP version of UC1611s, the content of the NV memory will be read automatically after the power-on and hardware pin RESET. There is no user intervention or external power source required. When set up properly, the  $V_{LCD}$  will be fine tuned to achieve high level of consistency for the LCM contrast.

The MTP-READ is a relatively slow process and the time required can vary quite a bit. For a successful MTP-READ operation, the MS and WS bits in the *Read Status* commands will exhibit the following waveforms.



As illustrated above, the {MS, WS} will go through a  $\{0,0\} \Rightarrow \{1,0\} \Rightarrow \{1,1\} \Rightarrow \{0,1\}$  transition. When the {MS, WS}= $\{0,1\}$  state is reached, it means the LCM is ready to be turned on.

During the MTP-READ process, it is actually safe to issue commands or perform data write to the LCM. The only thing that is blocked is the LSB of the Set Display Enable command, which results in the DC[2] being effectively locked at "0" during this auto-MTP-READ process.

Although user can use *Read Status* command in a polling loop to make sure {MS,WS}={0,1} before proceeding with the Set Display Enable command, however, it may be simpler to just issue the Set Display Enable command every 0.2~2 second, repeatedly, together with other LCM optimization settings, such as BR, CEN, TC, etc.

The above "Periodical re-initializing" approach is also an effective safeguard against accidental display off events such as

- ESD strikes
- Mechanical shocks causing LCM connector to malfunction temporarily

### HARDWARE VS. SOFTWARE RESET

The auto-MTP-READ is only performed for hardware RESET (power-ON and RST pin), but not for software *RESET* command. This enables the ICs to turn on display faster without the delay caused by MTP-READ.

It is recommended to use software *RESET* for normal operation control purpose and hardware RESET only during the event of power up and power down.

### **OPERATION FOR THE LCM MAKERS**

Always ERASE the MTP NV memory cells, before starting the Write process.

High-Voltage Mixed-Signal IC

# MTP OPERATION FOR LCM MAKERS

## 1. High voltage supply and timer setting

In MTP Program operation, two different high voltages are needed. In chip design, one high voltage is generated by internal charge pump ( $V_{LCD}$ ), the other high voltage must be input from TST4 by external voltage source.

V<sub>LCD</sub> value is controlled by register MTP3 and MTP2. The default values of these two registers are appropriate for most applications.

External TST4 power source is required for MTP Program operation. MTP Programming speed depends on the TST4 voltage. Considering the ITO trace resistance in COG modules, it is recommended to program the MTP cells one at a time, so that the required 10V at TST4 can be maintained with proper consistency.

No external power source is required for MTP Erase and Read operation. For these MTP operation, TST4 should be open, or connected to  $V_{\text{DD3}}$ .

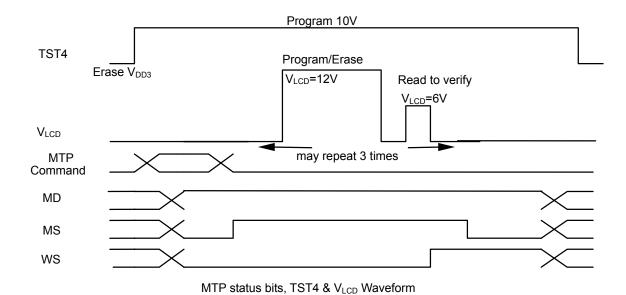
Operation	V <sub>LCD</sub>	TST4 (external input)
Program	MTP3: 15h (12V)	10V (1mA per bit)
Erase	MTP3: 15h (12V)	Floating or V <sub>DD3</sub>
Read	MTP2:69h (6V)	Floating or V <sub>DD3</sub>

### Note:

- 1. Do Erase before Program. Program one bit at a time.
- 2. When doing MTP Program or Erase, it's required to use  $V_{DD2/3} \ge 3.0V$ .

### 2. Read MTP status bits

With normal Get Status method (CD=0,W/R=1), MTP operation status can be monitored in the real time. There are 3 status bits (WS, MD, MS) in status register. MTP control circuit will read to verify if the operation (program, erase) success or not. If the operation succeeded, and current operation will be ended with WS=1. If it failed, last operation will be automatically retried two more times. If it fails 3 times, WS will be set to 0 and the operation is aborted. MD is MTP ID, which is either 1 for MTP IC. No transition.



# MTP CELL VALUE USAGE

There are 6 MTP cell bits.

PMO[5:0]: V<sub>LCD</sub> Trim

When PMO[5]=1: PM with trim = PM - PMO[4:0] When PMO[5]=0: PM with trim = PM + PMO[4:0]

High-Voltage Mixed-Signal IC

### MTP COMMAND SEQUENCE SAMPLE CODES

The following tables are examples of command sequence for MTP Program and Erase operations. These are only to demonstrate some "typical, generic" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

MTP operations (Erase, Program, Read) and Set Display ON is mutual exclusive. There is no harm done to the IC or the LCM if this is violated. However, the violating commands will be ignored.

Type Required: These items are required

<u>C</u>ustomized: These items are not necessary if customer parameters are the same as default <u>A</u>dvanced: We recommend new users to skip these commands and use default values.

Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

## (1) MTP Program Sample Code

Туре	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip Action	Comments
R	_	_	_	_	_	_	_	_	_	_	Set RST pin Low	Wait 1mS after RST is Low
R	_	_	_	_	_	_	_	_	_	_	Set RST pin High	
R	-	1	-	-	_	-	-	-	-	_	Automatic Power-ON Reset.	Wait ~150mS
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[5:4]=11b
R	0	0	1	1	1	1	0	1	0	0	Set V <sub>MTP1</sub> Potentiometer	Set MTP V <sub>LCD</sub>
R	0	0	0	1	1	0	1	0	0	1		MTP2: 69h(6V)
R	0	0	1	1	1	1	0	1	0	1	Set V <sub>MTP2</sub> Potentiometer	Set MTP V <sub>LCD</sub>
R	0	0	0	0	1	0	0	1	0	1		MTP3: 25h(12V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	0	1	0	0	1	0	1		MTP4:25h(100mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	0	1	0	1		MTP5:05h(10mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
С	0	0	0	0	0	0	0	0	0	1	МТРМ	Ex: To program PMO[5:0], set MTPM *
R	-	1	1	1	-	-	1	1	1	1		Apply TST4 voltage Program: 10V
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	•	1	0	0	1	0	1	1		Set MTPC[2:0]=011
R	0	1	-	-	-	-	ı	ws	-	MS	Get Status & PM	Check MTP Status until MS=0 and WS=1
R												Remove TST4 voltage
R											V <sub>DD</sub> =0V	Power OFF

<sup>\*</sup> It is recommended that users program one bit at a time.

# (2) MTP Erase Sample Code

Туре	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	_	-	-	-	_	-	-	-	_	-	Set RST pin Low	Wait 1mS after RST is Low
R	_	_	_	_	_	_	_	_	_	_	Set RST pin High	
R	_	_	_	_	_	_	_	_	_	_	Automatic Power-ON Reset.	Wait ~150mS
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[5:4]=11b
R	0	0	1	1	1	1	0	1	0	0	Set V <sub>MTP1</sub> Potentiometer	Set MTP V <sub>LCD</sub>
R	0	0	0	1	1	0	1	0	0	1		MTP2: 69h(6V)
R	0	0	1	1	1	1	0	1	0	1	Set V <sub>MTP2</sub> Potentiometer	Set MTP V <sub>LCD</sub>
R	0	0	0	0	1	0	0	1	0	1		MTP3: 25h(12V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	0	1	0	0	1	0	1		MTP4:25h(100mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	0	1	0	1		MTP5:05h(10mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
С	0	0	0	1	1	1	1	1	1	1	МТРМ	Ex: To erase PMO[5:0] , set MTPM
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	ı	ı	0	0	1	0	1	0		Set MTPC[2:0]=010
R	0	1	-	ı	-	-	-	ws	-	MS	Get Status & PM	Check MTP Status
												until MS=0 WS=1
R											V <sub>DD</sub> =0V	Power OFF

<sup>\*</sup> It is recommended that users clear all the bits to be programmed.



# SAMPLE COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "typical, generic" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

Type Required: These items are required

<u>C</u>ustomized: These items are not necessary, if customer parameters are the same as default <u>A</u>dvanced: We recommend new users to skip these commands and use default values.

Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1) W/R The direction of data-flow of the cycle. It can be either Write (0) or Read (1).

## Power-Up

Туре	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	ı	ı	ı	ı	ı	_	ı	ı	ı	ı	Turn on $V_{DD}$ and $V_{DD2/3}$	Wait until $V_{\text{DD}}$ and $V_{\text{DD2/3}}$ are stable
R	-	-	ı	ı	ı	-	-	ı	-	1	Set RST pin Low	Wait 1mS after RST is Low
R	_	-	_	_	_	_	-	_	1	-	Set RST pin High	
R	_	-	_	_	_	_	-	_	1	-	Automatic Power-ON Reset.	Wait ~150mS
С	0	0	0	0	1	0	0	1	#	#	Set Temp. Compensation	Cat up I CD format an acitic
С	0	0	1	1	0	0	0	0	0	0	Set LCD Mapping Control	Set up LCD format specific parameters, MX, MY, etc.
С	0	0	0	0	0	0	#	#	#	#	Set LCD Mapping Control	parameters, wix, wir, etc.
Α	0	0	1	0	1	0	0	0	#	#	Set Line Rate	Fine tune for power, flicker, contrast, and shading.
С	0	0	1	1	1	0	1	0	#	#	Set LCD Bias Ratio	LCD apositio apprating
R	0	0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set Gain and PM	LCD specific operating voltage setting
	1	0	#	#	#	#	#	#	#	#		
0											Write display RAM	Set up display image
	1	0	#	#	#	#	#	#	#	#	, ,	
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

## Power-Down

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	System Reset	
R	_	-	-	-	_	-	-	-	_	-	Draining capacitor	Wait ~1mS before V <sub>DD</sub> OFF

## DISPLAY-OFF

Туре	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	0	0	0	Set Display Disable	
0	1 1	· · 0	# #	# · · #	# #	# · · #	# #	# #	# #	# #	Write display RAM	Set up display image. (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

# **ESD CONSIDERATION**

UC1600 series products usually are provided in bare die format to customers. This makes the product
particularly sensitive to ESD damage during handling and manufacturing process. It is therefore highly
recommended that LCM makers strictly follow the "JESD 625-A Requirements for Handling
Electrostatic-Discharge-Sensitive (ESDS) Devices" when manufacturing LCM.

In particular, the following pins in UC1611s require special "ESD Sensitivity" consideration, please refer to Table below. According to UltraChip's Mass Production experience, the following ESD tolerance conditions has been shown be very stable and produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

Test N	lode	Machin	e Mode	Human B	ody Mode
Test IV	lode	$V_{DD}$	$V_{SS}$	$V_{DD}$	V <sub>SS</sub>
LCD D	river	200V	200V	2000V	2500V
LCM Int	erface	300V	300V	3000V	3000V
	TST1/2/4	300V	300V	3000V	3000V
LCM HV pin/	CB pins	300V	300V	3000V	3000V
Test pin	$V_{LCDIN}$	300V	300V	3000V	3000V
	V <sub>LCDOUT</sub>		300V	3000V	3000V
PWR / GND		-	300V	-	3000V

<sup>\*</sup> MM: Machine Mode

2. LCM design suggestions: To minimize potential ESD damages in assembly LCD modules(COG or COF) and modules test , please consider placing external components ( $C_{VLCD}$ , and  $C_{B0}$ ,  $C_{B1}$ ) in such a way that they will not be exposed to Machine Mode ESD zap path. For example, place  $C_{VLCD}$  and  $C_{B}$  capacitors on the internal side after folding FPC.



# **ABSOLUTE MAXIMUM RATINGS**

In accordance with IEC134, note 1, 2 and 3.

Symbol	Parameter	Min.	Max.	Unit
$V_{DD}$	Logic Supply voltage	-0.3	+4.0	V
$V_{DD2}$	LCD Generator Supply voltage	-0.3	+4.0	V
$V_{DD3}$	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$ - $V_{DD}$	Voltage difference between $V_{\text{DD}}$ and $V_{\text{DD2/3}}$		2.0	V
$V_{LCD}$	LCD Generated voltage (-30°C ~ +80°C)	-0.3	+19.8	٧
$V_{IN}$	Digital input voltage	-0.4	$V_{DD} + 0.5$	V
T <sub>OPR</sub>	Operating temperature range	-30	+85	°C
T <sub>STR</sub>	Storage temperature	-55	+125	°C

# Note:

- V<sub>DD</sub> is based on V<sub>SS</sub> = 0V
   Stress above values listed may cause permanent damages to the device.

# **SPECIFICATIONS**

## **DC CHARACTERISTICS**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
$V_{DD}$	Supply for digital circuit		1.65	1.8~3.3	3.6	V
$V_{\text{DD2/3}}$	Supply for bias & pump		2.7	2.8~3.3	3.6	V
$V_{LCD}$	Charge pump output	$V_{DD2/3} \ge 2.4V, 25^{\circ}C$		17	17.5	V
V <sub>D</sub>	LCD data voltage	$V_{DD2/3} \ge 2.4V, 25^{\circ}C$			1.69	V
V <sub>IL</sub>	Input logic LOW				$0.2V_{DD}$	V
V <sub>IH</sub>	Input logic HIGH		0.8V <sub>DD</sub>			V
$V_{OL}$	Output logic LOW				$0.2V_{DD}$	V
V <sub>OH</sub>	Output logic HIGH		0.8V <sub>DD</sub>			V
I <sub>IL</sub>	Input leakage current				1.5	μΑ
C <sub>IN</sub>	Input capacitance			5	10	pF
C <sub>OUT</sub>	Output capacitance			5	10	pF
R <sub>0(SEG)</sub>	SEG output impedance	V <sub>LCD</sub> = 17V		1.35	2.5	kΩ
R <sub>0(COM)</sub>	COM output impedance	V <sub>LCD</sub> = 17V		1.35	2.5	kΩ
f <sub>LINE</sub>	Average Line rate	LC[5:4] = 10b	-10%	28	+10%	kHz

# POWER CONSUMPTION

 $V_{DD} = 2.7 \text{ V},$ Bias Ratio = 11, PM = 234,

Line Rate = 10 b, Panel Loading (PC[1:0]) = 11 b,

 $V_{LCD} = 17.01 \text{ V},$ Mux Rate = 160, Bus mode = 6800, Temperature = 25 °C,  $C_L = 500 \text{ nF},$ MTP= 00 H,  $C_B = 5 \mu F$ ,

All HV outputs are open circuit.

Display Pattern	Conditions	Typ. (μA)	Max. (µA)
All-OFF	Bus = idle	1656	2484
2-pixel checker	Bus = idle	2031	3046
	Bus = idle (standby current)		5

High-Voltage Mixed-Signal IC

# **AC CHARACTERISTICS**

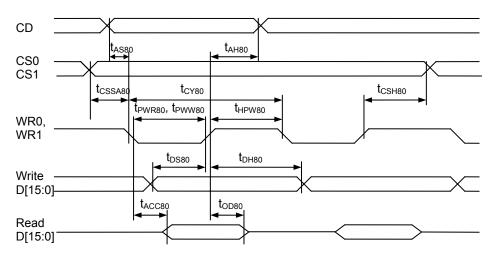


FIGURE 18: Parallel Bus Timing Characteristics (for 8080 MCU)

 $(2.5V \le V_{DD} < 3.6V, Ta = -30 \text{ to } +85^{\circ}C)$ 

Symbol	Signal	Description	Condition	Min. (nS)	Max.(nS)
t <sub>AS80</sub>	CD	Address setup time		0	_
t <sub>AH80</sub>		Address hold time		0	
t <sub>CY80</sub>		System cycle time			
		16-bit bus	(Read / Write)	410 / 330	_
		8-bit bus		150 / 130	
		4-bit bus		100 / 70	
t <sub>PWR80</sub>	WR1, WR0	Low Pulse width			
t <sub>PWW80</sub>		16-bit bus	(Read / Write)	205 / 165	_
		8-bit bus		75 / 65	
		4-bit bus		50 / 35	
t <sub>HPW80</sub>	WR1, WR0	High pulse width			
		16-bit bus	(Read / Write)	205 / 165	_
		8-bit bus		75 / 65	
		4-bit bus		50 / 35	
t <sub>DS80</sub>	D15~D0	Data setup time		30	_
t <sub>DH80</sub>		Data hold time		0	
t <sub>ACC80</sub>		Read access time	C <sub>L</sub> = 100pF	_	60
$t_{\text{OD80}}$		Output disable time	CL = 100pr	30	
t <sub>SSA80</sub>	CS1/CS0	Chip select setup time		0	
t <sub>CSH80</sub>		•		0	

 $(1.65V \le V_{DD} < 2.5V, Ta = -30 \text{ to } +85^{\circ}C)$ 

Symbol	Signal	Description	Condition	Min. (nS)	Max. (nS)
t <sub>AS80</sub>	CD	Address setup time		0	_
t <sub>AH80</sub>		Address hold time		0	
t <sub>CY80</sub>		System cycle time			
		16-bit bus	(Read / Write)	800 / 600	_
		8-bit bus		300 / 260	
		4-bit bus		200 / 140	
t <sub>PWR80</sub>	WR1	Low Pulse width			
t <sub>PWW80</sub>	WR0	16-bit bus	(	400 / 300	_
		8-bit bus		150 / 130	
		4-bit bus		100 / 70	
t <sub>HPW80</sub>	WR1, WR0	High pulse width			
		16-bit bus	(	400 / 300	_
		8-bit bus		150 / 130	
		4-bit bus		100 / 70	
t <sub>DS80</sub>	D15~D0	Data setup time		60	_
t <sub>DH80</sub>		Data hold time		0	
t <sub>ACC80</sub>		Read access time	C <sub>L</sub> = 100pF	_	120
t <sub>OD80</sub>		Output disable time	OL - 100pi	50	_
t <sub>SSA80</sub>	CS1/CS0	Chip select setup time		0	
t <sub>CSH80</sub>				0	

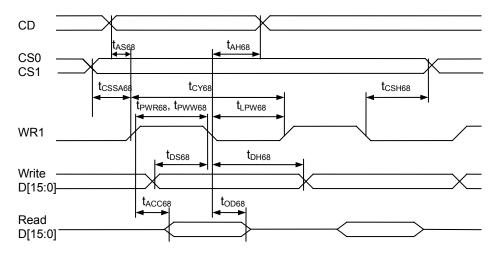


FIGURE 19: Parallel Bus Timing Characteristics (for 6800 MCU)

 $(2.5V \le V_{DD} < 3.6V, Ta = -30 \text{ to } +85^{\circ}C)$ 

Symbol	Signal	Description	Condition	Min. (nS)	Max. (nS)
t <sub>AS68</sub> t <sub>AH68</sub>	CD	Address setup time Address hold time		0 0	_
t <sub>CY68</sub>		System cycle time 16-bit bus 8-bit bus 4-bit bus	(Read / Write)	410 / 330 150 / 130 100 / 70	-
tpwR68 tpww68	WR1, WR0	Low Pulse width 16-bit bus 8-bit bus 4-bit bus	(Read / Write)	205 / 165 75 / 65 50 / 35	-
t <sub>LPW68</sub>	WR1, WR0	High Pulse width 16-bit bus 8-bit bus 4-bit bus	(Read / Write)	205 / 165 75 / 65 50 / 35	-
t <sub>DS68</sub> t <sub>DH68</sub>	D15~D0	Data setup time Data hold time		30 0	_
t <sub>ACC68</sub> t <sub>OD68</sub>		Read access time Output disable time	C <sub>L</sub> = 100pF	- 30	60 -
t <sub>CSSA68</sub> t <sub>CSH68</sub>	CS1/CS0	Chip select setup time		0 0	

 $(1.65V \le V_{DD} < 2.5V, Ta = -30 \text{ to } +85^{\circ}C)$ 

Symbol	Signal	Description	Condition	Min. (nS)	Max. (nS)
t <sub>AS68</sub>	CD	Address setup time		0	_
t <sub>AH68</sub>		Address hold time		0	
t <sub>CY68</sub>		System cycle time			
		16-bit bus	(Read / Write)	800 / 600	_
		8-bit bus		300 / 260	
		4-bit bus		200 / 140	
t <sub>PWR68</sub>	WR1, WR0	High Pulse width			
t <sub>PWW68</sub>		16-bit bus	(Read / Write)	400 / 300	_
		8-bit bus		150 / 130	
		4-bit bus		100 / 70	
t <sub>LPW68</sub>	WR1, WR0	Low pulse width			
		16-bit bus	(Read / Write)	400 / 300	_
		8-bit bus		150 / 130	
		4-bit bus		100 / 70	
t <sub>DS68</sub>	D15~D0	Data setup time		60	_
t <sub>DH68</sub>		Data hold time		0	
t <sub>ACC68</sub>		Read access time	C = 100pF	_	120
t <sub>OD68</sub>		Output disable time	$C_L = 100pF$	50	_
t <sub>CSSA68</sub>	CS1/CS0	Chip select setup time		0	
t <sub>CSH68</sub>				0	



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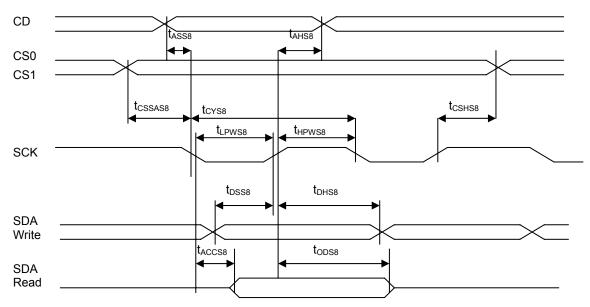


FIGURE 20: Serial Bus Timing Characteristics (for S8)

 $(2.5V \le V_{DD} < 3.6V, Ta = -30 \text{ to } +85^{\circ}C)$ 

Symbol	Signal	Description	Condition	Min. (nS)	Max. (nS)
t <sub>ASS8</sub> t <sub>AHS8</sub>	CD	Address setup time Address hold time		0 0	- -
t <sub>CYS8</sub> t <sub>LPWS8</sub> t <sub>HPWS8</sub>	SCK	System cycle time Low pulse width High pulse width	(Read / Write)	120 / 36 60 / 18 60 / 18	
t <sub>ACCS8</sub>		Read access time Output disable time	(Read)	_ 15	50 -
t <sub>DSS8</sub> t <sub>DHS8</sub>	SDA	Data setup time Data hold time	(Write)	15 0	_ _
t <sub>CSSAS8</sub> t <sub>CSHS8</sub>	CS1/CS0	Chip select setup time	(Read / Write)	0 / 0 0 / 0	

 $(1.65V \le V_{DD} < 2.5V, Ta = -30 \text{ to } +85^{\circ}C)$ 

Symbol	Signal	Description	Condition	Min. (nS)	Max. (nS)
t <sub>ASS8</sub>	CD	Address setup time Address hold time		0 0	-
t <sub>CYS8</sub> t <sub>LPWS8</sub> t <sub>HPWS8</sub>	SCK	System cycle time Low pulse width High pulse width	(Read / Write)	240 / 60 120 / 30 120 / 30	- - -
t <sub>ACCS8</sub> t <sub>ODS8</sub>		Read access time Output disable time	(Read)	- 30	90 -
t <sub>DSS8</sub> t <sub>DHS8</sub>	SDA	Data setup time Data hold time	(Write)	30 5	-
t <sub>CSSAS8</sub> t <sub>CSHS8</sub>	CS1/CS0	Chip select setup time	(Read / Write)	0 / 0 0 / 0	

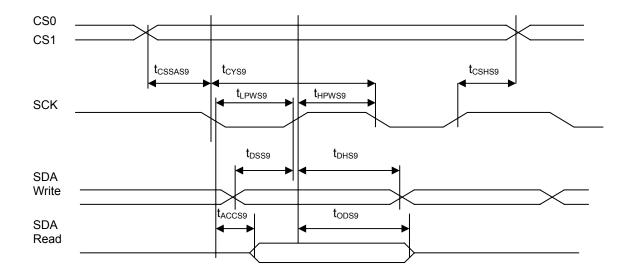


FIGURE 21: Serial Bus Timing Characteristics (for S9)

 $(2.5V \le V_{DD} < 3.6V, Ta = -30 \text{ to } +85^{\circ}C)$ 

Symbol	Signal	Description	Condition	Min. (nS)	Max. (nS)
t <sub>CYS9</sub> t <sub>LPWS9</sub> t <sub>HPWS9</sub>	SCK	System cycle time Low pulse width High pulse width	(Read / Write)	120 / 36 60 / 18 60 / 18	1 1
t <sub>ACCS9</sub> t <sub>ODS9</sub>	SDA	Read access time Output disable time	(Read)	_ 15	50 -
t <sub>DSS9</sub> t <sub>DHS9</sub>	SDA	Data setup time Data hold time	(Write)	15 0	-
t <sub>CSSAS9</sub> t <sub>CSHS9</sub>	CS1/CS0	Chip select setup time	(Read / Write)	0 / 0 0 / 0	

 $(1.65V \le V_{DD} < 2.5V, Ta = -30 \text{ to } +85^{\circ}C)$ 

Symbol	Signal	Description	Condition	Min. (nS)	Max. (nS)
t <sub>CYS9</sub> t <sub>LPWS9</sub> t <sub>HPWS9</sub>	SCK	System cycle time Low pulse width High pulse width	(Read / Write)	240 / 60 120 / 30 120 / 30	1 1 1
t <sub>ACCS9</sub> t <sub>ODS9</sub>	SDA	Read access time Output disable time	(Read)	- 30	90 -
t <sub>DSS9</sub> t <sub>DHS9</sub>	SDA	Data setup time Data hold time	(Write)	30 5	_
t <sub>CSSAS9</sub> t <sub>CSHS9</sub>	CS1/CS0	Chip select setup time	(Read / Write)	0 / 0 0 / 0	

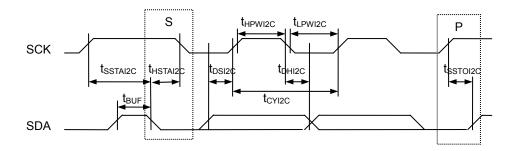


FIGURE 22: Serial bus timing characteristics (for I<sup>2</sup>C)

 $(2.5V \le V_{DD} < 3.6V, Ta = -30 \text{ to } +85^{\circ}C)$ 

Symbol	Signal	Description	Condition	Min. (nS)	Max. (nS)
t <sub>CYI2C</sub> t <sub>LPWI2C</sub> t <sub>HPWI2C</sub>	SCK	SCK cycle time Low pulse width High pulse width	tr+tf ≤ 100nS (Read / Write)	580 / 276 290 / 138 290 / 138	-
tdsi2c tdhi2c tsstai2c thstai2c tsstoi2c	SCK	Data setup time Data hold time START Setup time START Hold time STOP setup time		33 11 28 50 28	-
t <sub>BUF</sub>	SDA	Bus Free time between STOP and START condition		165	_

$$(1.65V \le V_{DD} \le 2.5V, Ta = -30 \text{ to } +85^{\circ}C)$$

Symbol	Signal	Description	Condition	Min. (nS)	Max. (nS)
tcyi2c t <sub>LPWi2C</sub> t <sub>HPWi2C</sub>	SCK	SCK cycle time Low pulse width High pulse width	tr+tf ≤ 100nS (Read / Write)	750 / 330 375 / 115 375 / 115	-
t <sub>DSI2C</sub> t <sub>DHI2C</sub> t <sub>SSTAI2C</sub> t <sub>HSTAI2C</sub> t <sub>HSTAI2C</sub> t <sub>SSTOI2C</sub>	SCK	Data setup time Data hold time START Setup time START Hold time STOP setup time		60 11 28 60 28	-
t <sub>BUF</sub>	SDA	Bus Free time between STOP and START condition		220	-

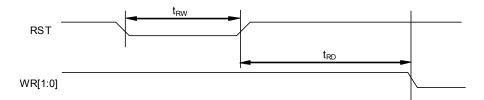


FIGURE 23: Reset Characteristics

 $(1.65V \le V_{DD} < 3.6V, Ta = -30 \text{ to } +85^{\circ}C)$ 

Symbol	Signal	Description	Condition	Min.	Max.
t <sub>RW</sub>	RST	Reset low pulse width		3 μS	_
$t_{RD}$	RST, WR	Reset to WR pulse delay		10 mS	_



# **PHYSICAL DIMENSIONS**

High-Voltage Mixed-Signal IC

## **DIE INFORMATION**

## DIE SIZE:

13754  $\mu M$  x 1120  $\mu M$   $\pm\,40$   $\mu M$ 

## **DIE THICKNESS:**

 $400~\mu M~\pm~20~\mu M$ 

## **BUMP HEIGHT:**

 $15 \mu M \pm 3 \mu M$ 

 $(H_{MAX}$  -  $H_{MIN})$  within die  $\leqslant 2\mu M$ 

## **BUMP PITCH:**

38 µM (Typ.)

## **BUMP SIZE:**

SEG/COM:  $25 \times 75.5 \, \mu M^2$  (Typ.)

## **BUMP AREA:**

1887.5 μM<sup>2</sup>

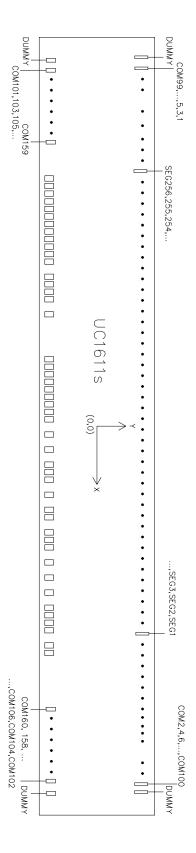
# PAD COORDINATES:

Pad center

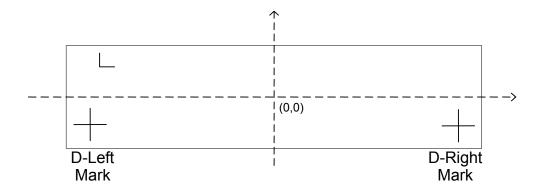
# PAD ORIGIN:

Chip center

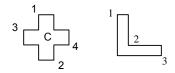
(Drawings and coordinates are in the circuit/bump view)



# **ALIGNMENT MARK INFORMATION**



# SHAPE OF THE ALIGNMENT MARK:



## Note:

Alignment marks are on Metal3 under Passivation.

The "x" and "+" marks are symmetric both horizontally and vertically.

## COORDINATES:

	Upper-Left Mark ( L )		(L) Upper-Right I	
Point	Х	Y		
1	-5160.4	394		
2	-5144.4	370		
3	-5120.4	354	-	
	Down-Left Mark ( + )		Down-Right Mark (+)	
1	-5365.225	-453.5	5549	-453.5
2	-5345.225	-513.5	5569	-513.5
3	-5385.225	-473.5	5529	-473.5
4	-5325.225	-493.5	5589	-493.5
С	-5355.225	-483.5	5559	-483.5

## TOP METAL AND PASSIVATION:



FOR NON-OTP PROCESS CROSS-SECTION



# PAD COORDINATES

High-Voltage Mixed-Signal IC

#	Pad	Х	Υ	W	Н
1	DUMMY	-6785.5	-487.5	30	75.5
2	COM101	-6745	-487.5	25	75.5
3	COM103	-6707	-487.5	25	75.5
4	COM105	-6669	-487.5	25	75.5
5	COM107	-6631	-487.5	25	75.5
6	COM109	-6593	-487.5	25	75.5
7	COM111	-6555	-487.5	25	75.5
8	COM113	-6517	-487.5	25	75.5
9	COM115	-6479	-487.5	25	75.5
10	COM117	-6441	-487.5	25	75.5
11	COM119	-6403	-487.5	25	75.5
12	COM121	-6365	-487.5	25	75.5
13	COM123	-6327	-487.5	25	75.5
14	COM125	-6289	-487.5	25	75.5
15	COM127	-6251	-487.5	25	75.5
16	COM129	-6213	-487.5	25	75.5
17	COM131	-6175	-487.5	25	75.5
18	COM133	-6137	-487.5	25	75.5
19	COM135	-6099	-487.5	25	75.5
20	COM137	-6061	-487.5	25	75.5
21	COM139	-6023	-487.5	25	75.5
22	COM141	-5985	-487.5	25	75.5
23	COM143	-5947	-487.5	25	75.5
24	COM145	-5909	-487.5	25	75.5
25	COM147	-5871	-487.5	25	75.5
26	COM149	-5833	-487.5	25	75.5
27	COM151	-5795	-487.5	25	75.5
28	COM153	-5757	-487.5	25	75.5
29	COM155	-5719	-487.5	25	75.5
30	COM157	-5681	-487.5	25	75.5
31	COM159	-5643	-487.5	25	75.5
32	D15	-5227.975	-483.275	69.1	82.45
33	vdd	-5156.425	-483.275	25	82.45
34	D14	-5084.875	-483.275	69.1	82.45
35	D13	-4999.775	-483.275	69.1	82.45
36	D12	-4914.675	-483.275	69.1	82.45
37	D11	-4829.575	-483.275	69.1	82.45
38	D10	-4744.475	-483.275	69.1	82.45
39	D9	-4659.375	-483.275	69.1	82.45
40	D8	-4574.275	-483.275	69.1	82.45
41	D7	-4489.175	-483.275	69.1	82.45
42	D6	-4404.075	-483.275	69.1	82.45
43	D5	-4318.975	-483.275	69.1	82.45
44	D4	-4233.875	-483.275	69.1	82.45
45	D3	-4148.775	-483.275	69.1	82.45
46	D2	-4063.675	-483.275	69.1	82.45
47	D1	-3978.575	-483.275	69.1	82.45
48	D0	-3893.475	-483.275	69.1	82.45
49	RST	-3786.925	-481	65	87
50	CS0	-3705.325	-481	65	87
51	vdd	-3625.525	-481	45	87

# Pad X Y W  52 CS1 -3545.725 -481 65  53 CD -3464.125 -481 65  54 WR0 -3382.525 -481 65  55 vdd -3302.725 -481 45  56 WR1 -3222.925 -481 65  57 BM1 -3141.325 -481 65  58 vdd -3061.525 -481 45  59 BM0 -2981.725 -481 45  60 TST4 -2901.925 -481 45  61 TST4 -2841.925 -481 45  62 ID0 -2554.125 -481 65  63 vdd -2474.325 -481 65  64 ID1 -2394.525 -481 45  65 vss -2314.725 -481 45  66 vss -2254.725 -481 45  67 vss -2194.725 -481 45  68 vss -2134.725 -481 45  69 vss -2074.725 -481 45  70 vss -2014.725 -481 45  71 vss -1954.725 -481 45  72 vss -1894.725 -481 45  73 vss -1834.725 -481 45	87 87 87 87 87 87 87 87 87 87 87 87 87 8
53         CD         -3464.125         -481         65           54         WR0         -3382.525         -481         65           55         vdd         -3302.725         -481         45           56         WR1         -3222.925         -481         65           57         BM1         -3141.325         -481         65           58         vdd         -3061.525         -481         45           59         BM0         -2981.725         -481         65           60         TST4         -2901.925         -481         45           61         TST4         -2841.925         -481         45           62         ID0         -2554.125         -481         65           63         vdd         -2474.325         -481         45           64         ID1         -2394.525         -481         45           65         vss         -2314.725         -481         45           66         vss         -2254.725         -481         45           67         vss         -2194.725         -481         45           68         vss         -2134.725         -481         <	87 87 87 87 87 87 87 87 87 87 87 87 87 8
54         WR0         -3382.525         -481         65           55         vdd         -3302.725         -481         45           56         WR1         -3222.925         -481         65           57         BM1         -3141.325         -481         65           58         vdd         -3061.525         -481         45           59         BM0         -2981.725         -481         65           60         TST4         -2901.925         -481         45           61         TST4         -2841.925         -481         45           62         ID0         -2554.125         -481         65           63         vdd         -2474.325         -481         45           64         ID1         -2394.525         -481         45           65         vss         -2314.725         -481         45           66         vss         -2254.725         -481         45           67         vss         -2194.725         -481         45           68         vss         -2134.725         -481         45           69         vss         -2074.725         -481	87 87 87 87 87 87 87 87 87 87 87 87 87 8
55         vdd         -3302.725         -481         45           56         WR1         -3222.925         -481         65           57         BM1         -3141.325         -481         65           58         vdd         -3061.525         -481         45           59         BM0         -2981.725         -481         65           60         TST4         -2901.925         -481         45           61         TST4         -2841.925         -481         45           62         ID0         -2554.125         -481         65           63         vdd         -2474.325         -481         45           64         ID1         -2394.525         -481         45           65         vss         -2314.725         -481         45           66         vss         -2254.725         -481         45           67         vss         -2194.725         -481         45           68         vss         -2134.725         -481         45           69         vss         -2074.725         -481         45           70         vss         -2014.725         -481	87 87 87 87 87 87 87 87 87 87 87 87 87
56         WR1         -3222.925         -481         65           57         BM1         -3141.325         -481         65           58         vdd         -3061.525         -481         45           59         BM0         -2981.725         -481         65           60         TST4         -2901.925         -481         45           61         TST4         -2841.925         -481         45           62         ID0         -2554.125         -481         65           63         vdd         -2474.325         -481         45           64         ID1         -2394.525         -481         65           65         vss         -2314.725         -481         45           66         vss         -2254.725         -481         45           67         vss         -2194.725         -481         45           68         vss         -2134.725         -481         45           69         vss         -2074.725         -481         45           70         vss         -2014.725         -481         45           71         vss         -1954.725         -481	87 87 87 87 87 87 87 87 87 87 87 87
57         BM1         -3141.325         -481         65           58         vdd         -3061.525         -481         45           59         BM0         -2981.725         -481         65           60         TST4         -2901.925         -481         45           61         TST4         -2841.925         -481         45           62         ID0         -2554.125         -481         65           63         vdd         -2474.325         -481         45           64         ID1         -2394.525         -481         65           65         vss         -2314.725         -481         45           66         vss         -2254.725         -481         45           67         vss         -2194.725         -481         45           68         vss         -2134.725         -481         45           69         vss         -2074.725         -481         45           70         vss         -2014.725         -481         45           71         vss         -1954.725         -481         45           72         vss         -1894.725         -481	87 87 87 87 87 87 87 87 87 87 87
58         vdd         -3061.525         -481         45           59         BM0         -2981.725         -481         65           60         TST4         -2901.925         -481         45           61         TST4         -2841.925         -481         45           62         ID0         -2554.125         -481         65           63         vdd         -2474.325         -481         45           64         ID1         -2394.525         -481         65           65         vss         -2314.725         -481         45           66         vss         -2254.725         -481         45           67         vss         -2194.725         -481         45           68         vss         -2134.725         -481         45           69         vss         -2074.725         -481         45           70         vss         -2014.725         -481         45           71         vss         -1954.725         -481         45           72         vss         -1894.725         -481         45	87 87 87 87 87 87 87 87 87 87
59         BM0         -2981.725         -481         65           60         TST4         -2901.925         -481         45           61         TST4         -2841.925         -481         45           62         ID0         -2554.125         -481         65           63         vdd         -2474.325         -481         45           64         ID1         -2394.525         -481         65           65         vss         -2314.725         -481         45           66         vss         -2254.725         -481         45           67         vss         -2194.725         -481         45           68         vss         -2134.725         -481         45           69         vss         -2074.725         -481         45           70         vss         -2014.725         -481         45           71         vss         -1954.725         -481         45           72         vss         -1894.725         -481         45           73         vss         -1834.725         -481         45	87 87 87 87 87 87 87 87 87 87
60         TST4         -2901.925         -481         45           61         TST4         -2841.925         -481         45           62         ID0         -2554.125         -481         65           63         vdd         -2474.325         -481         45           64         ID1         -2394.525         -481         65           65         vss         -2314.725         -481         45           66         vss         -2254.725         -481         45           67         vss         -2194.725         -481         45           68         vss         -2134.725         -481         45           69         vss         -2074.725         -481         45           70         vss         -2014.725         -481         45           71         vss         -1954.725         -481         45           72         vss         -1894.725         -481         45           73         vss         -1834.725         -481         45	87 87 87 87 87 87 87 87 87
61 TST4 -2841.925 -481 45 62 ID0 -2554.125 -481 65 63 vdd -2474.325 -481 45 64 ID1 -2394.525 -481 65 65 vss -2314.725 -481 45 66 vss -2254.725 -481 45 67 vss -2194.725 -481 45 68 vss -2134.725 -481 45 69 vss -2014.725 -481 45 70 vss -2014.725 -481 45 71 vss -1954.725 -481 45 72 vss -1894.725 -481 45 73 vss -1834.725 -481 45	87 87 87 87 87 87 87 87
62         ID0         -2554.125         -481         65           63         vdd         -2474.325         -481         45           64         ID1         -2394.525         -481         65           65         vss         -2314.725         -481         45           66         vss         -2254.725         -481         45           67         vss         -2194.725         -481         45           68         vss         -2134.725         -481         45           69         vss         -2074.725         -481         45           70         vss         -2014.725         -481         45           71         vss         -1954.725         -481         45           72         vss         -1894.725         -481         45           73         vss         -1834.725         -481         45	87 87 87 87 87 87 87
63         vdd         -2474.325         -481         45           64         ID1         -2394.525         -481         65           65         vss         -2314.725         -481         45           66         vss         -2254.725         -481         45           67         vss         -2194.725         -481         45           68         vss         -2134.725         -481         45           69         vss         -2074.725         -481         45           70         vss         -2014.725         -481         45           71         vss         -1954.725         -481         45           72         vss         -1894.725         -481         45           73         vss         -1834.725         -481         45	87 87 87 87 87 87
64         ID1         -2394.525         -481         65           65         vss         -2314.725         -481         45           66         vss         -2254.725         -481         45           67         vss         -2194.725         -481         45           68         vss         -2134.725         -481         45           69         vss         -2074.725         -481         45           70         vss         -2014.725         -481         45           71         vss         -1954.725         -481         45           72         vss         -1894.725         -481         45           73         vss         -1834.725         -481         45	87 87 87 87 87
65	87 87 87 87
66         vss         -2254.725         -481         45           67         vss         -2194.725         -481         45           68         vss         -2134.725         -481         45           69         vss         -2074.725         -481         45           70         vss         -2014.725         -481         45           71         vss         -1954.725         -481         45           72         vss         -1894.725         -481         45           73         vss         -1834.725         -481         45	87 87 87 87
67 vss -2194.725 -481 45 68 vss -2134.725 -481 45 69 vss -2074.725 -481 45 70 vss -2014.725 -481 45 71 vss -1954.725 -481 45 72 vss -1894.725 -481 45 73 vss -1834.725 -481 45	87 87 87
68 vss -2134.725 -481 45 69 vss -2074.725 -481 45 70 vss -2014.725 -481 45 71 vss -1954.725 -481 45 72 vss -1894.725 -481 45 73 vss -1834.725 -481 45	87 87
69         vss         -2074.725         -481         45           70         vss         -2014.725         -481         45           71         vss         -1954.725         -481         45           72         vss         -1894.725         -481         45           73         vss         -1834.725         -481         45	87
70         vss         -2014.725         -481         45           71         vss         -1954.725         -481         45           72         vss         -1894.725         -481         45           73         vss         -1834.725         -481         45	
71 vss -1954.725 -481 45 72 vss -1894.725 -481 45 73 vss -1834.725 -481 45	01
72 vss -1894.725 -481 45 73 vss -1834.725 -481 45	87
73 vss -1834.725 -481 45	87
	87
74 vss -1774.725 -481 45	87
75 vss -1714.725 -481 45	87
76 vss2 -1541.725 -481 45	87
77 vss2 -1481.725 -481 45	87
78 vss2 -1421.725 -481 45	87
79 vss2 -1361.725 -481 45	87
80 vss2 -1301.725 -481 45	87
81 vss2 -1241.725 -481 45	87
82 vss2 -1181.725 -481 45	87
83 vss2 -1121.725 -481 45	87
84 vss2 -1061.725 -481 45	87
85 vss2 -1001.725 -481 45	87
86 vss2 -941.725 -481 45	87
87 vdd2 -881.725 -481 45	87
88 vdd2 -821.725 -481 45	87
89 vdd2 -761.725 -481 45	87
90 vdd2 -701.725 -481 45	87
91 vdd2 -641.725 -481 45	87
92 vdd2 -581.725 -481 45	87
93 vdd2 -521.725 -481 45	87
94 vdd2 -461.725 -481 45	87
95 vdd2 -401.725 -481 45	87
96 vdd2 -341.725 -481 45	87
97 DUMMY -163.375 -481 45	87
98 vdd3 14.975 -481 45	87
99 vdd3 74.975 -481 45	87
100 vdd3 134.975 -481 45	87
101 vdd3 194.975 -481 45	87
102 vdd 254.975 -481 45	87

103	ш	Ded	V	V	18/	- 11
104	#	Pad	X	Y	W	H
105         Vdd         434.975         -481         45         87           106         Vdd         494.975         -481         45         87           107         Vdd         554.975         -481         45         87           108         Vdd         614.975         -481         45         87           109         Vdd         674.975         -481         45         87           110         Vdd         734.975         -481         45         87           111         Vdd         794.975         -481         45         87           112         Vdd         854.975         -481         45         87           113         DUMMY         1100.425         -481         45         87           114         DUMMY         1120.425         -481         45         87           115         DUMMY         1340.425         -481         4						
106         vdd         494.975         -481         45         87           107         vdd         554.975         -481         45         87           108         vdd         614.975         -481         45         87           109         vdd         674.975         -481         45         87           110         vdd         734.975         -481         45         87           111         vdd         794.975         -481         45         87           112         vdd         854.975         -481         45         87           114         DUMMY         1100.425         -481         45         87           114         DUMMY         1120.425         -481         45         87           115         DUMMY         1220.425         -481         45         87           117         DUMMY         1460.425         -481 <t< td=""><td></td><td></td><td></td><td></td><td></td><td></td></t<>						
107         vdd         554.975         -481         45         87           108         vdd         614.975         -481         45         87           109         vdd         674.975         -481         45         87           110         vdd         734.975         -481         45         87           111         vdd         794.975         -481         45         87           112         vdd         854.975         -481         45         87           113         DUMMY         1040.425         -481         45         87           114         DUMMY         1100.425         -481         45         87           115         DUMMY         1160.425         -481         45         87           116         DUMMY         1204.25         -481         45         87           117         DUMMY         1280.425         -481         45         87           117         DUMMY         1400.425         -481         45         87           118         DUMMY         1460.425         -481         45         87           120         DUMMY         1460.425         -481						
108         Vdd         614.975         -481         45         87           109         Vdd         674.975         -481         45         87           110         Vdd         734.975         -481         45         87           111         Vdd         794.975         -481         45         87           112         Vdd         854.975         -481         45         87           113         DUMMY         1040.425         -481         45         87           114         DUMMY         1100.425         -481         45         87           115         DUMMY         1160.425         -481         45         87           116         DUMMY         1280.425         -481         45         87           117         DUMMY         1340.425         -481         45         87           118         DUMMY         1400.425         -481         45         87           119         DUMMY         1400.425         -481         45         87           120         DUMMY         1400.425         -481         45         87           121         TST2         1650.475         -481 </td <td>_</td> <td></td> <td></td> <td></td> <td></td> <td></td>	_					
109         vdd         674.975         -481         45         87           110         vdd         734.975         -481         45         87           111         vdd         794.975         -481         45         87           112         vdd         854.975         -481         45         87           113         DUMMY         1040.425         -481         45         87           114         DUMMY         1100.425         -481         45         87           115         DUMMY         1160.425         -481         45         87           116         DUMMY         1220.425         -481         45         87           117         DUMMY         1280.425         -481         45         87           118         DUMMY         1340.425         -481         45         87           119         DUMMY         1400.425         -481         45         87           120         DUMMY         1400.425         -481         45         87           121         TST2         1650.475         -481         45         87           122         TST1         1710.475         -481						
110         vdd         734.975         -481         45         87           111         vdd         794.975         -481         45         87           112         vdd         854.975         -481         45         87           113         DUMMY         1040.425         -481         45         87           114         DUMMY         1100.425         -481         45         87           115         DUMMY         1160.425         -481         45         87           116         DUMMY         1220.425         -481         45         87           117         DUMMY         1280.425         -481         45         87           118         DUMMY         1340.425         -481         45         87           119         DUMMY         1460.425         -481         45         87           120         DUMMY         1460.425         -481         45         87           121         TST2         1650.475         -481         45         87           122         TST1         1710.475         -481         45         87           123         VLCDIN         2110.35         -						
111         vdd         794.975         -481         45         87           112         vdd         854.975         -481         45         87           113         DUMMY         1040.425         -481         45         87           114         DUMMY         1100.425         -481         45         87           115         DUMMY         1160.425         -481         45         87           116         DUMMY         1220.425         -481         45         87           117         DUMMY         1280.425         -481         45         87           118         DUMMY         1340.425         -481         45         87           119         DUMMY         1460.425         -481         45         87           120         DUMMY         1460.425         -481         45         87           121         TST2         1650.475         -481         45         87           122         TST1         1710.476         -481         45         87           122         TST1         1710.475         -481         45         87           123         VLCDIN         2110.35 <td< td=""><td></td><td></td><td></td><td></td><td></td><td></td></td<>						
1112         Vdd         854.975         -481         45         87           113         DUMMY         1040.425         -481         45         87           114         DUMMY         1100.425         -481         45         87           115         DUMMY         1160.425         -481         45         87           116         DUMMY         1220.425         -481         45         87           117         DUMMY         1280.425         -481         45         87           118         DUMMY         1340.425         -481         45         87           119         DUMMY         1400.425         -481         45         87           120         DUMMY         1460.425         -481         45         87           121         TST2         1650.475         -481         45         87           122         TST1         1710.475         -481         45         87           122         TST1         1710.475         -481         45         87           122         TST1         1710.475         -481         45         87           123         VLCDIN         2110.35	$\vdash$					
113         DUMMY         1040.425         -481         45         87           114         DUMMY         1100.425         -481         45         87           115         DUMMY         1160.425         -481         45         87           116         DUMMY         1220.425         -481         45         87           117         DUMMY         1280.425         -481         45         87           118         DUMMY         1340.425         -481         45         87           119         DUMMY         1460.425         -481         45         87           120         DUMMY         1460.425         -481         45         87           121         TST2         1650.475         -481         45         87           121         TST2         1650.475         -481         45         87           122         TST1         1710.475         -481         45         87           122         TST1         1710.475         -481         45         87           123         VLCDIN         2110.35         -481         45         87           125         VLCDOUT         2230.35			_			
114         DUMMY         1100.425         -481         45         87           115         DUMMY         1160.425         -481         45         87           116         DUMMY         1220.425         -481         45         87           117         DUMMY         1280.425         -481         45         87           118         DUMMY         1340.425         -481         45         87           119         DUMMY         1460.425         -481         45         87           120         DUMMY         1460.425         -481         45         87           121         TST2         1650.475         -481         45         87           121         TST2         1650.475         -481         45         87           122         TST1         1710.475         -481         45         87           122         TST1         1710.475         -481         45         87           122         TST1         1710.475         -481         45         87           123         VLCDIN         2110.35         -481         45         87           124         VLCDOUT         2230.35						
115         DUMMY         1160.425         -481         45         87           116         DUMMY         1220.425         -481         45         87           117         DUMMY         1280.425         -481         45         87           118         DUMMY         1340.425         -481         45         87           119         DUMMY         1460.425         -481         45         87           120         DUMMY         1460.425         -481         45         87           121         TST2         1650.475         -481         45         87           121         TST2         1650.475         -481         45         87           122         TST1         1710.475         -481         45         87           123         VLCDIN         210.35         -481         45         87           125         VLCDOUT         2230.35						
116         DUMMY         1220.425         -481         45         87           117         DUMMY         1280.425         -481         45         87           118         DUMMY         1340.425         -481         45         87           119         DUMMY         1460.425         -481         45         87           120         DUMMY         1460.425         -481         45         87           121         TST2         1650.475         -481         45         87           122         TST1         1710.475         -481         45         87           123         VLCDIN         2050.35         -481         45         87           123         VLCDIN         2110.35         -481         45         87           124         VLCDOUT         2230.35         -481         45         87           125         VLCDOUT         2230.35         -481         45         87           126         VLCDOUT         2230.35         -481         45         87           127         VAO-         2642.35         -481         45         87           129         VAO-         2762.35						
117         DUMMY         1280.425         -481         45         87           118         DUMMY         1340.425         -481         45         87           119         DUMMY         1460.425         -481         45         87           120         DUMMY         1460.425         -481         45         87           121         TST2         1650.475         -481         45         87           122         TST1         1710.475         -481         45         87           123         VLCDIN         2050.35         -481         45         87           124         VLCDIN         2110.35         -481         45         87           125         VLCDOUT         2170.35         -481         45         87           126         VLCDOUT         2230.35         -481         45         87           127         VA0-         2642.35         -481         45         87           128         VA0-         2762.35         -481         45         87           130         VA0-         2822.35         -481         45         87           131         VA1-         2882.35 <t< td=""><td></td><td></td><td></td><td></td><td></td><td></td></t<>						
118         DUMMY         1340.425         -481         45         87           119         DUMMY         1400.425         -481         45         87           120         DUMMY         1460.425         -481         45         87           121         TST2         1650.475         -481         45         87           122         TST1         1710.475         -481         45         87           122         TST1         1710.475         -481         45         87           123         VLCDIN         2050.35         -481         45         87           124         VLCDIN         2110.35         -481         45         87           125         VLCDOUT         2170.35         -481         45         87           126         VLCDOUT         2230.35         -481         45         87           127         VA0-         2642.35         -481         45         87           128         VA0-         2762.35         -481         45         87           130         VA0-         2822.35         -481         45         87           131         VA1-         2942.35 <td< td=""><td></td><td></td><td>_</td><td></td><td></td><td></td></td<>			_			
119         DUMMY         1400.425         -481         45         87           120         DUMMY         1460.425         -481         45         87           121         TST2         1650.475         -481         45         87           122         TST1         1710.475         -481         45         87           123         VLCDIN         2050.35         -481         45         87           124         VLCDIN         2110.35         -481         45         87           125         VLCDOUT         2170.35         -481         45         87           126         VLCDOUT         2230.35         -481         45         87           127         VA0-         2642.35         -481         45         87           128         VA0-         2702.35         -481         45         87           129         VA0-         2762.35         -481         45         87           130         VA0-         2822.35         -481         45         87           131         VA1-         2882.35         -481         45         87           132         VA1-         3002.35         -4						
120         DUMMY         1460.425         -481         45         87           121         TST2         1650.475         -481         45         87           122         TST1         1710.475         -481         45         87           123         VLCDIN         2050.35         -481         45         87           124         VLCDIN         2110.35         -481         45         87           125         VLCDOUT         2170.35         -481         45         87           126         VLCDOUT         2230.35         -481         45         87           127         VA0-         2642.35         -481         45         87           128         VA0-         2702.35         -481         45         87           129         VA0-         2762.35         -481         45         87           130         VA0-         2822.35         -481         45         87           131         VA1-         2882.35         -481         45         87           132         VA1-         2942.35         -481         45         87           133         VA1-         3062.35         -481	$\vdash$					
121         TST2         1650.475         -481         45         87           122         TST1         1710.475         -481         45         87           123         VLCDIN         2050.35         -481         45         87           124         VLCDIN         2110.35         -481         45         87           125         VLCDOUT         2170.35         -481         45         87           126         VLCDOUT         2230.35         -481         45         87           127         VA0-         2642.35         -481         45         87           128         VA0-         2702.35         -481         45         87           129         VA0-         2762.35         -481         45         87           130         VA0-         2822.35         -481         45         87           131         VA1-         2882.35         -481         45         87           132         VA1-         2942.35         -481         45         87           133         VA1-         3002.35         -481         45         87           134         VA1-         3062.35         -481 </td <td><math>\vdash</math></td> <td></td> <td></td> <td></td> <td></td> <td></td>	$\vdash$					
122         TST1         1710.475         -481         45         87           123         VLCDIN         2050.35         -481         45         87           124         VLCDIN         2110.35         -481         45         87           125         VLCDOUT         2170.35         -481         45         87           126         VLCDOUT         2230.35         -481         45         87           127         VA0-         2642.35         -481         45         87           128         VA0-         2762.35         -481         45         87           129         VA0-         2762.35         -481         45         87           130         VA0-         2822.35         -481         45         87           131         VA1-         2882.35         -481         45         87           132         VA1-         2942.35         -481         45         87           133         VA1-         3002.35         -481         45         87           134         VA1-         3062.35         -481         45         87           135         VA1+         3462.35         -481 <td><math>\vdash</math></td> <td></td> <td></td> <td></td> <td></td> <td></td>	$\vdash$					
123         VLCDIN         2050.35         -481         45         87           124         VLCDIN         2110.35         -481         45         87           125         VLCDOUT         2170.35         -481         45         87           126         VLCDOUT         2230.35         -481         45         87           127         VA0-         2642.35         -481         45         87           128         VA0-         2762.35         -481         45         87           129         VA0-         2762.35         -481         45         87           130         VA0-         2822.35         -481         45         87           131         VA1-         2882.35         -481         45         87           132         VA1-         2942.35         -481         45         87           133         VA1-         2942.35         -481         45         87           134         VA1-         3062.35         -481         45         87           135         VA1+         3462.35         -481         45         87           136         VA1+         3462.35         -481 <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>						
124         VLCDIN         2110.35         -481         45         87           125         VLCDOUT         2170.35         -481         45         87           126         VLCDOUT         2230.35         -481         45         87           127         VA0-         2642.35         -481         45         87           128         VA0-         2762.35         -481         45         87           129         VA0-         2762.35         -481         45         87           130         VA0-         2822.35         -481         45         87           131         VA1-         2882.35         -481         45         87           132         VA1-         2942.35         -481         45         87           133         VA1-         3002.35         -481         45         87           134         VA1-         3062.35         -481         45         87           135         VA1+         3402.35         -481         45         87           135         VA1+         3462.35         -481         45         87           137         VA1+         3522.35         -481			1710.475			87
125         VLCDOUT         2170.35         -481         45         87           126         VLCDOUT         2230.35         -481         45         87           127         VA0-         2642.35         -481         45         87           128         VA0-         2762.35         -481         45         87           129         VA0-         2762.35         -481         45         87           130         VA0-         2822.35         -481         45         87           131         VA1-         2882.35         -481         45         87           132         VA1-         2942.35         -481         45         87           133         VA1-         3002.35         -481         45         87           134         VA1-         3062.35         -481         45         87           135         VA1+         3402.35         -481         45         87           136         VA1+         3462.35         -481         45         87           137         VA1+         3522.35         -481         45         87           139         VA0+         3642.35         -481	-		2050.35			87
126         VLCDOUT         2230.35         -481         45         87           127         VA0-         2642.35         -481         45         87           128         VA0-         2702.35         -481         45         87           129         VA0-         2762.35         -481         45         87           130         VA0-         2822.35         -481         45         87           131         VA1-         2882.35         -481         45         87           132         VA1-         2942.35         -481         45         87           133         VA1-         3002.35         -481         45         87           134         VA1-         3062.35         -481         45         87           135         VA1+         3402.35         -481         45         87           136         VA1+         3462.35         -481         45         87           137         VA1+         3522.35         -481         45         87           139         VA0+         3642.35         -481         45         87           140         VA0+         3702.35         -481	-	VLCDIN	2110.35	-481	45	87
127         VA0-         2642.35         -481         45         87           128         VA0-         2702.35         -481         45         87           129         VA0-         2762.35         -481         45         87           130         VA0-         2822.35         -481         45         87           131         VA1-         2882.35         -481         45         87           132         VA1-         2942.35         -481         45         87           133         VA1-         3002.35         -481         45         87           134         VA1-         3062.35         -481         45         87           135         VA1+         3402.35         -481         45         87           136         VA1+         3402.35         -481         45         87           137         VA1+         3522.35         -481         45         87           138         VA1+         3582.35         -481         45         87           140         VA0+         3702.35         -481         45         87           141         VA0+         3762.35         -481		VLCDOUT	2170.35	-481	45	87
128         VA0-         2702.35         -481         45         87           129         VA0-         2762.35         -481         45         87           130         VA0-         2822.35         -481         45         87           131         VA1-         2882.35         -481         45         87           132         VA1-         2942.35         -481         45         87           133         VA1-         3002.35         -481         45         87           134         VA1-         3062.35         -481         45         87           135         VA1+         3402.35         -481         45         87           136         VA1+         3402.35         -481         45         87           137         VA1+         3522.35         -481         45         87           138         VA1+         3582.35         -481         45         87           139         VA0+         3642.35         -481         45         87           140         VA0+         3702.35         -481         45         87           141         VA0+         3822.35         -481	126	VLCDOUT	2230.35	-481	45	87
129         VA0-         2762.35         -481         45         87           130         VA0-         2822.35         -481         45         87           131         VA1-         2882.35         -481         45         87           132         VA1-         2942.35         -481         45         87           133         VA1-         3002.35         -481         45         87           134         VA1-         3062.35         -481         45         87           135         VA1+         3402.35         -481         45         87           136         VA1+         3462.35         -481         45         87           137         VA1+         3522.35         -481         45         87           138         VA1+         3582.35         -481         45         87           139         VA0+         3642.35         -481         45         87           140         VA0+         3702.35         -481         45         87           141         VA0+         3762.35         -481         45         87           142         VA0+         3822.35         -481	127	VA0-	2642.35	-481	45	87
130         VA0-         2822.35         -481         45         87           131         VA1-         2882.35         -481         45         87           132         VA1-         2942.35         -481         45         87           133         VA1-         3002.35         -481         45         87           134         VA1-         3062.35         -481         45         87           135         VA1+         3402.35         -481         45         87           136         VA1+         3462.35         -481         45         87           137         VA1+         3522.35         -481         45         87           138         VA1+         3582.35         -481         45         87           139         VA0+         3642.35         -481         45         87           140         VA0+         3702.35         -481         45         87           141         VA0+         3762.35         -481         45         87           142         VA0+         3822.35         -481         45         87           142         VA0+         3822.35         -481	128	VA0-	2702.35	-481	45	87
131         VA1-         2882.35         -481         45         87           132         VA1-         2942.35         -481         45         87           133         VA1-         3002.35         -481         45         87           134         VA1-         3062.35         -481         45         87           135         VA1+         3402.35         -481         45         87           136         VA1+         3462.35         -481         45         87           137         VA1+         3522.35         -481         45         87           138         VA1+         3582.35         -481         45         87           139         VA0+         3642.35         -481         45         87           140         VA0+         3702.35         -481         45         87           141         VA0+         3762.35         -481         45         87           142         VA0+         3822.35         -481         45         87           143         VB0-         4162.35         -481         45         87           144         VB0-         4222.35         -481	129	VA0-	2762.35	-481	45	87
132         VA1-         2942.35         -481         45         87           133         VA1-         3002.35         -481         45         87           134         VA1-         3062.35         -481         45         87           135         VA1+         3402.35         -481         45         87           136         VA1+         3462.35         -481         45         87           137         VA1+         3522.35         -481         45         87           138         VA1+         3582.35         -481         45         87           139         VA0+         3642.35         -481         45         87           140         VA0+         3702.35         -481         45         87           141         VA0+         3762.35         -481         45         87           142         VA0+         3822.35         -481         45         87           143         VB0-         4162.35         -481         45         87           144         VB0-         4222.35         -481         45         87           145         VB0-         4342.35         -481	130	VA0-	2822.35	-481	45	87
133         VA1-         3002.35         -481         45         87           134         VA1-         3062.35         -481         45         87           135         VA1+         3402.35         -481         45         87           136         VA1+         3462.35         -481         45         87           137         VA1+         3522.35         -481         45         87           138         VA1+         3582.35         -481         45         87           139         VA0+         3642.35         -481         45         87           140         VA0+         3702.35         -481         45         87           141         VA0+         3762.35         -481         45         87           142         VA0+         3822.35         -481         45         87           143         VB0-         4162.35         -481         45         87           144         VB0-         4222.35         -481         45         87           145         VB0-         4282.35         -481         45         87           146         VB0-         4342.35         -481	131		2882.35	-481	45	87
134         VA1-         3062.35         -481         45         87           135         VA1+         3402.35         -481         45         87           136         VA1+         3462.35         -481         45         87           137         VA1+         3522.35         -481         45         87           138         VA1+         3582.35         -481         45         87           139         VA0+         3642.35         -481         45         87           140         VA0+         3702.35         -481         45         87           141         VA0+         3762.35         -481         45         87           142         VA0+         3822.35         -481         45         87           143         VB0-         4162.35         -481         45         87           144         VB0-         4222.35         -481         45         87           145         VB0-         4282.35         -481         45         87           146         VB0-         4342.35         -481         45         87           148         VB1-         4462.35         -481	132	VA1-	2942.35	-481	45	87
135         VA1+         3402.35         -481         45         87           136         VA1+         3462.35         -481         45         87           137         VA1+         3522.35         -481         45         87           138         VA1+         3582.35         -481         45         87           139         VA0+         3642.35         -481         45         87           140         VA0+         3702.35         -481         45         87           141         VA0+         3762.35         -481         45         87           142         VA0+         3822.35         -481         45         87           143         VB0-         4162.35         -481         45         87           144         VB0-         4222.35         -481         45         87           145         VB0-         4282.35         -481         45         87           146         VB0-         4342.35         -481         45         87           147         VB1-         4402.35         -481         45         87           148         VB1-         4522.35         -481	133	VA1-	3002.35	-481	45	87
136         VA1+         3462.35         -481         45         87           137         VA1+         3522.35         -481         45         87           138         VA1+         3582.35         -481         45         87           139         VA0+         3642.35         -481         45         87           140         VA0+         3702.35         -481         45         87           141         VA0+         3762.35         -481         45         87           142         VA0+         3822.35         -481         45         87           143         VB0-         4162.35         -481         45         87           144         VB0-         4222.35         -481         45         87           145         VB0-         4282.35         -481         45         87           146         VB0-         4342.35         -481         45         87           147         VB1-         4402.35         -481         45         87           148         VB1-         4522.35         -481         45         87           149         VB1-         4582.35         -481	134	VA1-	3062.35	-481	45	87
137         VA1+         3522.35         -481         45         87           138         VA1+         3582.35         -481         45         87           139         VA0+         3642.35         -481         45         87           140         VA0+         3702.35         -481         45         87           141         VA0+         3762.35         -481         45         87           142         VA0+         3822.35         -481         45         87           143         VB0-         4162.35         -481         45         87           144         VB0-         4222.35         -481         45         87           145         VB0-         4282.35         -481         45         87           146         VB0-         4342.35         -481         45         87           147         VB1-         4402.35         -481         45         87           148         VB1-         4462.35         -481         45         87           149         VB1-         4522.35         -481         45         87           150         VB1+         4922.35         -481	135	VA1+	3402.35	-481	45	87
138         VA1+         3582.35         -481         45         87           139         VA0+         3642.35         -481         45         87           140         VA0+         3702.35         -481         45         87           141         VA0+         3762.35         -481         45         87           142         VA0+         3822.35         -481         45         87           143         VB0-         4162.35         -481         45         87           144         VB0-         4222.35         -481         45         87           145         VB0-         4282.35         -481         45         87           146         VB0-         4342.35         -481         45         87           147         VB1-         4402.35         -481         45         87           148         VB1-         4462.35         -481         45         87           149         VB1-         4522.35         -481         45         87           150         VB1-         4582.35         -481         45         87           151         VB1+         4922.35         -481	136	VA1+	3462.35	-481	45	87
139         VA0+         3642.35         -481         45         87           140         VA0+         3702.35         -481         45         87           141         VA0+         3762.35         -481         45         87           142         VA0+         3822.35         -481         45         87           143         VB0-         4162.35         -481         45         87           144         VB0-         4222.35         -481         45         87           145         VB0-         4282.35         -481         45         87           146         VB0-         4342.35         -481         45         87           147         VB1-         4402.35         -481         45         87           148         VB1-         4462.35         -481         45         87           149         VB1-         4582.35         -481         45         87           150         VB1+         4922.35         -481         45         87           152         VB1+         4982.35         -481         45         87	137	VA1+	3522.35	-481	45	87
140         VA0+         3702.35         -481         45         87           141         VA0+         3762.35         -481         45         87           142         VA0+         3822.35         -481         45         87           143         VB0-         4162.35         -481         45         87           144         VB0-         4222.35         -481         45         87           145         VB0-         4282.35         -481         45         87           146         VB0-         4342.35         -481         45         87           147         VB1-         4402.35         -481         45         87           148         VB1-         4462.35         -481         45         87           149         VB1-         4522.35         -481         45         87           150         VB1-         4582.35         -481         45         87           151         VB1+         4922.35         -481         45         87           152         VB1+         4982.35         -481         45         87						
141         VA0+         3762.35         -481         45         87           142         VA0+         3822.35         -481         45         87           143         VB0-         4162.35         -481         45         87           144         VB0-         4222.35         -481         45         87           145         VB0-         4282.35         -481         45         87           146         VB0-         4342.35         -481         45         87           147         VB1-         4402.35         -481         45         87           148         VB1-         4462.35         -481         45         87           149         VB1-         4522.35         -481         45         87           150         VB1-         4582.35         -481         45         87           151         VB1+         4922.35         -481         45         87           152         VB1+         4982.35         -481         45         87	139	VA0+	3642.35	-481	45	87
142         VA0+         3822.35         -481         45         87           143         VB0-         4162.35         -481         45         87           144         VB0-         4222.35         -481         45         87           145         VB0-         4282.35         -481         45         87           146         VB0-         4342.35         -481         45         87           147         VB1-         4402.35         -481         45         87           148         VB1-         4462.35         -481         45         87           149         VB1-         4522.35         -481         45         87           150         VB1-         4582.35         -481         45         87           151         VB1+         4922.35         -481         45         87           152         VB1+         4982.35         -481         45         87	140	VA0+	3702.35	-481	45	87
143         VB0-         4162.35         -481         45         87           144         VB0-         4222.35         -481         45         87           145         VB0-         4282.35         -481         45         87           146         VB0-         4342.35         -481         45         87           147         VB1-         4402.35         -481         45         87           148         VB1-         4462.35         -481         45         87           149         VB1-         4522.35         -481         45         87           150         VB1-         4582.35         -481         45         87           151         VB1+         4922.35         -481         45         87           152         VB1+         4982.35         -481         45         87	141	VA0+	3762.35	-481	45	87
144         VB0-         4222.35         -481         45         87           145         VB0-         4282.35         -481         45         87           146         VB0-         4342.35         -481         45         87           147         VB1-         4402.35         -481         45         87           148         VB1-         4462.35         -481         45         87           149         VB1-         4522.35         -481         45         87           150         VB1-         4582.35         -481         45         87           151         VB1+         4922.35         -481         45         87           152         VB1+         4982.35         -481         45         87	142	VA0+	3822.35	-481	45	87
145         VB0-         4282.35         -481         45         87           146         VB0-         4342.35         -481         45         87           147         VB1-         4402.35         -481         45         87           148         VB1-         4462.35         -481         45         87           149         VB1-         4522.35         -481         45         87           150         VB1-         4582.35         -481         45         87           151         VB1+         4922.35         -481         45         87           152         VB1+         4982.35         -481         45         87	143	VB0-	4162.35	-481	45	87
146         VB0-         4342.35         -481         45         87           147         VB1-         4402.35         -481         45         87           148         VB1-         4462.35         -481         45         87           149         VB1-         4522.35         -481         45         87           150         VB1-         4582.35         -481         45         87           151         VB1+         4922.35         -481         45         87           152         VB1+         4982.35         -481         45         87	144	VB0-	4222.35	-481	45	87
147         VB1-         4402.35         -481         45         87           148         VB1-         4462.35         -481         45         87           149         VB1-         4522.35         -481         45         87           150         VB1-         4582.35         -481         45         87           151         VB1+         4922.35         -481         45         87           152         VB1+         4982.35         -481         45         87	145	VB0-	4282.35	-481	45	87
148         VB1-         4462.35         -481         45         87           149         VB1-         4522.35         -481         45         87           150         VB1-         4582.35         -481         45         87           151         VB1+         4922.35         -481         45         87           152         VB1+         4982.35         -481         45         87	146	VB0-	4342.35	-481	45	87
149         VB1-         4522.35         -481         45         87           150         VB1-         4582.35         -481         45         87           151         VB1+         4922.35         -481         45         87           152         VB1+         4982.35         -481         45         87	147	VB1-	4402.35	-481	45	87
150     VB1-     4582.35     -481     45     87       151     VB1+     4922.35     -481     45     87       152     VB1+     4982.35     -481     45     87	148	VB1-	4462.35	-481	45	87
151         VB1+         4922.35         -481         45         87           152         VB1+         4982.35         -481         45         87	149	VB1-	4522.35	-481	45	87
152 VB1+ 4982.35 -481 45 87	150	VB1-	4582.35	-481	45	87
	151	VB1+	4922.35	-481	45	87
1-0 1-0 1-0 1-0 1-0 1-0 1-0 1-0 1-0 1-0	152	VB1+	4982.35	-481	45	87
153   VB1+   5042.35   -481   45   87	153	VB1+	5042.35	-481	45	87
154 VB1+ 5102.35 -481 45 87	154	VB1+	5102.35	-481	45	87
155 VB0+ 5162.35 -481 45 87						

#	Pad	Х	Υ	W	Н
156	VB0+	5222.35	-481	45	87
157	VB0+	5282.35	-481	45	87
158	VB0+	5342.35	-481	45	87
159	COM160	5643	-487.75	25	75.5
160	COM158	5681	-487.75	25	75.5
161	COM156	5719	-487.75	25	75.5
162	COM154	5757	-487.75	25	75.5
163	COM154	5795	-487.75	25	75.5
164	COM150	5833	-487.75	25	75.5
165	COM148	5871	-487.75	25	75.5
166	COM146	5909	-487.75	25	75.5
167	COM144	5947	-487.75	25	75.5
168	COM144	5985	-487.75	25	75.5
169	COM142	6023	-487.75	25	75.5
170	COM140	6061	-487.75	25	75.5
171	COM136	6099	-487.75	25	75.5
172	COM136 COM134	6137	-487.75	25	75.5
173	COM134 COM132	6175	-487.75	25	
174	COM132	6213	-487.75	25	75.5 75.5
175	COM130	6251	-487.75	25	75.5
+	COM126	6289			
176			-487.75	25	75.5
177	COM124	6327	-487.75	25	75.5
178	COM122	6365	-487.75	25 25	75.5 75.5
179	COM120	6403	-487.75		
180	COM118	6441	-487.75	25	75.5
181	COM116	6479	-487.75	25	75.5
182	COM114	6517	-487.75	25	75.5
183 184	COM112 COM110	6555 6593	-487.75	25 25	75.5
185	COM110		-487.75	25	75.5
$\vdash$		6631	-487.75		75.5
186	COM106 COM104	6669	-487.75	25	75.5
187		6707	-487.75	25	75.5
188 189	COM102 DUMMY	6745 6785.5	-487.75	25 30	75.5 75.5
190	DUMMY	6785.5	-487.75 487.75	30	75.5
191	COM100	6745	487.75		
-				25	75.5
192 193	COM98 COM96	6707 6669	487.75 487.75	25 25	75.5 75.5
194	COM94	6631	487.75	25	75.5
195	COM92	6593	487.75	25	75.5
+			487.75		
196 197	COM90 COM88	6555 6517	487.75	25 25	75.5 75.5
198				25	75.5
199	COM86 COM84	6479 6441	487.75 487.75	25	75.5
+	COM82				
200		6403	487.75 487.75	25	75.5 75.5
201	COM80 COM78	6365		25 25	75.5 75.5
202	COM76	6327 6289	487.75 487.75	25	75.5 75.5
203	COM76	6251	487.75	25	75.5
205	COM74 COM72	6213	487.75	25	75.5
206	COM70	6175	487.75	25	75.5
207	COM70	6137	487.75	25	75.5
1	COM66	6099		25	75.5
208	COIVIOD	0099	487.75	20	7 ປ.ວ



#	Pad	Х	Υ	W	Н
209	COM64	6061	487.75	25	75.5
210	COM62	6023		25	75.5
211	COM60		487.75 487.75	25	75.5
		5985			-
212	COM58	5947	487.75	25	75.5
213	COM56	5909	487.75	25	75.5
214	COM54	5871	487.75	25	75.5
215	COM52	5833	487.75	25	75.5
216	COM50	5795	487.75	25	75.5
217	COM48	5757	487.75	25	75.5
218	COM46	5719	487.75	25	75.5
219	COM44	5681	487.75	25	75.5
220	COM42	5643	487.75	25	75.5
221	COM40	5605	487.75	25	75.5
222	COM38	5567	487.75	25	75.5
223	COM36	5529	487.75	25	75.5
224	COM34	5491	487.75	25	75.5
225	COM32	5453	487.75	25	75.5
226	COM30	5415	487.75	25	75.5
227	COM28	5377	487.75	25	75.5
228	COM26	5339	487.75	25	75.5
229	COM24	5301	487.75	25	75.5
230	COM22	5263	487.75	25	75.5
231	COM20	5225	487.75	25	75.5
232	COM18	5187	487.75	25	75.5
233	COM16	5149	487.75	25	75.5
234	COM14	5111	487.75	25	75.5
235	COM12	5073	487.75	25	75.5
236	COM10	5035	487.75	25	75.5
237	COM8	4997	487.75	25	75.5
238	COM6	4959	487.75	25	75.5
239	COM4	4921	487.75	25	75.5
240	COM2	4883	487.75	25	75.5
241	SEG1	4845	487.75	25	75.5
242	SEG2	4807	487.75	25	75.5
243	SEG3	4769	487.75	25	75.5
244	SEG4	4731	487.75	25	75.5
245	SEG5	4693	487.75	25	75.5
246	SEG6	4655	487.75	25	75.5
247	SEG7	4617	487.75	25	75.5
248	SEG8	4579	487.75	25	75.5
249	SEG9	4541	487.75	25	75.5
250	SEG10	4503	487.75	25	75.5
251	SEG11	4465	487.75	25	75.5
252	SEG12	4427	487.75	25	75.5
253	SEG13	4389	487.75	25	75.5
254	SEG14	4351	487.75	25	75.5
255	SEG15	4313	487.75	25	75.5
256	SEG16	4275	487.75	25	75.5
257	SEG17	4237	487.75	25	75.5
258	SEG18	4199	487.75	25	75.5
259	SEG19	4161	487.75	25	75.5
260	SEG20	4123	487.75	25	75.5
261	SEG21	4085	487.75	25	75.5
20 I	OLOZ I	7000	TU1.13	20	10.0

#	Pad	Х	Υ	W	Н
# 262	SEG22	4047	487.75	25	75.5
263	SEG23	4047	487.75	25	75.5
264	SEG24	3971		25	75.5
265	SEG25	3933	487.75 487.75	25	75.5
266	SEG26	3895	487.75	25	75.5
267	SEG27	3857		25	75.5
		3819	487.75	25	75.5
268 269	SEG28 SEG29	3781	487.75 487.75	25	
270	SEG30	3743		25	75.5 75.5
271	SEG30 SEG31		487.75	25	75.5
	SEG32	3705	487.75		75.5
272		3667	487.75	25	
273	SEG33	3629	487.75	25	75.5
274	SEG34	3591	487.75	25	75.5
275	SEG35	3553	487.75	25	75.5
276	SEG36	3515	487.75	25	75.5
277	SEG37	3477	487.75	25	75.5
278	SEG38	3439	487.75	25	75.5
279	SEG39	3401	487.75	25	75.5
280	SEG40	3363	487.75	25	75.5
281	SEG41	3325	487.75	25	75.5
282	SEG42	3287	487.75	25	75.5
283	SEG43	3249	487.75	25	75.5
284	SEG44	3211	487.75	25	75.5
285	SEG45	3173	487.75	25	75.5
286	SEG46	3135	487.75	25	75.5
287	SEG47	3097	487.75	25	75.5
288	SEG48	3059	487.75	25	75.5
289	SEG49	3021	487.75	25	75.5
290	SEG50	2983	487.75	25	75.5
291	SEG51	2945	487.75	25	75.5
292	SEG52	2907	487.75	25	75.5
293	SEG53	2869	487.75	25	75.5
294	SEG54	2831	487.75	25	75.5
295	SEG55	2793	487.75	25	75.5
296	SEG56	2755	487.75	25	75.5
297	SEG57	2717	487.75	25	75.5
298	SEG58	2679	487.75	25	75.5
299	SEG59	2641	487.75	25	75.5
300	SEG60	2603	487.75	25	75.5
301	SEG61	2565	487.75	25	75.5
302	SEG62	2527	487.75	25	75.5
303	SEG63	2489	487.75	25	75.5
304	SEG64	2451	487.75	25	75.5
305	SEG65	2413	487.75	25	75.5
306	SEG66	2375	487.75	25	75.5
307	SEG67	2337	487.75	25	75.5
308	SEG68	2299	487.75	25	75.5
309	SEG69	2261	487.75	25	75.5
310	SEG70	2223	487.75	25	75.5
311	SEG71	2185	487.75	25	75.5
312	SEG72	2147	487.75	25	75.5
313	SEG73	2109	487.75	25	75.5
314	SEG74	2071	487.75	25	75.5

#	Pad	Х	Υ	W	Н
315	SEG75	2033	487.75	25	75.5
316	SEG76	1995	487.75	25	75.5
317	SEG77	1957	487.75	25	75.5
318	SEG78	1919	487.75	25	75.5
319	SEG79	1881	487.75	25	75.5
320	SEG80	1843	487.75	25	75.5
321	SEG81	1805	487.75	25	75.5
322	SEG82	1767	487.75	25	75.5
323	SEG83	1707	487.75	25	75.5
324	SEG84	1691	487.75	25	75.5
325	SEG85	1653	487.75	25	75.5
326	SEG86	1615	487.75	25	75.5
327	SEG87	1577		25	75.5
		1577	487.75	25	75.5
328	SEG88		487.75		
329	SEG89	1501	487.75	25	75.5
330	SEG90	1463	487.75	25	75.5
331	SEG91	1425	487.75	25	75.5
332	SEG92	1387	487.75	25	75.5
333	SEG93	1349	487.75	25	75.5
334	SEG94	1311	487.75	25	75.5
335	SEG95	1273	487.75	25	75.5
336	SEG96	1235	487.75	25	75.5
337	SEG97	1197	487.75	25	75.5
338	SEG98	1159	487.75	25	75.5
339	SEG99	1121	487.75	25	75.5
340	SEG100	1083	487.75	25	75.5
341	SEG101	1045	487.75	25	75.5
342	SEG102	1007	487.75	25	75.5
343	SEG103	969	487.75	25	75.5
344	SEG104	931	487.75	25	75.5
345	SEG105	893	487.75	25	75.5
346	SEG106	855	487.75	25	75.5
347	SEG107	817	487.75	25	75.5
348	SEG108	779	487.75	25	75.5
349	SEG109	741	487.75	25	75.5
350	SEG110	703	487.75	25	75.5
351	SEG111	665	487.75	25	75.5
352	SEG112	627	487.75	25	75.5
353	SEG113	589	487.75	25	75.5
354	SEG114	551	487.75	25	75.5
355	SEG115	513	487.75	25	75.5
356	SEG116	475	487.75	25	75.5
357	SEG117	437	487.75	25	75.5
358	SEG118	399	487.75	25	75.5
359	SEG119	361	487.75	25	75.5
360	SEG120	323	487.75	25	75.5
361	SEG121	285	487.75	25	75.5
362	SEG122	247	487.75	25	75.5
363	SEG123	209	487.75	25	75.5
364	SEG124	171	487.75	25	75.5
365	SEG125	133	487.75	25	75.5
366	SEG126	95	487.75	25	75.5
367	SEG127	57	487.75	25	75.5

#	Pad	Х	Υ	W	Н
368	SEG128	19	487.75	25	75.5
369	SEG129	-19	487.75	25	75.5
370	SEG130	-57	487.75	25	75.5
371	SEG131	-95	487.75	25	75.5
372	SEG132	-133	487.75	25	75.5
373	SEG133	-171	487.75	25	75.5
374	SEG134	-209	487.75	25	75.5
375	SEG135	-247	487.75	25	75.5
376	SEG136	-285	487.75	25	75.5
377	SEG137	-323	487.75	25	75.5
378	SEG138	-361	487.75	25	75.5
379	SEG139	-399	487.75	25	75.5
380	SEG140	-437	487.75	25	75.5
381	SEG141	-475	487.75	25	75.5
382	SEG142	-513	487.75	25	75.5
383	SEG143	-551	487.75	25	75.5
384	SEG144	-589	487.75	25	75.5
385	SEG145	-627	487.75	25	75.5
386	SEG146	-665	487.75	25	75.5
387	SEG147	-703	487.75	25	75.5
388	SEG148	-741	487.75	25	75.5
389	SEG149	-779	487.75	25	75.5
390	SEG150	-817	487.75	25	75.5
391	SEG151	-855	487.75	25	75.5
392	SEG152	-893	487.75	25	75.5
393	SEG153	-931	487.75	25	75.5
394	SEG154	-969	487.75	25	75.5
395	SEG155	-1007	487.75	25	75.5
396	SEG156	-1045	487.75	25	75.5
397	SEG157	-1083	487.75	25	75.5
398	SEG158	-1121	487.75	25	75.5
399	SEG159	-1159	487.75	25	75.5
400	SEG160	-1197	487.75	25	75.5
401	SEG161	-1235	487.75	25	75.5
402	SEG162	-1273	487.75	25	75.5
403	SEG163	-1311	487.75	25	75.5
404	SEG164	-1349	487.75	25	75.5
405	SEG165	-1387	487.75	25	75.5
406	SEG166	-1425	487.75	25	75.5
407	SEG167	-1463	487.75	25	75.5
408	SEG168	-1501	487.75	25	75.5
409	SEG169	-1539	487.75	25	75.5
410	SEG170	-1577	487.75	25	75.5
411	SEG171	-1615	487.75	25	75.5
412	SEG172	-1653	487.75	25	75.5
413	SEG173	-1691	487.75	25	75.5
414	SEG174	-1729	487.75	25	75.5
415	SEG175	-1767	487.75	25	75.5
416	SEG176	-1805	487.75	25	75.5
417	SEG177	-1843	487.75	25	75.5
418	SEG178	-1881	487.75	25	75.5
419	SEG179	-1919	487.75	25	75.5
420	SEG180	-1957	487.75	25	75.5



#	Pad	Х	Υ	W	Н
421	SEG181	-1995	487.75	25	75.5
422	SEG182	-2033	487.75	25	75.5
423	SEG183	-2071	487.75	25	75.5
424	SEG184	-2109	487.75	25	75.5
425	SEG185	-2147	487.75	25	75.5
426	SEG186	-2185	487.75	25	75.5
427	SEG187	-2223	487.75	25	75.5
428	SEG188	-2261	487.75	25	75.5
429	SEG189	-2299	487.75	25	75.5
430	SEG190	-2337	487.75	25	75.5
431	SEG191	-2375	487.75	25	75.5
432	SEG192	-2413	487.75	25	75.5
433	SEG193	-2451	487.75	25	75.5
434	SEG194	-2489	487.75	25	75.5
435	SEG195	-2527	487.75	25	75.5
436	SEG196	-2565	487.75	25	75.5
437	SEG197	-2603	487.75	25	75.5
438	SEG198	-2641	487.75	25	75.5
439	SEG199	-2679	487.75	25	75.5
440	SEG200	-2717	487.75	25	75.5
441	SEG201	-2755	487.75	25	75.5
442	SEG202	-2793	487.75	25	75.5
443	SEG203	-2831	487.75	25	75.5
444	SEG204	-2869	487.75	25	75.5
445	SEG205	-2907	487.75	25	75.5
446	SEG206	-2945	487.75	25	75.5
447	SEG207	-2983	487.75	25	75.5
448	SEG208	-3021	487.75	25	75.5
449	SEG209	-3059	487.75	25	75.5
450	SEG210	-3097	487.75	25	75.5
451	SEG211	-3135	487.75	25	75.5
452	SEG212	-3173	487.75	25	75.5
453	SEG213	-3211	487.75	25	75.5
454	SEG214	-3249	487.75	25	75.5
455	SEG215	-3287	487.75	25	75.5
456	SEG216	-3325	487.75	25	75.5
457	SEG217	-3363	487.75	25	75.5
458	SEG218	-3401	487.75	25	75.5
459	SEG219	-3439	487.75	25	75.5
460	SEG220	-3477	487.75	25	75.5
461	SEG221	-3515	487.75	25	75.5
462	SEG222	-3553	487.75	25	75.5
463	SEG223	-3591	487.75	25	75.5
464	SEG224	-3629	487.75	25	75.5
465	SEG225	-3667	487.75	25	75.5
466	SEG226	-3705	487.75	25	75.5
467	SEG227	-3743	487.75	25	75.5
468	SEG228	-3781	487.75	25	75.5
469	SEG229	-3819	487.75	25	75.5
470	SEG230	-3857	487.75	25	75.5
471	SEG231	-3895	487.75	25	75.5
472	SEG232	-3933	487.75	25	75.5
473	SEG233	-3971	487.75	25	75.5
	020200	557 1	.07.70	_0	, 5.0

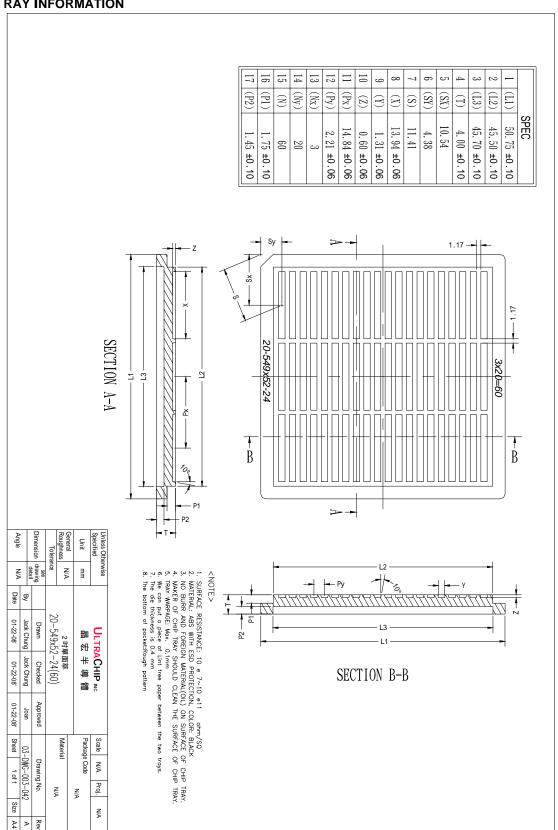
#	Pad	Х	Υ	W	Н
474	SEG234	-4009	487.75	25	75.5
475	SEG235	-4047	487.75	25	75.5
476	SEG236	-4085	487.75	25	75.5
477	SEG237	-4123	487.75	25	75.5
478	SEG238	-4161	487.75	25	75.5
479	SEG239	-4199	487.75	25	75.5
480	SEG240	-4237	487.75	25	75.5
481	SEG241	-4275	487.75	25	75.5
482	SEG242	-4313	487.75	25	75.5
483	SEG243	-4351	487.75	25	75.5
484	SEG244	-4389	487.75	25	75.5
485	SEG245	-4427	487.75	25	75.5
486	SEG246	-4465	487.75	25	75.5
487	SEG247	-4503	487.75	25	75.5
488	SEG248	-4541	487.75	25	75.5
489	SEG249	-4579	487.75	25	75.5
490	SEG249 SEG250	-4579 -4617	487.75	25	75.5
490	SEG250 SEG251	-4655	487.75	25	75.5
492	SEG251	-4693	487.75	25	75.5
493	SEG253	-4093 -4731	487.75	25	75.5
494				25	
+	SEG254	-4769 4807	487.75		75.5
495	SEG255	-4807 4845	487.75	25	75.5
496 497	SEG256	-4845	487.75	25 25	75.5 75.5
+	COM1	-4883	487.75		
498	COM5	-4921	487.75	25	75.5
499	COM5	-4959 4007	487.75	25	75.5
500	COM7 COM9	-4997 5035	487.75	25	75.5
501	COM9 COM11	-5035 5073	487.75	25 25	75.5
502	COM11	-5073 -5111	487.75	25	75.5
503			487.75		75.5
504	COM15 COM17	-5149 5197	487.75	25 25	75.5
505	COM17	-5187 -5225	487.75	25	75.5 75.5
506 507	COM19 COM21		487.75	25	
508	COM21	-5263 -5301	487.75 487.75	25	75.5 75.5
-	COM25				
509 510		-5339 5277	487.75	25 25	75.5
	COM27	-5377 5415	487.75		75.5
511 512	COM29 COM31	-5415 -5453	487.75 487.75	25 25	75.5 75.5
513	COM33	-5491	487.75	25	75.5
514				25	
515	COM35 COM37	-5529 -5567	487.75 487.75	25	75.5 75.5
516	COM39				75.5
-		-5605 5643	487.75	25	
517 518	COM41 COM43	-5643 -5681	487.75 487.75	25 25	75.5 75.5
519	COM45		487.75		
+	COM45 COM47	-5719 -5757		25	75.5 75.5
520 521	COM47 COM49	-5757 -5795	487.75	25	75.5 75.5
522	COM51	-5795	487.75	25 25	75.5 75.5
523	COM53	-5633 -5871	487.75 487.75	25	75.5
+					
524 525	COM55	-5909 5047	487.75	25	75.5 75.5
1 1	COM57	-5947 5085	487.75	25	75.5 75.5
526	COM59	-5985	487.75	25	75.5

160x256/16S Matrix LCD Controller-Driver

#	Pad	Х	Υ	W	Н
527	COM61	-6023	487.75	25	75.5
528	COM63	-6061	487.75	25	75.5
529	COM65	-6099	487.75	25	75.5
530	COM67	-6137	487.75	25	75.5
531	COM69	-6175	487.75	25	75.5
532	COM71	-6213	487.75	25	75.5
533	COM73	-6251	487.75	25	75.5
534	COM75	-6289	487.75	25	75.5
535	COM77	-6327	487.75	25	75.5
536	COM79	-6365	487.75	25	75.5
537	COM81	-6403	487.75	25	75.5
538	COM83	-6441	487.75	25	75.5
539	COM85	-6479	487.75	25	75.5
540	COM87	-6517	487.75	25	75.5
541	COM89	-6555	487.75	25	75.5
542	COM91	-6593	487.75	25	75.5
543	COM93	-6631	487.75	25	75.5
544	COM95	-6669	487.75	25	75.5
545	COM97	-6707	487.75	25	75.5
546	COM99	-6745	487.75	25	75.5
547	DUMMY	-6785.5	487.75	30	75.5

High-Voltage Mixed-Signal IC

# **TRAY INFORMATION**



# **REVISION HISTORY**

Revision	Contents	Date of Rev.
0.6	First-time release	Apr. 28, 2008
1.0	(1) The relationship between V <sub>DD</sub> and V <sub>DD2/3</sub> is adjusted to make V <sub>DD2/3</sub> between V <sub>DD</sub> ~ V <sub>DD</sub> +1.5V (Section "Pin Description" – V <sub>DD</sub> V <sub>DD2</sub> V <sub>DD3</sub> , page 6)  (2) The description of connection of capacitors is updated. (Section "Pin Description" – C <sub>AA</sub> /C <sub>BA</sub> , page 6)  (3) The recommended C <sub>B</sub> value is adjusted: 100~150 times → 100~250 times of (Section "Pin Description" – Notes, page 6; "Hi-V Generator and Bias Reference Circuit", page 30)  (4) The formula of Mux-rate is updated to DEN-DST+1+LC[3] x FL x 2 (Section "Control Registers" – LC, page 12; "Command Description" – (14) Set Partial Display Control, page 19; "Command Description" – (30) Set Display End, page 24)  (5) The description of LC[3] is updated. (Section "Command Description" – (21) Set LCD Mapping Control, page 22)  (6) The description of the command is updated. (Section "Command Description" – (9) Set Scroll Line, page 18)  (7) The V <sub>LCD</sub> chart and the table are updated. (Section "W <sub>LCD</sub> Quick Reference", page 29)  (8) Figures 4a and 5a illustrating Read in S8 and S9 modes are inserted. (Section "Host Interfaces", Pp 36~37)  (9) The description on Sleep Mode and Draining Circuit is updated. (Section "Reset and Power Management", page 49)  (10) The description of Power-Down Sequence is updated. (Section "Reset and Power Management", page 50)  (11) The settings of MTP2/3 for MTP Read/Program/Erase are updated: for Program/Erase, MTP3 : 28h → 25h for Read, MTP2 : 6Fh → 69h (Section "MTP Operation for LCM Makers", page 51; "MTP Command Sequence Sample Codes", Pp 54~55)  (12) V <sub>DD2/3</sub> - V <sub>DD</sub> (Max.) is adjusted : 1.2 → 2.0 V (Section "Absolute Maximum Ratings", page 58)  (13) Input logic Low, V <sub>IL</sub> (Max.), is adjusted : 0.15 → 0.2 times of V <sub>DD</sub> Input logic High, V <sub>IH</sub> (Min.), is adjusted : 0.15 → 0.8 times of V <sub>DD</sub> SEG output impedance, R <sub>0(COM)</sub> (Typ.), is adjusted : 1.2 → 1.35 kΩ (Section "Specifications" – DC Characteristics, page 59)  (14) Power consumption data (maximum) present. (Section "AC Characteristics", Pp 60~66)	Jun. 11, 2008