TW9900 – Low Power NTSC/PAL/SECAM Video Decoder with VBI Slicer

Data Sheet

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Features

Video decoder

- NTSC (M, 4.43) and PAL (B, D, G, H, I, M, N, N combination), PAL (60), SECAM support with automatic format detection
- Software selectable analog inputs allows any of the following combinations, e.g. 2 CVBS or 1 Y/C.
- Built-in analog anti-alias filter
- Two 10-bit ADCs and analog clamping circuit.
- Fully programmable static gain or automatic gain control for the Y channel
- Programmable white peak control for the Y channel
- 4-H adaptive comb filter Y/C separation
- PAL delay line for color phase error correction
- Image enhancement with peaking and CTI.
- Digital sub-carrier PLL for accurate color decoding
- Digital Horizontal PLL for synchronization processing and pixel sampling
- Advanced synchronization processing and sync detection for handling non-standard and weak signal
- Programmable hue, brightness, saturation, contrast, and sharpness.
- Automatic color control and color killer
- Chroma IF compensation
- Detection of level of copy protection according to Macrovision standard
- ITU-R 601 or ITU-R 656 compatible YCbCr(4:2:2) output format
- VBI slicer supporting industrial standard data services
- VBI data pass through, raw ADC data output
- Programmable output cropping

Miscellaneous

- Two wire MPU serial bus interface
- Support Real Time Control interface
- Power save and Power down mode
- Typical power consumption < 100mW
- Single 27MHz crystal for all standards
- Supports 24.54MHz and 29.5MHz crystal for high resolution square pixel format decoding
- 3.3V tolerant I/O
- 1.8V/3.3 V power supply
- 32pin TQFP and 32pin QFN package

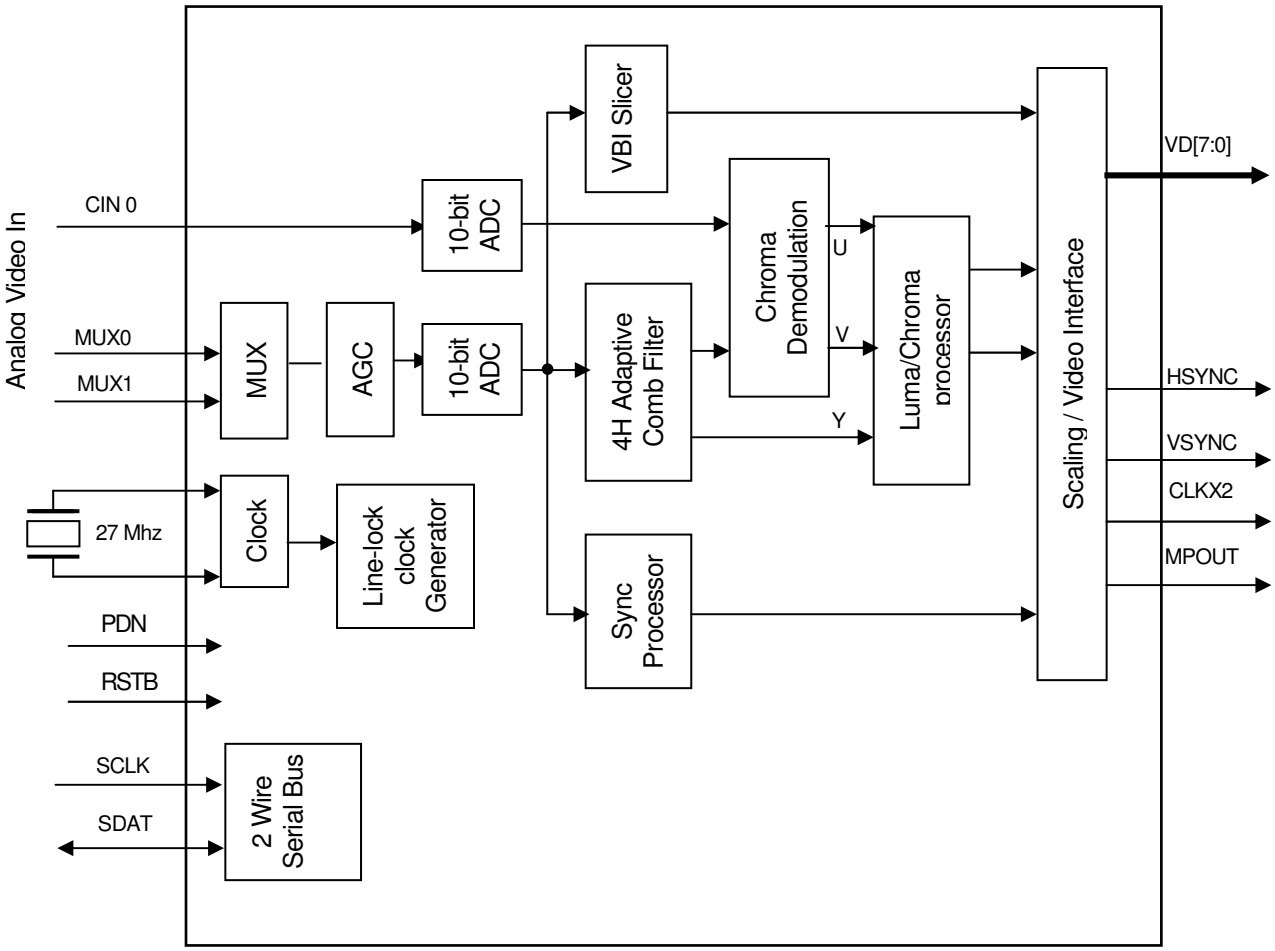
Order Information

Package Description

Part #	Name	Description	Pin Count	Body Size
TW9900-DBTA1-GR	TQFP 32	Thin Quad Flat Package	32	5 x 5 mm^2
TW9900-DBNA1-GR	QFN 32	Quad Flat No-Lead Package	32	4 x 4 mm^2

Functional Description

Figure 1: TW9900 Block Diagram



Introduction

The TW9900 is a low power NTSC/PAL/SECAM video decoder chip that is designed for portable applications. It consumes less than 100mW in typical composite input application. The available power down mode further reduces the power consumption. It uses the 1.8V for both analog and digital supply voltage and 3.3V for I/O power. A single 27MHz crystal is all that needed to decode all analog video standards.

The video decoder decodes the base-band analog CVBS or S-video signals into digital 8-bit 4:2:2 YCbCr for output. It consists of analog front-end with input source selection, variable gain amplifier and analog-to-digital converters, Y/C separation circuit, multi-standard color decoder (PAL BGHI, PAL M, PAL N, combination PAL N, NTSC M, NTSC 4.43 and SECAM) and synchronization circuitry. The Y/C separation is done with high quality adaptive 4H comb filter for reduced cross color and cross luminance. The advanced synchronization processing circuitry can produce stable pictures for non-standard signal as well as weak signal. The output of the decoder is line-locked and formatted to the ITU-R 656 output with embedded sync.

The TW9900 also includes circuits to detect and process vertical blanking interval (VBI) signal. It slices and process VBI data for output through video bus. Some information can also be alternatively retrieved through host interface. It also detects copy-protected signal according to Macrovision standard including AGC and colorstripe pulses.

A 2-wire serial host interface is used to simplify system integration. All the functions can be controlled through this interface.

Analog Front End

The analog front-end prepares and digitizes the AC coupled analog signal for further processing. Both channels have built-in anti-aliase filter and 10-bit over-sampling ADCs. The characteristic of the filter is available in the filter curve section. The Y channel has additional 2-input multiplexer, and a variable gain amplifier for automatic gain control (AGC). It can support a maximum input voltage range of 1.4V without attenuation. The C channel has only one input with built-in clamping circuit that restores the DC level. Software selectable analog inputs allow two possible input combinations:

1. Two selectable composite video inputs.
2. One S-video input.

Sync Processor

The sync processor of TW9900 detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-video or component signal. The processor contains a digital phase-locked-loop and decision logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward. It allows the sampling of the video signal in line-locked fashion.

Y/C separation

For NTSC and PAL standard signals, the luma/chroma separation can be done either by adaptive comb filtering or notch/band-pass filter combination. For SECAM standard signals, only notch/band-pass filter is available. The default selection for NTSC/PAL is comb filter. The characteristics of the band-pass filter are shown in the filter curve section.

TW9900 employs high quality 4-H adaptive comb filter to reduce artifacts like hanging dots and crawling dots. Due to the line buffer used in the comb filter, there is always two lines processing delay in the output images no matter what standard or filter option is chosen.

Color demodulation

The color demodulation of NTSC and PAL signal is done by first quadrature down mixing and then low-pass filtering. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

The SECAM decoding process consists of FM demodulator and de-emphasis filtering. During the FM demodulation, the chroma carrier frequency is identified and used to control the SECAM color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily with single crystal frequency.

Automatic Chroma Gain Control

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in video signal. The range of ACC control is –6db to +26db.

Color Killer

For low color amplitude signals, black and white video, or very noisy signals, the color will be “killed”. The color killer uses the burst amplitude measurement as well as sub-carrier PLL status to switch-off the color.

Automatic standard detection

The TW9900 has build-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Each standard can be included or excluded in the standard recognition process by software control. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

TW9900 supports all common video formats as shown in Table 1. The video decoder needs to be programmed appropriately for each of the composite video input formats.

Table 1. Video Input Formats Supported by the TW9900

Format	Lines	Fields	Fsc	Country
NTSC-M	525	60	3.579545 MHz	U.S., many others
NTSC-Japan (1)	525	60	3.579545 MHz	Japan
PAL-B, G, N	625	50	4.433619 MHz	Many
PAL-D	625	50	4.433619 MHz	China
PAL-H	625	50	4.433619 MHz	Belgium
PAL-I	625	50	4.433619 MHz	Great Britain, others
PAL-M	525	60	3.575612 MHz	Brazil
PAL-CN	625	50	3.582056 MHz	Argentina
SECAM	625	50	4.406MHz 4.250MHz	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.433619 MHz	China
NTSC (4.43)	525	60	4.433619 MHz	Transcoding
NTSC 50	625	50	3.579545 MHz	

Notes: (1). NTSC-Japan has 0 IRE setup.

Component Processing

The TW9900 supports the brightness, contrast, color saturation and Hue adjustment for changing the video characteristic. The Cb and Cr gain can be adjusted independently for flexibility.

Sharpness

The TW9900 also provides a sharpness control function through control registers. It provides the control up to +9db. The center frequency of the enhancement curve is selectable. A coring function is provided to prevent noise enhancement.

Color Transient Improvement

A programmable Color Transient Improvement circuit is provided to enhance the color bandwidth. Low level noise enhancement can be suppressed by a programmable coring logic. Overshoot and undershoot are also removed by special circuit to prevent false color generation at the color edge.

Power Management

The TW9900 can be put into power-down mode through both software and hardware control. The Y and C path can be separately powered down.

Host Interface

The TW9900 registers are accessed via 2-WIRE SERIAL MPU interface. It operates as a slave device. Serial clock and data lines, SCLK and SDAT, transfer data from the bus master at a rate of 400 Kbits/s. The TW9900 has one serial interface address select pin(VD[0]/SIAD0) to program up to two unique serial addresses TW9900. This allows as many as two TW9900 to share the same serial bus. Reset signals are also available to reset the control registers to their default values.

Cropping

Cropping allows only subsection of a video image to be output. The VACTIVE signal can be programmed to indicate the number of active lines to be displayed in a video field, and the HACTIVE signal can be programmed to indicate the number of active pixels to be displayed in a video line. The start of the field or frame in the vertical direction is indicated by the leading edge of VSYNC. The start of the line in the horizontal direction is indicated by the leading edge of the HSYNC. The start of the active lines from vertical sync edge is indicated by the VDELAY register. The start of the active pixels from the horizontal edge is indicated by the HDELAY register. The sizes and location of the active video are determined by HDELAY, HACTIVE, VDELAY, and VACTIVE registers. These registers are 8-bit wide, the lower 8-bits is, respectively, in HDELAY_LO, HACTIVE_LO, VDELAY_LO, and VACTIVE_LO. Their upper 2-bit shares the same register CROP_HI.

In order for the cropping to work properly, the following equation should be satisfied.

HDELAY + HACTIVE < Total number of pixels per line.

VDELAY + VACTIVE < Total number of lines per field

Table 2 shows some popular video formats and its recommended register settings. The CCIR601 format refers to the sampling rate of 13.5 MHz. The SQ format for 60 Hz system refers to the sampling rate of 12.27 MHz, and the SQ format for 50 Hz system refers to the use of sampling rate of 14.75 MHz.

Scaling Ratio	Format	Total Resolution	Output Resolution
1:1	NTSC SQ	780x525	640x480
	NTSC CCIR601	858x525	720x480
	PAL SQ	944x625	768x576
	PAL CCIR601	864x625	720x576

Table 2. some popular video formats.

Output Interface

ITU-R BT.656

ITU-R BT.656 defines strict EAV/SAV Code, video data output timing, H blanking timing, and V Blanking timing. In this mode, VD[7:0] pins are only effective and CLKX2 pin should be used for data clock signal. EAV/SAV Code format is shown as follows. Bit 7 of forth byte in EAV/SAV code must be "1" in ITU-R BT.656 standard. For that reason, VIPCFG Register bit must be set to "1".

Table3. ITU-R BT.656 SAV and EAV code sequence

	VD7	VD6	VD5	VD4	VD3	VD2	VD1	VD0
1st byte	1	1	1	1	1	1	1	1
2nd byte	0	0	0	0	0	0	0	0
3rd byte	0	0	0	0	0	0	0	0
4th byte	*C	F	V	H	V XOR H	F XOR H	F XOR V	F XOR V XOR H

*C is set by VIPCFG register bit.

For complete IRU-R BT.656 standard, following setting is recommended.

Table 4. ITU-R BT.656 Register set up

Register	525 line system	625 line system
MODE	1	1
LEN	0	0
VDELAY	0x012	0x018
VACTIVE	0X0F4	0x120
HACTIVE	0x2D0	0x2D0
HA_EN	1	1
VIPCFG	1	1
NTSC656	1	0

ITU-R BT.656 for 525-line system has 244 video active lines in odd field and 243 vide active lines in even field. NTSC656 register bit controls this video active line length.

Control Signals

TW9900 outputs several control signals. VSYNC is vertical timing control signals. HSYNC is horizontal timing control signals. These control signals are mainly used on 601 mode (MODE register bit is set to "0".).

Vertical timing diagram

Figure 2 shows typical vertical timing for 60Hz/525 lines system. Figure 3 shows typical vertical timing for 50Hz/625 lines system. On Figure 2,VDELAY register is 19DEC(0x13) and VACTIVE register is 241DEC(0x0F1). Figure 3 shows typical NTSC-M setting. On Figure 3, VDEALY register is 24 decimal (0x18) and VACTIVE register is 286 decimal (0x11E). FIGURE 2 shows typical PAL-B setting. The leading edge of VACTIVE is controlled by VDELAY register value. The length of video active lines is controlled by VACTIVE register value. As shown on Figure 2 and 3, output video data stream has 2 lines vertical delay compared to input VIDEO line timing.

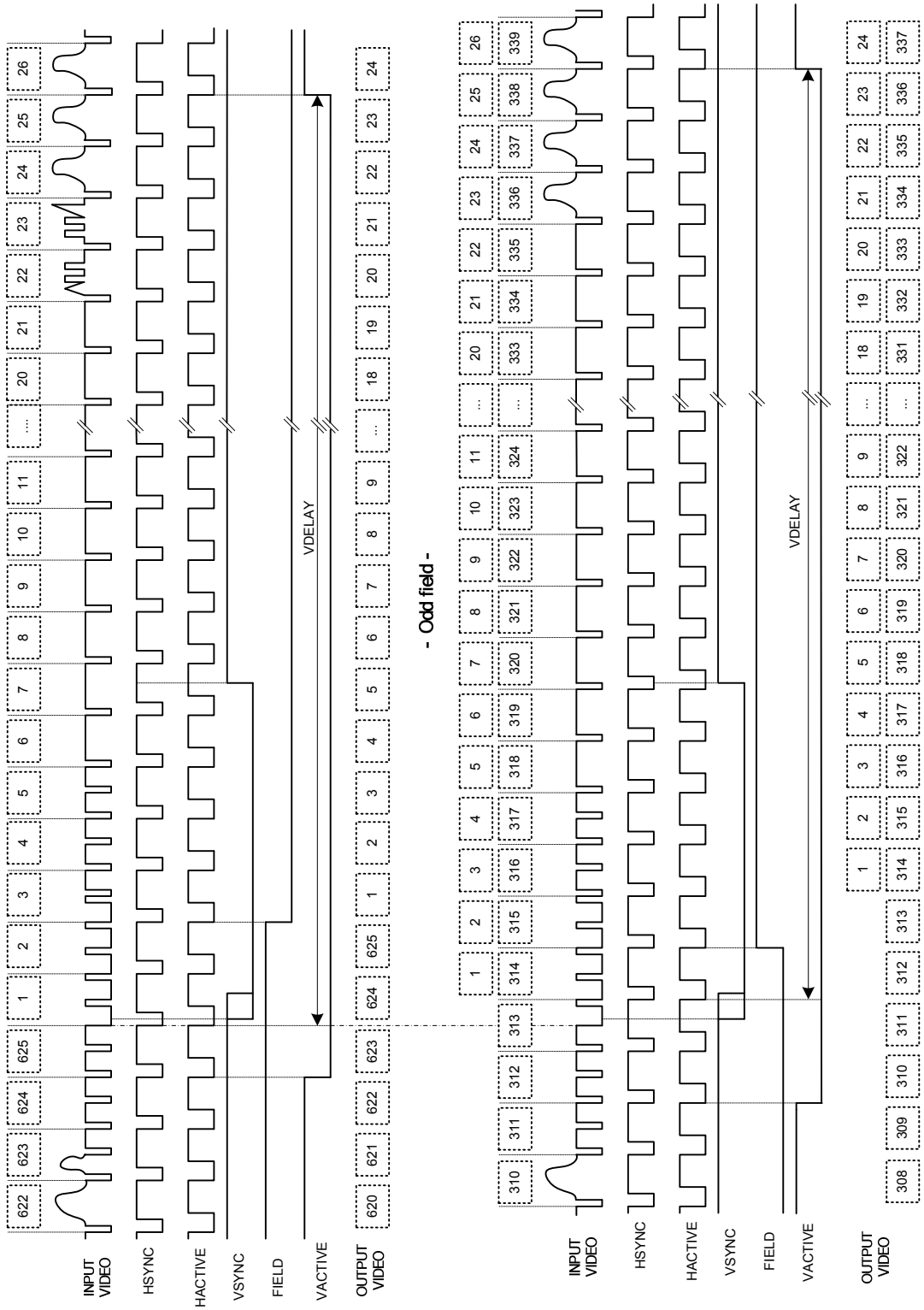


Figure 2.Vertical timing diagram for 50Hz/ 625 line system

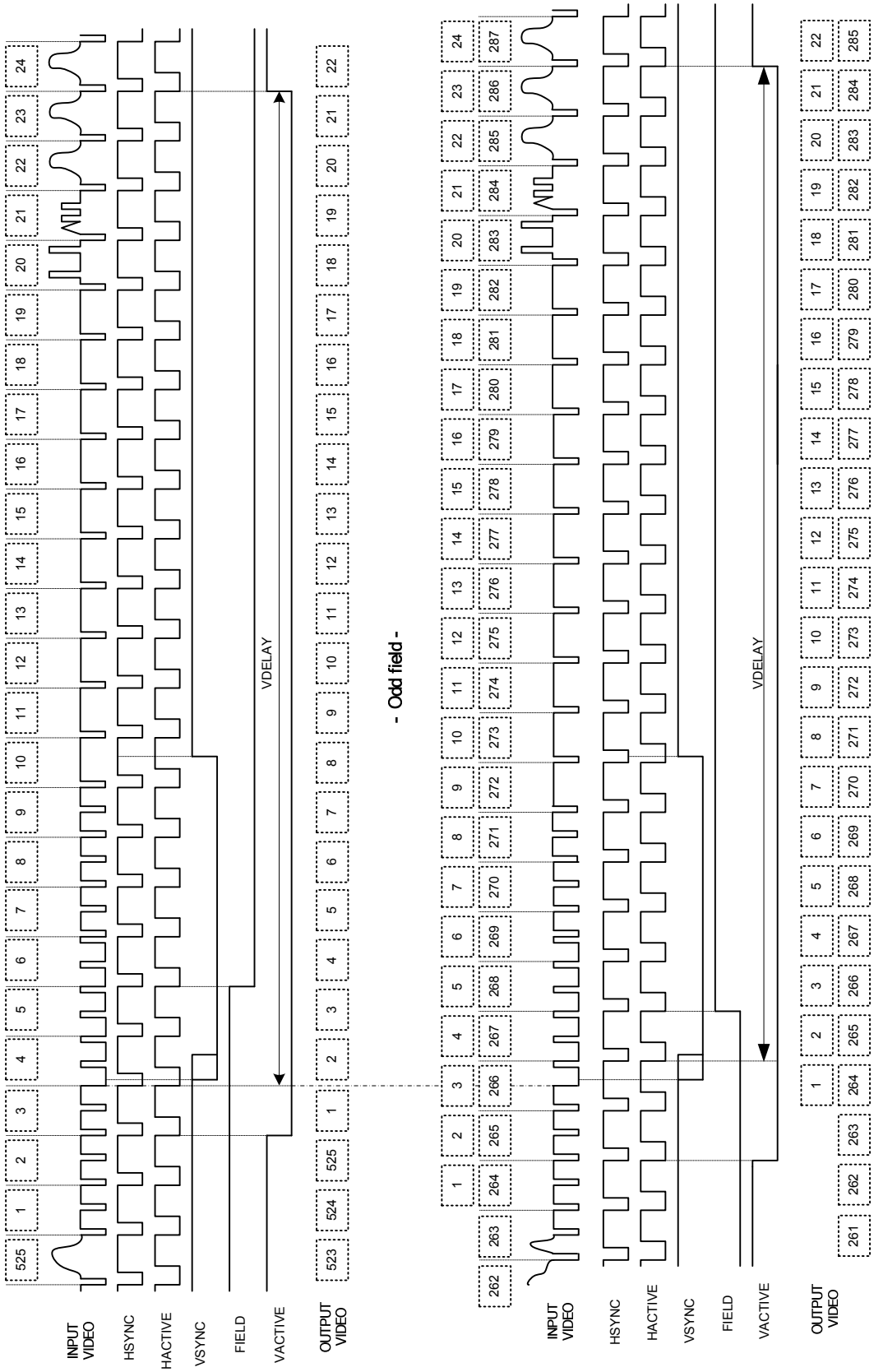


Figure 3.Vertical timing diagram for 60Hz/ 525 line system

HSYNC

The leading edge of HSYNC signal is synchronized to input Video horizontal sync timing. The start position of HSYNC signal is programmable by HSBEGIN register. The end position of HSYNC signal is also programmable by HSEND registers.

VSYNC

The leading edge of VSYNC signal is synchronized to vertical sync pulse of input Video. The leading edge position of VSYNC signal is programmable by OVSDLY register on a per clkx2 clock basis. The trailing edge of VSYNC signal is in the middle of HSYNC “1” period in odd field and in the middle of HSYNC “0” period in even field. The trailing edge of VSYNC changed on line 10 in 525 lines system and on line 7 in 625-line system as default. This line number is programmable by OVSEND register on a per line basis.

FIELD

FIELD signal can be output on MPOUT pin if RTSEL register select FIELD output.Figure 2 and Figure 3 show field signal output assuming default OFDLY register 2H.The line output timing of FIELD signal is programmable by OFDLY register value (1H to 6H). Default FIELD signal shows the ITU-R BT.656 field timing in 656 output video stream by OFDLY register 2H.

VBI Data Processing

Raw VBI data output

TW9900 supports raw VBI data output. Raw VBI data output has the same vertical line delay timing as video output. Horizontal output timing is also programmable by VBIDELAY register. Raw VBI data is generated during HACTIVE active period (from SAV to EAV) as Video data output. Total pixel number of raw VBI data per line is twice as many as HACTIVE register value. If VBI EN register is set to "1", all vertical blanking output while VACTIVE is inactive will be raw VBI data output. If VVBI registers are set to more than "1", the VVBI number lines from top video active lines will also be raw VBI data output lines.

VBI Data Slicer

The following VBI standards are supported by VBI Data slicer. The VBI Data slicing is controlled by the registers LCTL6 to LCTL26. Registers LCTL6 to LCTL26 are controlling the slicing process itself. LCTL6 to LCTL26 defines the Data Type to be decoded. The Data Type can be specified on a line by line basis for line6 to line26 and for even and odd field depending on the detected TV system standard. The setting for LCTL26 is valid for the rest of the corresponding field. Normally no text data 0H (video data) should be selected to render the VBI Data slicer inactive during active video. LCTRL26 is useful for Full-Field Teletext mode in the case of NABTS.

NABTS is 525 Teletext-C. Japan's MOJI is 525 Teletext-D. Didon Antiope is 625 Teletext-A. VBI Data slicer supports up to Physical layer, Link layer in ITU-R BT.653-2. Japan's EIAJ CPR-1204 shown as 525 WSS has the same physical layer protocol as that of CGMS.

The sliced VBI data is embedded in the ITU-R BT.656 output stream, using the intervals between the End of Active Video (EAV) and the Start of Active Vide(SAV) codes of each line and formatted according to ITU-R BT.1364 Ancillary data packet Type 2.

Table 5. VBI Standard.

STANDARD TYPE	TV Systems (lines/freq)	Bit Rate (Mbits/s)	Modulation	Data Type
625 Teletext-B	625/50	6.9375	NRZ	1H
525 Teletext-B	525/60	5.727272	NRZ	1H
625 Teletext-C	625/50	5.734375	NRZ	2H
525 Teletext-C	525/60	5.727272	NRZ	2H
625 Teletext-D	625/50	5.6427875	NRZ	3H
525 Teletext-D	525/60	5.727272	NRZ	3H
625 CC	625/50	0.500	NRZ	4H
525 CC	525/60	0.503	NRZ	4H
625 WSS	626/50	5	Bi-phase	5H
525 WSS(CGMS)	525/60	0.447443	NRZ	5H
625 VITC	625/50	1.8125	NRZ	6H
525 VITC	525/60	1.7898	NRZ	6H
Gemstar 2x	525/60	1.007	NRZ	7H
Gemstar 1x	525/60	0.503	NRZ	8H
VPS	625/50	5	Bi-phase	9H
625 Teletext-A	625/50	6.203125	NRZ	AH

Sliced VBI Data output format

After 4 bytes of EAV code, sliced VBI ANC data packets are generated by following format. Byte1 to Byte4N+7 data stream is formatted according to ITU-R BT.1364 ANC data packet type2. BC data byte is optional and not included in ANC data packet type 2 BC data byte is inserted after ANC data packet type2.

Table 6. Sliced VBI ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	NEP	EP	DC5	DC4	DC3	DC2	DC1	DC0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	DT3	DT2	DT1	DT0	IDI2. UDW 2
9	Sliced VBI Data byte 1								Sliced VBI Data No.1. UDW3
10	Sliced VBI Data byte 2								Sliced VBI Data No.2. UDW4
11	Sliced VBI Data byte 3								Sliced VBI Data No.3 UDW5
12	Sliced VBI Data byte 4								Sliced VBI Data No.4. UDW6
13	Sliced VBI Data byte 5								Sliced VBI Data No.5. UDW7
.	.								
.	.								
4N+6	Sliced VBI Data byte last or FILLDATA								Sliced VBI Data Last or FILLDATA. UDW 4N
4N+7	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
4N+8	OP	0	BC5	BC4	BC3	BC2	BC1	BC0	BC

1. EP is Even Parity of bits 5 to 0 in same 1 byte.
2. NEP is inverted EP in same 1 byte.
3. {DID4,DID3,DID2,DID1,DID0} is DID register value.
4. {SDID5,SDID4,SDID3,SDID2,SDID1,SDID0} is SDID register value.
5. {DC5,DC4,DC3,DC2,DC1,DC0} is the number of DOWRD data length from UDW1 to UDW4N.On this table, {DC5,DC4,DC3,DC2,DC1,DC0} is N(decimal).
6. OP is Odd Parity of bits 6 to 0 in same 1 byte.
7. FID=0: odd field ; FID=1: even field.
8. {LN8,LN7,LN6,LN5,LN4,LN3,LN2,LN1,LN0} is the line number of current sliced VBI data.
9. {DT3,DT2,DT1,DT0} is the Data Type shown on Table
10. NCS6 is inverted CS6.
11. {CS6,CS5,CS4,CS3,CS2,CS1,CS0} is the checksum value calculated from DID to UDW4N.
12. UDW1 to UDW4N are the User data words(UDW) shown on ITU-R BT.1364 ANC data packet type 2.
13. [BC5,BC4,BC3,BC2,BC1,BC0] is the number of valid bytes from UDW1 to UDW4N.
14. FILLDATA is FILLDATA register value. FILLDATA is inserted after last valid bytes to make 4N number byte stream sometimes.

Following shows various type of ANC data packet to be output

Table 7. Closed Captioning ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary data flag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	0	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	0	0	IDI2. UDW 2
9	1st Character byte								UDW3
10	2nd Character byte								UDW4
11	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
12	0	0	0	0	0	1	0	0	BC

Table 8. CGMS ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	0	1	IDI2. UDW 2
9	WSS[7:0]								UDW3
10	WSS[7:0]								UDW4
11	{0H,WSS[19:16]}								UDW5
12	CRCERRORCODE								UDW6
13	FILLDATA								UDW7
14	FILLDATA								UDW8
15	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
16	1	0	0	0	0	1	1	0	BC

1.CRCERRORCODE is optional byte. 41H means “this wss data has CRC Error”. 80H means no CRC error.

Table 9. 625 line Wide Screen signaling ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	0	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	0	1	IDI2. UDW 2
9	WSS[7:0]								UDW3
10	{00b,WSS[13:8]								UDW4
12	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
13	0	0	0	0	0	1	0	0	BC

Table 10. 625 Teletext-A ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	1	0	1	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	1	0	1	0	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
46	BYTE40								UDW40
47	HAMM84ERROR								UDW41
48	FILLDATA								UDW42
49	FILLDATA								UDW43
50	FILLDATA								UDW44
51	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
52	0	0	1	0	1	0	0	1	BC

1.FRAME CODE is E7H if it's received correctly.
2.HAMM84ERROR is 41H if more than 1 8/4 Hamming code error in this packet,80H means no 8/4 Hamming error.

Table 11. 625 Teletext-B ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	1	1	0	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	0	0	1	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
50	BYTE44								UDW44
51	BYTE45								UDW45
52	HAMM84ERROR								UDW46
53	FILLDATA								UDW47
54	FILLDATA								UDW48
55	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
56	1	0	1	0	1	1	1	0	BC

1.FRAME CODE is 27H if it's received correctly.
2.HAMM84ERROR is 41H if more than 1 8/4 Hamming code error in this packet,80H means no 8/4 Hamming error.

Table 12. 525 Teletext-B ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	1	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	0	0	1	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
30	BYTE36								UDW36
31	BYTE37								UDW37
32	HAMM84ERROR								UDW38
33	FILLDATA								UDW39
34	FILLDATA								UDW40
35	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
36	1	0	1	0	0	1	1	0	BC

1.FRAME CODE is 27H if it's received correctly.
2.HAMM84ERROR is 41H if more than 1 8/4 Hamming code error in this packet,80H means no 8/4 Hamming error.

Table 13. 625 Teletext-C and 525 Teletext-C ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	1	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	0	1	0	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
42	BYTE36								UDW36
43	HAMM84ERROR								UDW37
44	FILLDATA								UDW38
45	FILLDATA								UDW39
46	FILLDATA								UDW40
47	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
48	0	0	1	0	0	1	0	1	BC

1.FRAME CODE is E7H if it's received correctly.
2.HAMM84ERROR is 41H if more than 1 8/4 Hamming code error in this packet,80H means no 8/4 Hamming error.

Table 14. 625 Teletext-D and 525 Teletext-D ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	1	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	0	1	1	IDI2. UDW 2
9	FRAME CDDE								UDW3
10	BYTE4								UDW4
11	BYTE5								UDW5
.	.								
.	.								
42	BYTE36								UDW36
43	BYTE37								UDW37
44	FILLDATA								UDW38
45	FILLDATA								UDW39
46	FILLDATA								UDW40
47	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
48	0	0	1	0	0	1	0	1	BC

1.FRAME CODE is A7H if it's received correctly.

Table 15. Line16 VPS ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	0	1	0	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	1	0	0	1	IDI2. UDW 2
9	START CDDE1(51H)								UDW3
10	START CODE2(99H)								UDW4
11	BYTE3								UDW5
.	.								
.	.								
22	BYTE14								UDW16
23	BYTE15								UDW17
24	BI-PHASEERROR								UDW18
25	FILLDATA								UDW19
26	FILLDATA								UDW20
27	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
28	1	0	0	1	0	0	1	0	BC

1.START CODE1 is the first byte of Start Code by 5Mbps slicing.
2.START CODE2 is the second byte of Start Code by 5Mbps slicing.
3.BYTE3~BYTE15 are data bytes by 5/2 Mbps Bi-phase slicing.
4.BI-PHASEEROOR is Bi-phase coding error detection.80H means No error.41H means Bi-phase coding error is detected.

Table 16. VITC ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	1	0	0	0	0	0	1	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	1	0	IDI2. UDW 2
9	Bit[9:2]								UDW3
10	Bit[19:12]								UDW4
11	Bit[29:22]								UDW5
12	.Bit[39:32]								UDW6
13	.Bit[49:42]								UDW7
14	Bit[59:52]								UDW8
15	Bit[69:62]								UDW9
16	Bit[79:72]								UDW10
17	Bit[89:82]								UDW11
18	CRCERROR								UDW12
19	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
20	1	0	0	0	1	1	0	0	BC

1.CRCERROR is CRC Error information.41H means CRC Error is deteced.80H means no CRC error.

Table 17. Gemstar 1X ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	0	1	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	1	0	0	0	IDI2. UDW 2
9	1st Character byte								UDW3
10	2nd Character byte								UDW4
11	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
12	0	0	0	0	0	1	0	0	BC

Table 18. Gemstar 2X ANC data packet

BYTE No.	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	DESCRIPTION
1	0	0	0	0	0	0	0	0	Ancillary dataflag
2	1	1	1	1	1	1	1	1	
3	1	1	1	1	1	1	1	1	
4	NEP	EP	0	DID4	DID3	DID2	DID1	DID0	DID
5	NEP	EP	SDID5	SDID4	SDID3	SDID2	SDID1	SDID0	SDID
6	0	1	0	0	0	0	1	0	DC
7	OP	FID	LN8	LN7	LN6	LN5	LN4	LN3	IDI1. UDW1
8	OP	LN2	LN1	LN0	0	1	1	1	IDI2. UDW 2
9	FRAMECODE1								UDW3
10	FRAMECODE2								UDW4
11	Data Byte 1								UDW5
12	Data Byte 2								UDW6
13	Data Byte 3								UDW7
14	Data Byte 4								UDW8
15	NCS6	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CS
16	0	0	0	0	1	0	0	0	BC

1.FRAMCODE1 is B9H if Frame Code is correctly received.
2.FRAMCODE2 is 05H if Frame Code is correctly received.

VBI Control Registers

PDNSVBI=1 makes VBI slicer function enable.ANCEN=1 makes VBI ANC data output enable.HAMM84=1 makes 8/4Hamming code decoding enable in 8/4 Hamming codes data on Teletext ANC data output.At this time,recieved 7-0 8bit data is converted to 3-0 4bit nibble data with 7-4 bits fixed to 0h. 3-0 4bits has meanings in this HAMM84=1 mode.Typical LCTLn register setting for WSS and CCF1/CCF2 are as follows.

NTSC-M	PAL/SECAM
LCTL20=0x55	LCTL22=0x44
LCTL21=0x44	LCTL23=0x50

Typical European 625-Line Teletext-B settings are as follows.

LCTL6 =0x11	LCTL7 =0x11	LCTL8 =0x11	LCTL9 =0x11	LCTL10=0x11
LCTL11=0x11	LCTL12=0x11	LCTL13=0x11	LCTL14=0x11	LCTL15=0x11
LCTL16=0x11	LCTL17=0x00	LCTL18=0x00	LCTL19=0x00	LCTL20=0x11
LCTL21=0x11	LCTL22=0x11	LCTL23=0x50	LCTL24=0x00	LCTL25=0x00
LCTL26=0x00				

VBI Received Data Registers

TW9900 supports two type VBI received data registers.CCF1DATA1/CCF1DATA2 registers contain Filed 1 Closed Captioning data.CCF2DATA1/CCF2DATA2 registers contain Field 2 Closed Captioning data(EDS data).WSS registers contain 20bit CGMS(WSS) data for NTSC or 14bit WSS data for PAL. Following Figure 4 shows typical access flow of VBI Received Data Registers.

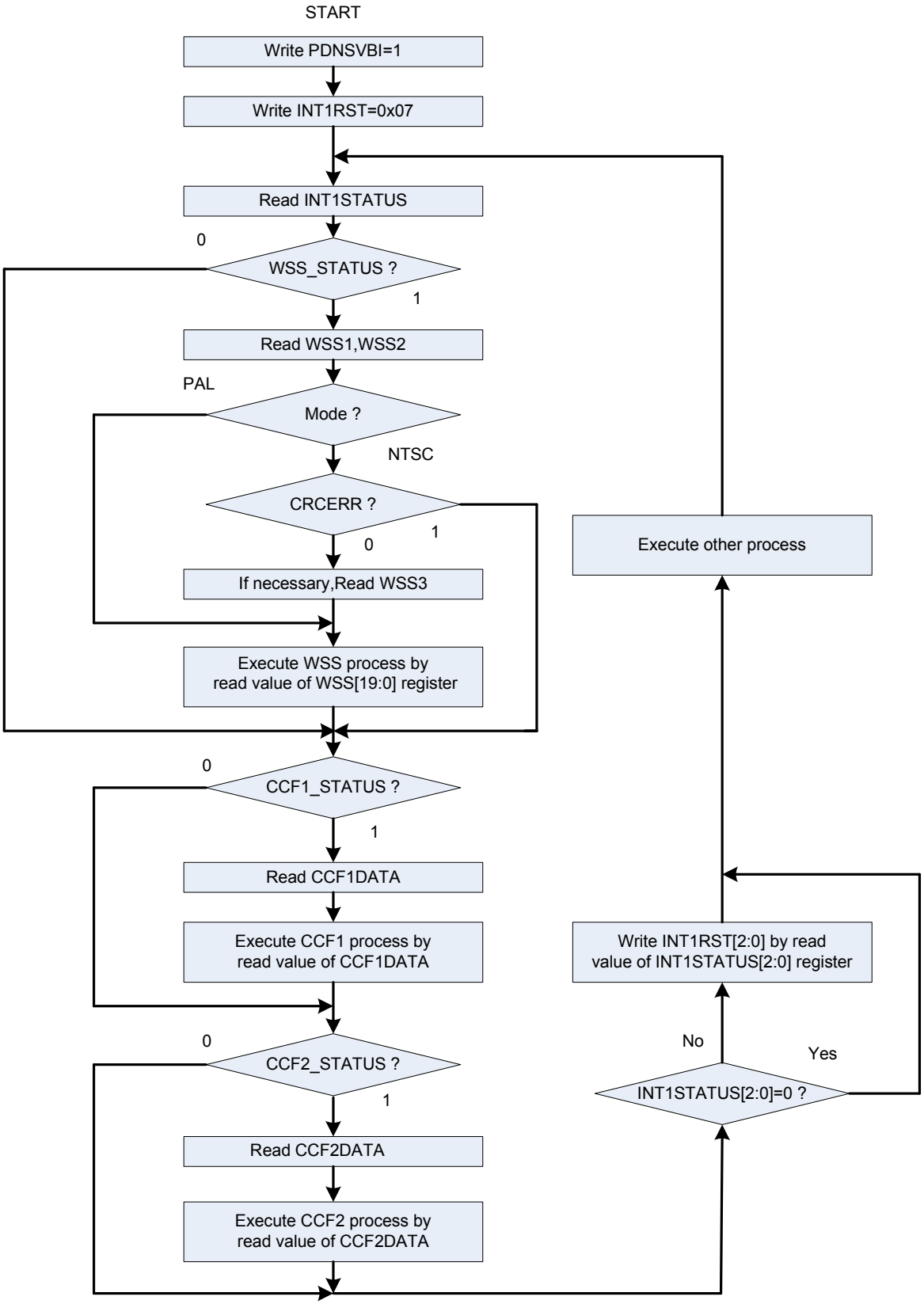


Figure 4. VBI Received Data Register Access

Two Wire Serial Bus Interface

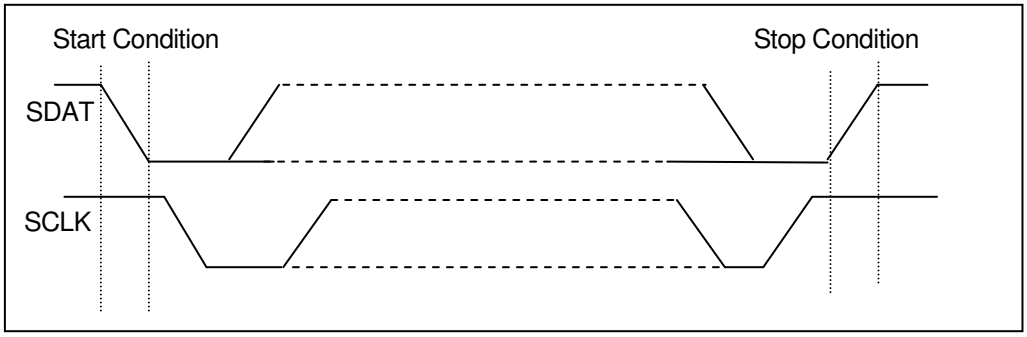


Figure 5. Definition of the serial bus interface bus start and stop

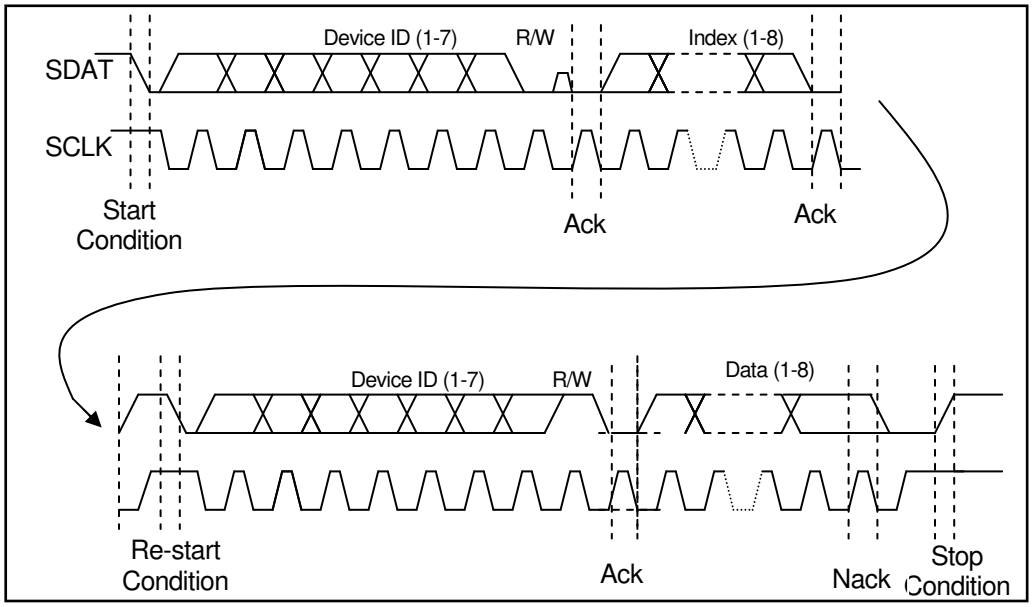


Figure 6. One complete register read sequence via the serial bus interface

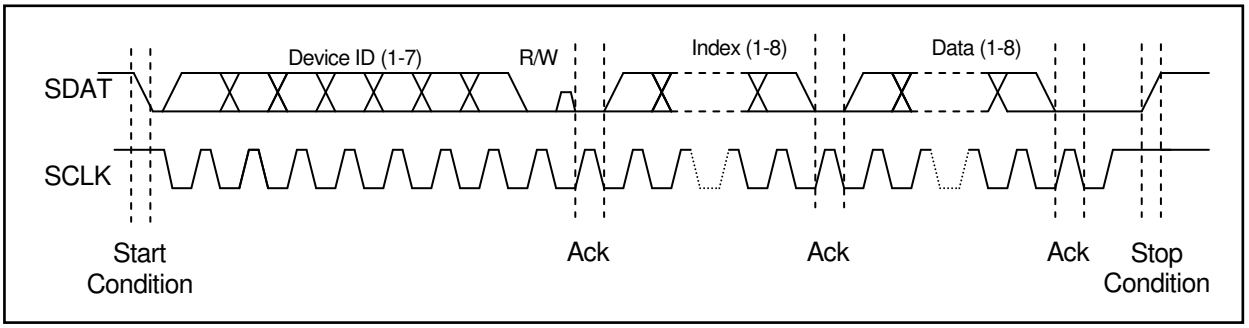


Figure 7. One complete register write sequence via the serial bus interface

The two wire serial bus interface is used to allow an external micro-controller to write control data to, and read control or other information from the TW9900 registers. SCLK is the serial clock and SDAT is the data line. Both lines are pulled high by resistors connected to VDD33. ICs communicate on the bus by pulling SCLK and SDAT low through open drain outputs. In normal operation the master generates all clock pulses, but control of the SDAT line alternates back and forth between the master and the slave. For both read and write, each byte is transferred MSB first, and the data bit is valid whenever SCLK is high.

The TW9900 is operated as a bus slave device. It can be programmed to respond to one of two 7-bit slave device addresses by tying the SIAD (Serial Interface ADdress) pin to either VDD33 or VSSPST (See Table 19) through a pull-up or pull-down resister. The SIAD pin is multi-purpose pin and must not tied to supply voltage or ground directly. If the SIAD pin is tied to VDD33, then the least significant bit of the 7-bit address is a "1". If the SIAD pin is tied to VSSPST then the least significant bit of the 7-bit address is a "0". The most significant 6-bits are fixed. The 7-bit address field is concatenated with the read/write control bit to form the first byte transferred during a new transfer. If the read/write control bit is high the next byte will be read from the slave device. If it is low the next byte will be a write to the slave. When a bus master (the host microprocessor) drives SDAT from high to low, while SCLK is high, this is defined to be a start condition (See Figure 5.). All slaves on the bus listen to determine when a start condition has been asserted.

After a start condition, all slave devices listen for the their device addresses. The host then sends a byte consisting of the 7-bit slave device ID and the R/W bit. This is shown in Figure 6. (For the TW9900, the next byte is normally the index to the TW9900 registers and is a write to the TW9900 therefore the first R/W bit is normally low.)

After transmitting the device address and the R/W bit, the master must release the SDAT line while holding SCLK low, and wait for an acknowledgement from the slave. If the address matches the device address of a slave, the slave will respond by driving the SDAT line low to acknowledge the condition. The master will then continue with the next 8-bit transfer. If no device on the bus responds, the master transmits a stop condition and ends the cycle. Notice that a successful transfer always includes nine clock pulses.

To write to the internal register of theTW9900, the master sends another 8-bits of data, the TW9900 loads this to the register pointed by the internal index register. The TW9900 will acknowledge the 8-bit data transfer and automatically increment the index in preparation for the next data. The master can do multiple writes to the TW9900 if they are in ascending sequential order. After each 8-bit transfer the TW9900 will acknowledge the receipt of the 8-bits with an acknowledge pulse. To end all transfers to the TW9900 the host will issue a stop condition.

Serial Bus Interface 7-bit Slave Address							Read/Write bit
1	0	0	0	1	0	SIAD0	1=Read 0=Write

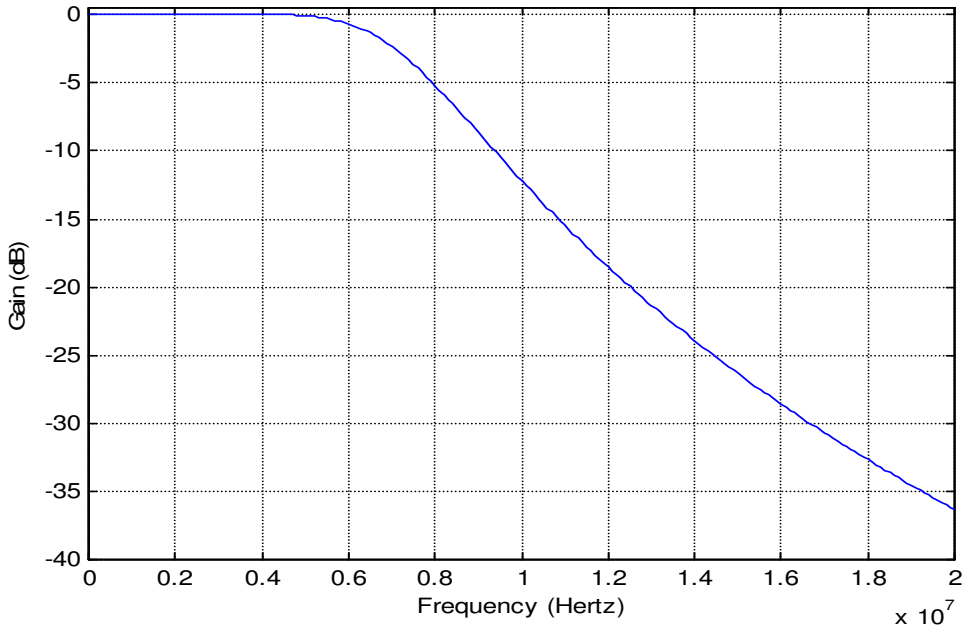
Table 19 TW9900 serial bus interface 7-bit slave address and read write bit

A TW9900 read cycle has two phases. The first phase is a write to the internal index register. The second phase is the read from the data register. (See figure 6). The host initiates the first phase by sending the start condition. It then sends the slave device ID together with a 0 in the R/W bit position. The index is then sent followed by either a stop condition or a second start condition. The second phase starts with the second start condition. The master then resends the same slave device ID with a 1 in the R/W bit position to indicate a read. The slave will transfer the contents of the desired register. The master remains in control of the clock. After transferring eight bits, the slave releases and the master takes control of the SDAT line and acknowledges the receipt of data to the slave. To terminate

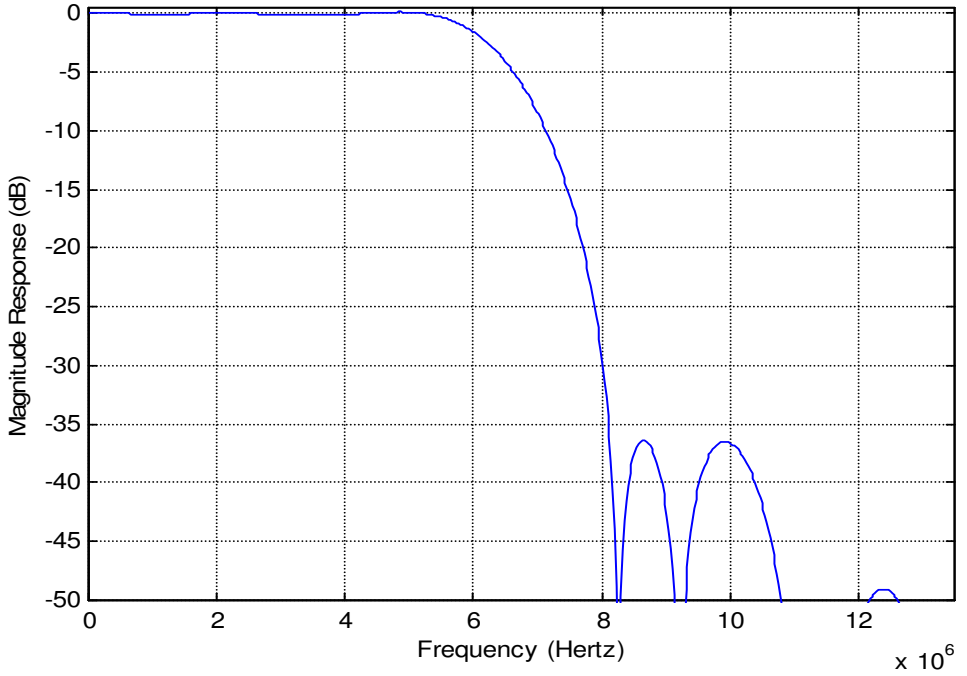
the last transfer the master will issue a negative acknowledge (SDAT is left high during a clock pulse) and issue a stop condition.

Filter Curves

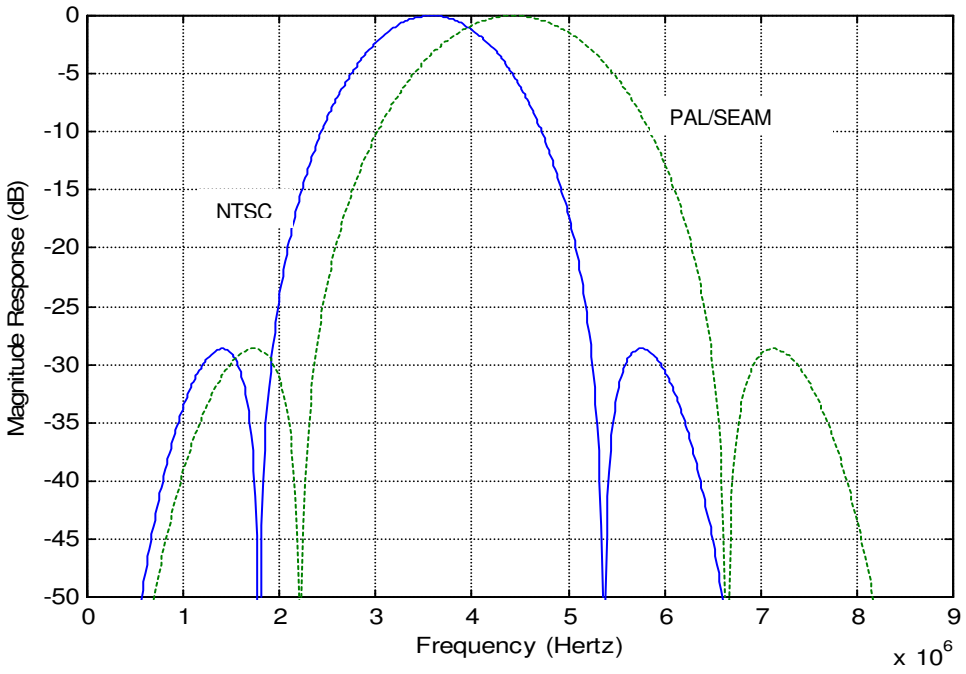
Anti-alias filter



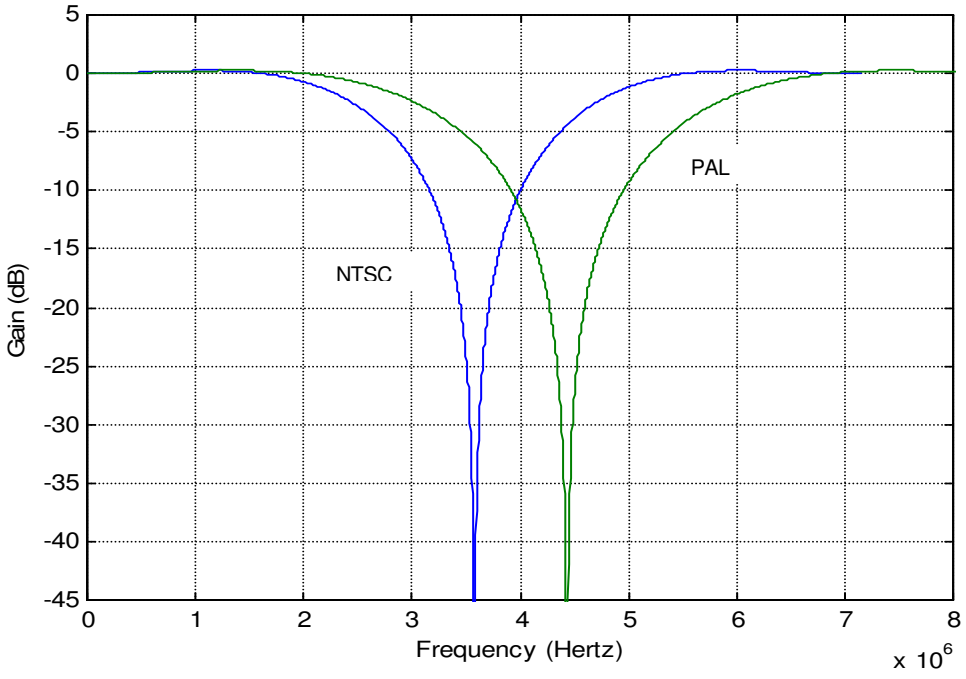
Decimation filter



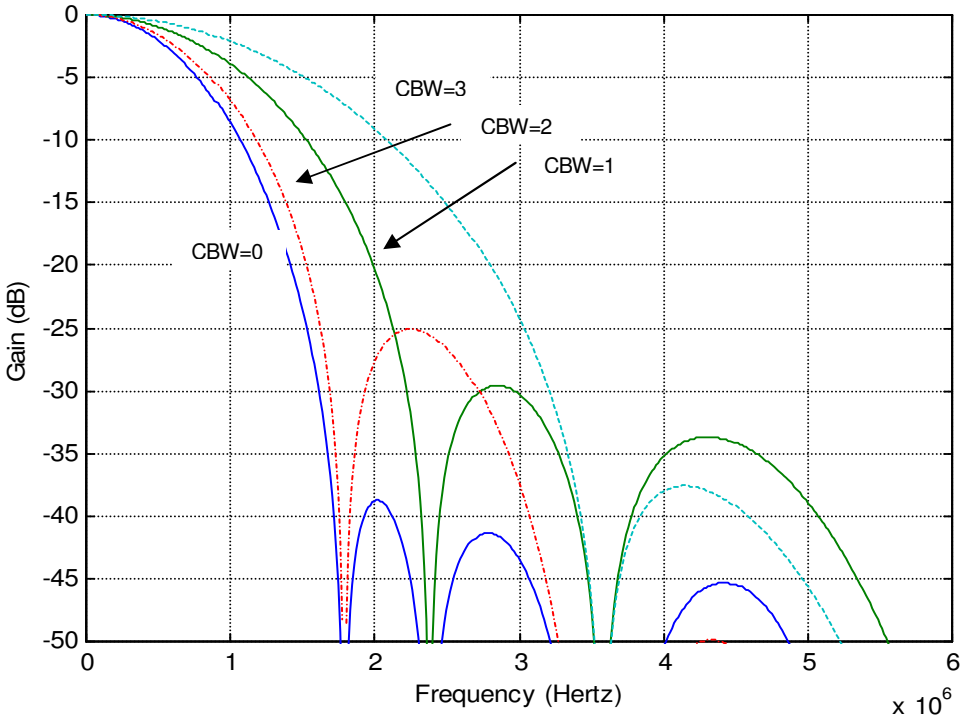
Chroma Band Pass Filter Curves



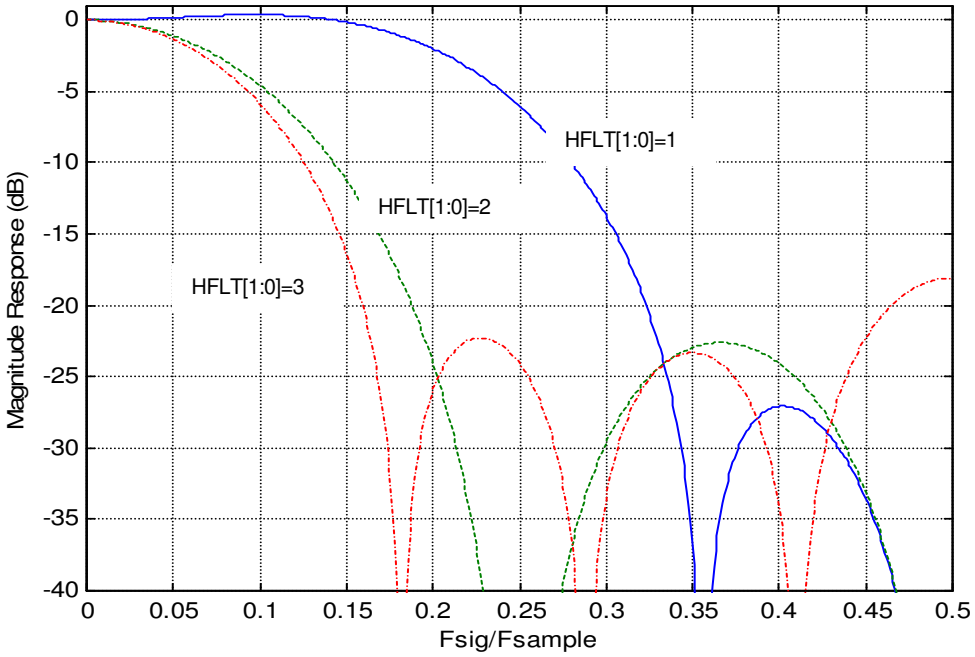
Luma Notch Filter Curve for NTSC and PAL/SECAM



Chrominance Low-Pass Filter Curve

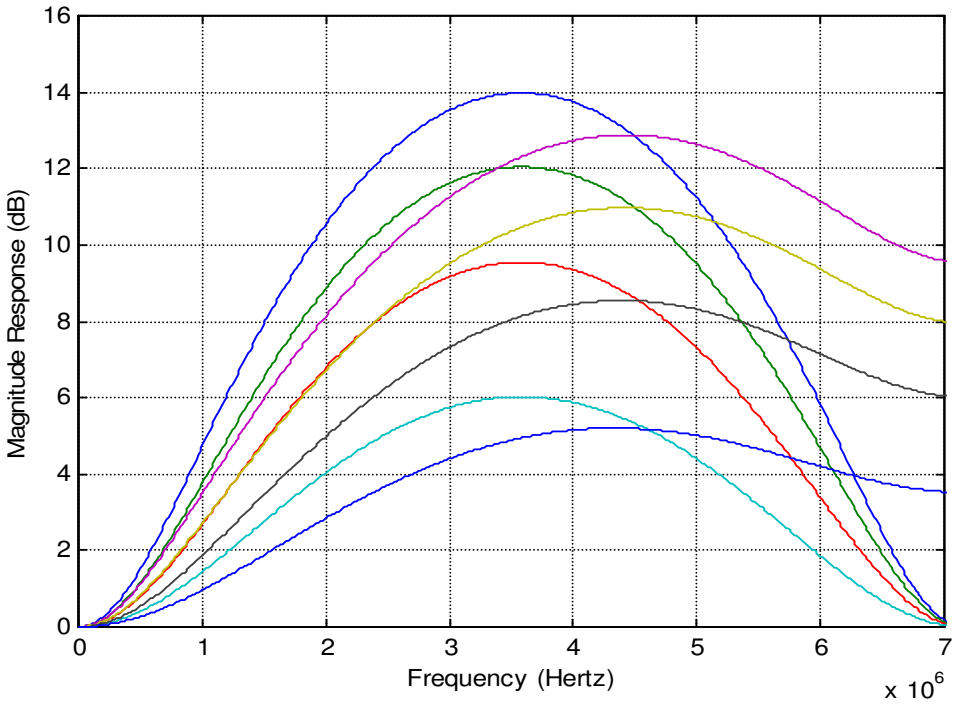


Horizontal Scaler Pre- Filter curves

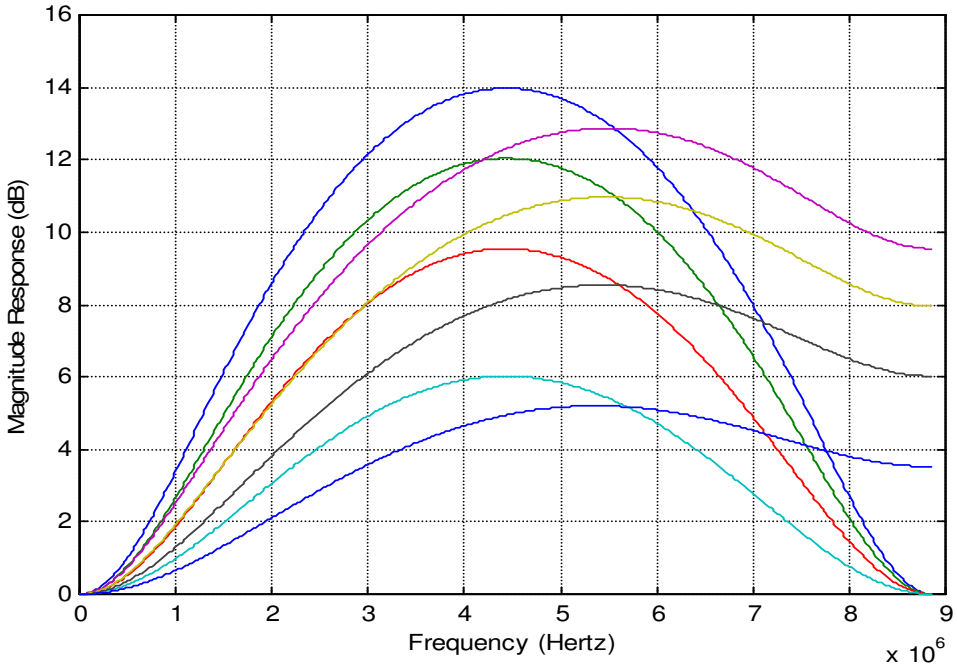


Peaking Filter Curves

NTSC

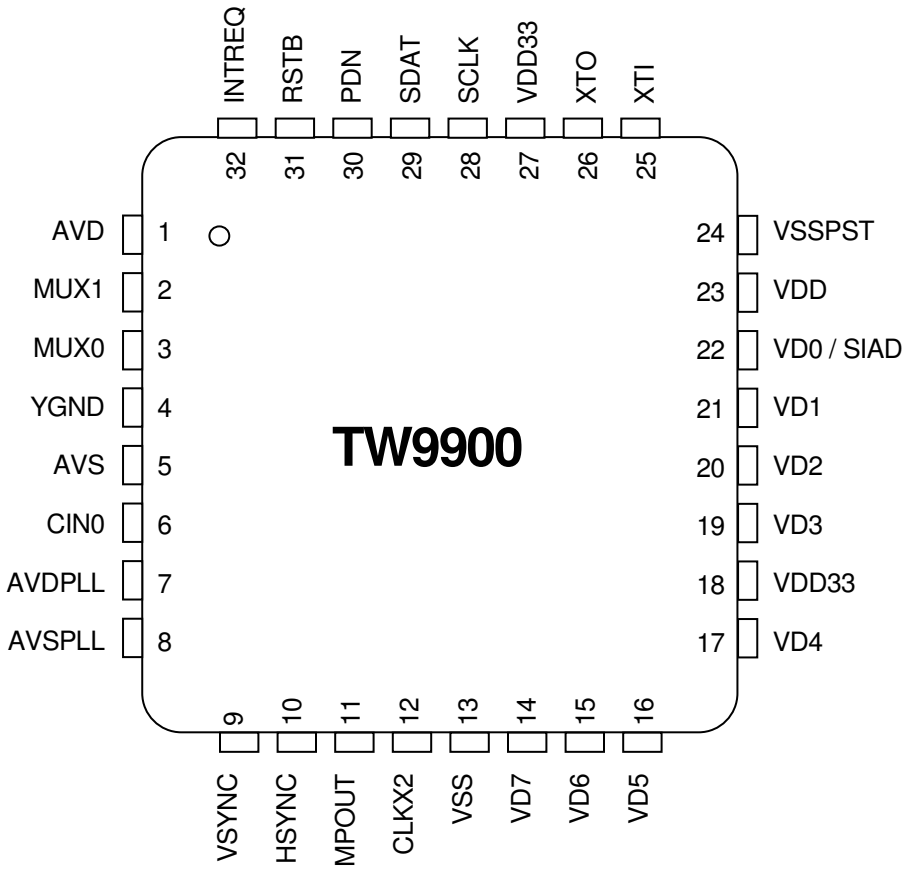


PAL



Pin Diagram

32 PIN TQFP, 32 PIN QFN



Pin Description

Pin#	I/O	Pin Name	Description
Analog video signals			
3	I	MUX0	Analog CVBS or Y input. Connect unused input to AGND through 0.1uF capacitor.
2	I	MUX1	Analog CVBS or Y input. Connect unused input to AGND through 0.1uF capacitor.
4		YGND	Analog Differential input for Y-ADC.
6	I	CIN0	Analog chroma input. Connect unused input to AGND through 0.1uF capacitor.
Clock Signals			
25	I	XTI	Clock input. A 27MHz fundamental (or 3rd overtone) crystal or a single-ended oscillator can be connected.
26	O	XTO	Clock output. For connecting a crystal.
Host Interface			
28	I	SCLK	The MPU Serial interface Clock Line.
29	I/O	SDAT	The MPU Serial interface Data Line.
General signals			
31	I	RSTB	Reset input. Low active.
30	I	PDN	Power down control pin. It is high active.
32	O	INTREQ	Interrupt output signal.
Video output Signals			
10	O	HSYNC	Horizontal sync and multi-purpose output pin. See register for control information.
9	O	VSYNC	Vertical Sync and multi-purpose output. See register for control information.
12	O	CLKX2	Data Clock output. See register for control information.
11	O	MPOUT	Multi-purpose output pin. The output function can be selected by RTSEL of register 0x19
14 **15** **16** **17** **19** **20** **21**	I/O	VD[7:1]	Digitized video data output of 4:2:2 YCbCr. VD[7] is the MSB.
22	I/O	VD[0]/ SIAD0	LSB of digitized video data output of 4:2:2 YCbCr. SIAD0 : The MPU interface address select pin 0. A pullup or pulldown resister is needed for select one of the two addresses that chip will respond.

Power and Ground Pins

Pin#	I/O	Pin Name	Description
23	I	VDD	1.8V digital core power.
13	I	VSS	1.8V digital core return
18 **27**	I	VDD33	3.3V digital I/O power.
24	I	VSSPST	3.3V digital I/O return
1	I	AVD	1.8V analog ADC supply
5	I	AVS	1.8V analog ADC return
7	I	AVDPLL	1.8V PLL supply
8	I	AVSPLL	1.8V PLL return

Parametric Information

AC/DC Electrical Parameters

Table 21. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
AVD, AVDPLL (measured to AVS, AVSPLL)	V_{DDAM}	-	-	1.92	V
V DD (measured to VSS)	V_{DDM}		-	1.98	V
VDD33 (measured to VSSPST)	V_{DD33M}		-	3.6	V
Voltage on any digital signal pin (See the note below)	-	VSSPST –0.5	-	5.5	V
Analog Input Voltage	-	AVS – 0.5	-	1.92	V
Storage Temperature	T_S	–65	-	+150	℃
Junction Temperature	T_J	-	-	+125	℃
Reflow Soldering	T_{PEAK}	255 +5/-0 (10-30 seconds)			℃

NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the ranges list in Table 21 can induce destructive latch-up.

Table 22. characteristics

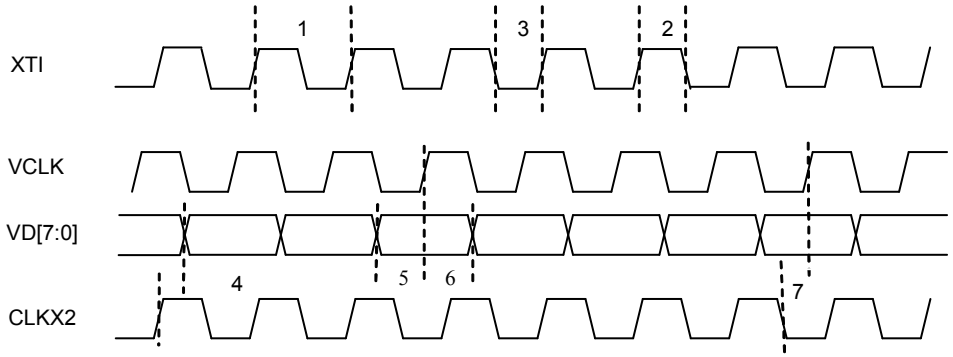
Parameter	Symbol	Min	Typ	Max	Units
Supply					
Power Supply — IO	V_{DD33}	3.15	3.3	3.6	V
Power Supply — Analog	V_{DDA}	1.62	1.8	1.92	V
Power Supply — Digital	V_{DD}	1.62	1.8	1.98	V
Maximum $\|V_{DD} - AVD\|$		-	-	0.3	V
MUX0, MUX1 Input Range (AC coupling required)		0.5	1.00	1.40	V
CIN0 Amplitude Range (AC coupling required)		0.5	1.00	1.40	V
Ambient Operating Temperature	T_A	-40		+85	℃
Analog Supply current : CVBS	Iaa	-	14.6	-	mA
S-video		-	23.4	-	mA
Digital I/O Supply current	Idde	-	8	-	mA
Digital Core Supply Current	Idd	-	25	-	mA
Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0	-	-	V
Input Low Voltage (TTL)	V_{IL}	-	-	0.8	V
Input High Voltage (XTI)	V_{IH}	2.0	-	V_{DD33} + 0.5	V

Input Low Voltage (XTI)	V_{IL}	-	-	0.8	V
Input High Current ($V_{IN}=V_{DD}$)	I_{IH}	-	-	10	µA
Input Low Current (V_{IN}=VSS)	I_{IL}	-	-	–10	µA
Input Capacitance (f=1 MHz, V_{IN}=2.4 V)	C_{IN}	-	5	-	pF

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Digital Outputs					
Output High Voltage (I_{OH} = –2 mA)	V_{OH}	2.4	-	V_{DD33}	V
Output Low Voltage (I_{OL} = 2 mA)	V_{OL}	-	0.2	0.4	V
3-State Current	I_{OZ}	-	-	10	µA
Output Capacitance	C_O	-	5	-	pF
Analog Input					
Analog Pin Input voltage	Vi	-	1	-	Vpp
Analog Pin Input Capacitance	C_A	-	7	-	pF
ADCs					
ADC resolution	ADCR	-	10	-	bits
ADC integral Non-linearity	AINL	-	±1	-	LSB
ADC differential non-linearity	ADNL	-	±1	-	LSB
ADC clock rate	f_{ADC}	24	27	30	MHz
Video bandwidth (-3db)	BW	-	10	-	MHz
Horizontal PLL					
Line frequency (50Hz)	f_{LN}	-	15.625	-	KHz
Line frequency (60Hz)	f_{LN}	-	15.734	-	KHz
static deviation	Δf_H	-	-	6.2	%
Subcarrier PLL					
subcarrier frequency (NTSC-M)	f_{SC}	-	3579545	-	Hz
subcarrier frequency (PAL-BDGHI)	f_{SC}	-	4433619	-	Hz
subcarrier frequency (PAL-M)	f_{SC}	-	3575612	-	Hz
subcarrier frequency (PAL-N)	f_{SC}	-	3582056	-	Hz
lock in range	Δf_H	±450	-	-	Hz
Crystal spec					
nominal frequency (fundamental)		-	27	-	MHz
Deviation * * Crystal deviation is base on normal operation condition		-	-	±50	ppm
load capacitance	CL	-	20	-	pF
series resistor	RS	-	80	-	Ohm
Oscillator Input					
nominal frequency		-	27	-	MHz
deviation		-	-	±50	ppm
duty cycle		-	-	55	%

Parameter	Symbol	Min	Typ	Max	Units
Output CLK					
CLKX2	1	24	27	30	MHz
CLKX2 Duty Cycle	2	-	-	55	%
CLKX2 to Data Delay	4	-	5	-	ns
CLKX2 (Falling Edge) to VCLK (Rising Edge)	7	-	0	-	ns
Output Video Data					
Data to VCLK (Rising Edge) Delay	5	-	18	-	ns
VCLK (Rising Edge) to Data Delay	6	-	18	-	ns

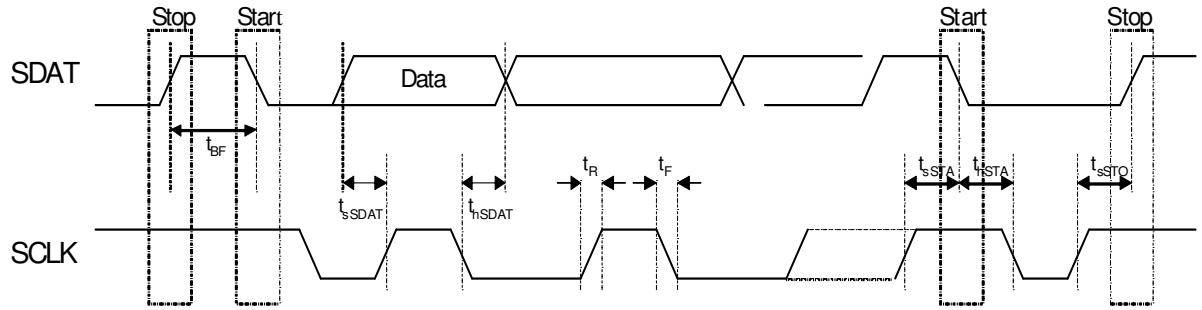
Clock Timing Diagram



Serial Host Interface Timing

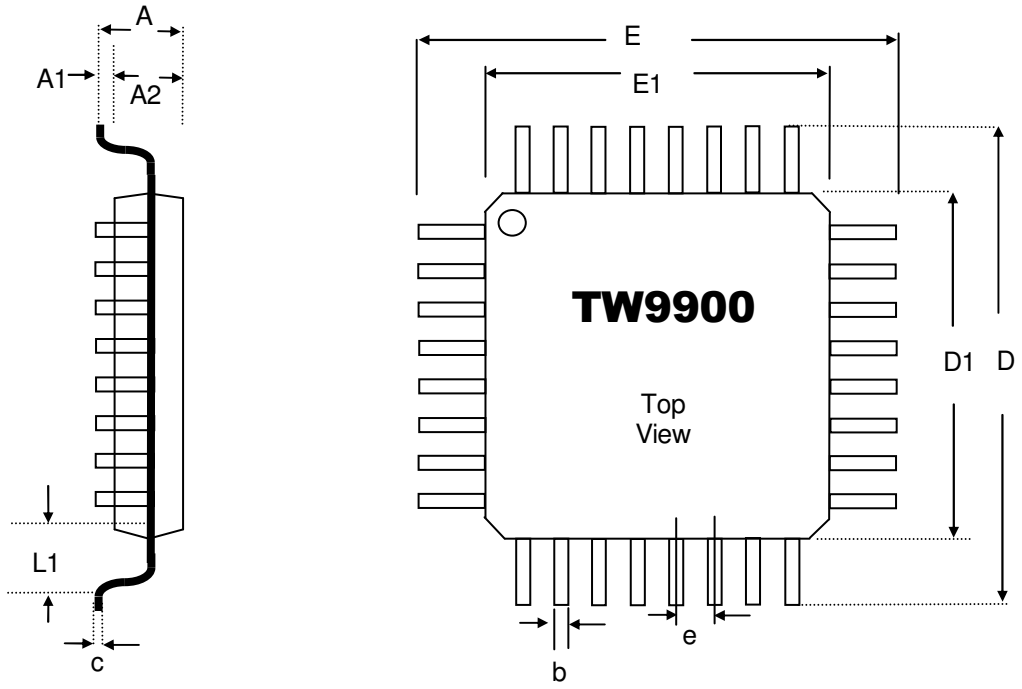
Parameter	Symbol	Min	Typ	Max	Units
Bus Free Time between STOP and START	t_{BF}	740			ns
SDAT setup time	t_{sSDAT}	74			ns
SDAT hold time	t_{hSDAT}	50		900	ns
Setup time for START condition	t_{sSTA}	370			ns
Setup time for STOP condition	t_{sSTOP}	370			ns
Hold time for START condition	t_{hSTA}	74			ns
Rise time for SCLK and SDAT	t_R			300	ns
Fall time for SCLK and SDAT	t_F			300	ns
Capacitive load for each bus line	C_{BUS}			400	pF
SCLK clock frequency	f_{SCLK}			400	KHz

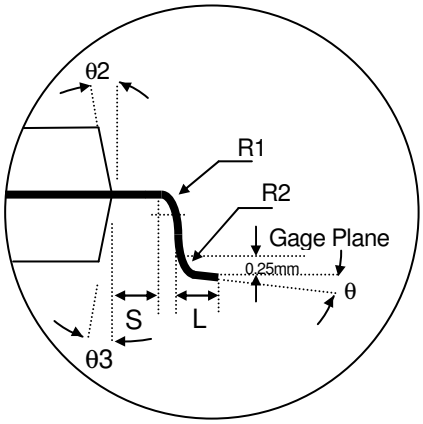
Serial Host Interface Timing Diagram

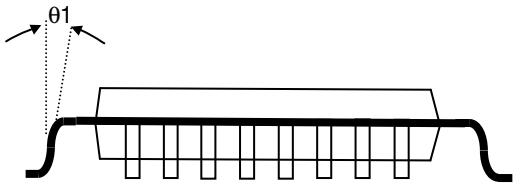


Mechanical Data

32 Pin TQFP





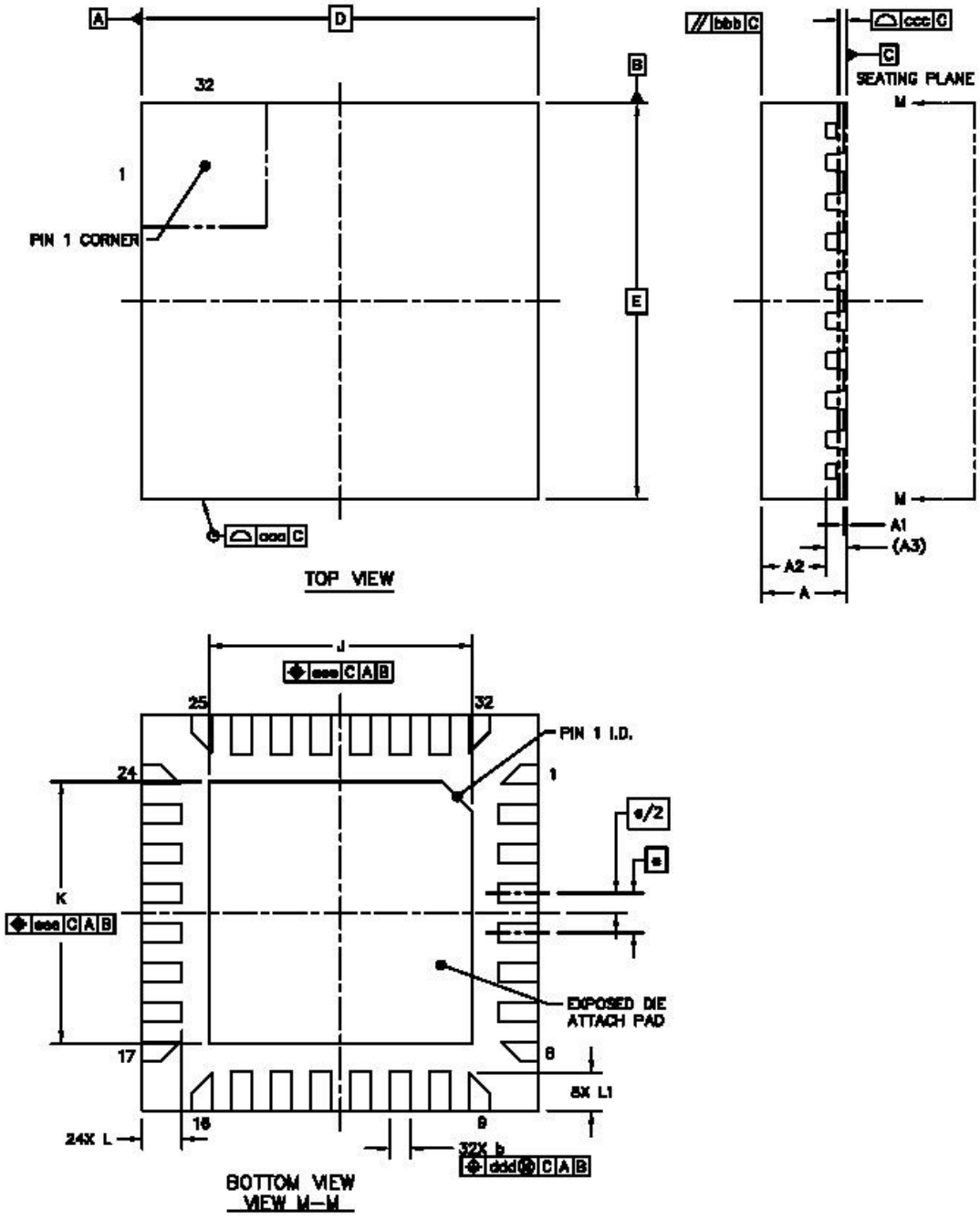


SYMBOL	MILLIMETER		
	MIN		MAX
A	---		1.2
A1	0.05		0.15
A2	0.95		1.05
D	7 BSC		
D1	5 BSC		
E	7 BSC		
E1	5 BSC		
R2	0.08		---
R1	0.08		
θ	0°		7°
θ1	0°		---
θ2	11°		13°
θ3	11°		13°
c	0.09		0.2
L	0.45		0.75
L1	1 REF		
S	0.2		---
b	0.17		0.27
e	0.5 BSC		

NOTES:

1. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
2. Dimension b does not include dam bar protrusion. Allowable dam bar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm.
   Dam bar can not be located on the lower radius or the foot. Minimum space between protrusion and a adjacent lead is 0.07mm.

32 Pin QFN

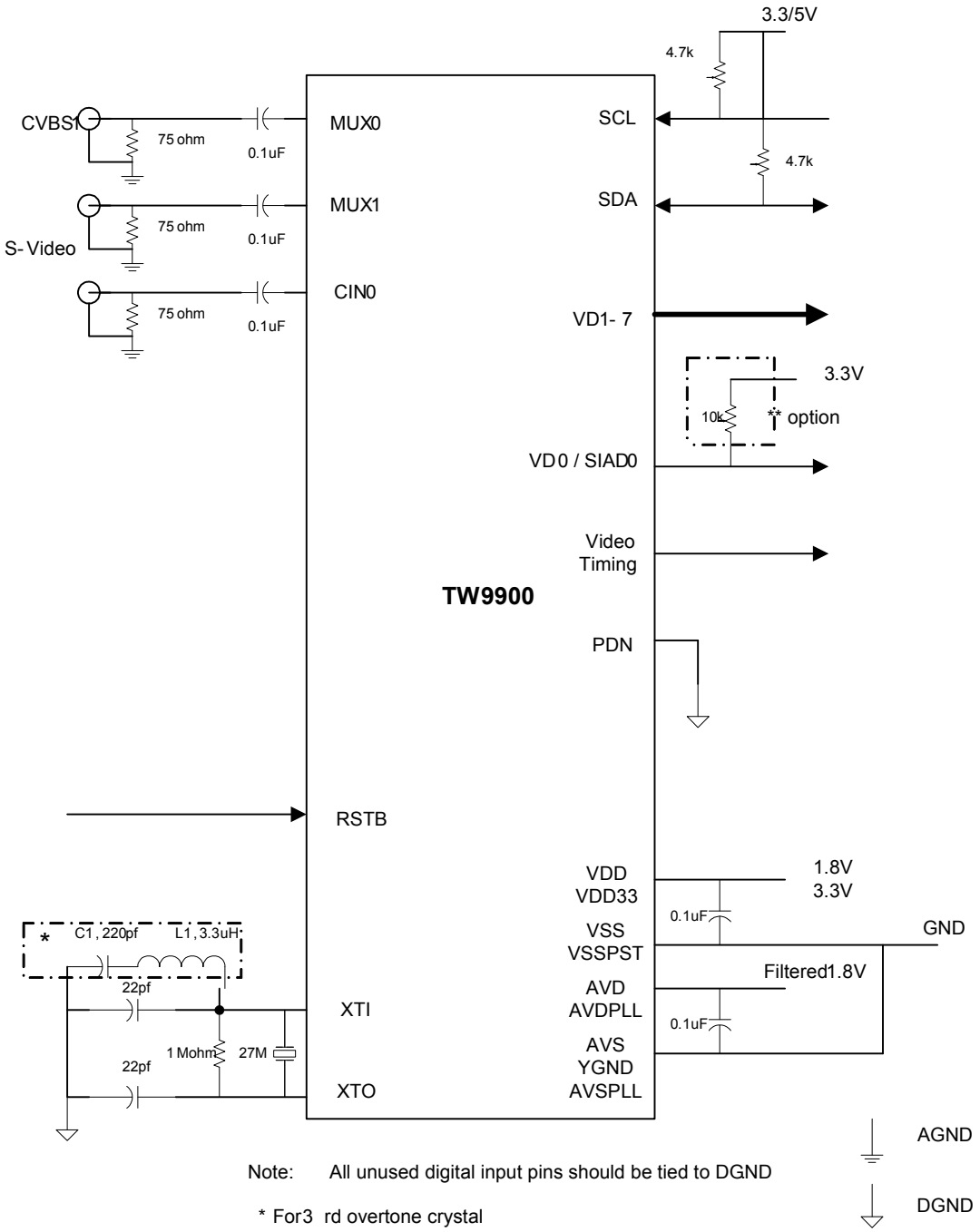

A
D
B
32
1
PIN 1 CORNER
E
TOP VIEW
bbb C
ccc C
C
SEATING PLANE
M
A1
(A3)
A2
A
J
eee C A B
25
32
PIN 1 I.D.
24
1
e/2
e
K
EXPOSED DIE
ATTACH PAD
17
8
8X L1
16
9
24X L
32X b
ddd M C A B
BOTTOM VIEW
VIEW M–M

	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	0.8	0.85	0.90
STAND OFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	---	0.65	0.67
L/F THICKNESS	A3	0.203 REF.		
LEAD WIDTH	b	0.15	0.2	0.25
BODY SIZE	D	4 BSC		
	E	4 BSC		
LEAD PITCH	e	0.4 BSC		
EP SIZE	J	2.55	2.65	2.75
	K	2.55	2.65	2.75
LEAD LENGTH	L	0.35	0.40	0.45
	L1	0.332	0.382	0.432
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	bbb	0.1		
COPLANARITY	ccc	0.08		
LEAD OFFSET	ddd	0.1		
EXPOSED PAD OFFSET	eee	0.1		

Notes :

1. Coplanarity applies to leads, corner leads and die attach pad.

Application Schematics



Note: All unused digital input pins should be tied to DGND

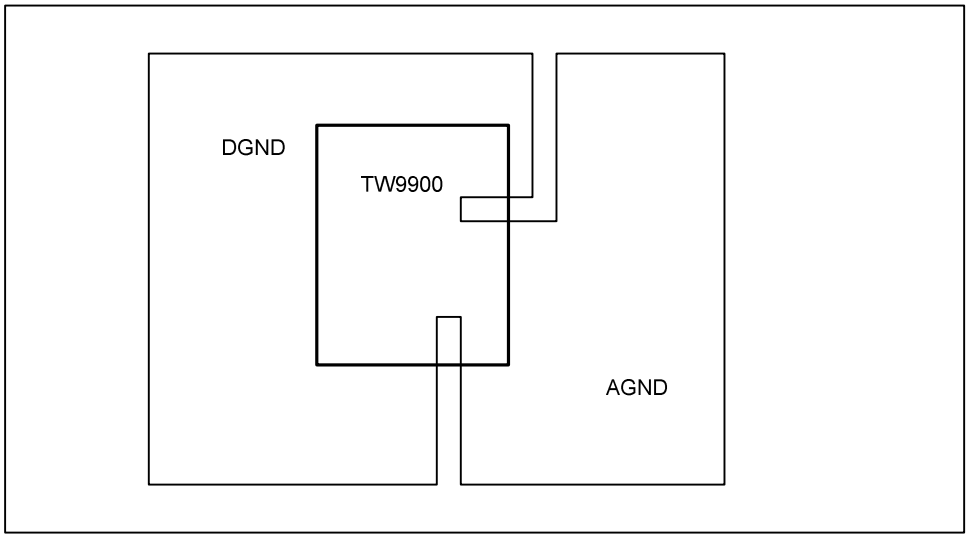
* For3 rd overtone crystal

Typical TW9900 External Circuitry

PCB Layout Considerations

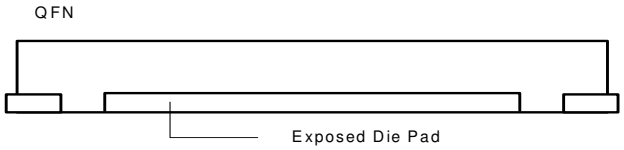
The PCB layout should be done to minimize the power and ground noise on the TW9900. This is done by good power de-coupling with minimum lead length on the de-coupling capacitors; well-filtered and regulated analog power input shielding and ground plane isolation.

The ground plane should cover most of the PCB area with separated digital and analog ground planes surrounding the chip. These two planes should be at the same electrical potential and connected together under TW9900. The following figure shows a ground plane layout example.



To minimize crosstalk, the digital signals of TW9900 should be separated from the analog circuitry. Moreover, the digital signals should not cross over the analog power and ground plane. Parallel running of digital lines for long distance should also be avoided.

For QFN Package, the Exposed die pad (Ground bond) can be either floating or soldered to PCB Ground to enhance thermal performance.



Thermal Pad Consideration

Thermal Pad Land Design

The size of the thermal land should at least match the exposed die flag size. But it is necessary to avoid solder bridging between thermal pad and the perimeter pads. We recommend the clearance between thermal pad and perimeter pads is 0.15 mm.

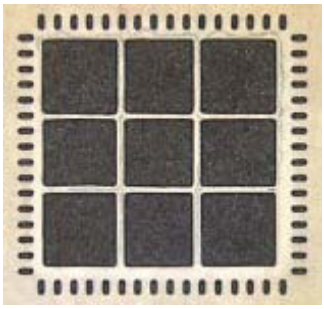
Thermal Via Design

In order to take full advantage of QFN thermal performance, thermal vias are needed to provide a thermal path from top to inner/ bottom layers of the motherboard to remove the heat.

- Via size(in diameter): 0.3 ~ 0.33mm
- Via pitch: 1.0 ~ 1.2 mm
- # of thermal vias : depend on the application

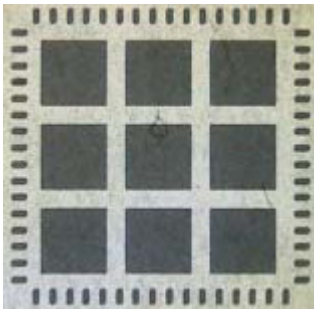
Stencil recommendation *

- The small multiple openings should be used in steady of one big opening.
  - 60 ~ 85% solder paste coverage
  - Rounded corners to minimize clogging
  - Positive taper with bottom opening larger than the top



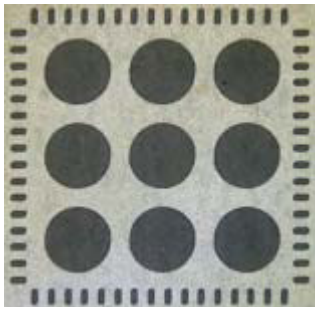
Don't recommend

Coverage 91%



Recommend

Coverage 77%



Recommend

Coverage 65%

* Note: About stencil opening pictures are for reference only, please check 48 pin QFN Mechanical Data for detail size information.

Control Register

TW9900 Register SUMMARY

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
00	ID					REV			00
01	VDLOSS	HLOCK	SLOCK	FIELD	VLOCK	-	MONO	DET50	00
02	-	FC27	IFSEL		YSEL		-	-	40
03	MODE	-	LLCMODE	AINC	-	OEN	TRI_SEL		04
04	GMEN	CKHY		HSDLY					00
05	VSP	VSSL			HSP	HSSL			00
06	SRESET	IREF	VREF	AGC_EN	CLKPDN	Y_PDN	C_PDN	-	00
07	VDELAY_HI		VACTIVE_HI		HDELAY_HI		HACTIVE_HI		02
08	VDELAY_LO								12
09	VACTIVE_LO								F0
0A	HDELAY_LO								10
0B	HACTIVE_LO								D0
0C	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY	CC
0D	-								00
0E	-								11
0F	-								00
10	BRIGHTNESS								00
11	CONTRAST								64
12	SCURVE	-	CTI		SHARPNESS				11
13	SAT_U								80
14	SAT_V								80
15	HUE								00
16	-	SV_DET	-	-	-				00
17	SHCOR				-	VSHP			30
18	CTCOR		CCOR		VCOR		CIF		44
19	VBI_EN	VBI_BYT	VBI_FRAM	HA_EN	-	RTSEL			58
1A	LLCTEST	PLL_PDN	-	-	YFLEN	YSV	CFLEN	CSV	00
1B	CK2S		CK1S		-	-			00
1C	DTSTUS	STDNOW			ATREG	STANDARD			07
1D	START	PAL60	PALCN	PALM	NTSC4	SECAM	PALB	NTSC	7F
1E	NT50	-	-	-	-				08
1F	TEST								00

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
20	CLPEND				CLPST				50
21	NMGAIN				WPGAIN			AGCGAIN[8]	42
22	AGCGAIN[7:0]								F0
23	PEAKWT								D8
24	CLMPLD	CLMPL							BC
25	SYNCTD	SYNCT							B8
26	MISSCNT				HSWIN				44
27	PCLAMP								2A
28	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT	00
29	BSHT			VSHT					00
2A	CKILMAX		CKILMIN						78
2B	HTL				VTL				44
2C	CKLM	YDLY			HFLT				30
2D	HPLC	EVCNT	PALC	SDET	OPLMT	BYPASS	SYOUT	HADV	14
2E	HPM		ACCT		SPM		CBW		A5
2F	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST	E0
30	SF	PF	FF	KF	CSBAD	MCVSN	CSTRIPE	CTYPE	00
31	VCR	WKAIR	WKAIR1	VSTD	NINTL	WSSDET	EDSDET	CCDET	00
32	HFREF								X
33	FRM		YNR		CLMD		PSP		05
34	IDX		NSEN / SSEN / PSEN / WKTH						1E
35	CTEST	YCLEN	CCLEN	VCLEN	GTEST	VLPF	CKLY	CKLC	00
36	-								
.	-								
.	-								
.	-								
4C	0	0	0	0	PLL_IREF	CP_SEL	BYPASS_SEL	LPRES_SEL	05

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
4D	ADCMD	VBIMIN							40
4E	0	HSBEGIN[2:0]			0	HSEND[2:0]			00
4F	0	0	WSS[19:14]						00
50	FILLDATA								A0
51	NODAEN	SYRM	SDID						22
52	ANCEN	-	VIPCFG	DID					31
53	CRCERR	WSSFLD	WSS[13:8]						80
54	WSS[7:0]								00
55	HA656	-	HAMM84	NTSC656	VVBI				00
56	LCTL6								00
57	LCTL7								00
58	LCTL8								00
59	LCTL9								00
5A	LCTL10								00
5B	LCTL11								00
5C	LCTL12								00
5D	LCTL13								00
5E	LCTL14								00
5F	LCTL15								00
60	LCTL16								00
61	LCTL17								00
62	LCTL18								00
63	LCTL19								00
64	LCTL20								00
65	LCTL21								00
66	LCTL22								00
67	LCTL23								00
68	LCTL24								00
69	LCTL25								00
6A	LCTL26								00
6B	HSBEGIN[10:3]								06
6C	HSEND[10:3]								24
6D	OVSDLY								00
6E	HSPIN	OFDLY			VSMODE	OVSEND			20
6F	PDNSVBI	ANCDMODE	VBIDELAY						13

Index (HEX)	7	6	5	4	3	2	1	0	Reset (hex)
AE	F1LIEN	F2LIEN	LINENUMBER						1A
AF	INTOEN	INTPOL	-						80
B0	INT1ENABLE								00
B1	INT2ENABLE								00
B2	-								00
B3	INT1RST								00
B4	INT2RST								00
B5	-								00
B6	INT1RAWSTATUS								00
B7	INT2RAWSTATUS								20
B8	-								00
B9	INT1STATUS								00
BA	INT2STATUS								00
BB	-								00
BC	-								00
BD	CCF1DATA1								80
BE	CCF1DATA2								80
BF	CCF2DATA1								80
C0	CCF2DATA2								80

0x00 – Product ID Code Register (ID)

Bit	Function	R/W	Description	Reset
7-3	ID	R	The TW9900 Product ID code is 00000.	0
2-0	Revision	R	The revision number.	0

0x01 – Chip Status Register I (STATUS1)

Bit	Function	R/W	Description	Reset
7	VDLOSS	R	1 = Video not present. (Sync is not detected in number of line periods specified by MISSCNT register) 0 = Video detected.	0
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK	R	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
4	FIELD	R	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2			Reserved	0
1	MONO	R	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual output vertical scanning frequency depends on the current standard invoked.	0

0x02 – Input Format (INFORM)

Bit	Function	R/W	Description	Reset
7		R/W	Reserved.	0
6	FC27	R/W	1 = Input crystal clock frequency is 27MHz. 0 = Square pixel mode. Must use 24.54MHz for 60Hz field rate source or 29.5MHz for 50Hz field rate source.	1
5-4	IFSEL	R/W	01 = S-video decoding 00 = Composite video decoding	0
3-2	YSEL	R/W	These two bits control the Y input video selection. 00 = Mux0 selected 01 = Mux1 selected 10 = Reserved 11 = Reserved	0
1-0		R/W	Reserved	0

0x03 – Output Format Control Register (OPFORM)

Bit	Function	R/W	Description	Reset
7	MODE	R/W	0 = CCIR601 compatible YCrCb 4:2:2 format with separate syncs and flags. 1 = ITU-R-656 compatible data sequence format.	0
6	LEN	R/W	0 = 8-bit YCrCb 4:2:2 output format. 1 = Reserved	0
5	LLCMODE	R/W	1 = LLC output mode. 0 = Reserved	1
4	AINC	R/W	Serial interface auto-indexing control 0 = auto-increment 1 = non-auto	0
3		R/W	Reserved	0
2	OEN	R/W	Output Enable together with TRI_SEL.	1
1-0	TRI_SEL	R/W	With bit OEN, there three bits select the outputs to be tri-stated(OEN, TRI_SEL[1], TRI_SEL[0]). There are three major groups that can be independently tri-stated: timing group (HSYNC, VSYNC, MPOUT), data group VD[7:0], and clock CLKX1 according to following definition. 000 = All output on. 001 = Data group and Clock group on. 010 = All output on. 011 = Reserved. 100 = All tri-state except Clock group. 101 = Data group and Clock group on. 110 = All output on. 111 = All tri-stated.	0

0x04 – Color Killer Hysteresis and HSYNC Delay Control

Bit	Function	R/W	Description	Reset
7	GMEN	R/W	Factory use only	0
6-5	CKHY	R/W	Color killer hysteresis. 0 – fastest 1 – fast 2 – medium 3 - slow	0
4-0	HSDLY	R/W	Factory use only	0

0x05 – Output Control I

Bit	Function	R/W	Description	Reset
7	VSP	R/W	0 = VSYNCS pin output polarity is active low 1 = VSYNC pin output polarity is active high.	0
6-4	VSSL	R/W	VSYNC pin output control 0 = VSYNC 1 = VACT 2 = FIELD 3 - 5 = Reserved 6 = Factory test only 7 = 0	0
3	HSP	R/W	0 = HSYNC pin output polarity is active low 1 = HSYNC pin output polarity is active high.	0
2-0	HSSL	R/W	HSYNC pin output control 0 = HACT 1 = HSYNC 2 = HLOCK 3 = ASYNCW 4 - 5 = Reserved 6 = Factory test only 7 = 0	0

0x06 – Analog Control Register (ACNTL)

Bit	Function	R/W	Description	Reset
7	SRESET	W	An 1 written to this bit resets the device to its default state but all register content remain unchanged. This bit is self-resetting.	0
6	IREF	R/W	0 = Internal current reference 1. 1 = Internal current reference 2.	0
5	VREF	R/W	1 = Internal voltage reference. 0 = Internal voltage reference shut down.	0
4	AGC_EN	R/W	0 = AGC loop function enabled. 1 = AGC loop function disabled. Gain is set to by AGCGAIN.	0
3	CLK_PDN	R/W	0 = Normal clock operation. 1 = System clock in power down mode, but the MPU INTERFACE module and output clocks (CLKX1 and CLKX2) are still active.	0
2	Y_PDN	R/W	0 = Luma ADC in normal operation. 1 = Luma ADC in power down mode.	0
1	C_PDN	R/W	0 = Chroma ADC in normal operation. 1 = Chroma ADC in power down mode.	0
0		R/W	Reserved for future use	0

0x07 – Cropping Register, High (CROP_HI)

Bit	Function	R/W	Description	Reset
7-6	VDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg09 for its shadow register.	0
3-2	HDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit HACTIVE register.	2

0x08 – Vertical Delay Register, Low (VDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	VDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12

0x09 – Vertical Active Register, Low (VACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	VACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when Atreg of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	F0

0x0A – Horizontal Delay Register, Low (HDELAY_LO)

Bit	Function	R/W	Description	Reset
7-0	HDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video. The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.	10h

0x0B – Horizontal Active Register, Low (HACTIVE_LO)

Bit	Function	R/W	Description	Reset
7-0	HACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.	D0

0x0C – Control Register I (CNTRL1)

Bit	Function	R/W	Description	Reset
7	PBW	R/W	1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW	1
6	DEM	R/W	Secam false color reduction mode 1 = reduction 0 = normal	1
5	PALSW	R/W	1 = PAL switch sensitivity low. 0 = PAL switch sensitivity normal.	0
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level.	0
3	COMB	R/W	1 = Adaptive comb filter on for NTSC 0 = Notch filter	1
2	HCOMP	R/W	1 = operation mode 1. (Recommended) 0 = mode 0.	1
1	YCOMB	R/W	Comb filter operation in monochrome mode 1 = Off 0 = On	0
0	PDLY	R/W	PAL delay line control 1 = disable. 0 = enable.	0

0x10 – BRIGHTNESS Control Register (BRIGHT)

Bit	Function	R/W	Description	Reset
7-0	BRIGHT	R/W	These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00

0x11 – CONTRAST Control Register (CONTRAST)

Bit	Function	R/W	Description	Reset
7-0	CNTRST	R/W	These bits control the luminance contrast gain. A value of 100 (64h) has a gain of 1. The range of adjustment is from 0% to 255% in 1% per step.	64

0x12 – SHARPNESS Control Register I (SHARPNESS)

Bit	Function	R/W	Description	Reset
7	SCURVE	R/W	This bit controls the sharpness filter center frequency. 0 = Normal 1 = High	0
6	VSF	R/W	This bit is for internal used.	1
5-4	CTI	R/W	CTI level selection. 0 = lowest. 3 = hightest.	1
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image. 1 through 15 provides sharpness enhancement with 'F' being the strongest.	1

0x13 – Chroma (U) Gain Register (SAT_U)

Bit	Function	R/W	Description	Reset
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

0x14 – Chroma (V) Gain Register (SAT_V)

Bit	Function	R/W	Description	Reset
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

0x15 – Hue Control Register (HUE)

Bit	Function	R/W	Description	Reset
7-0	HUE	R/W	These bits control the color hue as 2's complement number. They have value from $+36^{o}$ (7Fh) to -36^{o} (80h) with an increment of 0.28^{o}. The positive value gives greenish tone and negative value gives purplish tone. The default value is 0^{o} (00h). This is effective only on NTSC system.	00

0x16 – SV_DET

Bit	Function	R/W	Description	Reset
7	Reserved	R		
6	SV_DET	R	1 = Detection of color sub-carrier on C-channel	
5-4	Reserved	R		
3-0	Reserved	R/W		0

0x17 – Coring

Bit	Function	R/W	Description	Reset
7-4	SHCOR	R/W	These bits provide coring function for the sharpness control.	3
3	RTSEL3	R/W	The real time signal output	0
2-0	VSHP	R/W	Vertical peaking level. 0 = none. 7 = highest.	0

0x18 – Coring and IF compensation (CORING)

Bit	Function	R/W	Description	Reset
7-6	CTCOR	R/W	These bits control the coring for CTI.	1
5-4	CCOR	R/W	These bits control the low level coring function for the Cb/Cr output.	0
3-2	VCOR	R/W	These bits control the coring function of vertical peaking.	1
1-0	CIF	R/W	These bits control the IF compensation level. 0 = None 1 = 1.5dB 2 = 3dB 3 = 6dB	0

0x19 – VBI Control Register (VBICNTL)

Bit	Function	R/W	Description	Reset
7	VBI_EN	R/W	0 = VBI capture disabled. 1 = VBI capture enabled.	0
6	VBI Byte Order	R/W	0 = Pixel 2,1,4,3,6,5,…. on the VD[7:0] data bus. 1 = Pixel 1,2,3,4,5,6,…. on the VD[7:0] data bus.	1
5	VBI_ FRAM	R/W	0 = Normal mode 1 = ADC output mode If ADCMD=0,VD[7:0] pin is 10bit Y-ADC data bit9-2 If ADCMD=1,VD[7:0] pin is 10bit C-YADC data bit9-2	0
4	HA_EN	R/W	0 = HACTIVE output is disabled during vertical blanking period. 1 = HACTIVE output is enabled during vertical blanking period.	1
3		R/W	Reserved	1
2-0	RTSEL	R/W	Register 0x17[3] RTSEL3 together with bits RTSEL control the real time signal output from the MPOUT pin. 0000 = Video loss 0001 = H-lock 0010 = S-lock 0011 = V-lock 0100 = MONO 0101 = DET50 0110 = FIELD 0111 = RTCO (Real Time Control) 1110 = Factory test only 1111 = 0	0

0x1A – Analog Control II

Bit	Function	R/W	Description	Reset
7	LLCTEST	R/W	LLC test mode	0
6	PLL_PDN	R/W	0 = LLC PLL in normal operation. 1 = PLL in power down mode.	0
5-4			Reserved	0
3	YFLEN	R/W	Y-Ch anti-alias filter control 1 = enable 0 = disable	0
2	YSV	R/W	Y-Ch power saving mode 1 = enable 0 = disable	0
1	CFLEN	R/W	C-Ch anti-alias filter control 1 = enable 0 = disable	0
0	CSV	R/W	C-Ch power saving mode 1 = enable 0 = disable	0

0x1B – Output Control II

Bit	Function	R/W	Description	Reset
7-6	CK2S	R/W	CLKX2 pin output control. CK1S[0] together with these two bits (CK1S[0], CK2S) control CLKX2 pin output selection. 000 = VCLK 001 = CLKX1 010 = CLKX2 011 = LLCK 100 = LLCK2 101 = LLCK4 110 = Factory test only 111 = 0	0
5-4	CK1S	R/W	See CK2S	0
3-0	Reserved	R/W		0

0x1C – Standard Selection (SDT)

Bit	Function	R/W	Description	Reset
7	DETSTUS	R	0 = Idle 1 = detection in progress	0
6-4	STDNOW	R	Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid	0
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	STD	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7

0x1D – Standard Recognition (SDTR)

Bit	Function	R/W	Description	Reset
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = enable recognition of PAL60. 0 = disable recognition.	1
5	PALN_EN	R/W	1 = enable recognition of PAL (CN). 0 = disable recognition.	1
4	PALM_EN	R/W	1 = enable recognition of PAL (M). 0 = disable recognition.	1
3	NT44_EN	R/W	1 = enable recognition of NTSC 4.43. 0 = disable recognition.	1
2	SEC_EN	R/W	1 = enable recognition of SECAM. 0 = disable recognition.	1
1	PALB_EN	R/W	1 = enable recognition of PAL (B,D,G,H,I). 0 = disable recognition.	1
0	NTSC_EN	R/W	1 = enable recognition of NTSC (M). 0 = disable recognition.	1

0x1E – Reserved

Bit	Function	R/W	Description	Reset
7	NT50	R/W	1 = Force decoding format to 50Hz NTSC. 0 = decoding format is set by register 0x1C (SDT)	0
6-4		R	Reserved	0
3-0	Reserved	R/W		8

0x1F – Test Control Register (TEST)

Bit	Function	R/W	Description	Reset
7-0	TEST	R/W	This register is reserved for testing purpose. In normal operation, only 0 should be written into this register. 1 = Analog test mode1. The Y channel 10bit ADC output can be obtained from {VD[7:0],HSYNC,VSYBC}. 2 = Analog test mode2. The C channel 10bit ADC output can be obtained from {VD[7:0],HSYNC,VSYNC}. 4 = Digital test mode1. This is the CVBS test mode. The 8-bit input corresponds to VD[7:0] in the order of bit 7 to 0. B = Clamp test mode. Clamp control input YU, YUX, YD, YDX, CU, CUX, CD, and CDX are mapped to VD[3:0]. YU = VD[3],YUX = VD[2],YD = VD[1],YDX = VD[0] CU = VD[3],CUX = VD[2],CD = VD[1],CDX = VD[0] C = Memory Bist test mode. Internal Memories are tested with XTI clock input and following pin outputs. VD[7] = comb4_fail_h. VD[6] = comb4_tst_done VD[5] = bcs_fail_h VD[4] = bcs_tst_done Other values are reserved.	0

0x20 – Clamping Gain (CLMPG)

Bit	Function	R/W	Description	Reset
7-4	CLPEND	R/W	These 4 bits set the end time of the clamping pulse in the increment of 8 system clocks. The clamping period is determined by this and CLPST.	5
3-0	CLPST	R/W	These 4 bits set the start time of the clamping pulse in the increment of 8 system clocks. It is referenced to PCLAMP position.	0

0x21 – Individual AGC Gain (IAGC)

Bit	Function	R/W	Description	Reset
7-4	NMGAIN	R/W	These bits control the normal AGC loop maximum correction value.	4
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1
0	AGCGAIN8	R/W	This bit is the MSB of the 10-bit register that controls the AGC gain when AGC loop is disabled.	0

0x22 – AGC Gain (AGCGAIN)

Bit	Function	R/W	Description	Reset
7-0	AGCGAIN	R/W	These bits are the lower 8 bits of the 10-bit register that controls the AGC gain when AGC loop is disabled.	F0

0x23 – White Peak Threshold (PEAKWT)

Bit	Function	R/W	Description	Reset
7-0	PEAKWT	R/W	These bits control the white peak detection threshold. Setting 'FF' disables this function.	D8

0x24– Clamp level (CLMPL)

Bit	Function	R/W	Description	Reset
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL. 1 = Clamping level preset at 60d for 60Hz field rate or 63d for 50Hz.	1
6-0	CLMPL	R/W	These bits determine the clamping level of the Y channel.	3C

0x25– Sync Amplitude (SYNCT)

Bit	Function	R/W	Description	Reset
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h.	1
6-0	SYNCT	R/W	These bits determine the standard sync pulse amplitude for AGC reference.	38

0x26 – Sync Miss Count Register (MISSCNT)

Bit	Function	R/W	Description	Reset
7-4	MISSCNT	R/W	MISSCNT[3] controls the speed of VDLOSS detection with '0' being fast and '1' being slow. MISSCNT[2:0] control the threshold of horizontal sync miss detection per field before VDLOSS is flagged.	4
3-0	HSWIN	R/W	These bits determine the VCR mode Hsync detection window.	4

0x27 – Clamp Position Register (PCLAMP)

Bit	Function	R/W	Description	Reset
7-0	PCLAMP	R/W	These bits set the clamping position from the PLL sync edge	2A

0x28 – Vertical Control I (VCNTL1)

Bit	Function	R/W	Description	Reset
7-6	VLCKI	R/W	Vertical lock in time. 0 = fastest 3 = slowest.	0
5-4	VLCKO	R/W	Vertical lock out time. 0 = fastest 3 = slowest.	0
3	VMODE	R/W	This bit controls the vertical detection window. 1 = search mode. 0 = vertical count down mode.	0
2	DETV	R/W	1 = recommended for special application only. 0 = Normal Vertical sync logic	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 1 = long 0 = normal	0

0x29 – Vertical Control II (VCNTL2)

Bit	Function	R/W	Description	Reset
7-5	BSHT	R/W	Burst PLL center frequency control. Factory use only.	0
5-0	VSHT	R/W	Vertical sync output delay control in the increment of half line length.	00

0x2A – Color Killer Level Control (CKILL)

Bit	Function	R/W	Description	Reset
7-6	CKILMAX	R/W	These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	1
5-0	CKILMIN	R/W	These bits control the color killer threshold. Larger value gives lower killer level.	28

0x2B – Comb Filter Control (COMB)

Bit	Function	R/W	Description	Reset
7	HTL	R/W	0 = Adaptive comb mode 1 = fixed comb mode	0
6-4	HTL	R/W	Adaptive Comb filter threshold control 1.	4
3-0	VTL	R/W	Adaptive Comb filter threshold control 2.	4

0x2C – Luma Delay and H Filter Control (LDLY)

Bit	Function	R/W	Description	Reset
7	CKLM	R/W	Color Killer mode. 0 = normal 1 = fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provide –4 to +3 unit delay control.	3
3-0	HFLT	R/W	Alternative peaking control. Larger value gives larger enhancement.	0

0x2D – Miscellaneous Control I (MISC1)

Bit	Function	R/W	Description	Reset
7	HPLC	R/W	Reserved for Internal use.	0
6	EVCNT	R/W	1 = Even field counter in special mode. 0 = Normal operation	0
5	PALC	R/W	Reserved.	0
4	SDET	R/W	ID detection sensitivity. A '1' is recommended.	1
3	OPLMT	R/W		0
2	BYPASS	R/W	It controls the standard detection and should be set to '1' in normal use.	1
1	SYOUT	R/W	1 = Hsync output is disabled when video loss is detected 0 = Hsync output is always enabled	0
0	HADV	R/W	This bit advances the HACTIVE pin output by one data clock when set.	0

0x2E – LOOP Control Register (LOOP)

Bit	Function	R/W	Description	Reset
7-6	HPM	R/W	Horizontal PLL acquisition time. 3 = Fast 2 = Auto1 1 = Auto2 0 = Normal	2
5-4	ACCT	R/W	ACC time constant 0 = No ACC 1 = slow 2 = medium 3 = fast	2
3-2	SPM	R/W	Burst PLL speed control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1
1-0	CBW	R/W	Chroma low pass filter bandwidth control. Refer to filter curves.	1

0x2F – Miscellaneous Control II (MISC2)

Bit	Function	R/W	Description	Reset
7	NKILL	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL	R/W	0 = Normal output 1 = special output mode.	0
3	FCS	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0x30 – Macrovision Detection (MVSN)

Bit	Function	R/W	Description	Reset
7	SF	R		0
6	PF	R		0
5	FF	R		0
4	KF	R		0
3	CSBAD	R	Set when Macrovision color stripe detection may be un-reliable	0
2	MCVSN	R	1 = Macrovision AGC pulse detected. 0 = Not detected.	0
1	CSTRIPE	R	1 = Macrovision color stripe protection burst detected. 0 = Not detected.	0
0	CTYPE	R	This bit is valid only when color stripe protection is detected, i.e. Cstripe=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	0

0x31 – Chip STATUS II (STATUS2)

Bit	Function	R/W	Description	Reset
7	VCR	R	VCR signal indicator	0
6	WKAIR	R	Weak signal indicator 2.	0
5	WKAIR1	R	Weak signal indicator controlled by WKTH.	0
4	VSTD	R	1 = 525/625 line signal 0 = Non-standard signal	0
3	NINTL	R	1 = Non-interlaced signal 0 = interlaced signal	0
2	WSSDET	R	1 = WSS data detected. 0 = Not detected.	0
1	EDSDET	R	1 = EDS data detected. 0 = Not detected.	0
0	CCDET	R	1 = CC data detected. 0 = Not detected.	0

0x32 – H monitor (HFREF)

Bit	Function	R/W	Description	Reset
7-0	HFREF	R	Horizontal line frequency indicator	X

0x33 – CLAMP MODE (CLMD)

Bit	Function	R/W	Description	Reset
7-6	FRM	R/W	Free run mode control 0 = Auto 2 = default to 60Hz 3 = default to 50Hz	0
5-4	YNR	R/W	Y HF noise reduction 0 = None 1 = smallest 2 = small 3 = medium	0
3-2	CLMD	R/W	Clamping mode control. 0 = Sync top 1 = Auto 2 = Pedestal 3 = N/A	1
1-0	PSP	R/W	Slice level control 0 = low 1 = medium 2 = high	1

0x34 – ID Detection Control (IDCNTL)

Bit	Function	R/W	Description	Reset
7-6	IDX	R/W	These two bits indicate which of the four lower 6-bit registers is currently be controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.	0
5-0	NSEN / SSEN / PSEN / WKTH	R/W	IDX = 0 controls the NTSC ID detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1A / 20 / 1C / 11

0x35 – Clamp Control I (CLCNTL1)

Bit	Function	R/W	Description	Reset
7	CTEST	R/W	Clamping control.	1
6	YCLEN	R/W	1 = Y channel clamp disabled 0 = Enabled.	0
5	CCLEN	R/W	1 = C channel clamp disabled 0 = Enabled.	0
4	VCLEN	R/W	Reserved	0
3	GTEST	R/W	1 = Test. 0 = Normal operation.	0
2	VLPF	R/W	Sync filter control	0
1	CKLY	R/W	Clamping current control 1.	0
0	CKLC	R/W	Clamping current control 2.	0

0x4C – ANAPLLCTL

Bit	Function	R/W	Description	Reset
7-5		R	Reserved	0
4	PLL_IREF	R/W	Current bias 0:default,1:33% more current	0
3-2	CP_SEL	R/W	Charge-pump current 00:1uA, 01:5uA, 10:10uA, 11:15uA	1
1	BYPASS_SEL	R/W	Test mode 0:PLL clock output, 1:PLL reference clock	0
0	LPRES_SEL	R/W	Loop-filter resistance 0:60K, 1:35K	1

0x4D – VBIMIN

Bit	Function	R/W	Description	Reset
7	ADCMD	R/W	Test purpose only for ADC data output. When VBI_FRAM=1,this function is effective. 0:VD[7:0] pin output 10bit Y-ADC data bit9-2. 1:VD[7:0] pin output 10bit C-ADC data bit9-2.	0
6-0	VBIMIN	R/W	VBI Minimum Level.	40

0x4E – HSLOWCTL

Bit	Function	R/W	Description	Reset
7	Reserved	R		0
6-4	HSBEGIN[2:0]	R/W	HSYNC Start position Control Bit2-0.	00
3	Reserved	R		0
2-0	HSEND[2:0]	R/W	HSYNC End position Control Bit2-0.	00

0x4F – WSS3

Bit	Function	R/W	Description	Reset
7-0	WSS[19:14]	R	CGMS(WSS525) Bit19-14 in 525 line video system. These bits show CRC 6bits in CGMS(WSS525). These bits are only valid in 525 line video system.	0

0x50 – FILLDATA

Bit	Function	R/W	Description	Reset
7-0	FILLDATA	R/W	Filled data as dummy data in ANC Dword data packet.	A0

0x51 – SDID

Bit	Function	R/W	Description	Reset
7	NODAEN	R/W	1:Bit7 in 4th byte of EAV/SAV code will be 0 when sync lost(No Video input.) 0: Bit7 in 4th byte of EAV/SAV is always VIPCFG register bit.	0
6	SYRM	R/W	1: Minimum value in raw VBI will be 0x10 for Sync Level remove. 0:none.	0
5-0	SDID	R/W	Secondary data ID in ANC data packet type 2	22

0x52 – DID

Bit	Function	R/W	Description	Reset
7	ANCEN	R/W	ANC data packet output control. 1 = enable. 0:disable.	0
6		R	Reserved	0
5	VIPCFG	R/W	Set up Bit7 in 4th byte of EAV/SAV code.	1
4-0	DID	R/W	Data ID in ANC data packet type 2.	11

0x53 – WSS1

Bit	Function	R/W	Description	Reset
7	CRCERR	R	This bit is only valid in 525 line video system. 1: CGMS(WSS525) CRC error detected in current field. 0:No CRC error	1
6	WSSFLD	R	0:current WSS data is received in Odd field. 1: current WSS data is received in Even field.	0
5-0	WSS[13:8]	R	CGMS(WSS525) Bit13-8 in 525 line video system. Wide Screen Signaling Bit13-8 in 625 line video system.	0

0x54 – WSS2

Bit	Function	R/W	Description	Reset
7-0	WSS[7:0]	R	CGMS(WSS525) Bit7-0 in 525 line video system. Wide Screen Signaling Bit7-0 in 625 line video system.	0

0x55 – VVBI

Bit	Function	R/W	Description	Reset
7-6		R	Reserved	0
5	HAMM84	R/W	1:enable 84 Hamming Code checking BI Slicer.0: disable.	0
4	NTSC656	R/W	1:Number of Even Field Video output line is (the number of Odd field Video output line – 1). This bit is required for ITU-R BT.656 output for 525-line system standard. 0: Number of Even Field Video output line is same as the number of Odd field Video output line.	0
3-0	VVBI	R/W	The number of raw VBI data output line counted from top video active line signal timing.	0

0x56~6A LCTL6~LCTL26

Bit	Function	R/W	Description	Reset
7-4	LCTLn	R/W	Set up VBI Data Slicer Decoding mode on Line-n. Value is set up by upper bit7-4 meaning for Line-n in odd field.	0
3-0		R/W	Value is set up by below bit3-0 meaning for Line-n in even field. 0h:disable decoding. 1h:Teletext-B 2h:Teletext-C 3h:Teletext-D 4h:Closed Captioning and Extended Data service. (EIA-608 type). 5h:CGMS (WSS525) in 525 line system or WSS625 in 625 line system. 6h:VITC 7h:Gemstar 1x 8h:Gemstar 2x 9h:VPS (Line16 VPS type) Ah: Teletext-A Bh~Fh: reserved	0

0x6B – HSGEGIN

Bit	Function	R/W	Description	Reset
7-0	HSBEGIN[10:3]	R/W	HSYNC Start position Bit10-3.	06

0x6C – HSEND

Bit	Function	R/W	Description	Reset
7-0	HSEND[10:3]	R/W	HSYNC End position Bit10-3.	24

0x6D – OVSDLY

Bit	Function	R/W	Description	Reset
7-0	OVSDLY	R/W	VSYNC Start position.	00

0x6E – OVSEND

Bit	Function	R/W	Description	Reset
7	HSPIN	R/W	1:HSYNC output is HACTIVE. 0:HSYNC output is HSYNC.	0
6-4	OFDLY	R/W	FIELD output delay.This bit is only effective for FIELD signal on MPOUT pin output. 0h:0H line delay FIELD output. 1h-7h: 1-H to 7-H line delay FIELD output.	2
3	VSMODE	R/W	1:VSYNC output is HACTIVE-VSYNC mode. 0:VSYNC output is HSYNC-VSYNC mode.	0
2-0	OVSEND	R/W	Line delay for VSYNC end position.	0

0x6F – VBIDELAY

Bit	Function	R/W	Description	Reset
7	PDNSVBI	R/W	1:VBI data slicer enable 0: VBI data slicer is in reset and power-down mode	0
6	ANCDMODE	R/W	0:0xFF/0x00 data value in ANC data packet will be converted to 0xFC/0x03 value. 1:no change	0
5-0	VBIDELAY	R/W	Raw VBI output delay Typical setting value: NTSC-M 13h, PAL 8h	13

0xAE – LINENUMBERINT

Bit	Function	R/W	Description	Reset
7	F1LIEN	R/W	0: disable LINE_INT during field 1. 1: enable LINE_INT during field 1.	0
6	F2LIEN	R/W	0: disable LINE_INT during field 2. 1: enable LINE_INT during field 2.	0
5-0	LINENUMBER	R/W	LINE_INT register bit is “1” while video line number is more than this value.LINE_INT_CH register bit is also set to “1” at the start of this video number.	1A

0xAE – INTOEN

Bit	Function	R/W	Description	Reset
7	INTOEN	R/W	0: enable INTREQ pin output. 1: INTREQ pin output is tri-state.	1
6	INTPOL	R/W	0: INTREQ pin is negative active. 1: INTREQ pin is positive active.	0
5-0		R	Reserved	0

0xB0 – INT1ENABLE

Bit	Function	R/W	Description	Reset
7	GEM1XCH_ENABLE	R/W	0:disable GEMSTAR1X status changed interrupt on INTREQ pin. 1:enable GEMSTAR1X status changed interrupt on INTREQ pin.	0
6	GEM2XCH_ENABLE	R/W	0:disable GEMSTAR2X status changed interrupt on INTREQ pin. 1:enable GEMSTAR2X status changed interrupt on INTREQ pin.	0
5	VITCCH_ENABLE	R/W	0:disable VITC status changed interrupt on INTREQ pin. 1:enable VITC status changed interrupt on INTREQ pin.	0
4	VPSCH_ENABLE	R/W	0:disable VPS status changed interrupt on INTREQ pin. 1:enable VPS status changed interrupt on INTREQ pin.	0
3	WSTCH_ENABLE	R/W	0:disable WST(Teletext) status changed interrupt on INTREQ pin. 1:enable WST(Teletext) status changed interrupt on INTREQ pin.	0
2	WSSCH_ENABLE	R/W	0:disable WSS status changed interrupt on INTREQ pin. 1:enable WSS status changed interrupt on INTREQ pin.	0
1	CCF2CH_ENABLE	R/W	0:disable CCF2 status changed interrupt on INTREQ pin. 1:enable CCF2 status changed interrupt on INTREQ pin.	0
0	CCF1CH_ENABLE	R/W	0:disable CCF1 status changed interrupt on INTREQ pin. 1:enable CCF1 status changed interrupt on INTREQ pin.	0

0xB1 – INT2ENABLE

Bit	Function	R/W	Description	Reset
7	LINE_INT_CH_ ENABLE	R/W	0:disable LINE_INT_CH interrupt on INTREQ pin. 1:enable LINE_INT_CH interrupt on INTREQ pin.	0
6	MACROCH_EN ABLE	R/W	0:disable Macrovision status changed interrupt on INTREQ pin. 1:enable Macrovision status changed interrupt on INTREQ pin.	0
5	VDLOSSCH_E NABLE	R/W	0:disable VDLOSS status changed interrupt on INTREQ pin. 1:enable VDLOSS status changed interrupt on INTREQ pin.	0
4	DET50CH_ENA BLE	R/W	0:disable DET50 status changed interrupt on INTREQ pin. 1:enable DET50 status changed interrupt on INTREQ pin.	0
3		R	Reserved	0
2	SLOCKCH_EN ABLE	R/W	0:disable SLOCK status changed interrupt on INTREQ pin. 1:enable SLOCK status changed interrupt on INTREQ pin.	0
1	HVLOCKCH_E NABLE	R/W	0:disable HVLOCK status changed interrupt on INTREQ pin. 1:enable HVLOCK status changed interrupt on INTREQ pin.	0
0	VCRCH_ENAB LE	R/W	0:disable VCR status changed interrupt on INTREQ pin. 1:enable VCR status changed interrupt on INTREQ pin.	0

0xB3 – INT1RST

Bit	Function	R/W	Description	Reset
7	GEM1XCH_RST	R/W	0:no action. 1:Reset GEM1XCH_STATUS bit to 0.	0
6	GEM2XCH_RST	R/W	0:no action. 1: Reset GEM2XCH_STATUS bit to 0.	0
5	VITCCH_RST	R/W	0:no action. 1: Reset VITCCH_STATUS bit to 0.	0
4	VPSCH_RST	R/W	0:no action. 1: Reset VPSCH_STATUS bit to 0.	0
3	WSTCH_RST	R/W	0:no action. 1: Reset WSTCH_STATUS bit to 0.	0
2	WSSCH_RST	R/W	0:no action. 1: Reset WSSCH_STATUS bit to 0.	0
1	CCF2CH_RST	R/W	0:no action. 1: Reset CCF2CH_STATUS bit to 0.	0
0	CCF1CH_RST	R/W	0:no action. 1: Reset CCF1CH_STATUS bit to 0.	0

0xB4 – INT2RST

Bit	Function	R/W	Description	Reset
7	LINE_INT_CH_RST	R/W	0:no action. 1:Reset LINE_INT_CH_STATUS bit to 0.	0
6	MACROCH_RST	R/W	0:no action, 1: Reset MACROCH_STATUS bit to 0.	0
5	VDLOSSCH_RST	R/W	0:.no action. 1: Reset VDLOSSCH_STATUS bit to 0.	0
4	DET50CH_RST	R/W	0:no action. 1: Reset DET50CH_STATUS bit to 0.	0
3		R	Reserved	0
2	SLOCKCH_RST	R/W	0:no action. 1: Reset SLOCKCH_STATUS bit to 0.	0
1	HVLOCKCH_RST	R/W	0:no action. 1: Reset HVLOCKCH_STATUS bit to 0.	0
0	VCRCH_RST	R/W	0:no action. 1: Reset VCRCH_STATUS bit to 0.	0

0xB6 – INT1RAWSTATUS

Bit	Function	R/W	Description	Reset
7	GEM1X_DET	R	0:not available. 1:GEMSTAR1X type data is detected.	0
6	GEM2X_DET	R	0:not available. 1:GEMSTAR2X type data is detected..	0
5	VITC_DET	R	0:not available. 1:VITC data is detected.	0
4	VPS_DET	R	0:not available. 1:VPS data is detected.	0
3	WST_DET	R	0:not available. 1:WST(Teletext) data is deteted.	0
2	WSS_DET	R	0:not available. 1:WSS data is detected.	0
1	CCF2_DET	R	0:not available. 1:CCF2(Field2 Closed Captioning) data is detected.	0
0	CCF1_DET	R	0:not available. 1:CCF1(Field1 Closed Captioning) data is detected.	0

0xB7 – INT2RAWSTATUS

Bit	Function	R/W	Description	Reset
7	LINE_INT	R	0:Current Video line number is smaller than the number of LINENUMBER register. 1:Current Video line number is larger than the number of LINENUMBER register.	0
6	MACRO	R	0: Macrovision status is not changing in current field. 1: Macrovision status is changing in current field.	0
5	VDLOSS	R	This bit is same as VDLOSS in reg0x00[7].This bit exists here for INT2STATUS and INTREQ pin interrupt. 1 = Video not present. (Sync is not detected in number of line periods specified by MISSCNT register) 0 = Video detected.	0
4	DET50	R	This bit is same as DET50 in reg0x00[0].This bit exists here for INT2STATUS and INTREQ pin interrupt. 0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0
3		R	Reserved	0
2	SLOCK	R	This bit is same as SLOCK in reg0x00[5].This bit exists here for INT2STATUS and INTREQ pin interrupt. 1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
1	HVLOCK	R	0:{HLOCK,VLOCK}=2'b00. 1:{HLOCK,VLOCK} is not 2'b00.	0
0	VCR	R	This bit is same as VCR in reg0x31[7].This bit exists here for INT2STATUS and INTREQ pin interrupt. VCR signal indicator.	0

0xB9 – INT1STATUS

Bit	Function	R/W	Description	Reset
7	GEM1X_STATUS	R	0:This status was being reset and has not been changed since then. 1:GEMSTAR1X detection status changed.	0
6	GEM2X_STATUS	R	0:This status was being reset and has not been changed since then. 1:GEMSTAR2X detection status changed.	0
5	VITC_STATUS	R	0:This status was being reset and has not been changed since then. 1:VITC detection status changed.	0
4	VPS_STATUS	R	0:This status was being reset and has not been changed since then. 1:VPS detection status changed.	0
3	WST_STATUS	R	0:This status was being reset and has not been changed since then. 1:WST(Teletext) detection status changed.	0
2	WSS_STATUS	R	0:This status was being reset and has not been changed since then. 1:WSS is detected and WSS registers are updated.	0
1	CCF2_STATUS	R	0:This status was being reset and has not been changed since then. 1:CCF2 is detected and CCF2DATA1/CCF2DATA2 registers are updated.	0
0	CCF1_STATUS	R	0:This status was being reset and has not been changed since then. 1:CCF1 is detected and CCF1DATA1/CCF1DATA2 registers are updated	0

0xBA – INT2STATUS

Bit	Function	R/W	Description	Reset
7	LINE_INT_CH	R	0:This status was being reset and has not been changed since then. 1:LINE_INT detection status changed.	0
6	MACROCH	R	0:This status was being reset and has not been changed since then. 1:Macrovision detection status changed.	0
5	VDLOSSCH	R	0:This status was being reset and has not been changed since then. 1:VDLOSS detection status changed.	0
4	DET50CH	R	0:This status was being reset and has not been changed since then. 1:DET50 detection status changed.	0
3		R	Reserved	0
2	SLOCKCH	R	0:This status was being reset and has not been changed since then. 1:SLOCK detection status changed.	0
1	HVLOCKCH	R	0:This status was being reset and has not been changed since then. 1:HVLOCK detection status changed.	0
0	VCRCH	R	0:This status was being reset and has not been changed since then. 1:VCR detection status changed.	0

0xBD – CCF1DATA1

Bit	Function	R/W	Description	Reset
7	CCF1DATA1	R	Field1 CC data 1st byte.	80

0xBE – CCF1DATA2

Bit	Function	R/W	Description	Reset
7	CCF1DATA2	R	Field1 CC data 2nd byte.	80

0xBF – CCF2DATA1

Bit	Function	R/W	Description	Reset
7	CCF2DATA1	R	Field2 CC data 1st byte.	80

0xC0 – CCF2DATA2

Bit	Function	R/W	Description	Reset
7	CCF2DATA2	R	Field2 CC data 2nd byte.	80

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09/18/2009	Add QFN mechanical data, exposed pad soldering consideration.
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