32 Configuration Registers

The configuration of ***CC2500*** is done by programming 8-bit registers. The optimum configuration data based on selected system parameters are most easily found by using the SmartRF® Studio software [5]. Complete descriptions of the registers are given in the following tables. After chip reset, all the registers have default values as shown in the tables. The optimum register setting might differ from the default value. After a reset all registers that shall be different from the default value therefore needs to be programmed through the SPI interface.

There are 13 command strobe registers, listed in Table 34. Accessing these registers will initiate the change of an internal state or mode. There are 47 normal 8-bit configuration registers, listed in Table 35. Many of these registers are for test purposes only, and need not be written for normal operation of ***CC2500***.

There are also 12 status registers, which are listed in Table 36. These registers, which are read-only, contain information about the status of ***CC2500***.

The two FIFOs are accessed through one 8-bit register. Write operations write to the TX FIFO, while read operations read from the RX FIFO.

During the header byte transfer and while writing data to a register or the TX FIFO, a status byte is returned on the S0 line. This status byte is described in Table 17 on page 23.

Table 37 summarizes the SPI address space. The address to use is given by adding the base address to the left and the burst and R/W bits on the top. Note that the burst bit has different meaning for base addresses above and below 0x2F.

Address	Strobe Name	Description
0x30	SRES	Reset chip.
0x31	SFSTXON	Enable and calibrate frequency synthesizer (if MCSM0.FS_AUTOCAL=1). If in RX (with CCA): Go to a wait state where only the synthesizer is running (for quick RX / TX turnaround).
0x32	SXOFF	Turn off crystal oscillator.
0x33	SCAL	Calibrate frequency synthesizer and turn it off. SCAL can be strobed from IDLE mode without setting manual calibration mode (MCSM0.FS_AUTOCAL=0)
0x34	SRX	Enable RX. Perform calibration first if coming from IDLE and MCSM0.FS_AUTOCAL=1.
0x35	STX	In IDLE state: Enable TX. Perform calibration first if MCSM0.FS_AUTOCAL=1. If in RX state and CCA is enabled: Only go to TX if channel is clear.
0x36	SIDLE	Exit RX / TX, turn off frequency synthesizer and exit Wake-On-Radio mode if applicable.
0x38	SWOR	Start automatic RX polling sequence (Wake-on-Radio) as described in Section 19.5 if WORCTRL.RC_PD=0.
0x39	SPWD	Enter power down mode when CSn goes high.
0x3A	SFRX	Flush the RX FIFO buffer. Only issue SFRX in IDLE or RXFIFO_OVERFLOW states.
0x3B	SFTX	Flush the TX FIFO buffer. Only issue SFTX in IDLE or TXFIFO_UNDERFLOW states.
0x3C	SWORRST	Reset real time clock to Event1 value.
0x3D	SNOP	No operation. May be used to get access to the chip status byte.

Table 34: Command Strobes

Address	Register	Description	Preserved in SLEEP State	Details on Page Number
0x00	IOCFG2	GDO2 output pin configuration	Yes	61
0x01	IOCFG1	GDO1 output pin configuration	Yes	61
0x02	IOCFG0	GDO0 output pin configuration	Yes	61
0x03	FIFOTHR	RX FIFO and TX FIFO thresholds	Yes	62
0x04	SYNC1	Sync word, high byte	Yes	62
0x05	SYNC0	Sync word, low byte	Yes	62
0x06	PKTLEN	Packet length	Yes	62
0x07	PKTCTRL1	Packet automation control	Yes	63
0x08	PKTCTRL0	Packet automation control	Yes	64
0x09	ADDR	Device address	Yes	64
0x0A	CHANNR	Channel number	Yes	64
0x0B	FSCTRL1	Frequency synthesizer control	Yes	65
0x0C	FSCTRL0	Frequency synthesizer control	Yes	65
0x0D	FREQ2	Frequency control word, high byte	Yes	65
0x0E	FREQ1	Frequency control word, middle byte	Yes	65
0x0F	FREQ0	Frequency control word, low byte	Yes	65
0x10	MDMCFG4	Modem configuration	Yes	66
0x11	MDMCFG3	Modem configuration	Yes	66
0x12	MDMCFG2	Modem configuration	Yes	67
0x13	MDMCFG1	Modem configuration	Yes	68
0x14	MDMCFG0	Modem configuration	Yes	68
0x15	DEVIATN	Modem deviation setting	Yes	69
0x16	MCSM2	Main Radio Control State Machine configuration	Yes	70
0x17	MCSM1	Main Radio Control State Machine configuration	Yes	71
0x18	MCSM0	Main Radio Control State Machine configuration	Yes	72
0x19	FOCCFG	Frequency Offset Compensation configuration	Yes	73
0x1A	BSCFG	Bit Synchronization configuration	Yes	74
0x1B	AGCTRL2	AGC control	Yes	75
0x1C	AGCTRL1	AGC control	Yes	76
0x1D	AGCTRL0	AGC control	Yes	77
0x1E	WOREVT1	High byte Event 0 timeout	Yes	77
0x1F	WOREVT0	Low byte Event 0 timeout	Yes	78
0x20	WORCTRL	Wake On Radio control	Yes	78
0x21	FREND1	Front end RX configuration	Yes	78
0x22	FREND0	Front end TX configuration	Yes	79
0x23	FSCAL3	Frequency synthesizer calibration	Yes	79
0x24	FSCAL2	Frequency synthesizer calibration	Yes	79
0x25	FSCAL1	Frequency synthesizer calibration	Yes	80
0x26	FSCAL0	Frequency synthesizer calibration	Yes	80
0x27	RCCTRL1	RC oscillator configuration	Yes	80
0x28	RCCTRL0	RC oscillator configuration	Yes	80
0x29	FSTEST	Frequency synthesizer calibration control	No	80
0x2A	PTEST	Production test	No	80
0x2B	AGCTEST	AGC test	No	81
0x2C	TEST2	Various test settings	No	81
0x2D	TEST1	Various test settings	No	81
0x2E	TEST0	Various test settings	No	81

Table 35: Configuration Registers Overview

Address	Register	Description	Details on Page Number
0x30 (0xF0)	PARTNUM	***CC2500*** part number	81
0x31 (0xF1)	VERSION	Current version number	81
0x32 (0xF2)	FREQEST	Frequency offset estimate	81
0x33 (0xF3)	LQI	Demodulator estimate for Link Quality	82
0x34 (0xF4)	RSSI	Received signal strength indication	82
0x35 (0xF5)	MARCSTATE	Control state machine state	82
0x36 (0xF6)	WORTIME1	High byte of WOR timer	83
0x37 (0xF7)	WORTIME0	Low byte of WOR timer	83
0x38 (0xF8)	PKTSTATUS	Current GDOx status and packet status	83
0x39 (0xF9)	VCO_VC_DAC	Current setting from PLL calibration module	83
0x3A (0xFA)	TXBYTES	Underflow and number of bytes in the TX FIFO	83
0x3B (0xFB)	RXBYTES	Overflow and number of bytes in the RX FIFO	84
0x3C (0xFC)	RCCTRL1_STATUS	Last RC oscillator calibration result	84
0x3D (0xFD)	RCCTRL0_STATUS	Last RC oscillator calibration result	84

Table 36: Status Registers Overview

	Write		Read		
	Single byte	Burst	Single byte	Burst	
	+0x00	+0x40	+0x80	+0xC0	
0x00	IOCFG2				R/W configuration registers, burst access possible
0x01	IOCFG1				
0x02	IOCFG0				
0x03	FIFOTHR				
0x04	SYNC1				
0x05	SYNC0				
0x06	PKTLEN				
0x07	PKTCTRL1				
0x08	PKTCTRL0				
0x09	ADDR				
0x0A	CHANNR				
0x0B	FSCTRL1				
0x0C	FSCTRL0				
0x0D	FREQ2				
0x0E	FREQ1				
0x0F	FREQ0				
0x10	MDMCFG4				
0x11	MDMCFG3				
0x12	MDMCFG2				
0x13	MDMCFG1				
0x14	MDMCFG0				
0x15	DEVIATN				
0x16	MCSM2				
0x17	MCSM1				
0x18	MCSM0				
0x19	FOCCFG				
0x1A	BSCFG				
0x1B	AGCCTRL2				
0x1C	AGCCTRL1				
0x1D	AGCCTRL0				
0x1E	WOREVT1				
0x1F	WOREVT0				
0x20	WORCTRL				
0x21	FREND1				
0x22	FREND0				
0x23	FSCAL3				
0x24	FSCAL2				
0x25	FSCAL1				
0x26	FSCAL0				
0x27	RCCTRL1				
0x28	RCCTRL0				
0x29	FSTEST				
0x2A	PTEST				
0x2B	AGCTEST				
0x2C	TEST2				
0x2D	TEST1				
0x2E	TEST0				
0x2F					
0x30	SRES		SRES	PARTNUM	Command strobes, status registers (read only) and multi byte registers
0x31	SFSTXON		SFSTXON	VERSION	
0x32	SXOFF		SXOFF	FREQEST	
0x33	SCAL		SCAL	LQI	
0x34	SRX		SRX	RSSI	
0x35	STX		STX	MARCSTATE	
0x36	SIDLE		SIDLE	WORTIME1	
0x37				WORTIME0	
0x38	SWOR		SWOR	PKTSTATUS	
0x39	SPWD		SPWD	VCO_VC_DAC	
0x3A	SFRX		SFRX	TXBYTES	
0x3B	SFTX		SFTX	RXBYTES	
0x3C	SWORRST		SWORRST	RCCTRL1_STATUS	
0x3D	SNOP		SNOP	RCCTRL0_STATUS	
0x3E	PATABLE	PATABLE	PATABLE	PATABLE	
0x3F	TX FIFO	TX FIFO	RX FIFO	RX FIFO	

Table 37: SPI Address Space

32.1 Configuration Register Details – Registers with Preserved Values in SLEEP State

0x00: IOCFG2 – GDO2 Output Pin Configuration

Bit	Field Name	Reset	R/W	Description
7	Reserved		R0	
6	GDO2_INV	0	R/W	Invert output, i.e. select active low (1) / high (0)
5:0	GDO2_CFG[5:0]	41 (0x29)	R/W	Default is CHIP_RDYn (see Table 33 on page 53).

0x01: IOCFG1 – GDO1 Output Pin Configuration

Bit	Field Name	Reset	R/W	Description
7	GDO_DS	0	R/W	Set high (1) or low (0) output drive strength on the GDO pins.
6	GDO1_INV	0	R/W	Invert output, i.e. select active low (1) / high (0)
5:0	GDO1_CFG[5:0]	46 (0x2E)	R/W	Default is 3-state (see Table 33 on page 53)

0x02: IOCFG0 – GDO0 Output Pin Configuration

Bit	Field Name	Reset	R/W	Description
7	TEMP_SENSOR_ENABLE	0	R/W	Enable analog temperature sensor. Write 0 in all other register bits when using temperature sensor.
6	GDO0_INV	0	R/W	Invert output, i.e. select active low (1) / high (0)
5:0	GDO0_CFG[5:0]	63 (0x3F)	R/W	Default is CLK_XOSC/192 (see Table 33 on page 53).

0x03: FIFOTHR – RX FIFO and TX FIFO Thresholds

Bit	Field Name	Reset	R/W	Description
7:4	Reserved	0	R0	Write 0 for compatibility with possible future extensions
3:0	FIFO_THR[3:0]	7 (0111)	R/W	Set the threshold for the TX FIFO and RX FIFO. The threshold is exceeded when the number of bytes in the FIFO is equal to or higher than the threshold value.

Setting	Bytes in TX FIFO	Bytes in RX FIFO
0 (0000)	61	4
1 (0001)	57	8
2 (0010)	53	12
3 (0011)	49	16
4 (0100)	45	20
5 (0101)	41	24
6 (0110)	37	28
7 (0111)	33	32
8 (1000)	29	36
9 (1001)	25	40
10 (1010)	21	44
11 (1011)	17	48
12 (1100)	13	52
13 (1101)	9	56
14 (1110)	5	60
15 (1111)	1	64

0x04: SYNC1 – Sync Word, High Byte

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[15:8]	211 (0xD3)	R/W	8 MSB of 16-bit sync word

0x05: SYNC0 – Sync Word, Low Byte

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[7:0]	145 (0x91)	R/W	8 LSB of 16-bit sync word

0x06: PKTLEN – Packet Length

Bit	Field Name	Reset	R/W	Description
7:0	PACKET_LENGTH	255 (0xFF)	R/W	Indicates the packet length when fixed packet length is enabled. If variable length packets are used, this value indicates the maximum length packets allowed.

0x07: PKTCTRL1 – Packet Automation Control

Bit	Field Name	Reset	R/W	Description
7:5	PQT[2:0]	0 (000)	R/W	Preamble quality estimator threshold. The preamble quality estimator increases an internal counter by one each time a bit is received that is different from the previous bit, and decreases the counter by 8 each time a bit is received that is the same as the last bit. A threshold of 4·PQT for this counter is used to gate sync word detection. When PQT=0 a sync word is always accepted.
4	Reserved	0	R0	
3	CRC_AUTOFLUSH	0	R/W	Enable automatic flush of RX FIFO when CRC is not OK. This requires that only one packet is in the RX FIFO and that packet length is limited to the RX FIFO size. PKTCTRL0.CC2400_EN must be 0 (default) for the CRC autoflush function to work correctly.
2	APPEND_STATUS	1	R/W	When enabled, two status bytes will be appended to the payload of the packet. The status bytes contain RSSI and LQI values, as well as the CRC OK flag.
1:0	ADR_CHK[1:0]	0 (00)	R/W	Controls address check configuration of received packages. Setting: Address check configuration 0 (00): No address check 1 (01): Address check, no broadcast 2 (10): Address check and 0 (0x00) broadcast 3 (11): Address check and 0 (0x00) and 255 (0xFF) broadcast

0x08: PKTCTRL0 – Packet Automation Control

Bit	Field Name	Reset	R/W	Description
7	Reserved		R0	
6	WHITE_DATA	1	R/W	Turn data whitening on / off 0: Whitening off 1: Whitening on Data whitening can only be used when PKTCTRL0.CC2400_EN=0 (default).
5:4	PKT_FORMAT[1:0]	0 (00)	R/W	Format of RX and TX data Setting: 0 (00) – Normal mode, use FIFOs for RX and TX 1 (01) – Synchronous serial mode, used for backwards compatibility. Data in on GDO0 2 (10) – Random TX mode; sends random data using PN9 generator. Used for test. Works as normal mode, setting 0 (00), in RX. 3 (11) – Asynchronous serial mode. Data in on GDO0 and data out on either of the GDO0 pins
3	CC2400_EN	0	R/W	Enable CC2400 support. Use same CRC implementation as CC2400. PKTCTRL1.CRC_AUTOFLUSH must be 0 if PKTCTRL0.CC2400_EN=1. PKTCTRL0.WHITE_DATA must be 0 if PKTCTRL0.CC2400_EN=1.
2	CRC_EN	1	R/W	1: CRC calculation in TX and CRC check in RX enabled 0: CRC disabled for TX and RX
1:0	LENGTH_CONFIG[1:0]	1 (01)	R/W	Configure the packet length Setting: 0 (00) – Fixed packet length mode. Length configured in PKTLEN register 1 (01) – Variable packet length mode. Packet length configured by the first byte after sync word 2 (10) – Infinite packet length mode 3 (11) – Reserved

0x09: ADDR – Device Address

Bit	Field Name	Reset	R/W	Description
7:0	DEVICE_ADDR[7:0]	0 (0x00)	R/W	Address used for packet filtration. Optional broadcast addresses are 0 (0x00) and 255 (0xFF).

0x0A: CHANNR – Channel Number

Bit	Field Name	Reset	R/W	Description
7:0	CHAN[7:0]	0 (0x00)	R/W	The 8-bit unsigned channel number, which is multiplied by the channel spacing setting and added to the base frequency.

0x0B: FSCTRL1 – Frequency Synthesizer Control

Bit	Field Name	Reset	R/W	Description
7:5	Reserved		R0	
4:0	FREQ_IF[4:0]	15 (0x0F)	R/W	The desired IF frequency to employ in RX. Subtracted from FS base frequency in RX and controls the digital complex mixer in the demodulator. $f_{IF} = \frac{f_{XOSC}}{2^{10}} \cdot FREQ\_IF$ The default value gives an IF frequency of 381 kHz, assuming a 26.0 MHz crystal.

0x0C: FSCTRL0 – Frequency Synthesizer Control

Bit	Field Name	Reset	R/W	Description
7:0	FREQOFF[7:0]	0 (0x00)	R/W	Frequency offset added to the base frequency before being used by the FS. (2's complement). Resolution is $F_{XTAL}/2^{14}$ (1.59 - 1.65 kHz); range is ±202 kHz to ±210 kHz, dependent of XTAL frequency.

0x0D: FREQ2 – Frequency Control Word, High Byte

Bit	Field Name	Reset	R/W	Description
7:6	FREQ[23:22]	1 (01)	R	FREQ[23:22] is always binary 01 (the FREQ2 register is in the range 85 to 95 with 26-27 MHz crystal)
5:0	FREQ[21:16]	30 (0x1E)	R/W	FREQ[23:0] is the base frequency for the frequency synthesiser in increments of $F_{XOSC}/2^{16}$. $f_{carrier} = \frac{f_{XOSC}}{2^{16}} \cdot FREQ[23:0]$

0x0E: FREQ1 – Frequency Control Word, Middle Byte

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[15:8]	196 (0xC4)	R/W	Ref. FREQ2 register

0x0F: FREQ0 – Frequency Control Word, Low Byte

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[7:0]	236 (0xEC)	R/W	Ref. FREQ2 register

0x10: MDMCFG4 – Modem Configuration

Bit	Field Name	Reset	R/W	Description
7:6	CHANBW_E[1:0]	2 (10)	R/W	
5:4	CHANBW_M[1:0]	0 (00)	R/W	Sets the decimation ratio for the delta-sigma ADC input stream and thus the channel bandwidth. $BW_{channel} = \frac{f_{XOSC}}{8 \cdot (4 + CHANBW\_M) \cdot 2^{CHANBW\_E}}$ The default values give 203 kHz channel filter bandwidth, assuming a 26.0 MHz crystal.
3:0	DRATE_E[3:0]	12 (1100)	R/W	The exponent of the user specified symbol rate

0x11: MDMCFG3 – Modem Configuration

Bit	Field Name	Reset	R/W	Description
7:0	DRATE_M[7:0]	34 (0x22)	R/W	The mantissa of the user specified symbol rate. The symbol rate is configured using an unsigned, floating-point number with 9-bit mantissa and 4-bit exponent. The 9th bit is a hidden '1'. The resulting data rate is: $R_{DATA} = \frac{(256 + DRATE\_M) \cdot 2^{DRATE\_E}}{2^{28}} \cdot f_{XOSC}$ The default values give a data rate of 115.051 kBaud (closest setting to 115.2 kBaud), assuming a 26.0 MHz crystal.

0x12: MDMCFG2 – Modem Configuration

Bit	Field Name	Reset	R/W	Description
7	DEM_DCFILT_OFF	0	R/W	Disable digital DC blocking filter before demodulator. 0 = Enable (better sensitivity) 1 = Disable (current optimized). Only for data rates ≤ 250 kBaud The recommended IF frequency changes when the DC blocking is disabled. Please use SmartRF® Studio [5] to calculate correct register setting.
6:4	MOD_FORMAT[2:0]	0 (000)	R/W	The modulation format of the radio signal Setting: Modulation format 0 (000): 2-FSK 1 (001): GFSK 2 (010): - 3 (011): OOK 4 (100): - 5 (101): - 6 (110): - 7 (111): MSK
3	MANCHESTER_EN	0	R/W	Enables Manchester encoding/decoding. 0 = Disable 1 = Enable
2:0	SYNC_MODE[2:0]	2 (010)	R/W	Combined sync-word qualifier mode. The values 0 (000) and 4 (100) disables preamble and sync word transmission in TX and preamble and sync word detection in RX. The values 1 (001), 2 (010), 5 (101) and 6 (110) enables 16-bit sync word transmission in TX and 16-bits sync word detection in RX. Only 15 of 16 bits need to match in RX when using setting 1 (001) or 5 (101). The values 3 (011) and 7 (111) enables repeated sync word transmission in TX and 32-bits sync word detection in RX (only 30 of 32 bits need to match). Setting: Sync-word qualifier mode 0 (000): No preamble/sync 1 (001): 15/16 sync word bits detected 2 (010): 16/16 sync word bits detected 3 (011): 30/32 sync word bits detected 4 (100): No preamble/sync, carrier-sense above threshold 5 (101): 15/16 + carrier-sense above threshold 6 (110): 16/16 + carrier-sense above threshold 7 (111): 30/32 + carrier-sense above threshold

0x13: MDMCFG1 – Modem Configuration

Bit	Field Name	Reset	R/W	Description
7	FEC_EN	0	R/W	Enable Forward Error Correction (FEC) with interleaving for packet payload 0 = Disable 1 = Enable (Only supported for fixed packet length mode, i.e. PKTCTRL0.LENGTH_CONFIG=0)
6:4	NUM_PREAMBLE[2:0]	2 (010)	R/W	Sets the minimum number of preamble bytes to be transmitted
3:2	Reserved		R0	
1:0	CHANSPC_E[1:0]	2 (10)	R/W	2 bit exponent of channel spacing

Setting	Number of preamble bytes
0 (000)	2
1 (001)	3
2 (010)	4
3 (011)	6
4 (100)	8
5 (101)	12
6 (110)	16
7 (111)	24

0x14: MDMCFG0 – Modem Configuration

Bit	Field Name	Reset	R/W	Description
7:0	CHANSPC_M[7:0]	248 (0xF8)	R/W	8-bit mantissa of channel spacing. The channel spacing is multiplied by the channel number CHAN and added to the base frequency. It is unsigned and has the format: $\Delta f_{CHANNEL} = \frac{f_{XOSC}}{2^{18}} \cdot (256 + CHANSPC\_M) \cdot 2^{CHANSPC\_E}$ The default values give 199.951 kHz channel spacing (the closest setting to 200 kHz), assuming 26.0 MHz crystal frequency.

0x15: DEVIATN – Modem Deviation Setting

Bit	Field Name	Reset	R/W	Description
7	Reserved		R0	
6:4	DEVIATION_E[2:0]	4 (100)	R/W	Deviation exponent
3	Reserved		R0	
2:0	DEVIATION_M[2:0]	7 (111)	R/W	When MSK modulation is enabled: Sets fraction of symbol period used for phase change. Refer to the SmartRF® Studio software [5] for correct DEVIATN setting when using MSK. When 2-FSK/GFSK modulation is enabled: Deviation mantissa, interpreted as a 4-bit value with MSB implicit 1. The resulting deviation is given by: $f_{dev} = \frac{f_{xosc}}{2^{17}} \cdot (8 + DEVIATION\_M) \cdot 2^{DEVIATION\_E}$ The default values give ±47.607 kHz deviation, assuming 26.0 MHz crystal frequency.

0x16: MCSM2 – Main Radio Control State Machine Configuration

Bit	Field Name	Reset	R/W	Description
7:5	Reserved		R0	Reserved
4	RX_TIME_RSSI	0	R/W	Direct RX termination based on RSSI measurement (carrier sense).
3	RX_TIME_QUAL	0	R/W	When the RX_TIME timer expires the chip stays in RX mode if sync word is found when RX_TIME_QUAL=0, or either sync word is found or PQT is set when RX_TIME_QUAL=1.
2:0	RX_TIME[2:0]	7 (111)	R/W	Timeout for sync word search in RX for both WOR mode and normal RX operation. The timeout is relative to the programmed EVENT0 timeout.

The RX timeout in µs is given by EVENT0·C(RX_TIME, WOR_RES) ·26/X, where C is given by the table below and X is the crystal oscillator frequency in MHz:

RX_TIME[2:0]	WOR_RES = 0	WOR_RES = 1	WOR_RES = 2	WOR_RES = 3
0 (000)	3.6058	18.0288	32.4519	46.8750
1 (001)	1.8029	9.0144	16.2260	23.4375
2 (010)	0.9014	4.5072	8.1130	11.7188
3 (011)	0.4507	2.2536	4.0565	5.8594
4 (100)	0.2254	1.1268	2.0282	2.9297
5 (101)	0.1127	0.5634	1.0141	1.4648
6 (110)	0.0563	0.2817	0.5071	0.7324
7 (111)	Until end of packet			

As an example, EVENT0=34666, WOR_RES=0 and RX_TIME=6 corresponds to 1.95 ms RX timeout, 1 s polling interval and 0.195% duty cycle. Note that WOR_RES should be 0 or 1 when using WOR because using WOR_RES > 1 will give a very low duty cycle. In applications where WOR is not used all settings of WOR_RES can be used.

The duty cycle using WOR is approximated by:

RX_TIME[2:0]	WOR_RES = 0	WOR_RES = 1
0 (000)	12.50%	1.95%
1 (001)	6.250%	9765 ppm
2 (010)	3.125%	4883 ppm
3 (011)	1.563%	2441 ppm
4 (100)	0.781%	NA
5 (101)	0.391%	NA
6 (110)	0.195%	NA
7 (111)	NA	

Note that the RC oscillator must be enabled in order to use setting 0-6, because the timeout counts RC oscillator periods. WOR mode does not need to be enabled.
The timeout counter resolution is limited: With RX_TIME=0, the timeout count is given by the 13 MSBs of EVENT0, decreasing to the 7 MSBs of EVENT0 with RX_TIME=6.

0x17: MCSM1 – Main Radio Control State Machine Configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:6</td><td>Reserved</td><td></td><td>R0</td><td></td></tr>
<tr><td>5:4</td><td>CCA_MODE[1:0]</td><td>3 (11)</td><td>R/W</td><td>Selects CCA_MODE; Reflected in CCA signal
<table><tr><td>Setting</td><td>Clear channel indication</td></tr><tr><td>0 (00)</td><td>Always</td></tr><tr><td>1 (01)</td><td>If RSSI below threshold</td></tr><tr><td>2 (10)</td><td>Unless currently receiving a packet</td></tr><tr><td>3 (11)</td><td>If RSSI below threshold unless currently receiving a packet</td></tr></table></td></tr>
<tr><td>3:2</td><td>RXOFF_MODE[1:0]</td><td>0 (00)</td><td>R/W</td><td>Select what should happen when a packet has been received
<table><tr><td>Setting</td><td>Next state after finishing packet reception</td></tr><tr><td>0 (00)</td><td>IDLE</td></tr><tr><td>1 (01)</td><td>FSTXON</td></tr><tr><td>2 (10)</td><td>TX</td></tr><tr><td>3 (11)</td><td>Stay in RX</td></tr></table>It is not possible to set RXOFF_MODE to be TX or FSTXON and at the same time use CCA.</td></tr>
<tr><td>1:0</td><td>TXOFF_MODE[1:0]</td><td>0 (00)</td><td>R/W</td><td>Select what should happen when a packet has been sent (TX)
<table><tr><td>Setting</td><td>Next state after finishing packet transmission</td></tr><tr><td>0 (00)</td><td>IDLE</td></tr><tr><td>1 (01)</td><td>FSTXON</td></tr><tr><td>2 (10)</td><td>Stay in TX (start sending preamble)</td></tr><tr><td>3 (11)</td><td>RX</td></tr></table></td></tr>
</table>

0x18: MCSM0 – Main Radio Control State Machine Configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:6</td><td>Reserved</td><td></td><td>R0</td><td></td></tr>
<tr><td>5:4</td><td>FS_AUTOCAL[1:0]</td><td>0 (00)</td><td>R/W</td><td>Automatically calibrate when going to RX or TX, or back to IDLE
<table><tr><td>Setting</td><td>When to perform automatic calibration</td></tr><tr><td>0 (00)</td><td>Never (manually calibrate using SCAL strobe)</td></tr><tr><td>1 (01)</td><td>When going from IDLE to RX or TX (or FSTXON)</td></tr><tr><td>2 (10)</td><td>When going from RX or TX back to IDLE automatically</td></tr><tr><td>3 (11)</td><td>Every 4th time when going from RX or TX to IDLE automatically</td></tr></table>In some automatic wake-on-radio (WOR) applications, using setting 3 (11) can significantly reduce current consumption.</td></tr>
<tr><td>3:2</td><td>PO_TIMEOUT</td><td>1 (01)</td><td>R/W</td><td>Programs the number of times the six-bit ripple counter must expire after XOSC has stabilized before CHP_RDYn goes low.
If XOSC is on (stable) during power-down, PO_TIMEOUT should be set so that the regulated digital supply voltage has time to stabilize before CHP_RDYn goes low (PO_TIMEOUT=2 recommended). Typical start-up time for the voltage regulator is 50 us.
If XOSC is off during power-down and the regulated digital supply voltage has sufficient time to stabilize while waiting for the crystal to be stable, PO_TIMEOUT can be set to 0. For robust operation it is recommended to use PO_TIMEOUT=2.
<table><tr><td>Setting</td><td>Expire count</td><td>Timeout after XOSC start</td></tr><tr><td>0 (00)</td><td>1</td><td>Approx. 2.3 – 2.4 µs</td></tr><tr><td>1 (01)</td><td>16</td><td>Approx. 37 – 39 µs</td></tr><tr><td>2 (10)</td><td>64</td><td>Approx. 149 – 155 µs</td></tr><tr><td>3 (11)</td><td>256</td><td>Approx. 597 – 620 µs</td></tr></table>Exact timeout depends on crystal frequency.</td></tr>
<tr><td>1</td><td>PIN_CTRL_EN</td><td>0</td><td>R/W</td><td>Enables the pin radio control option</td></tr>
<tr><td>0</td><td>XOSC_FORCE_ON</td><td>0</td><td>R/W</td><td>Force the XOSC to stay on in the SLEEP state.</td></tr>
</table>

0x19: FOCCFG – Frequency Offset Compensation Configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:6</td><td>Reserved</td><td></td><td>R0</td><td></td></tr>
<tr><td>5</td><td>FOC_BS_CS_GATE</td><td>1</td><td>R/W</td><td>If set, the demodulator freezes the frequency offset compensation and clock recovery feedback loops until the CARRIER_SENSE signal goes high.</td></tr>
<tr><td>4:3</td><td>FOC_PRE_K[1:0]</td><td>2 (10)</td><td>R/W</td><td>The frequency compensation loop gain to be used before a sync word is detected.
<table>
<tr><th>Setting</th><th>Freq. compensation loop gain before sync word</th></tr>
<tr><td>0 (00)</td><td>K</td></tr>
<tr><td>1 (01)</td><td>2K</td></tr>
<tr><td>2 (10)</td><td>3K</td></tr>
<tr><td>3 (11)</td><td>4K</td></tr>
</table></td></tr>
<tr><td>2</td><td>FOC_POST_K</td><td>1</td><td>R/W</td><td>The frequency compensation loop gain to be used after a sync word is detected.
<table>
<tr><th>Setting</th><th>Freq. compensation loop gain after sync word</th></tr>
<tr><td>0</td><td>Same as FOC_PRE_K</td></tr>
<tr><td>1</td><td>K/2</td></tr>
</table></td></tr>
<tr><td>1:0</td><td>FOC_LIMIT[1:0]</td><td>2 (10)</td><td>R/W</td><td>The saturation point for the frequency offset compensation algorithm:
<table>
<tr><th>Setting</th><th>Saturation point (max compensated offset)</th></tr>
<tr><td>0 (00)</td><td>±0 (no frequency offset compensation)</td></tr>
<tr><td>1 (01)</td><td>$\pm BW_{CHAN}/8$</td></tr>
<tr><td>2 (10)</td><td>$\pm BW_{CHAN}/4$</td></tr>
<tr><td>3 (11)</td><td>$\pm BW_{CHAN}/2$</td></tr>
</table>
Frequency offset compensation is not supported for OOK; Always use FOC_LIMIT=0 with this modulation format.</td></tr>
</table>

0x1A: BSCFG – Bit Synchronization Configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:6</td><td>BS_PRE_KI[1:0]</td><td>1 (01)</td><td>R/W</td><td>The clock recovery feedback loop integral gain to be used before a sync word is detected (used to correct offsets in data rate):
<table>
<tr><th>Setting</th><th>Clock recovery loop integral gain before sync word</th></tr>
<tr><td>0 (00)</td><td>K_I</td></tr>
<tr><td>1 (01)</td><td>$2K_I$</td></tr>
<tr><td>2 (10)</td><td>$3K_I$</td></tr>
<tr><td>3 (11)</td><td>$4K_I$</td></tr>
</table></td></tr>
<tr><td>5:4</td><td>BS_PRE_KP[1:0]</td><td>2 (10)</td><td>R/W</td><td>The clock recovery feedback loop proportional gain to be used before a sync word is detected.
<table>
<tr><th>Setting</th><th>Clock recovery loop proportional gain before sync word</th></tr>
<tr><td>0 (00)</td><td>K_P</td></tr>
<tr><td>1 (01)</td><td>$2K_P$</td></tr>
<tr><td>2 (10)</td><td>$3K_P$</td></tr>
<tr><td>3 (11)</td><td>$4K_P$</td></tr>
</table></td></tr>
<tr><td>3</td><td>BS_POST_KI</td><td>1</td><td>R/W</td><td>The clock recovery feedback loop integral gain to be used after a sync word is detected.
<table>
<tr><th>Setting</th><th>Clock recovery loop integral gain after sync word</th></tr>
<tr><td>0</td><td>Same as BS_PRE_KI</td></tr>
<tr><td>1</td><td>$K_I/2$</td></tr>
</table></td></tr>
<tr><td>2</td><td>BS_POST_KP</td><td>1</td><td>R/W</td><td>The clock recovery feedback loop proportional gain to be used after a sync word is detected.
<table>
<tr><th>Setting</th><th>Clock recovery loop proportional gain after sync word</th></tr>
<tr><td>0</td><td>Same as BS_PRE_KP</td></tr>
<tr><td>1</td><td>K_P</td></tr>
</table></td></tr>
<tr><td>1:0</td><td>BS_LIMIT[1:0]</td><td>0 (00)</td><td>R/W</td><td>The saturation point for the data rate offset compensation algorithm:
<table>
<tr><th>Setting</th><th>Data rate offset saturation (max data rate difference)</th></tr>
<tr><td>0 (00)</td><td>±0 (No data rate offset compensation performed)</td></tr>
<tr><td>1 (01)</td><td>±3.125% data rate offset</td></tr>
<tr><td>2 (10)</td><td>±6.25% data rate offset</td></tr>
<tr><td>3 (11)</td><td>±12.5% data rate offset</td></tr>
</table></td></tr>
</table>

0x1B: AGCCTRL2 – AGC Control

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:6</td><td>MAX_DVGA_GAIN[1:0]</td><td>0 (00)</td><td>R/W</td><td>Reduces the maximum allowable DVGA gain.
<table>
<tr><th>Setting</th><th>Allowable DVGA settings</th></tr>
<tr><td>0 (00)</td><td>All gain settings can be used</td></tr>
<tr><td>1 (01)</td><td>The highest gain setting can not be used</td></tr>
<tr><td>2 (10)</td><td>The 2 highest gain settings can not be used</td></tr>
<tr><td>3 (11)</td><td>The 3 highest gain settings can not be used</td></tr>
</table></td></tr>
<tr><td>5:3</td><td>MAX_LNA_GAIN[2:0]</td><td>0 (000)</td><td>R/W</td><td>Sets the maximum allowable LNA + LNA 2 gain relative to the maximum possible gain.
<table>
<tr><th>Setting</th><th>Maximum allowable LNA + LNA 2 gain</th></tr>
<tr><td>0 (000)</td><td>Maximum possible LNA + LNA 2 gain</td></tr>
<tr><td>1 (001)</td><td>Approx. 2.6 dB below maximum possible gain</td></tr>
<tr><td>2 (010)</td><td>Approx. 6.1 dB below maximum possible gain</td></tr>
<tr><td>3 (011)</td><td>Approx. 7.4 dB below maximum possible gain</td></tr>
<tr><td>4 (100)</td><td>Approx. 9.2 dB below maximum possible gain</td></tr>
<tr><td>5 (101)</td><td>Approx. 11.5 dB below maximum possible gain</td></tr>
<tr><td>6 (110)</td><td>Approx. 14.6 dB below maximum possible gain</td></tr>
<tr><td>7 (111)</td><td>Approx. 17.1 dB below maximum possible gain</td></tr>
</table></td></tr>
<tr><td>2:0</td><td>MAGN_TARGET[2:0]</td><td>3 (011)</td><td>R/W</td><td>These bits set the target value for the averaged amplitude from the digital channel filter (1 LSB = 0 dB).
<table>
<tr><th>Setting</th><th>Target amplitude from channel filter</th></tr>
<tr><td>0 (000)</td><td>24 dB</td></tr>
<tr><td>1 (001)</td><td>27 dB</td></tr>
<tr><td>2 (010)</td><td>30 dB</td></tr>
<tr><td>3 (011)</td><td>33 dB</td></tr>
<tr><td>4 (100)</td><td>36 dB</td></tr>
<tr><td>5 (101)</td><td>38 dB</td></tr>
<tr><td>6 (110)</td><td>40 dB</td></tr>
<tr><td>7 (111)</td><td>42 dB</td></tr>
</table></td></tr>
</table>

0x1C: AGCCTRL1 – AGC Control

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>Reserved</td><td></td><td>R0</td><td></td></tr>
<tr><td>6</td><td>AGC_LNA_PRIORITY</td><td>1</td><td>R/W</td><td>Selects between two different strategies for LNA and LNA2 gain adjustment. When 1, the LNA gain is decreased first. When 0, the LNA2 gain is decreased to minimum before decreasing LNA gain.</td></tr>
<tr><td>5:4</td><td>CARRIER_SENSE_REL_THR[1:0]</td><td>0 (00)</td><td>R/W</td><td>Sets the relative change threshold for asserting carrier sense.
<table>
<tr><th>Setting</th><th>Carrier sense relative threshold</th></tr>
<tr><td>0 (00)</td><td>Relative carrier sense threshold disabled</td></tr>
<tr><td>1 (01)</td><td>6 dB increase in RSSI value</td></tr>
<tr><td>2 (10)</td><td>10 dB increase in RSSI value</td></tr>
<tr><td>3 (11)</td><td>14 dB increase in RSSI value</td></tr>
</table></td></tr>
<tr><td>3:0</td><td>CARRIER_SENSE_ABS_THR[3:0]</td><td>0 (0000)</td><td>R/W</td><td>Sets the absolute RSSI threshold for asserting carrier sense. The 2’s complement signed threshold is programmed in steps of 1 dB and is relative to the MAGN_TARGET setting.
<table>
<tr><th>Setting</th><th>Carrier sense absolute threshold
(Equal to channel filter amplitude when AGC has not decreased gain)</th></tr>
<tr><td>-8 (1000)</td><td>Absolute carrier sense threshold disabled</td></tr>
<tr><td>-7 (1001)</td><td>7 dB below MAGN_TARGET setting</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>-1 (1111)</td><td>1 dB below MAGN_TARGET setting</td></tr>
<tr><td>0 (0000)</td><td>At MAGN_TARGET setting</td></tr>
<tr><td>1 (0001)</td><td>1 dB above MAGN_TARGET setting</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>7 (0111)</td><td>7 dB above MAGN_TARGET setting</td></tr>
</table></td></tr>
</table>

0x1D: AGCCTRL0 – AGC Control

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:6</td><td>HYST_LEVEL[1:0]</td><td>2 (10)</td><td>R/W</td><td>Sets the level of hysteresis on the magnitude deviation (internal AGC signal that determines gain changes).
<table>
<tr><th>Setting</th><th>Description</th></tr>
<tr><td>0 (00)</td><td>No hysteresis, small symmetric dead zone, high gain</td></tr>
<tr><td>1 (01)</td><td>Low hysteresis, small asymmetric dead zone, medium gain</td></tr>
<tr><td>2 (10)</td><td>Medium hysteresis, medium asymmetric dead zone, medium gain</td></tr>
<tr><td>3 (11)</td><td>Large hysteresis, large asymmetric dead zone, low gain</td></tr>
</table></td></tr>
<tr><td>5:4</td><td>WAIT_TIME[1:0]</td><td>1 (01)</td><td>R/W</td><td>Sets the number of channel filter samples from a gain adjustment has been made until the AGC algorithm starts accumulating new samples.
<table>
<tr><th>Setting</th><th>Channel filter samples</th></tr>
<tr><td>0 (00)</td><td>8</td></tr>
<tr><td>1 (01)</td><td>16</td></tr>
<tr><td>2 (10)</td><td>24</td></tr>
<tr><td>3 (11)</td><td>32</td></tr>
</table></td></tr>
<tr><td>3:2</td><td>AGC_FREEZE[1:0]</td><td>0 (00)</td><td>R/W</td><td>Controls when the AGC gain should be frozen.
<table>
<tr><th>Setting</th><th>Function</th></tr>
<tr><td>0 (00)</td><td>Normal operation. Always adjust gain when required.</td></tr>
<tr><td>1 (01)</td><td>The gain setting is frozen when a sync word has been found.</td></tr>
<tr><td>2 (10)</td><td>Manually freezes the analog gain setting and continue to adjust the digital gain.</td></tr>
<tr><td>3 (11)</td><td>Manually freezes both the analog and the digital gain settings. Used for manually overriding the gain.</td></tr>
</table></td></tr>
<tr><td>1:0</td><td>FILTER_LENGTH[1:0]</td><td>1 (01)</td><td>R/W</td><td>Sets the averaging length for the amplitude from the channel filter. Sets the OOK decision boundary for OOK reception.
<table>
<tr><th>Setting</th><th>Channel filter samples</th><th>OOK decision</th></tr>
<tr><td>0 (00)</td><td>8</td><td>4 dB</td></tr>
<tr><td>1 (01)</td><td>16</td><td>8 dB</td></tr>
<tr><td>2 (10)</td><td>32</td><td>12 dB</td></tr>
<tr><td>3 (11)</td><td>64</td><td>16 dB</td></tr>
</table></td></tr>
</table>

0x1E: WOREVT1 – High Byte Event0 Timeout

Bit	Field Name	Reset	R/W	Description
7:0	EVENT0[15:8]	135 (0x87)	R/W	High byte of Event 0 timeout register $t_{Event0} = \frac{750}{f_{XOSC}} \cdot EVENT0 \cdot 2^{5 \cdot WOR\_RES}$

0x1F: WOREVT0 – Low Byte Event0 Timeout

Bit	Field Name	Reset	R/W	Description
7:0	EVENT0[7:0]	107 (0x6B)	R/W	Low byte of Event 0 timeout register. The default Event 0 value gives 1.0 s timeout, assuming a 26.0 MHz crystal.

0x20: WORCTRL – Wake On Radio Control

Bit	Field Name	Reset	R/W	Description
7	RC_PD	1	R/W	Power down signal to RC oscillator. When written to 0, automatic initial calibration will be performed
6:4	EVENT1[2:0]	7 (111)	R/W	Timeout setting from register block. Decoded to Event 1 timeout. RC oscillator clock frequency equals F_{XOSC}/750, which is 34.7-36 kHz, depending on crystal frequency. The table below lists the number of clock periods after Event 0 before Event 1 times out.
3	RC_CAL	1	R/W	Enables (1) or disables (0) the RC oscillator calibration.
2	Reserved		R0	
1:0	WOR_RES[1:0]	0 (00)	R/W	Controls the Event 0 resolution as well as maximum timeout of the WOR module and maximum timeout under normal RX operation:

Setting	t_event1
0 (000)	4 (0.111 – 0.115 ms)
1 (001)	6 (0.167 – 0.173 ms)
2 (010)	8 (0.222 – 0.230 ms)
3 (011)	12 (0.333 – 0.346 ms)
4 (100)	16 (0.444 – 0.462 ms)
5 (101)	24 (0.667 – 0.692 ms)
6 (110)	32 (0.889 – 0.923 ms)
7 (111)	48 (1.333 – 1.385 ms)

Setting	Resolution (1 LSB)	Max timeout
0 (00)	1 period (28 – 29 µs)	1.8 – 1.9 seconds
1 (01)	2^5 periods (0.89 – 0.92 ms)	58 – 61 seconds
2 (10)	2^{10} periods (28 – 30 ms)	31 – 32 minutes
3 (11)	2^{15} periods (0.91 – 0.94 s)	16.5 – 17.2 hours

Note that WOR_RES should be 0 or 1 when using WOR because WOR_RES > 1 will give a very low duty cycle.

In normal RX operation all settings of WOR_RES can be used.

0x21: FREND1 – Front End RX Configuration

Bit	Field Name	Reset	R/W	Description
7:6	LNA_CURRENT[1:0]	1 (01)	R/W	Adjusts front-end LNA PTAT current output
5:4	LNA2MIX_CURRENT[1:0]	1 (01)	R/W	Adjusts front-end PTAT outputs
3:2	LODIV_BUF_CURRENT_RX[1:0]	1 (01)	R/W	Adjusts current in RX LO buffer (LO input to mixer)
1:0	MIX_CURRENT[1:0]	2 (10)	R/W	Adjusts current in mixer

0x22: FREND0 – Front End TX configuration

Bit	Field Name	Reset	R/W	Description
7:6	Reserved		R0	
5:4	LODIV_BUF_CURRENT_TX[1:0]	1 (01)	R/W	Adjusts current TX LO buffer (input to PA). The value to use in this field is given by the SmartRF® Studio software [5].
3	Reserved		R0	
2:0	PA_POWER[2:0]	0 (000)	R/W	Selects PA power setting. This value is an index to the PATABLE. In OOK mode, this selects the PATABLE index to use when transmitting a '1'. PATABLE index zero is used in OOK when transmitting a '0'.

0x23: FSCAL3 – Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7:6	FSCAL3[7:6]	2 (10)	R/W	Frequency synthesizer calibration configuration. The value to write in this register before calibration is given by the SmartRF® Studio software [5].
5:4	CHP_CURR_CAL_EN[1:0]	2 (10)	R/W	Disable charge pump calibration stage when 0
3:0	FSCAL3[3:0]	9 (1001)	R/W	Frequency synthesizer calibration result register. Digital bit vector defining the charge pump output current, on an exponential scale: $IOUT=I_0 \cdot 2^{FSCAL3[3:0]/4}$ Fast frequency hopping without calibration for each hop can be done by calibrating upfront for each frequency and saving the resulting FSCAL3, FSCAL2 and FSCAL1 register values. Between each frequency hop, calibration can be replaced by writing the FSCAL3, FSCAL2 and FSCAL1 register values corresponding to the next RF frequency.

0x24: FSCAL2 – Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7:6	Reserved		R0	
5	VCO_CORE_H_EN	0	R/W	Choose high (1) / low (0) VCO
4:0	FSCAL2[4:0]	10 (0x0A)	R/W	Frequency synthesizer calibration result register. VCO current calibration result and override value Fast frequency hopping without calibration for each hop can be done by calibrating upfront for each frequency and saving the resulting FSCAL3, FSCAL2 and FSCAL1 register values. Between each frequency hop, calibration can be replaced by writing the FSCAL3, FSCAL2 and FSCAL1 register values corresponding to the next RF frequency.

0x25: FSCAL1 – Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7:6	Reserved		R0	
5:0	FSCAL1[5:0]	32 (0x20)	R/W	Frequency synthesizer calibration result register. Capacitor array setting for VCO coarse tuning. Fast frequency hopping without calibration for each hop can be done by calibrating upfront for each frequency and saving the resulting FSCAL3, FSCAL2 and FSCAL1 register values. Between each frequency hop, calibration can be replaced by writing the FSCAL3, FSCAL2 and FSCAL1 register values corresponding to the next RF frequency.

0x26: FSCAL0 – Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7	Reserved		R0	
6:0	FSCAL0[6:0]	13 (0x0D)	R/W	Frequency synthesizer calibration control. The value to use in this register is given by the SmartRF® Studio software [5].

0x27: RCCTRL1 – RC Oscillator Configuration

Bit	Field Name	Reset	R/W	Description
7	Reserved	0	R0	
6:0	RCCTRL1[6:0]	65 (0x41)	R/W	RC oscillator configuration.

0x28: RCCTRL0 – RC Oscillator Configuration

Bit	Field Name	Reset	R/W	Description
7	Reserved	0	R0	
6:0	RCCTRL0[6:0]	0 (0x00)	R/W	RC oscillator configuration.

32.2 Configuration Register Details – Registers that Lose Programming in SLEEP State

0x29: FSTEST – Frequency Synthesizer Calibration Control

Bit	Field Name	Reset	R/W	Description
7:0	FSTEST[7:0]	89 (0x59)	R/W	For test only. Do not write to this register.

0x2A: PTEST – Production Test

Bit	Field Name	Reset	R/W	Description
7:0	PTEST[7:0]	127 (0x7F)	R/W	Writing 0xBF to this register makes the on-chip temperature sensor available in the IDLE state. The default 0x7F value should then be written back before leaving the IDLE state. Other use of this register is for test only.

0x2B: AGCTEST – AGC Test

Bit	Field Name	Reset	R/W	Description
7:0	AGCTEST[7:0]	63 (0x3F)	R/W	For test only. Do not write to this register.

0x2C: TEST2 – Various Test Settings

Bit	Field Name	Reset	R/W	Description
7:0	TEST2[7:0]	136 (0x88)	R/W	Set to 0x81 for improved sensitivity at data rates ≤100 kBaud. The temperature range is then from 0°C to +85°C.

0x2D: TEST1 – Various Test Settings

Bit	Field Name	Reset	R/W	Description
7:0	TEST1[7:0]	49 (0x31)	R/W	Set to 0x35 for improved sensitivity at data rates ≤100 kBaud. The temperature range is then from 0°C to +85°C.

0x2E: TEST0 – Various Test Settings

Bit	Field Name	Reset	R/W	Description
7:2	TEST0[7:2]	2 (0x02)	R/W	The value to use in this register is given by the SmartRF® Studio software [5].
1	VCO_SEL_CAL_EN	1	R/W	Enable VCO selection calibration stage when 1
0	TEST0[0]	1	R/W	The value to use in this register is given by the SmartRF® Studio software [5].

32.3 Status Register Details

0x30 (0xF0): PARTNUM – Chip ID

Bit	Field Name	Reset	R/W	Description
7:0	PARTNUM[7:0]	128 (0x80)	R	Chip part number

0x31 (0xF1): VERSION – Chip ID

Bit	Field Name	Reset	R/W	Description
7:0	VERSION[7:0]	3 (0x03)	R	Chip version number.

0x32 (0xF2): FREQEST – Frequency Offset Estimate from Demodulator

Bit	Field Name	Reset	R/W	Description
7:0	FREQOFF_EST		R	The estimated frequency offset (2's complement) of the carrier. Resolution is $F_{XTAL}/2^{14}$ (1.59 - 1.65 kHz); range is ±202 kHz to ±210 kHz, dependent of XTAL frequency. Frequency offset compensation is only supported for 2-FSK; GFSK and MSK modulation. This register will read 0 when using OOK modulation.

0x33 (0xF3): LQI – Demodulator Estimate for Link Quality

Bit	Field Name	Reset	R/W	Description
7	CRC_OK		R	The last CRC comparison matched. Cleared when entering/restarting RX mode. Only valid if PKTCTRL0.CC2400_EN=1.
6:0	LQI_EST[6:0]		R	The Link Quality Indicator estimates how easily a received signal can be demodulated. Calculated over the 64 symbols following the sync word.

0x34 (0xF4): RSSI – Received Signal Strength Indication

Bit	Field Name	Reset	R/W	Description
7:0	RSSI		R	Received signal strength indicator

0x35 (0xF5): MARCSTATE – Main Radio Control State Machine State

Bit	Field Name	Reset	R/W	Description
7:5	Reserved		R0	
4:0	MARC_STATE[4:0]		R	Main Radio Control FSM State

Value	State name	State (Figure 15, page 39)
0 (0x00)	SLEEP	SLEEP
1 (0x01)	IDLE	IDLE
2 (0x02)	XOFF	XOFF
3 (0x03)	VCOON_MC	MANCAL
4 (0x04)	REGON_MC	MANCAL
5 (0x05)	MANCAL	MANCAL
6 (0x06)	VCOON	FS_WAKEUP
7 (0x07)	REGON	FS_WAKEUP
8 (0x08)	STARTCAL	CALIBRATE
9 (0x09)	BWBOOST	SETTLING
10 (0x0A)	FS_LOCK	SETTLING
11 (0x0B)	IFADCON	SETTLING
12 (0x0C)	ENDCAL	CALIBRATE
13 (0x0D)	RX	RX
14 (0x0E)	RX_END	RX
15 (0x0F)	RX_RST	RX
16 (0x10)	TXRX_SWITCH	TXRX_SETTLING
17 (0x11)	RXFIFO_OVERFLOW	RXFIFO_OVERFLOW
18 (0x12)	FSTXON	FSTXON
19 (0x13)	TX	TX
20 (0x14)	TX_END	TX
21 (0x15)	RXTX_SWITCH	RXTX_SETTLING
22 (0x16)	TXFIFO_UNDERFLOW	TXFIFO_UNDERFLOW

Note: it is not possible to read back the SLEEP or XOFF state numbers because setting CSn low will make the chip enter the IDLE mode from the SLEEP or XOFF states.

0x36 (0xF6): WORTIME1 – High Byte of WOR Time

Bit	Field Name	Reset	R/W	Description
7:0	TIME[15:8]		R	High byte of timer value in WOR module

0x37 (0xF7): WORTIME0 – Low Byte of WOR Time

Bit	Field Name	Reset	R/W	Description
7:0	TIME[7:0]		R	Low byte of timer value in WOR module

0x38 (0xF8): PKTSTATUS – Current GDOx Status and Packet Status

Bit	Field Name	Reset	R/W	Description
7	CRC_OK		R	The last CRC comparison matched. Cleared when entering/restarting RX mode. Only valid if PKTCTRL0.CC2400_EN=1.
6	CS		R	Carrier sense
5	PQT_REACHED		R	Preamble Quality reached
4	CCA		R	Channel is clear
3	SFD		R	Sync word found
2	GDO2		R	Current GDO2 value. Note: the reading gives the non-inverted value irrespective what IOCFG2.GDO2_INV is programmed to. It is not recommended to check for PLL lock by reading PKTSTATUS[2] with GDO2_CFG=0x0A.
1	Reserved		R0	
0	GDO0		R	Current GDO0 value. Note: the reading gives the non-inverted value irrespective what IOCFG0.GDO0_INV is programmed to. It is not recommended to check for PLL lock by reading PKTSTATUS[0] with GDO0_CFG=0x0A.

0x39 (0xF9): VCO_VC_DAC – Current Setting from PLL Calibration Module

Bit	Field Name	Reset	R/W	Description
7:0	VCO_VC_DAC[7:0]		R	Status register for test only

0x3A (0xFA): TXBYTES – Underflow and Number of Bytes

Bit	Field Name	Reset	R/W	Description
7	TXFIFO_UNDERFLOW		R	
6:0	NUM_TXBYTES		R	Number of bytes in TX FIFO

0x3B (0xFB): RXBYTES – Underflow and Number of Bytes

Bit	Field Name	Reset	R/W	Description
7	RXFIFO_OVERFLOW		R	
6:0	NUM_RXBYTES		R	Number of bytes in RX FIFO

0x3C (0xFC): RCCTRL1_STATUS – Last RC Oscillator Calibration Result

Bit	Field Name	Reset	R/W	Description
7	Reserved		R0	
6:0	RCCTRL1_STATUS[6:0]		R	Contains the value from the last run of the RC oscillator calibration routine. For usage description refer to AN047 [3].

0x3D (0xFC): RCCTRL0_STATUS – Last RC Oscillator Calibration Result

Bit	Field Name	Reset	R/W	Description
7	Reserved		R0	
6:0	RCCTRL0_STATUS[6:0]		R	Contains the value from the last run of the RC oscillator calibration routine. For usage description refer to AN047 [3].