# Lab 2 Report

**Name: Frank Le**

**UT EID: fpl227**

**Section: Tuesday 2 – 3 p.m. (16100)**

## Checklist:

### Part 1 –

i. Simulation waveforms for Part 1 for Structural as well as Behavioral modelling (Screenshots)

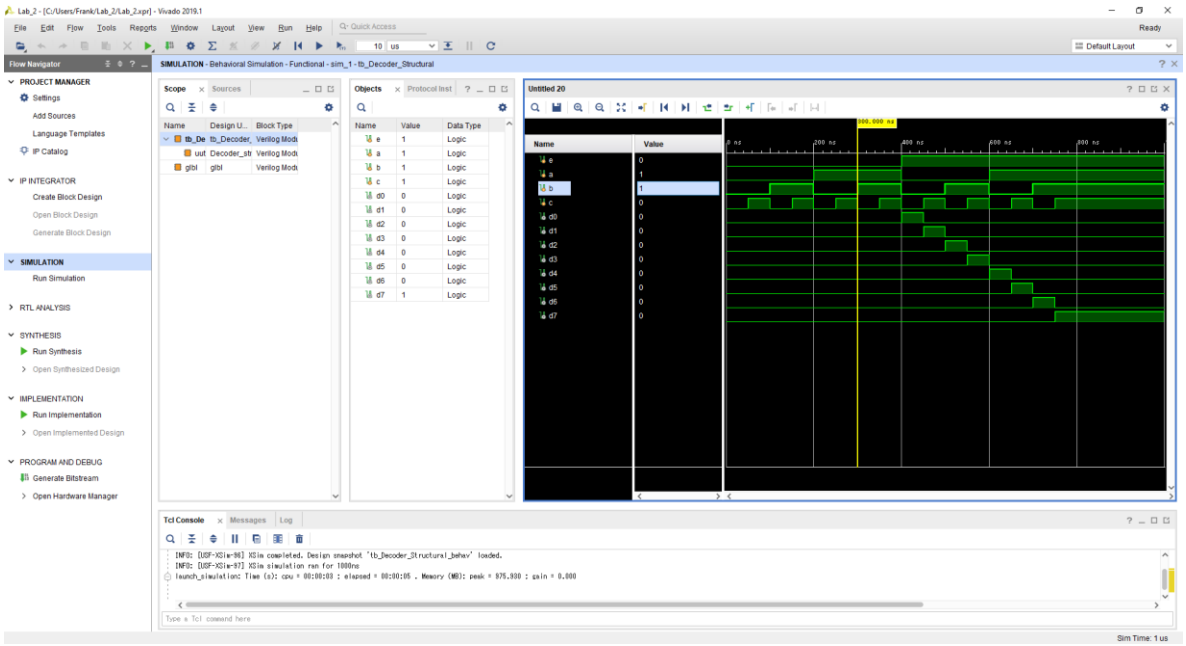
### Part 2 –

ii. Truth table of the function
iii. Algebraic expression of the logic function
iv. Logic circuit schematic
v. Verilog codes for module and testbench for structural modelling
vi. Simulation waveform for structural modelling (Screenshot)
vii. Verilog codes for module and testbench for behavioral modelling
viii. Simulation waveform for behavioral modelling (Screenshot)

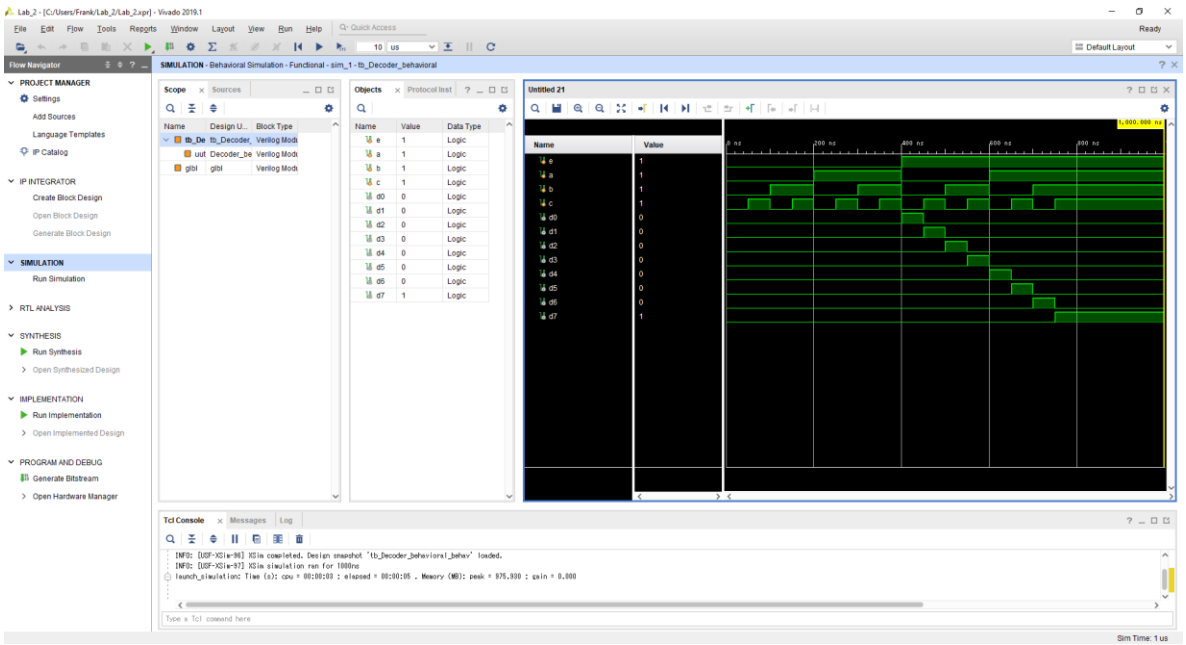
***Note** –> The Verilog codes should be copied in your lab report, and the actual Verilog (.v) files need to be zipped and submitted as well on Canvas. You are not allowed to change your Verilog codes after final submission as the TAs may download the submitted codes from Canvas during checkouts. For the truth table, algebraic expression and circuit schematic, you are free to draw it on paper and then put the pictures in your lab report, but please make sure it is legible for the TAs to grade it properly.*

# Part 1)

## i) Decoder Structural Waveform



## i) Decoder Behavioral Waveform



**Part 2)**

Frank Le
fpl227
EE316
Dr. Orshansky

# Lab 2 Part 2

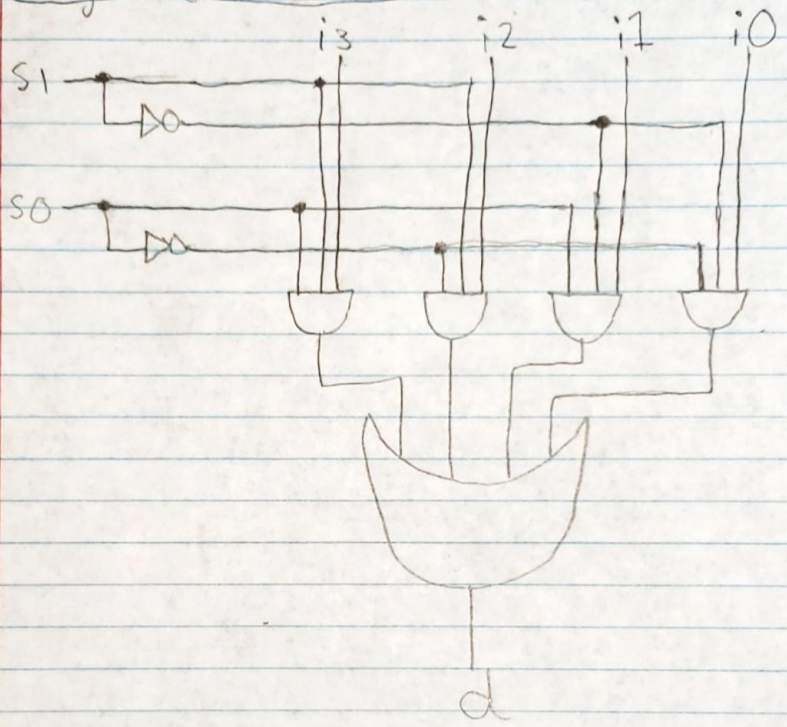
ii) Truth Table

| S1 | S0 | d |
|---|---|---|
| 0 | 0 | i0 |
| 0 | 1 | i1 |
| 1 | 0 | i2 |
| 1 | 1 | i3 |

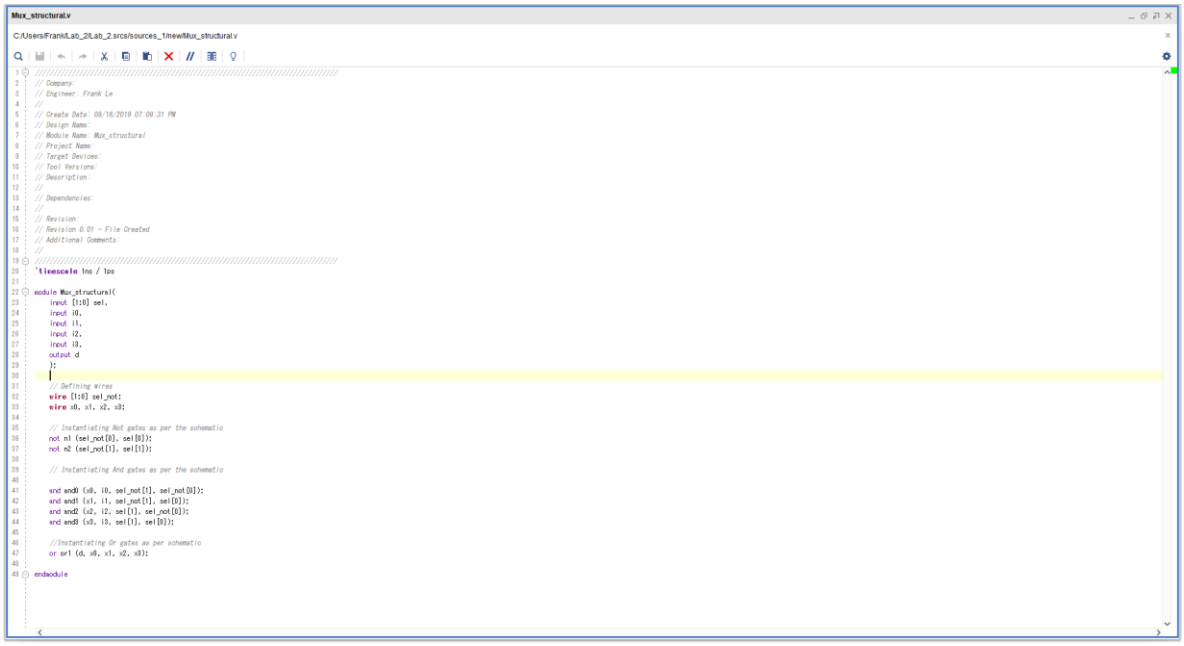
iii) Algebraic Expression

$$d = S1'S0'i0 + S1'S0i1 + S1S0'i2 + S1S0i3$$

iv) Logic circuit schematic



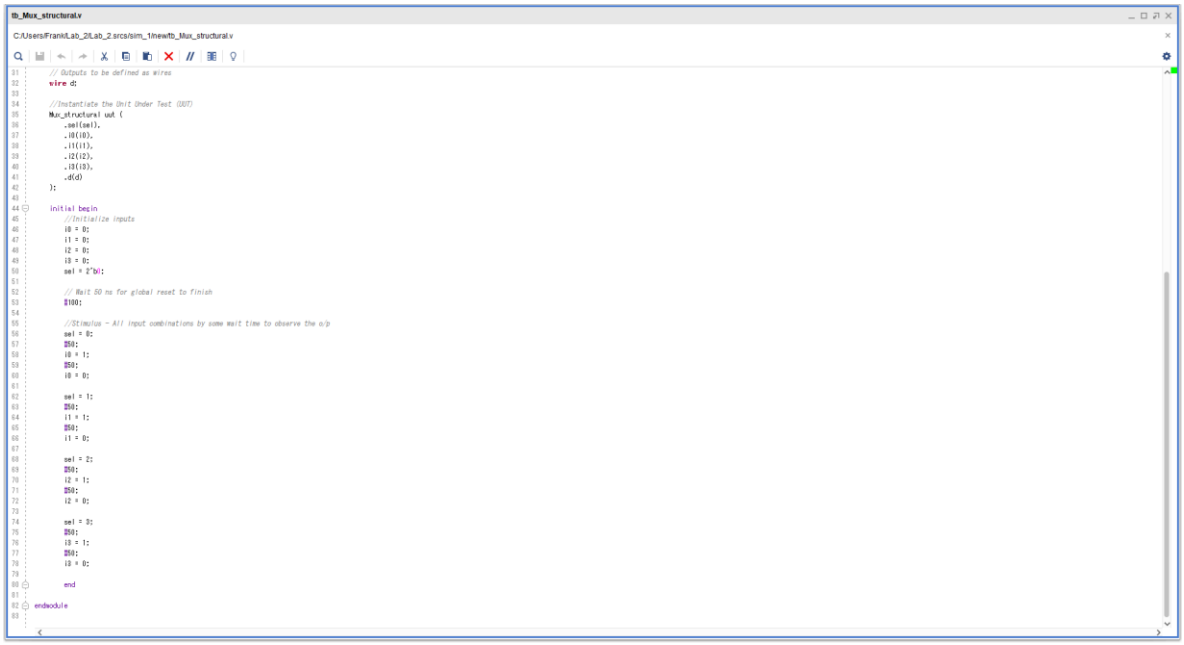
## v) Mux Structural Module Verilog code



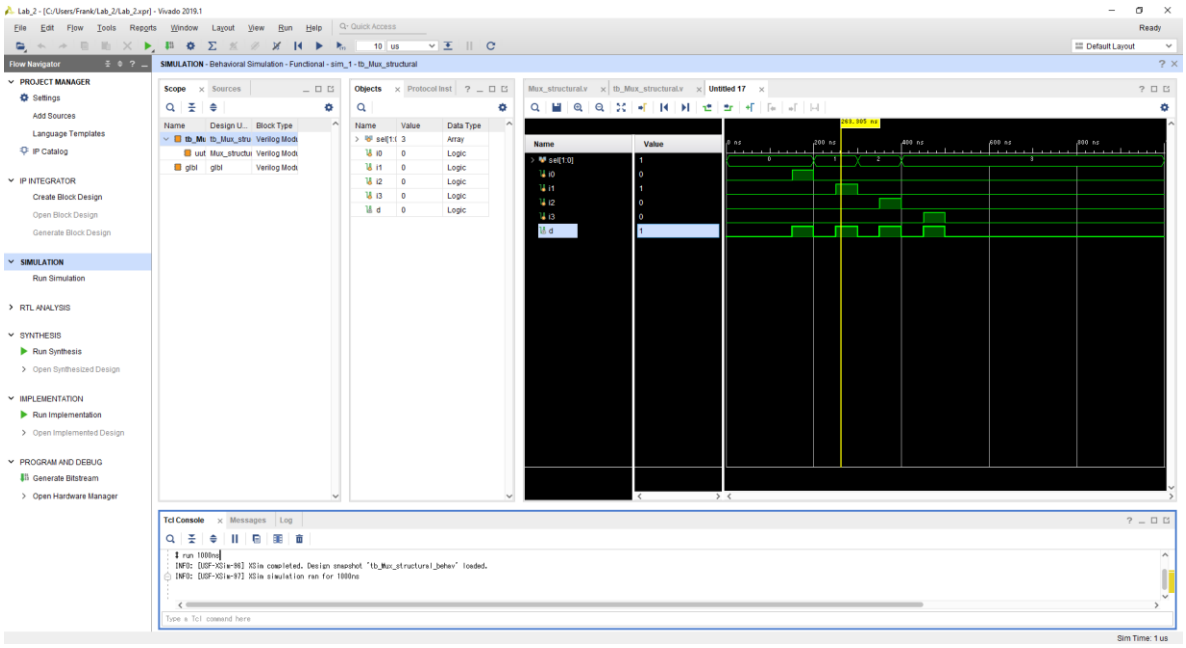
```
Mux_structural.v
C:/Users/Frank/Lab_2/Lab_2.srcs/sources_1/new/Mux_structural.v

//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer: Frank Le
//
// Create Date: 09/16/2019 07:09:31 PM
// Design Name:
// Module Name: Mux_structural
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
`timescale 1ns / 1ps

module Mux_structural(
    input [1:0] sel,
    input i0,
    input i1,
    input i2,
    input i3,
    output d
    );

    // Defining wires
    wire [1:0] sel_not;
    wire x0, x1, x2, x3;

    // Instantiating Not gates as per the schematic
    not n1 (sel_not[0], sel[0]);
    not n2 (sel_not[1], sel[1]);

    // Instantiating And gates as per the schematic

    and and0 (x0, i0, sel_not[1], sel_not[0]);
    and and1 (x1, i1, sel_not[1], sel[0]);
    and and2 (x2, i2, sel[1], sel_not[0]);
    and and3 (x3, i3, sel[1], sel[0]);

    //Instantiating Or gates as per schematic
    or or1 (d, x0, x1, x2, x3);

endmodule
```

## v) Mux Structural Testbench Verilog Code

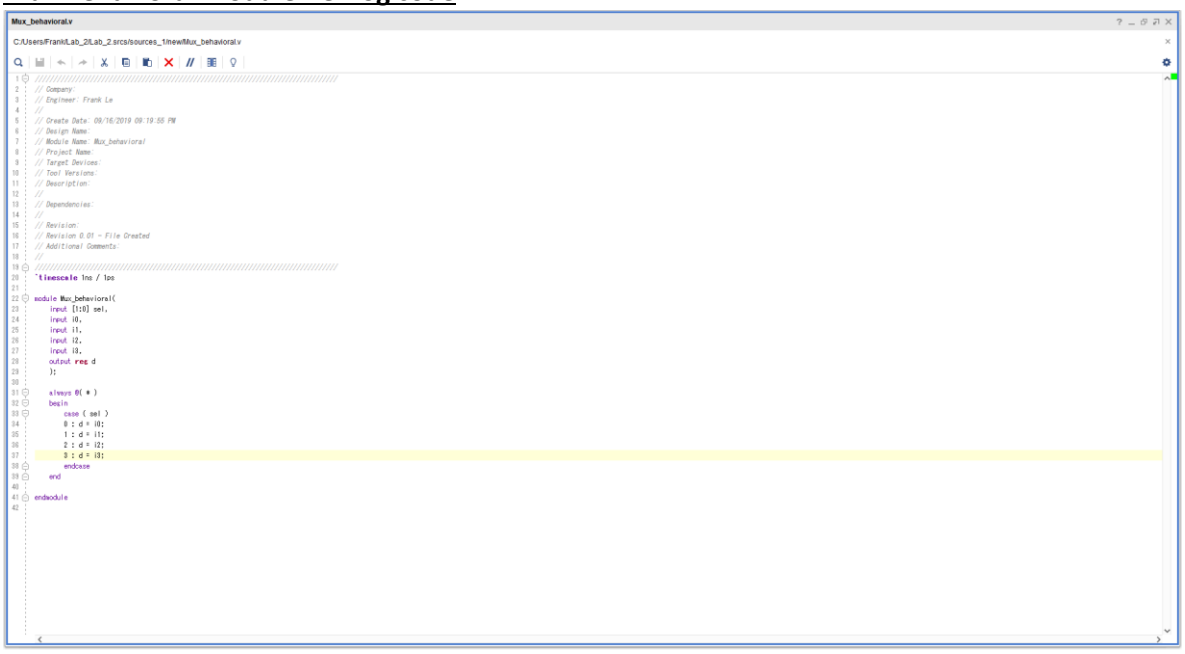
```
tb_Mux_structural.v
C:/Users/Frank/Lab_2/Lab_2.srcs/sim_1/new/tb_Mux_structural.v

//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer: Frank Le
//
// Create Date: 09/16/2019 07:28:55 PM
// Design Name:
// Module Name: tb_Mux_structural
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
`timescale 1ns / 1ps

module tb_Mux_structural;

    // Inputs to be defined as registers
    reg [1:0] sel;
    reg i0;
    reg i1;
    reg i2;
    reg i3;

    // Outputs to be defined as wires
    wire d;

    //Instantiate the Unit Under Test (UUT)
    Mux_structural uut (
        .sel(sel),
        .i0(i0),
        .i1(i1),
        .i2(i2),
        .i3(i3),
        .d(d)
    );

    initial begin
        //Initialize Inputs
        i0 = 0;
        i1 = 0;
        i2 = 0;
        i3 = 0;
        sel = 2'b0;

        // Wait 80 ns for global reset to finish
        #100;
```



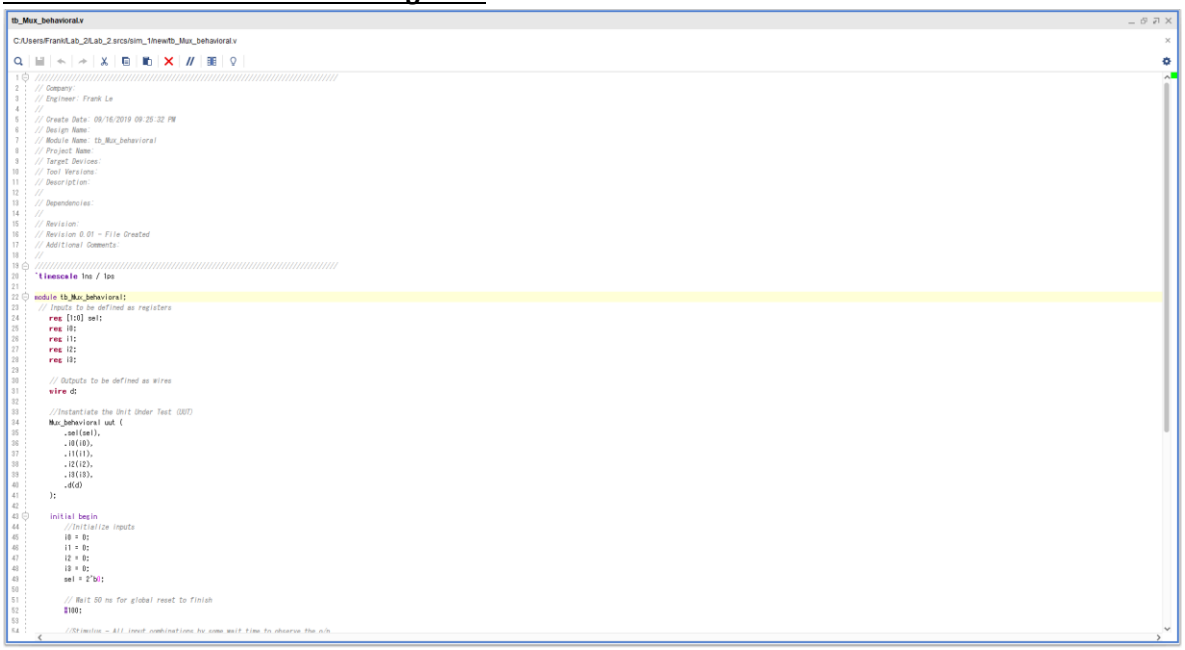

## vi) Mux Structural Waveform

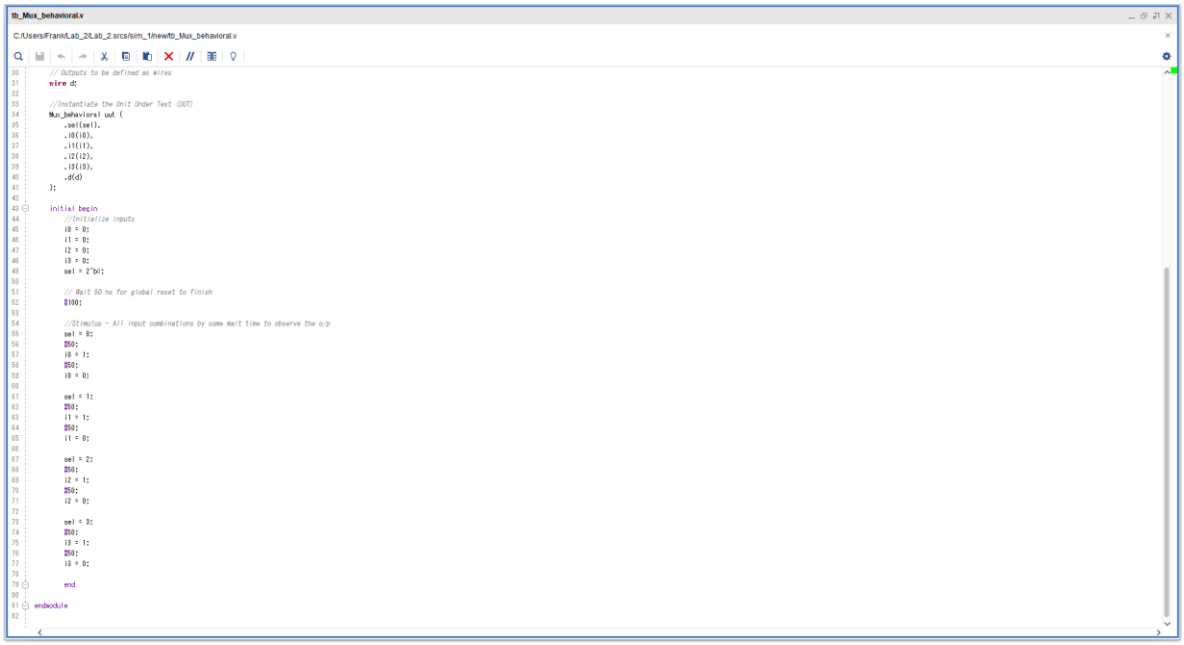


## vii) Mux Behavioral Module Verilog code




## vii) Mux Behavioral Testbench Verilog code






## viii) Mux Behavioral Waveform