Lab 3 Report

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Checklist:

Part 2 -

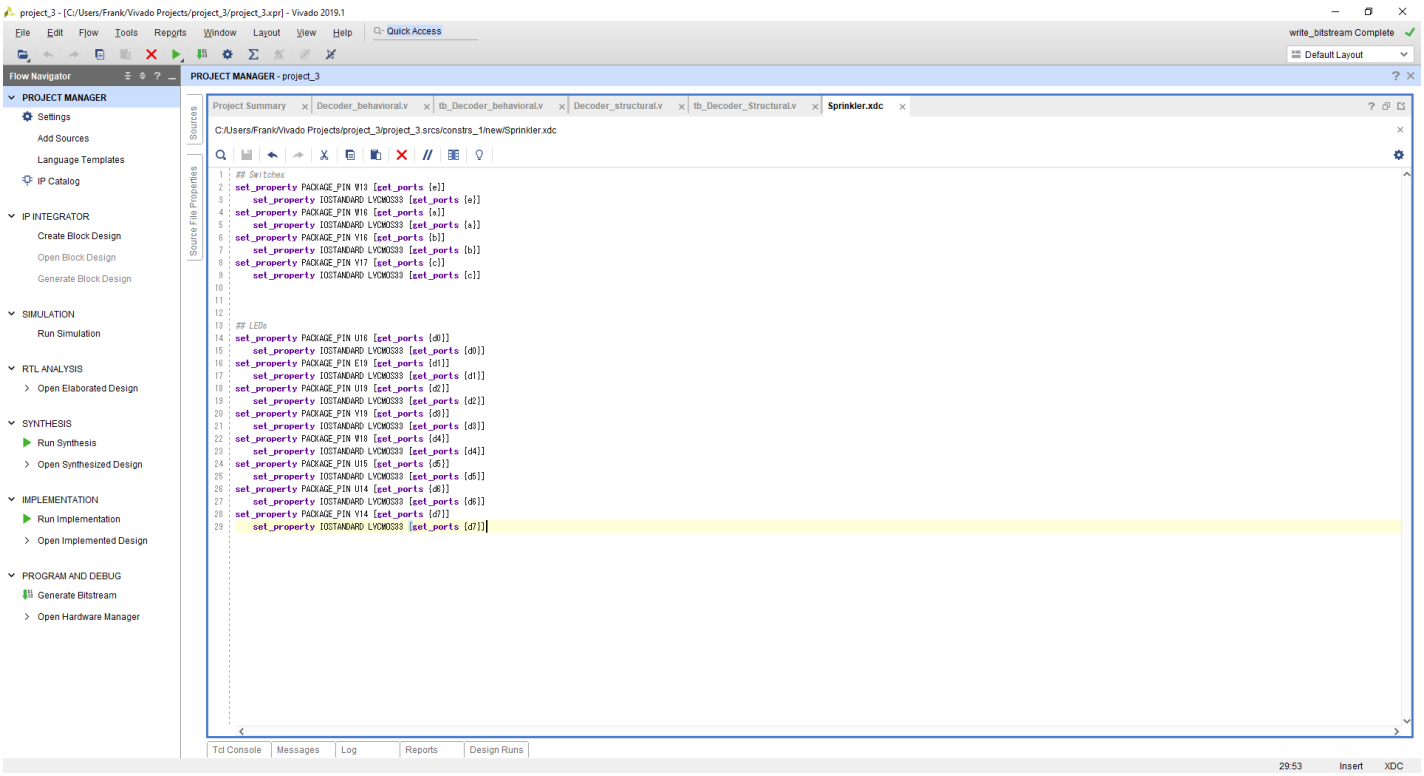
i. Constraint file (Just the uncommented portion)

Part 3 -

ii. Truth table of the function
iii. K-maps showing minimization of the logic functions (outputs)
iv. Algebraic expression of the minimized logic functions (outputs)
v. Verilog codes of module and testbench for structural modelling
vi. Simulation waveform for structural modelling
vii. Constraint file (Just the uncommented portion)

Note → *The Verilog code and the uncommented portions of the constraint files should be copied in your lab report and the actual Verilog (.v) and constraint (.xdc) files need to be zipped and submitted as well on Canvas. You are not allowed to change your Verilog code after final submission as the TAs may download the submitted codes from Canvas during checkouts. For the truth table, K-maps minimizations and algebraic expressions, you are free to draw them on paper and then put the pictures in your lab report, but please make sure it is legible for the TAs to grade it properly.*

i) Constraint File Sprinkler



ii) Truth Table

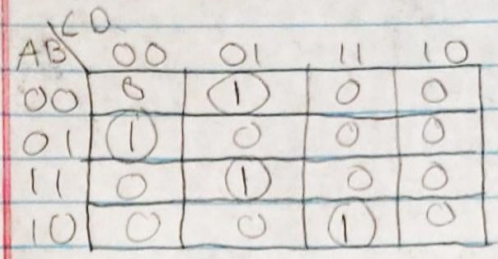
Inputs (SW[3:0])	Display (an[0])	a	b	c	d	e	f	g
0000	0	0	0	0	0	0	0	1
0001	1	1	0	0	1	1	1	1
0010	2	0	0	1	0	0	1	0
0011	3	0	0	0	0	1	1	0
0100	4	1	0	0	1	1	0	0
0101	5	0	1	0	0	1	0	0
0110	6	0	1	0	0	0	0	0
0111	7	0	0	0	1	1	1	1
1000	8	0	0	0	0	0	0	0
1001	9	0	0	0	0	1	0	0
1010	A	0	0	0	1	0	0	0
1011	b	1	1	0	0	0	0	0
1100	C	0	1	1	0	0	0	1
1101	d	1	0	0	0	0	1	0
1110	E	0	1	1	0	0	0	0
1111	F	0	1	1	1	0	0	0

iii) K-Maps

iv) Algebraic Expressions

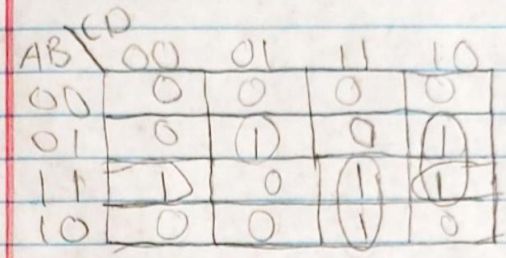
SOP & K-Maps

a



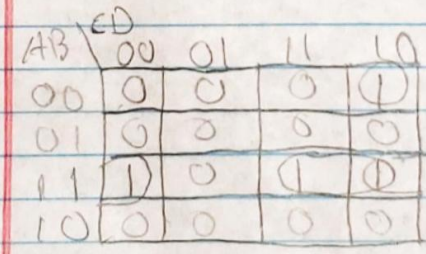
$a = A'B'C'D + A'BC'D' + ABC'D + AB'CD$

b



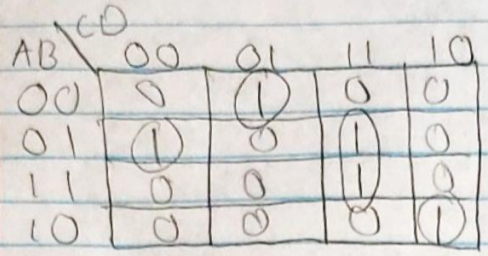
$b = A'BC'D + BCD' + ABD' + ACD$

c



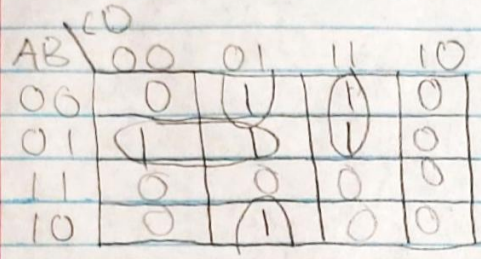
$C = A'B'CD' + ABC + ABD'$

d



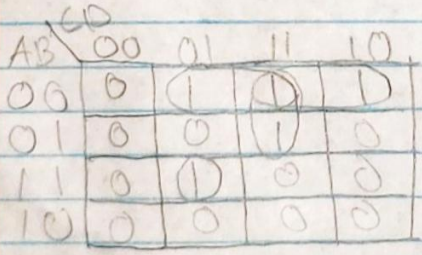
$$d = A'B'C'D + A'BC'D' + BCD + AB'CD'$$

e



$$e = B'C'D + A'BC' + A'CD$$

f



$$f = A'B'D + A'B'C + A'CD + ABC'D$$

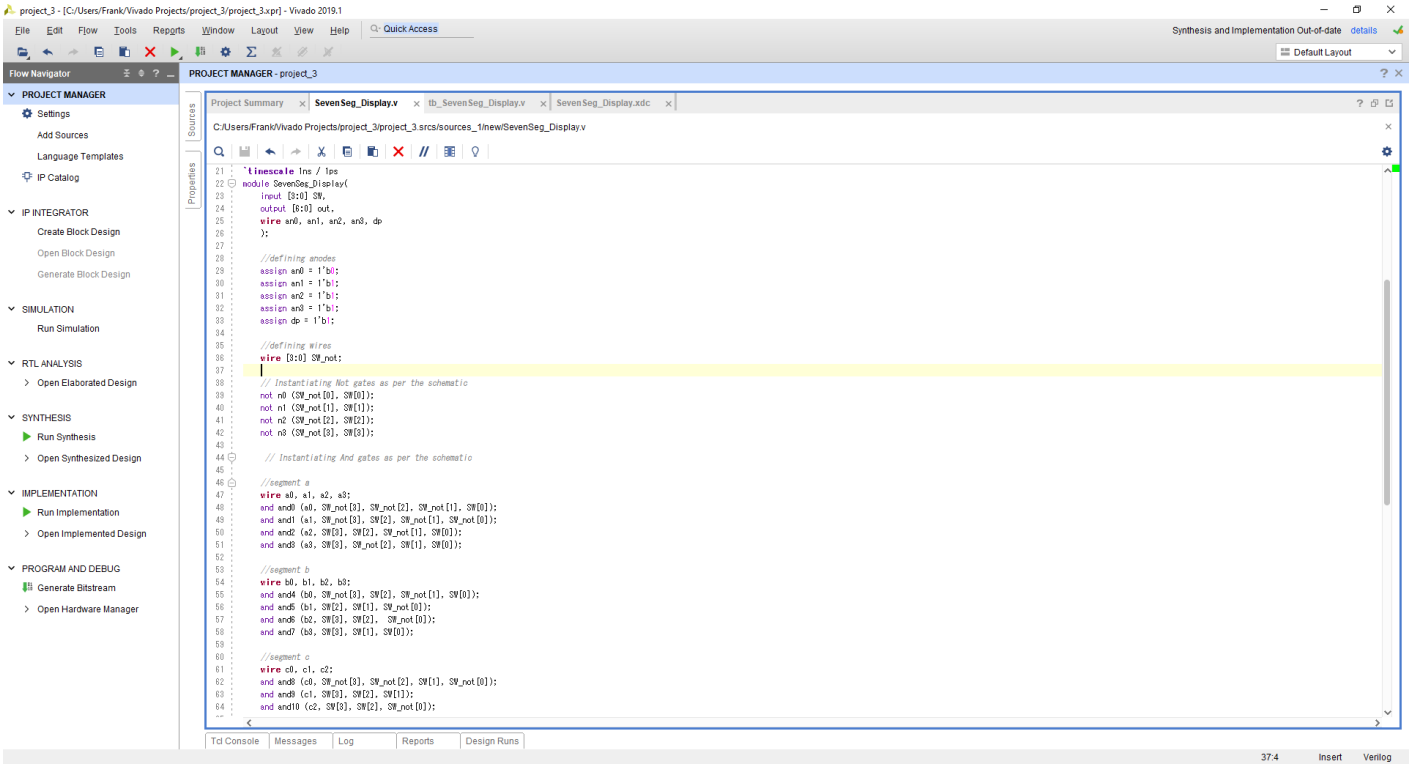
g

AB \ CD	00	01	11	10
00	1	1	0	0
01	0	0	1	0
11	1	0	0	0
10	0	0	0	0

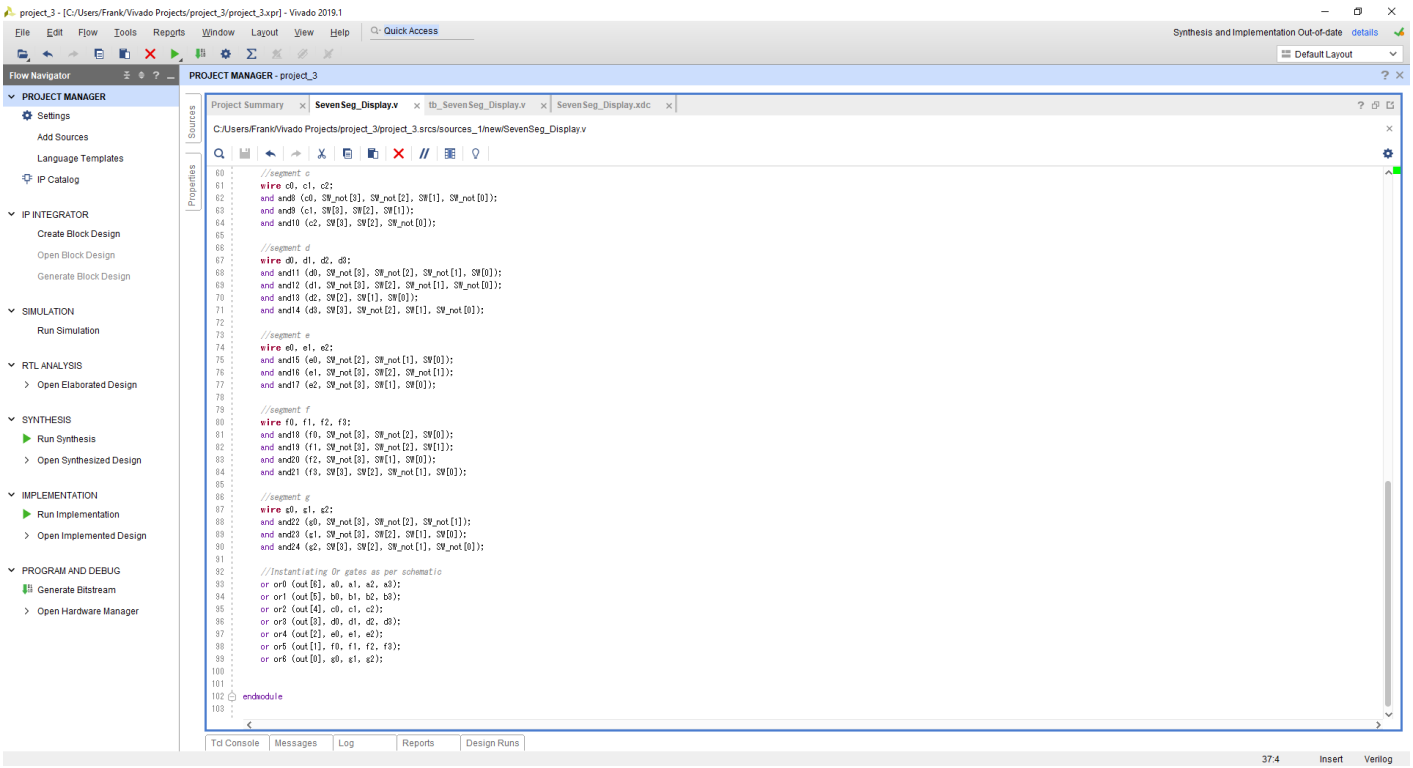
$$g = A'B'C' + A'BCD + ABC'D'$$

v) Verilog Code of Module and Testbench

Structural Module

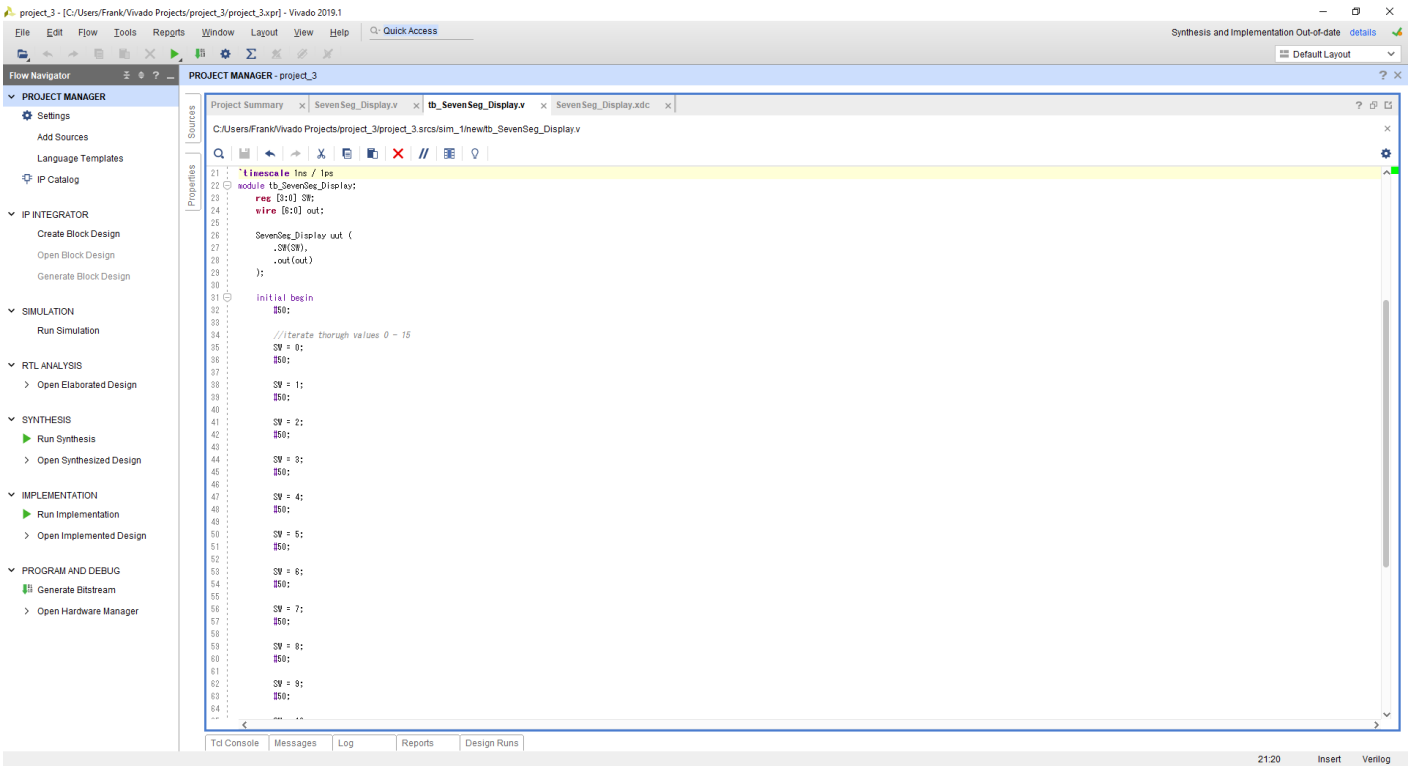


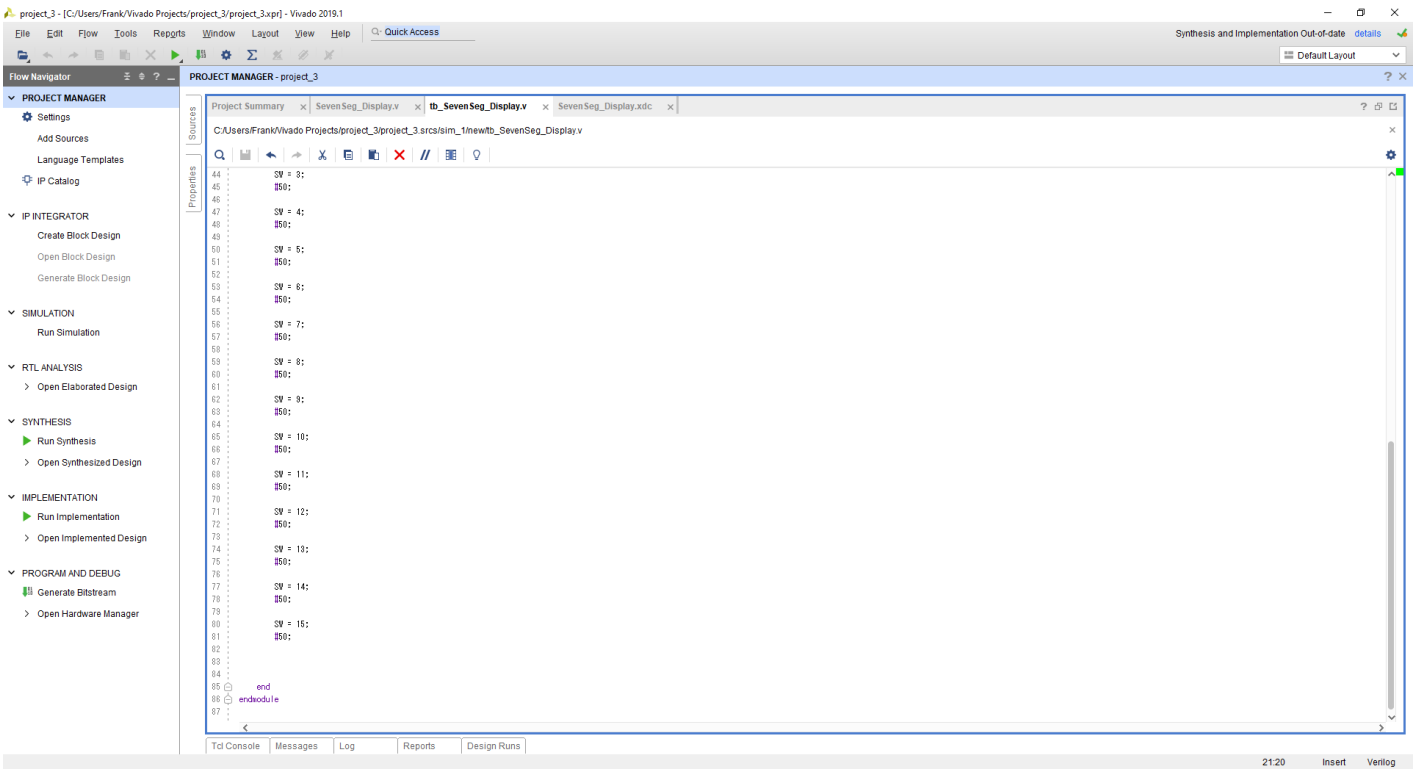
```
`timescale 1ns / 1ps
module SevenSeg_Display(
    input [3:0] SW,
    output [8:0] out,
    wire an0, an1, an2, an3, dp
    );

    //defining anodes
    assign an0 = 1'b0;
    assign an1 = 1'b1;
    assign an2 = 1'b1;
    assign an3 = 1'b1;
    assign dp = 1'b1;

    //defining wires
    wire [3:0] SW_not;

    // Instantiating Not gates as per the schematic
    not n0 (SW_not[0], SW[0]);
    not n1 (SW_not[1], SW[1]);
    not n2 (SW_not[2], SW[2]);
    not n3 (SW_not[3], SW[3]);

     // Instantiating And gates as per the schematic

    //segment a
    wire a0, a1, a2, a3;
    and and0 (a0, SW_not[3], SW_not[2], SW_not[1], SW[0]);
    and and1 (a1, SW_not[3], SW[2], SW_not[1], SW_not[0]);
    and and2 (a2, SW[3], SW[2], SW_not[1], SW[0]);
    and and3 (a3, SW[3], SW_not[2], SW[1], SW[0]);

    //segment b
    wire b0, b1, b2, b3;
    and and4 (b0, SW_not[3], SW[2], SW_not[1], SW[0]);
    and and5 (b1, SW[2], SW[1], SW_not[0]);
    and and6 (b2, SW[3], SW[2],  SW_not[0]);
    and and7 (b3, SW[3], SW[1], SW[0]);

    //segment c
    wire c0, c1, c2;
    and and8 (c0, SW_not[3], SW_not[2], SW[1], SW_not[0]);
    and and9 (c1, SW[3], SW[2], SW[1]);
    and and10 (c2, SW[3], SW[2], SW_not[0]);
```



```
    //segment c
    wire c0, c1, c2;
    and and8 (c0, SW_not[3], SW_not[2], SW[1], SW_not[0]);
    and and9 (c1, SW[3], SW[2], SW[1]);
    and and10 (c2, SW[3], SW[2], SW_not[0]);

    //segment d
    wire d0, d1, d2, d3;
    and and11 (d0, SW_not[3], SW_not[2], SW_not[1], SW[0]);
    and and12 (d1, SW_not[3], SW[2], SW_not[1], SW_not[0]);
    and and13 (d2, SW[2], SW[1], SW[0]);
    and and14 (d3, SW[3], SW_not[2], SW[1], SW_not[0]);

    //segment e
    wire e0, e1, e2;
    and and15 (e0, SW_not[2], SW_not[1], SW[0]);
    and and16 (e1, SW_not[3], SW[2], SW_not[1]);
    and and17 (e2, SW_not[3], SW[1], SW[0]);

    //segment f
    wire f0, f1, f2, f3;
    and and18 (f0, SW_not[3], SW_not[2], SW[0]);
    and and19 (f1, SW_not[3], SW_not[2], SW[1]);
    and and20 (f2, SW_not[3], SW[1], SW[0]);
    and and21 (f3, SW[3], SW[2], SW_not[1], SW[0]);

    //segment g
    wire g0, g1, g2;
    and and22 (g0, SW_not[3], SW_not[2], SW_not[1]);
    and and23 (g1, SW_not[3], SW[2], SW[1], SW[0]);
    and and24 (g2, SW[3], SW[2], SW_not[1], SW_not[0]);

    //Instantiating Or gates as per schematic
    or or0 (out[6], a0, a1, a2, a3);
    or or1 (out[5], b0, b1, b2, b3);
    or or2 (out[4], c0, c1, c2);
    or or3 (out[3], d0, d1, d2, d3);
    or or4 (out[2], e0, e1, e2);
    or or5 (out[1], f0, f1, f2, f3);
    or or6 (out[0], g0, g1, g2);


endmodule
```

Testbench


project_3 - [C:/Users/Frank/Vivado Projects/project_3/project_3.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Synthesis and Implementation Out-of-date details
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
PROJECT MANAGER - project_3
Project Summary
SevenSeg_Display.v
tb_SevenSeg_Display.v
SevenSeg_Display.xdc
C:/Users/Frank/Vivado Projects/project_3/project_3.srcs/sim_1/new/tb_SevenSeg_Display.v
Sources
Properties
`timescale 1ns / 1ps
module tb_SevenSeg_Display;
reg [3:0] SW;
wire [6:0] out;
SevenSeg_Display uut (
.SW(SW),
.out(out)
);
initial begin
#50;
//iterate thorugh values 0 - 15
SW = 0;
#50;
SW = 1;
#50;
SW = 2;
#50;
SW = 3;
#50;
SW = 4;
#50;
SW = 5;
#50;
SW = 6;
#50;
SW = 7;
#50;
SW = 8;
#50;
SW = 9;
#50;
Tcl Console
Messages
Log
Reports
Design Runs
21:20
Insert
Verilog


project_3 - [C:/Users/Frank/Vivado Projects/project_3/project_3.xpr] - Vivado 2019.1
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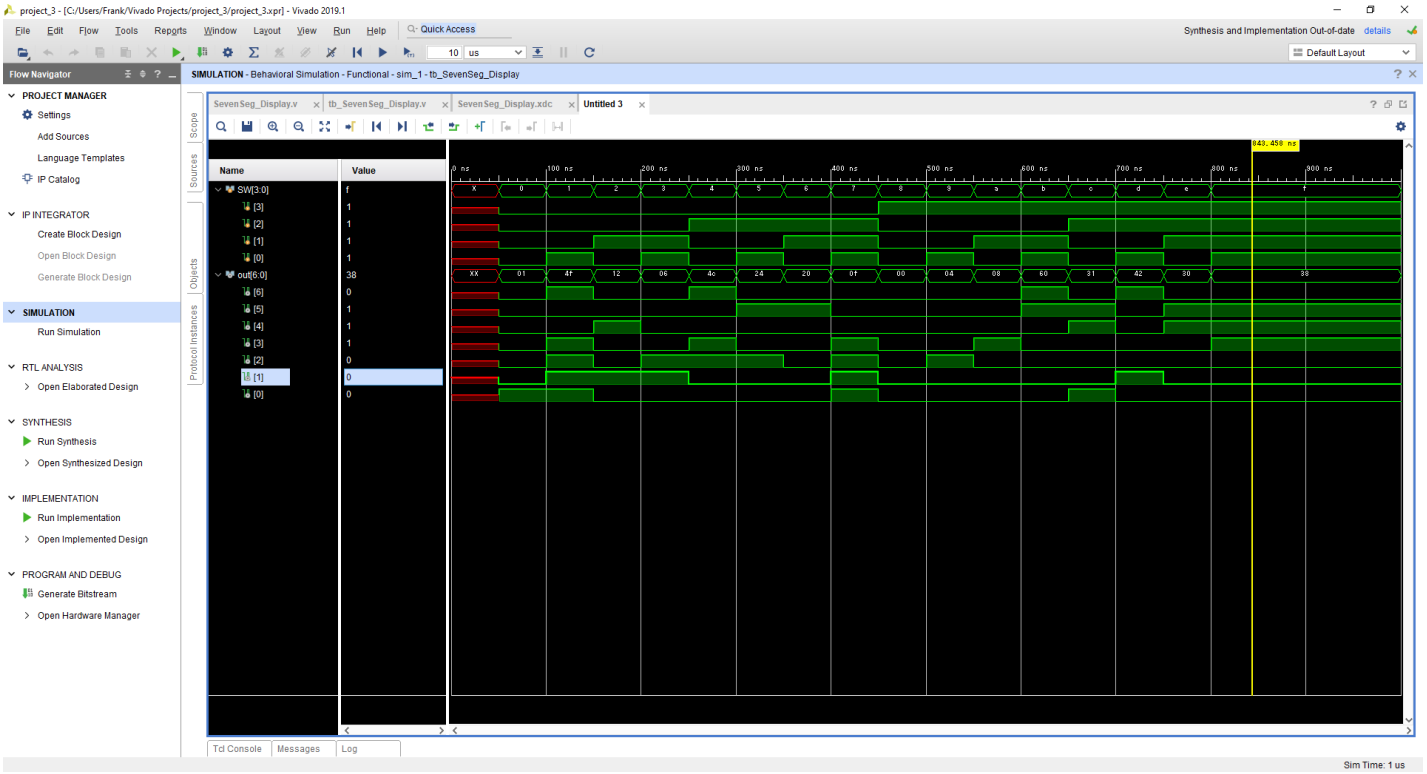
PROJECT MANAGER - project_3
Project Summary
SevenSeg_Display.v
tb_SevenSeg_Display.v
SevenSeg_Display.xdc
C:/Users/Frank/Vivado Projects/project_3/project_3.srcs/sim_1/new/tb_SevenSeg_Display.v
Sources
Properties
SW = 3;
#50;
SW = 4;
#50;
SW = 5;
#50;
SW = 6;
#50;
SW = 7;
#50;
SW = 8;
#50;
SW = 9;
#50;
SW = 10;
#50;
SW = 11;
#50;
SW = 12;
#50;
SW = 13;
#50;
SW = 14;
#50;
SW = 15;
#50;
end
endmodule
Tcl Console
Messages
Log
Reports
Design Runs
21:20
Insert
Verilog

vi) Simulation Waveform



vii) Constraint File Seven Segment Display