

# Lab 2 Report

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**UT EID: fpl227**

**Section: Tuesday 2 – 3 p.m. (16100)**

## Checklist:

### Part 1 –

- i. Simulation waveforms for Part 1 for Structural as well as Behavioral modelling (Screenshots)

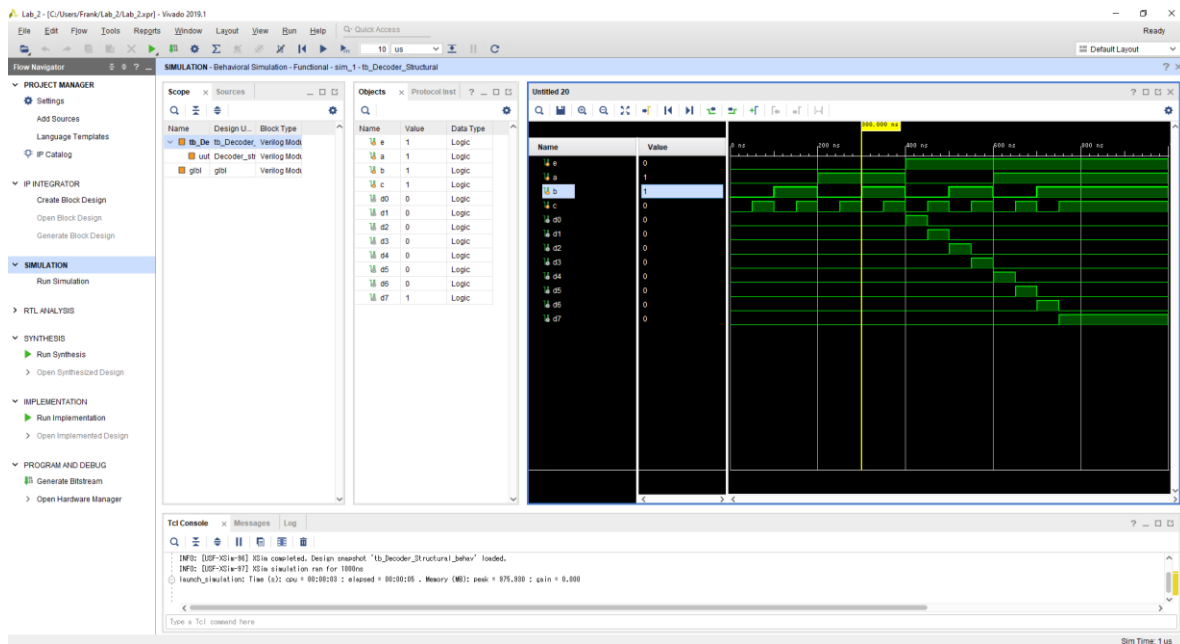
### Part 2 –

- ii. Truth table of the function
- iii. Algebraic expression of the logic function
- iv. Logic circuit schematic
- v. Verilog codes for module and testbench for structural modelling
- vi. Simulation waveform for structural modelling (Screenshot)
- vii. Verilog codes for module and testbench for behavioral modelling
- viii. Simulation waveform for behavioral modelling (Screenshot)

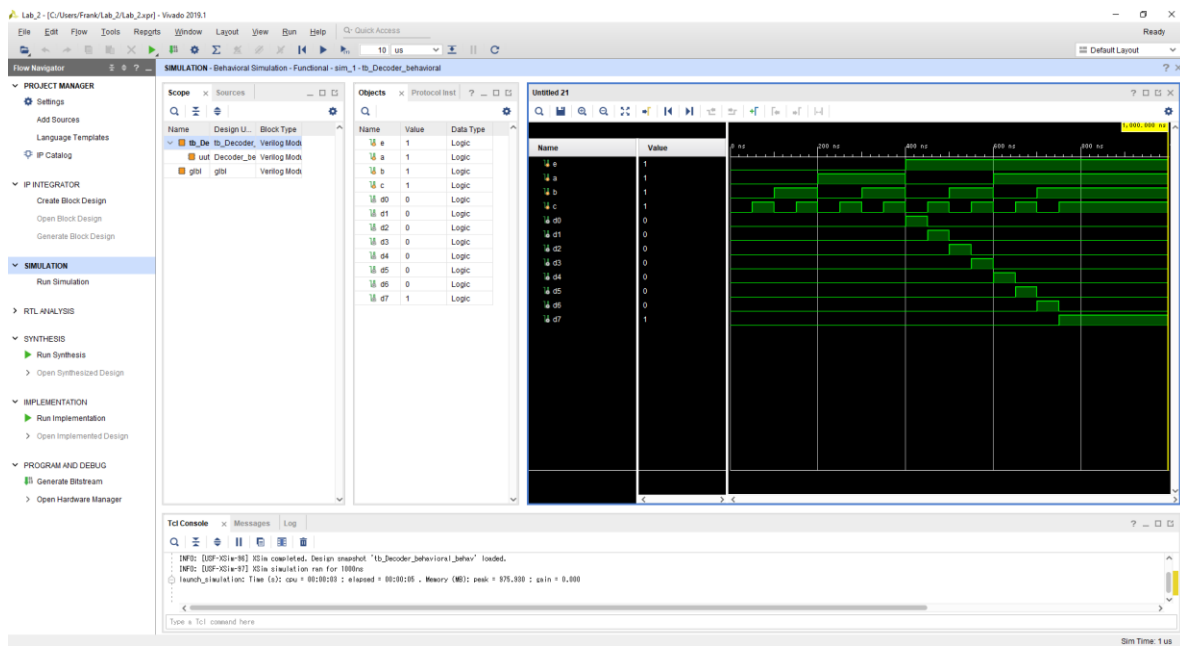
**Note** → The Verilog codes should be copied in your lab report, and the actual Verilog (.v) files need to be zipped and submitted as well on Canvas. You are not allowed to change your Verilog codes after final submission as the TAs may download the submitted codes from Canvas during checkouts. For the truth table, algebraic expression and circuit schematic, you are free to draw it on paper and then put the pictures in your lab report, but please make sure it is legible for the TAs to grade it properly.

## Part 1)

### i) Decoder Structural Waveform



### i) Decoder Behavioral Waveform



## Part 2)

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### Lab 2 Part 2

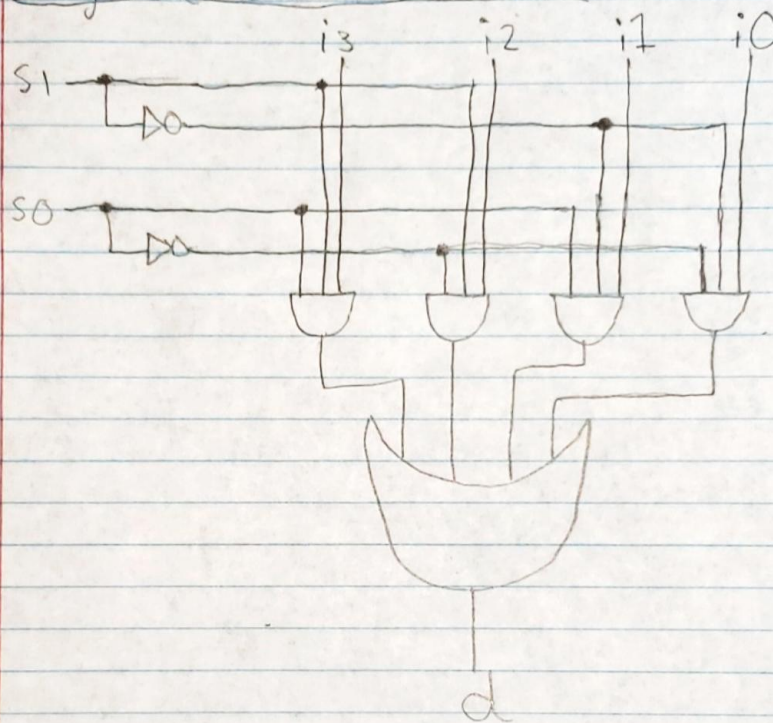
#### ii) Truth Table

$s_1$	$s_0$	$d$
0	0	$i_0$
0	1	$i_1$
1	0	$i_2$
1	1	$i_3$

#### iii) Algebraic Expression

$$d = s_1's_0'i_0 + s_1's_0i_1 + s_1s_0'i_2 + s_1s_0i_3$$

#### iv) Logic Circuit schematic



## v) Mux Structural Module Verilog code

```
Mux_structural.v
C:\Users\Frank.Lab_2\srcs\srcs_tnew\Mux_structural.v

1 // Company:
2 // Engineer: Frank Le
3 //
4 // Create Date: 09/16/2019 07:09:31 PM
5 // Design Name:
6 // Module Name: Mux_structural
7 // Project Name:
8 // Target Devices:
9 // Tool Versions:
10 // Description:
11 //
12 // Dependencies:
13 //
14 //
15 // Revision:
16 // Revision 0.01 - File Created
17 // Additional Comments:
18 //
19 //=====
20 //timescale 1ns / 1ps
21 //
22 module Mux_structural(
23     input [1:0] sel,
24     input i0,
25     input i1,
26     input i2,
27     input i3,
28     output d
29 );
30 //
31 // Defining wires
32 wire [1:0] sel_not;
33 wire a0, a1, a2, a3;
34 //
35 // Instantiating Not gates as per the schematic
36 not n0(sel_not[0], sel[0]);
37 not n1(sel_not[1], sel[1]);
38 //
39 // Instantiating And gates as per the schematic
40 and a0(i0, sel_not[0], sel_not[1]);
41 and a1(i1, sel_not[0], sel[0]);
42 and a2(i2, sel[1], sel_not[0]);
43 and a3(i3, sel[1], sel[0]);
44 //Instantiating Or gates as per schematic
45 or o0(a0, a1, a2, a3);
46 endmodule
```

## v) Mux Structural Testbench Verilog Code

```
tb_Mux_structural.v
C:\Users\Frank.Lab_2\srcs\srcs_tnew\tb_Mux_structural.v

1 // Company:
2 // Engineer: Frank Le
3 //
4 // Create Date: 09/16/2019 07:28:55 PM
5 // Design Name:
6 // Module Name: tb_Mux_structural
7 // Project Name:
8 // Target Devices:
9 // Tool Versions:
10 // Description:
11 //
12 // Dependencies:
13 //
14 //
15 // Revision:
16 // Revision 0.01 - File Created
17 // Additional Comments:
18 //
19 //=====
20 //timescale 1ns / 1ps
21 //
22 module tb_Mux_structural;
23 //
24 // Inputs to be defined as registers
25 reg [1:0] sel;
26 reg i0;
27 reg i1;
28 reg i2;
29 reg i3;
30 //
31 // Outputs to be defined as wires
32 wire d;
33 //
34 //Instantiate the Unit Under Test (UUT)
35 Mux_structural uut (
36     .sel(sel),
37     .i0(i0),
38     .i1(i1),
39     .i2(i2),
40     .i3(i3),
41     .d(d)
42 );
43 //
44 initial begin
45     //Initialize inputs
46     i0 = 0;
47     i1 = 0;
48     i2 = 0;
49     i3 = 0;
50     sel = 2'b01;
51 //
52 // Wait 50 ns for global reset to finish
53 #50;
54 end
```

```

tb_mux_structural.v
C:\Users\Frank\Lab_2\src\sim_1\tb_mux_structural.v

// Outputs to be defined as wires
wire d;

// Instantiate the Unit Under Test (UUT)
tb_mux_structural uut (
    .sel(sel),
    .i0(i0),
    .i1(i1),
    .i2(i2),
    .i3(i3),
    .d(d)
);

initial begin
    // Initialize inputs
    i0 = 0;
    i1 = 0;
    i2 = 0;
    i3 = 0;
    sel = 2'b0;

    // Wait 50 ns for global reset to finish
    #50;

    // Stimulus - All input combinations by some wait time to observe the o/p
    sel = 0;
    #50;
    i0 = 1;
    #50;
    i0 = 0;

    sel = 1;
    #50;
    i1 = 1;
    #50;
    i1 = 0;

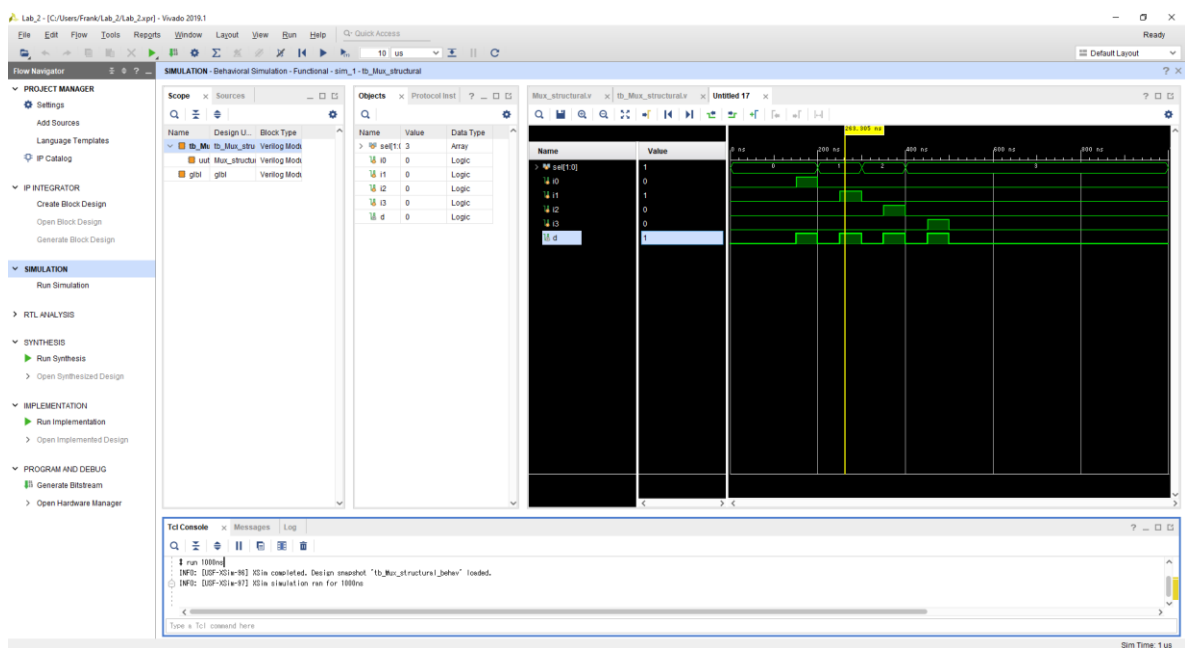
    sel = 2;
    #50;
    i2 = 1;
    #50;
    i2 = 0;

    sel = 3;
    #50;
    i3 = 1;
    #50;
    i3 = 0;

    end
endmodule

```

## vi) Mux Structural Waveform



## vii) Mux Behavioral Module Verilog code

```
Mux_behavioral.v
C:\Users\FrankLab_2\Lab_2\srcs\srcs_1\newMux_behavioral.v

1 // Company:
2 // Engineer: Frank Le
3 //
4 // Create Date: 09/16/2019 09:19:55 PM
5 // Design Name:
6 // Module Name: Mux_behavioral
7 // Project Name:
8 // Target Device:
9 // Tool Versions:
10 // Description:
11 //
12 // Dependencies:
13 //
14 // Revision:
15 // Revision 0.01 - File Created
16 // Additional Comments:
17 //
18 ////////////////////////////////////////////////////////////////////////////////////
19 //
20 //timescale 1ns / 1ps
21 //
22 module Mux_behavioral(
23     input [1:0] sel,
24     input i0,
25     input i1,
26     input i2,
27     input i3,
28     output reg d
29 )
30
31     always @( * )
32     begin
33         case (sel)
34             0 : d = i0;
35             1 : d = i1;
36             2 : d = i2;
37             3 : d = i3;
38         endcase
39     end
40
41 endmodule
42
```

## vii) Mux Behavioral Testbench Verilog code

```
tb_Mux_behavioral.v
C:\Users\FrankLab_2\Lab_2\srcs\srcs_1\newMux_behavioral.v

1 // Company:
2 // Engineer: Frank Le
3 //
4 // Create Date: 09/16/2019 09:25:32 PM
5 // Design Name:
6 // Module Name: tb_Mux_behavioral
7 // Project Name:
8 // Target Device:
9 // Tool Versions:
10 // Description:
11 //
12 // Dependencies:
13 //
14 // Revision:
15 // Revision 0.01 - File Created
16 // Additional Comments:
17 //
18 ////////////////////////////////////////////////////////////////////////////////////
19 //
20 //timescale 1ns / 1ps
21 //
22 module tb_Mux_behavioral(
23     // Inputs to be defined as registers
24     reg i0;
25     reg i1;
26     reg i2;
27     reg i3;
28
29     // Outputs to be defined as wires
30     wire d;
31
32     //Instantiate the Unit Under Test (UUT)
33     Mux_behavioral uut (
34         .sel(sel),
35         .i0(i0),
36         .i1(i1),
37         .i2(i2),
38         .i3(i3),
39         .d(d)
40     );
41
42     initial begin
43         //Initialize inputs
44         i0 = 0;
45         i1 = 0;
46         i2 = 0;
47         i3 = 0;
48         sel = 2'b1;
49
50         // Wait 50 ns for global reset to finish
51         #100;
52
53         //Stimulus - All input combinations for some wait time to observe the o/c.
54     end
55
```

```

tb_mux_behavioral.v
C:\Users\Frank\Lab_2\src\sim_1\src\tb_mux_behavioral.v

// Outputs to be defined as wires
wire d;

// Instantiate the Unit Under Test (UUT)
Mux_behavioral uut (
    .sel(sel),
    .i0(i0),
    .i1(i1),
    .i2(i2),
    .i3(i3),
    .d(d)
);

initial begin
    // Initialize inputs
    i0 = 0;
    i1 = 0;
    i2 = 0;
    i3 = 0;
    sel = 2'b0;

    // Wait 50 ns for global reset to finish
    #50;

    // Stimulus - All input combinations by some wait time to observe the o/p
    sel = 0;
    #50;
    i0 = 1;
    #50;
    i0 = 0;

    sel = 1;
    #50;
    i1 = 1;
    #50;
    i1 = 0;

    sel = 2;
    #50;
    i2 = 1;
    #50;
    i2 = 0;

    sel = 3;
    #50;
    i3 = 1;
    #50;
    i3 = 0;

    end
endmodule

```

### viii) Mux Behavioral Waveform

