Lab 5 Report

Name: Frank Le

UT EID: fpl227

Section #: 16100

Checklist:

Part 1 –

i. Design files (.v) for RCA and load register
ii. Completed testcase table
iii. Testbench and simulation waveform for the testcases in the table
iv. Constraints File (Just the uncommented portion)

Part 2 –

v. All the equations for C_i's and S_i's
vi. Design file (.v) for the CLA
vii. Constraints File (Just the uncommented portion)
viii. Simulation waveform for the testcases in the table

Part 3 –

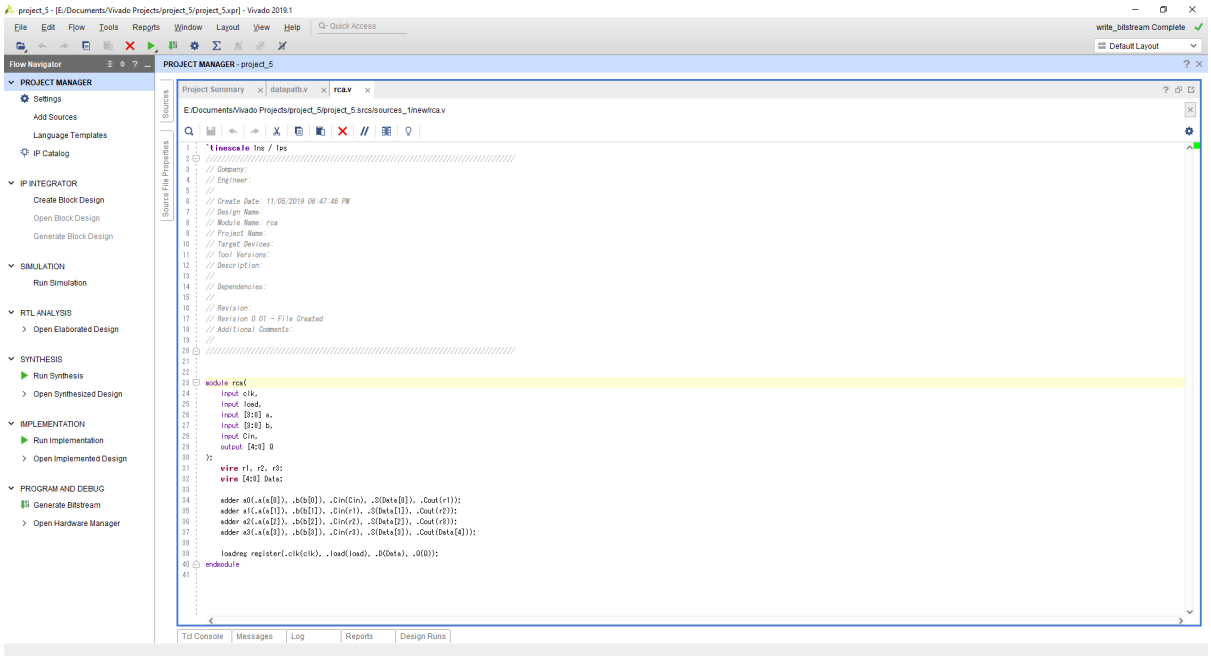
ix. High-level block diagram of system
x. Design file for datapath.v
xi. Testbench and simulation waveform
xii. Screenshot of full circuit and each adder module
xiii. Calculations of delay and area for each adder

***Note** –> The Verilog codes and the uncommented portions of the constraint files should be copied in your lab report and the **actual Verilog (.v), Constraint (.xdc) files and Bitstream (.bit) files** need to be zipped and submitted as well on Canvas. You are not allowed to change your codes after final submission as the*

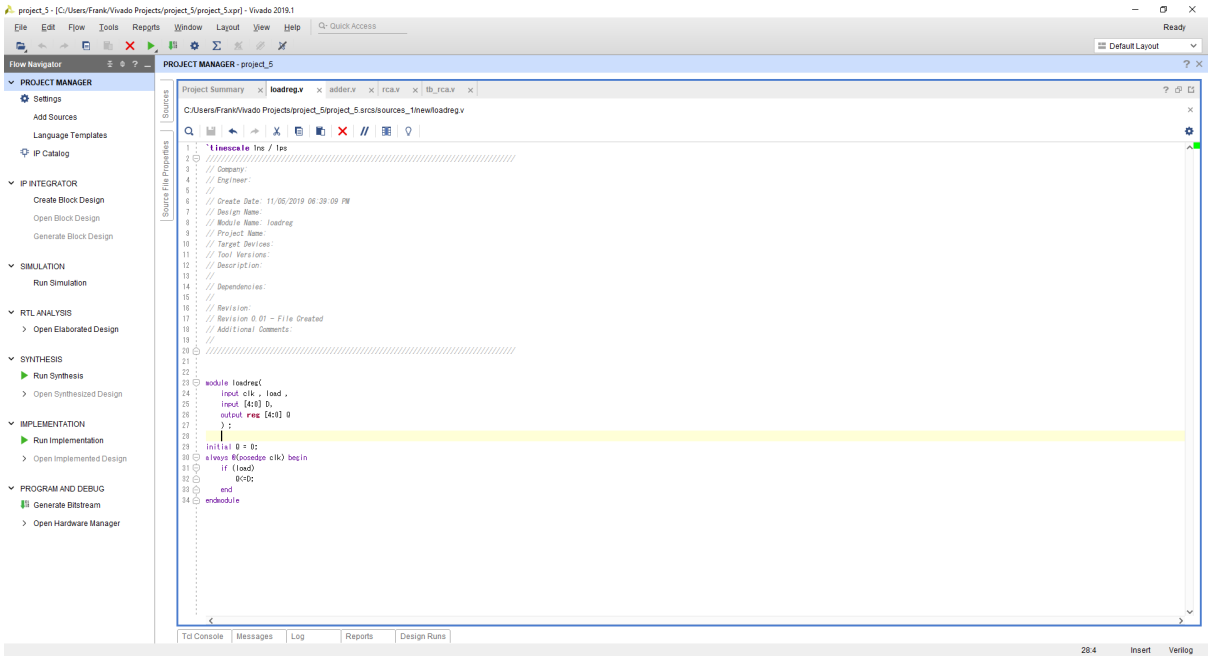
TAs may download the submitted codes or bitstream files from Canvas during checkouts. For the truth Table, K-maps minimizations and algebraic expressions, you are free to draw them on paper and then put the pictures in your lab report, but please make sure it is legible for the TAs to grade it properly.

i) Design files (.v) for RCA and load register

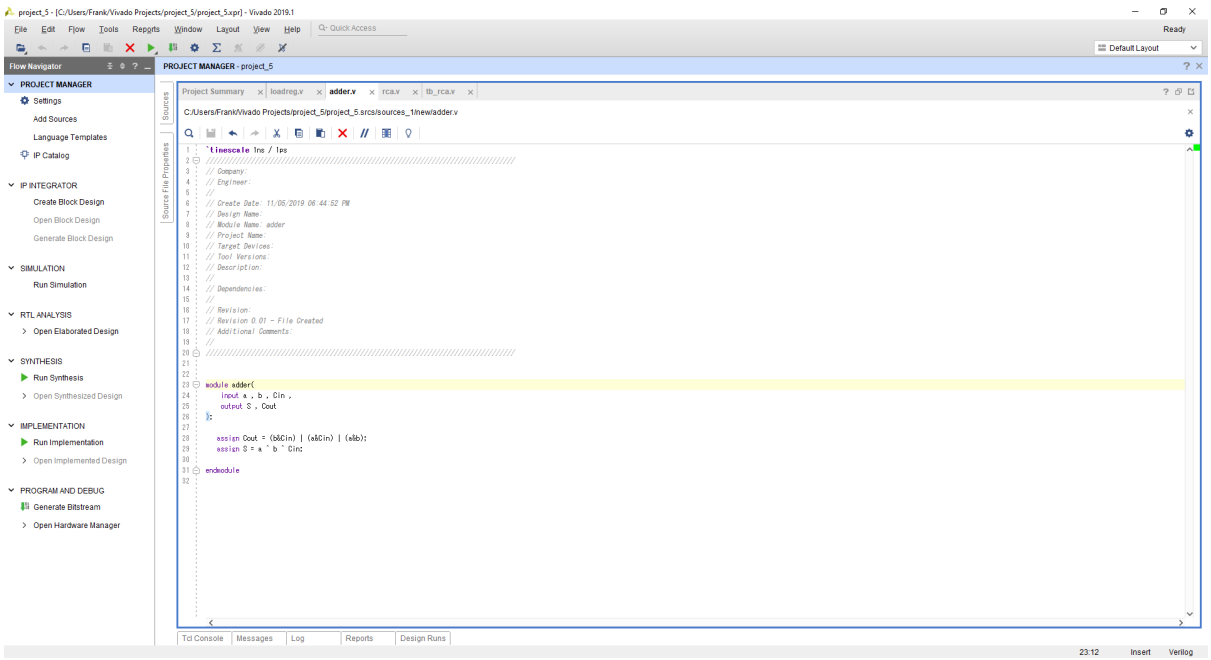
RCA:



Load Register:



Full Adder:

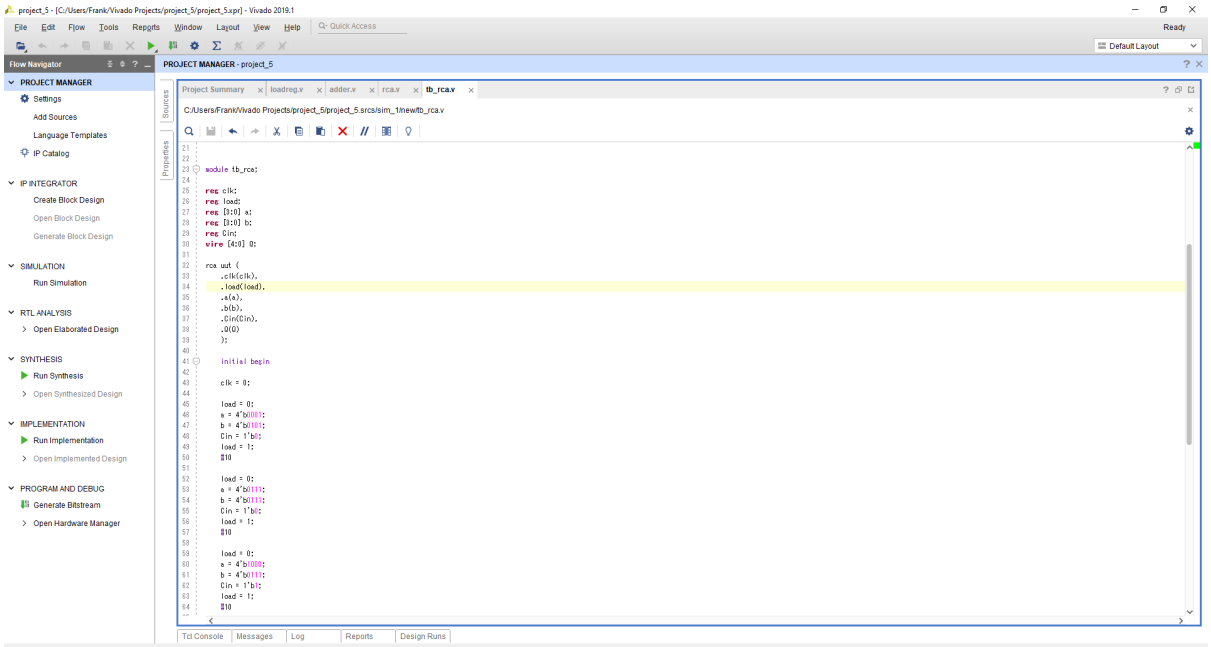


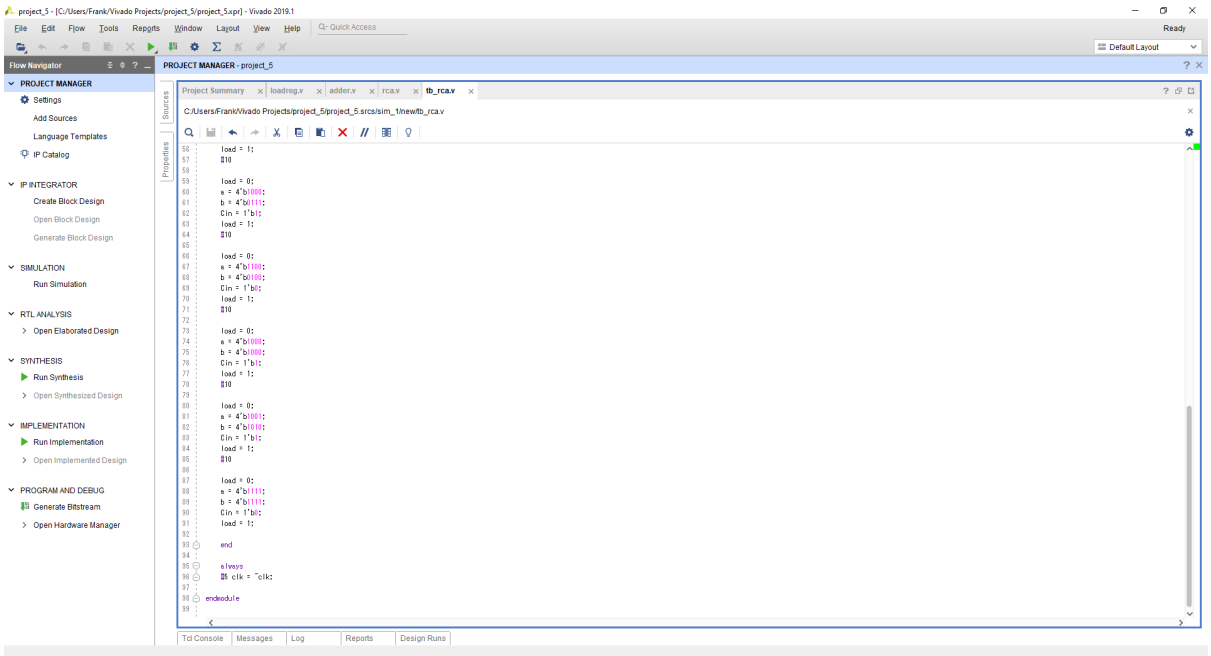
ii) Completed testcase table

a[3:0]	b[3:0]	Cin	S	Cout
0001	0101	0	0110	0
0111	0111	0	1110	0
1000	0111	1	0000	1
1100	0100	0	0000	1
1000	1000	1	0001	1
1001	1010	1	0100	1
1111	1111	0	1110	1

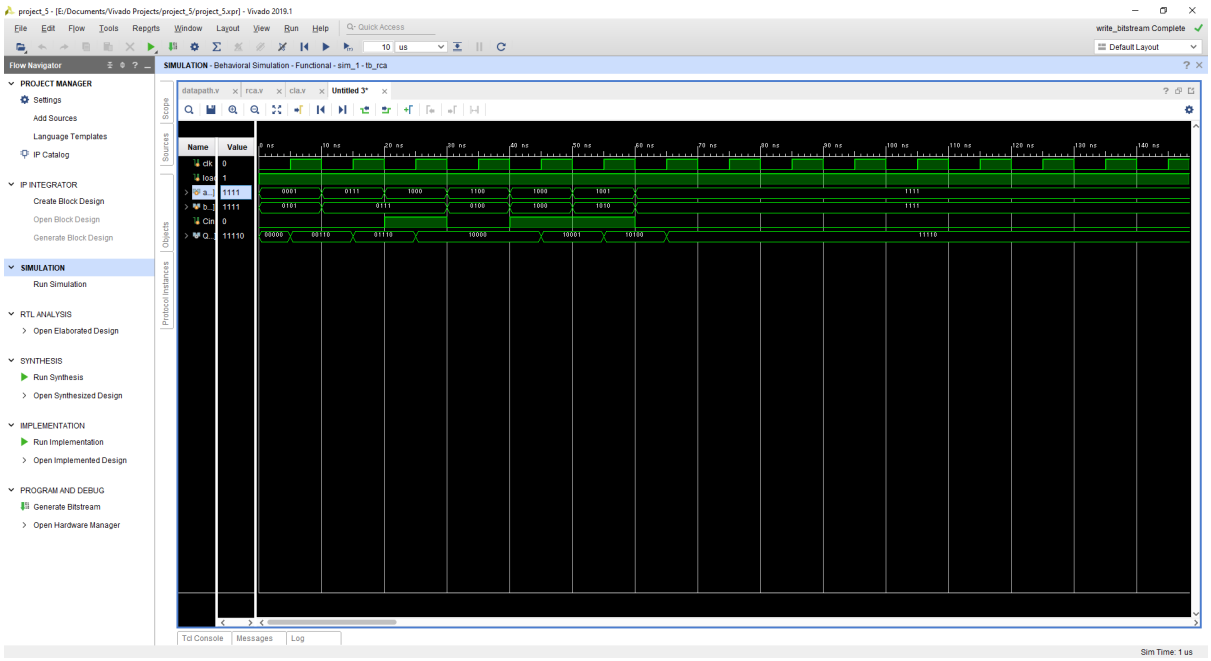
iii) Testbench and simulation waveform for the testcases in the table

Testbench:

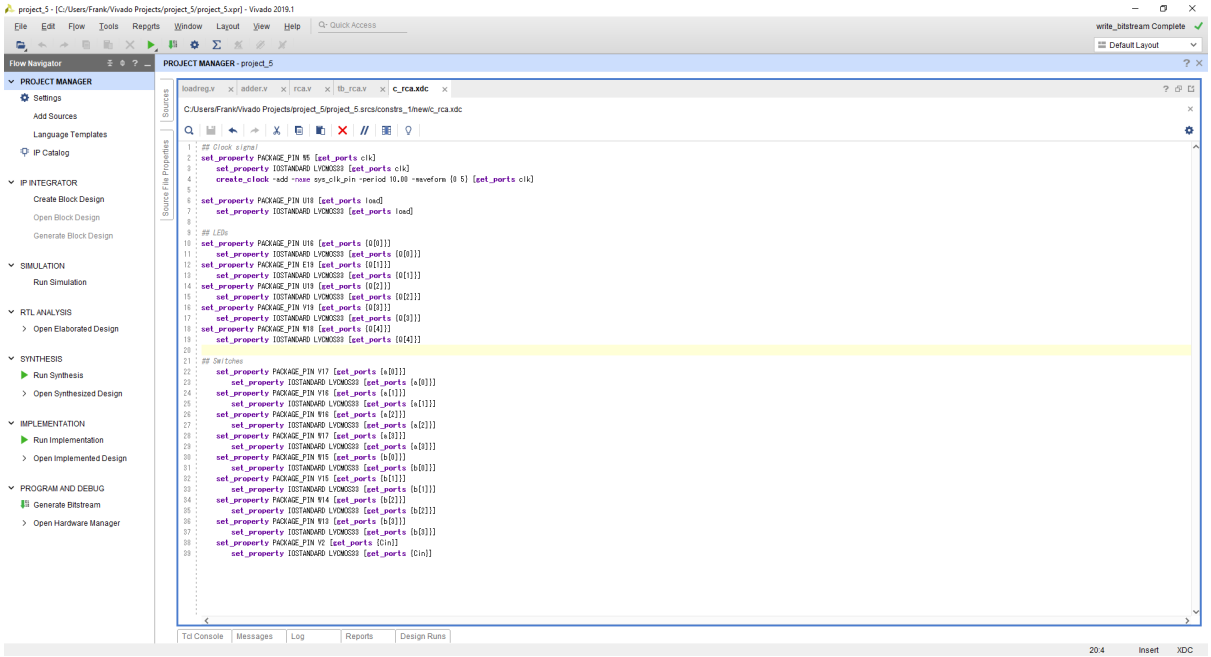




Simulation Waveform:



iv) Constraints File (Just the uncommented portion)



v) All the equations for C_i's and S_i's

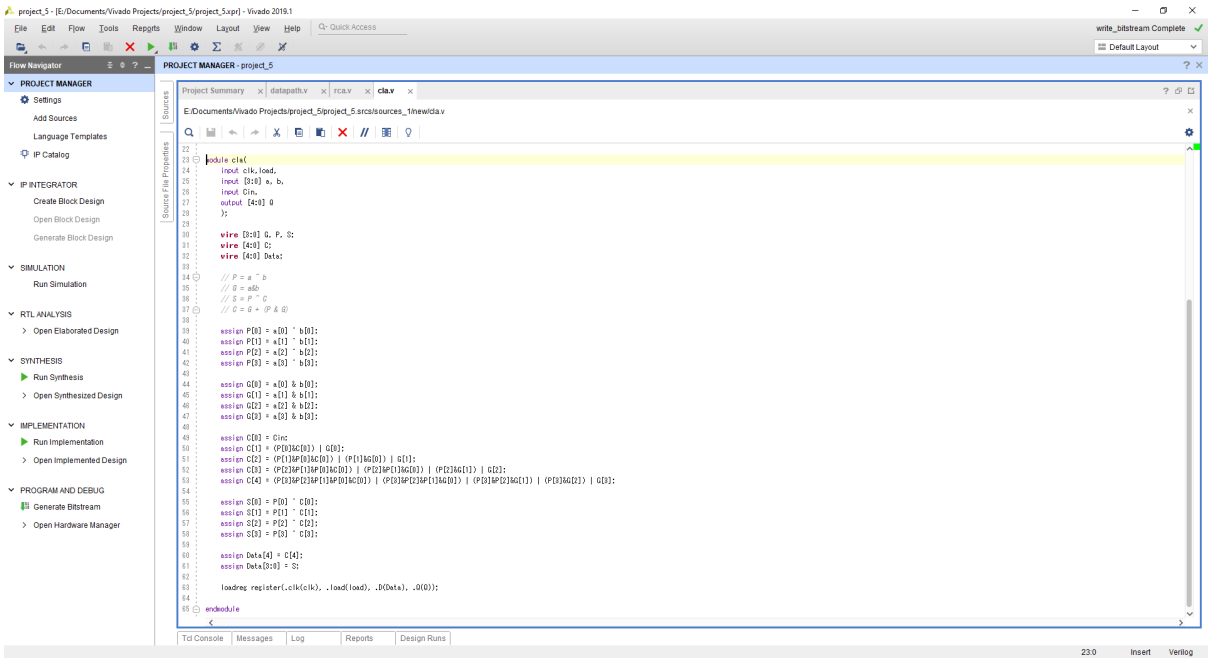
C_i's :

- $C_0 = Cin$
- $C_1 = G_0 + P_0C_0$
- $C_2 = G_1 + P_1G_0 + P_1P_0C_0$
- $C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0$
- $C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_0$

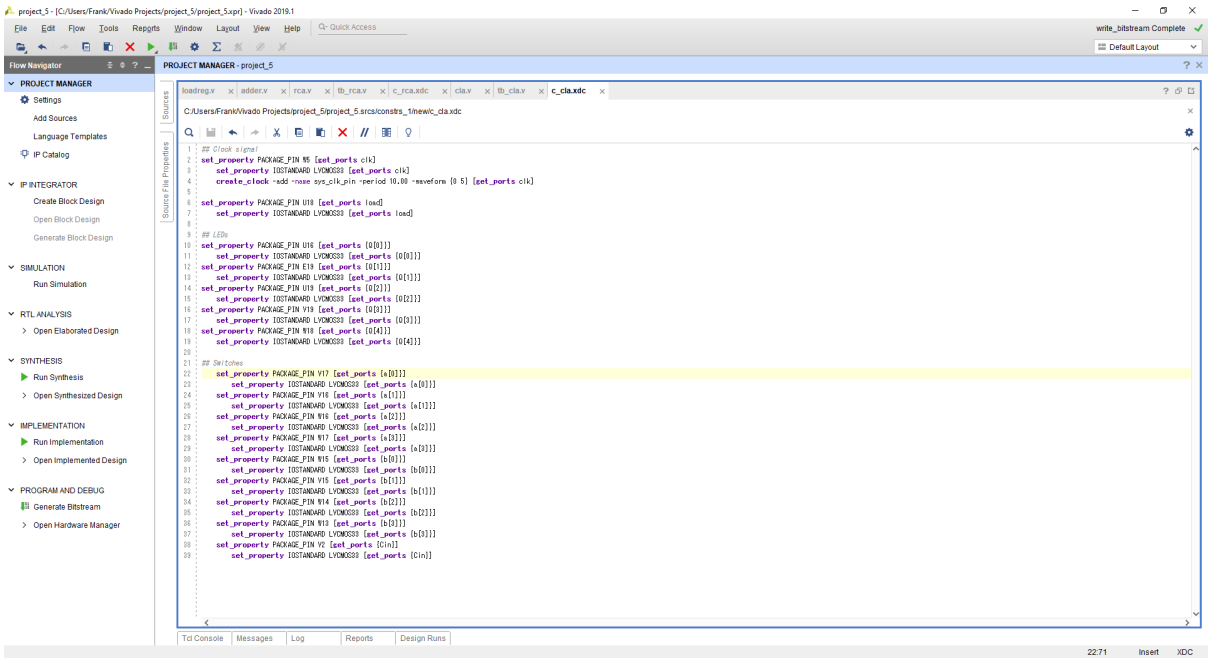
S_i's:

- $S_0 = P_0 \oplus C_0 = P_0 \oplus (Cin)$
- $S_1 = P_1 \oplus C_1 = P_1 \oplus (G_0 + P_0C_0)$
- $S_2 = P_2 \oplus C_2 = P_2 \oplus (G_1 + P_1G_0 + P_1P_0C_0)$
- $S_3 = P_3 \oplus C_3 = P_3 \oplus (G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0)$

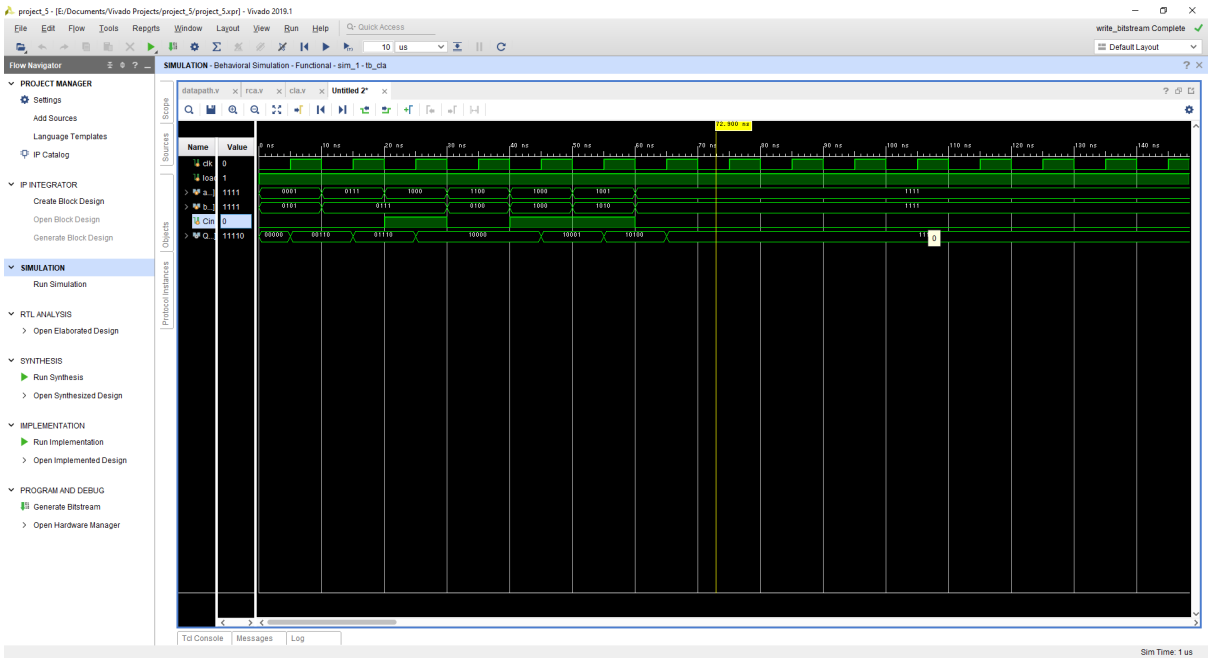
vi) Design file (.v) for the CLA



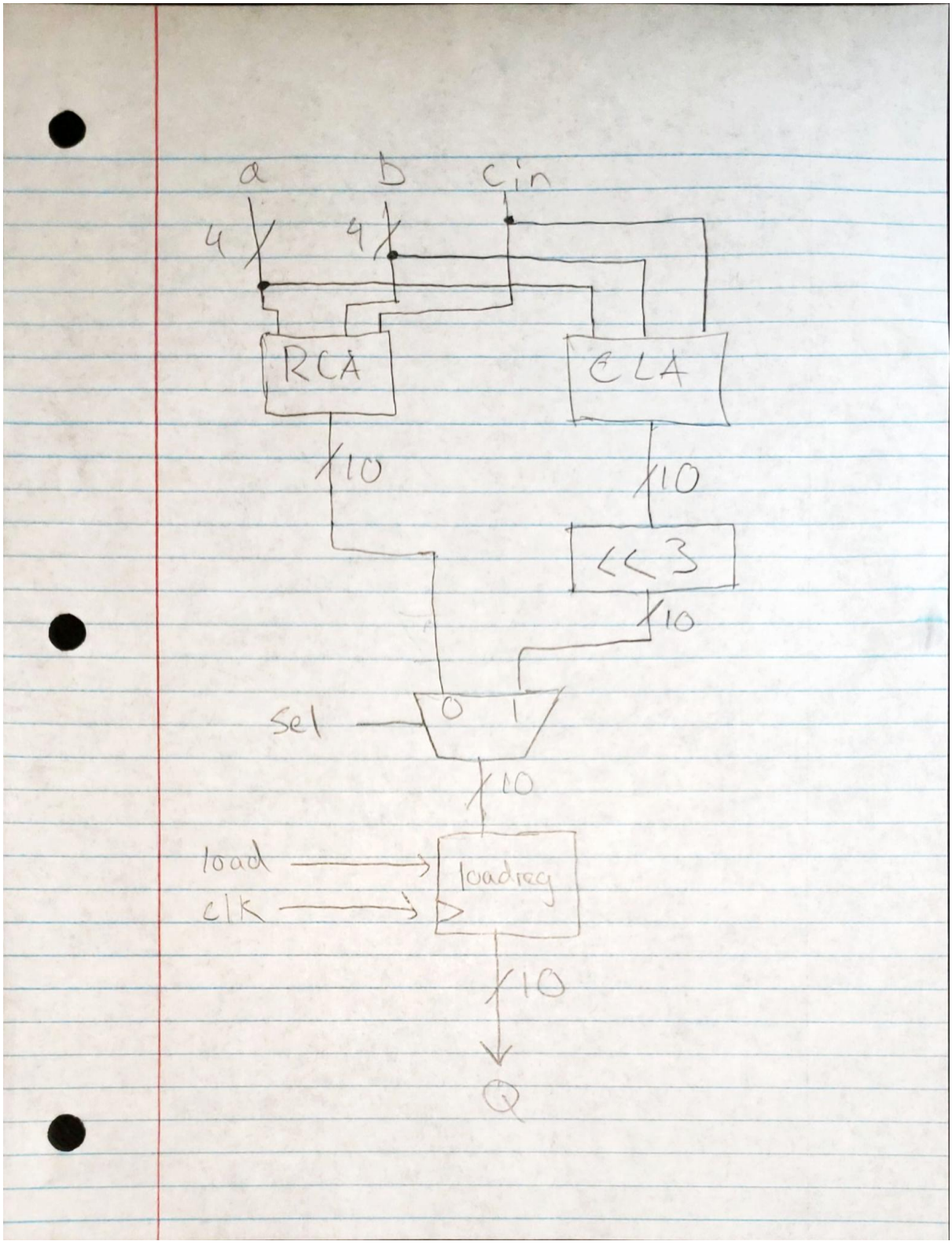
vii) Constraints File (Just the uncommented portion)



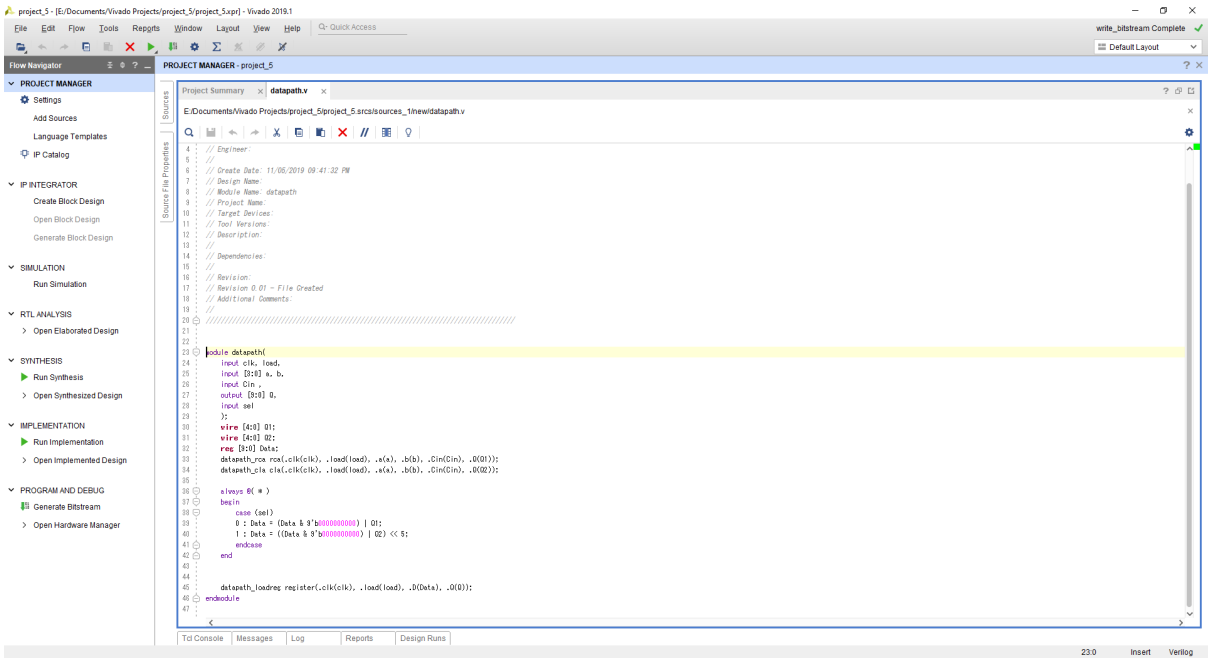
viii) Simulation waveform for the testcases in the table



ix) High-level block diagram of system

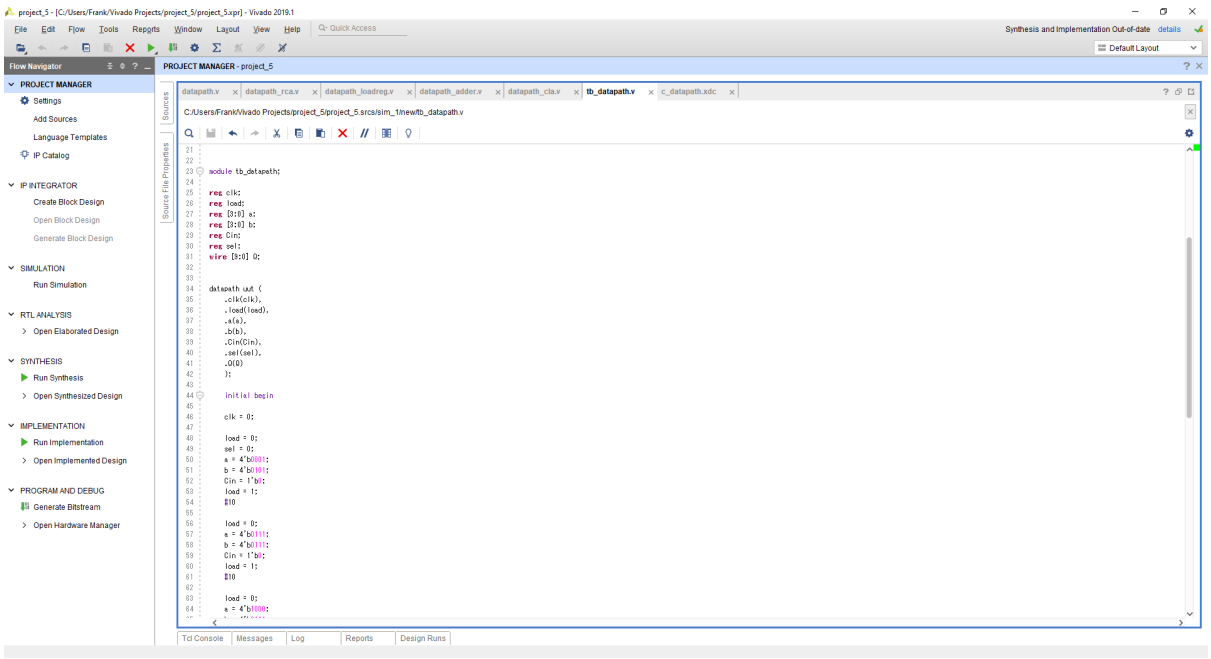


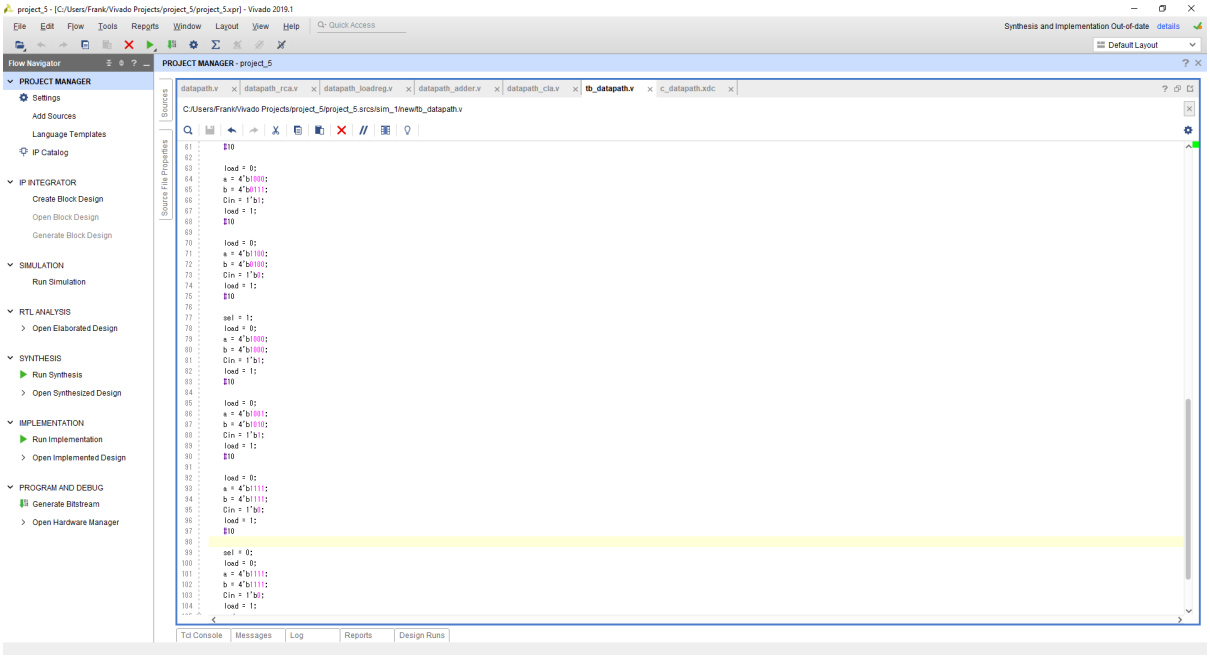
x) Design file for datapath.v



xi) Testbench and simulation waveform

Testbench:

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IMPLEMENTATION
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datapath_loadreg.v
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datapath_cla.v
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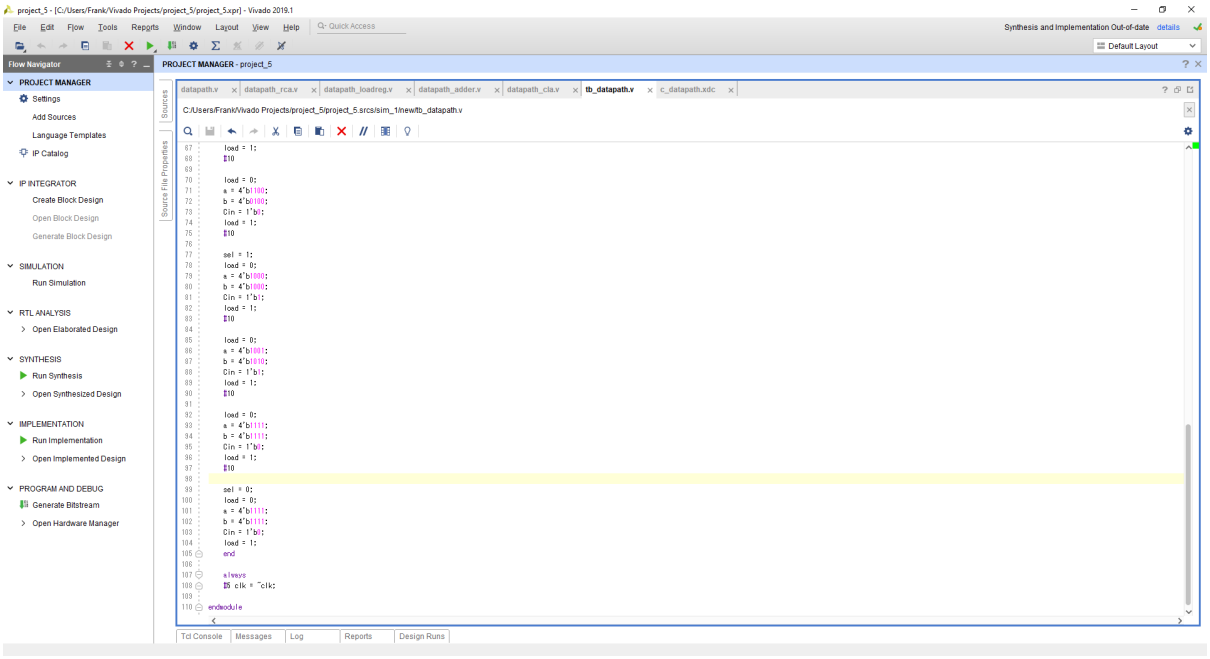
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datapath_cla.v
tb_datapath.v
c_datapath.xdc
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Sources
Source File Properties
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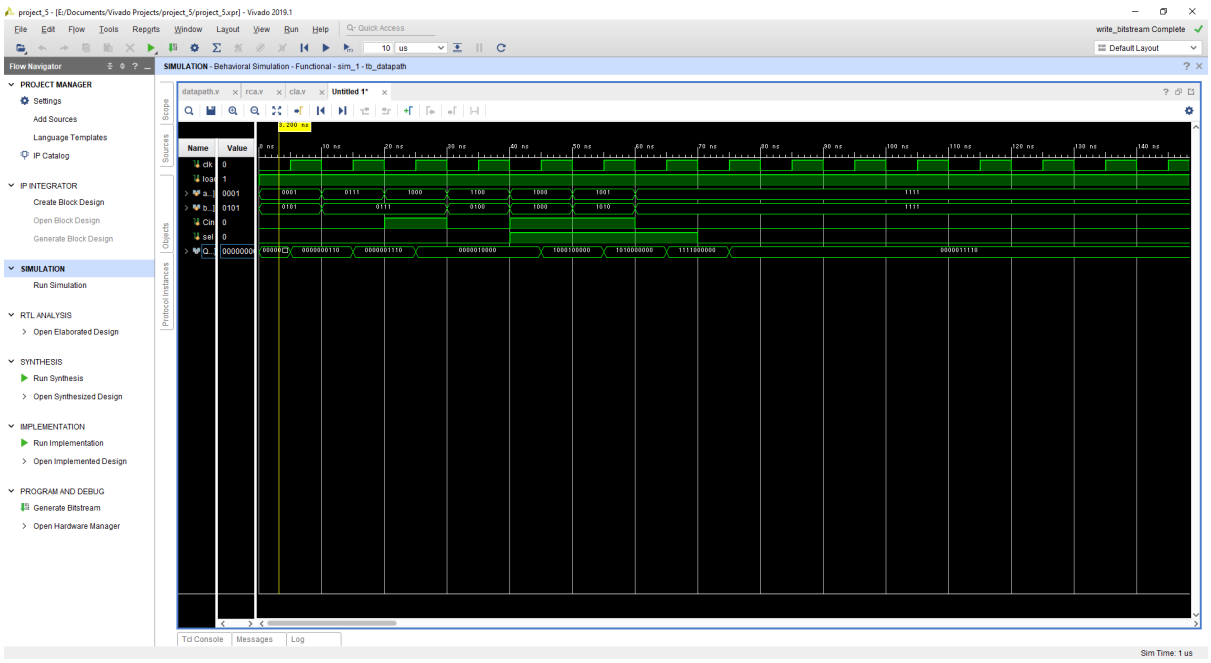
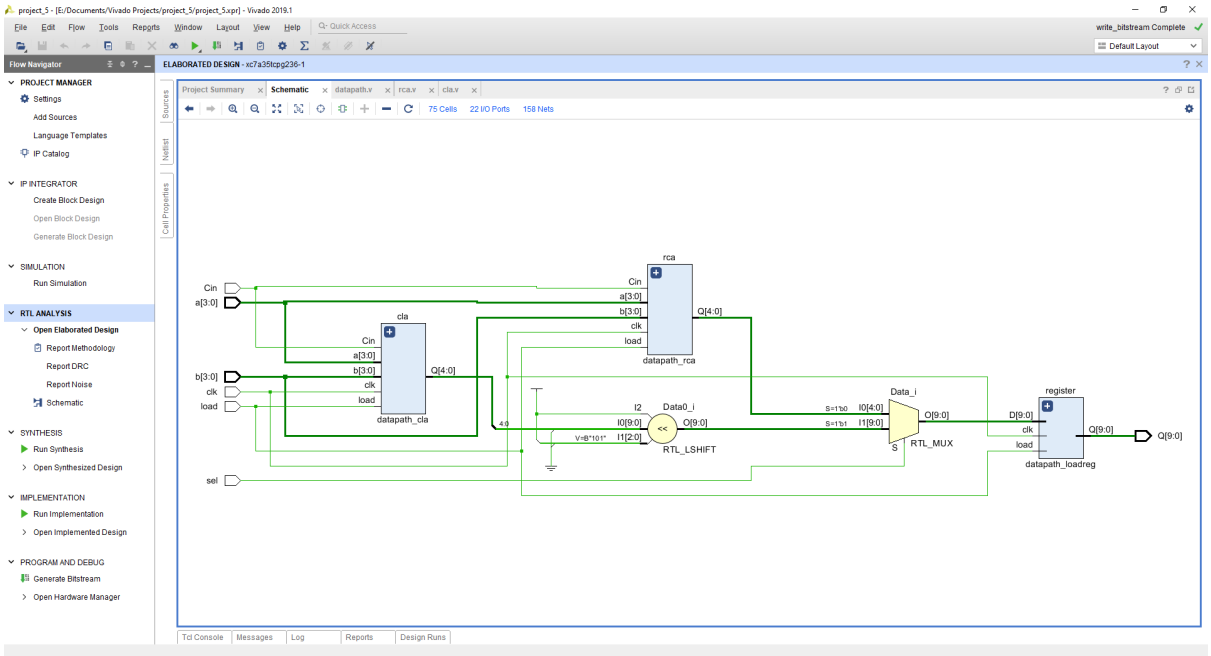
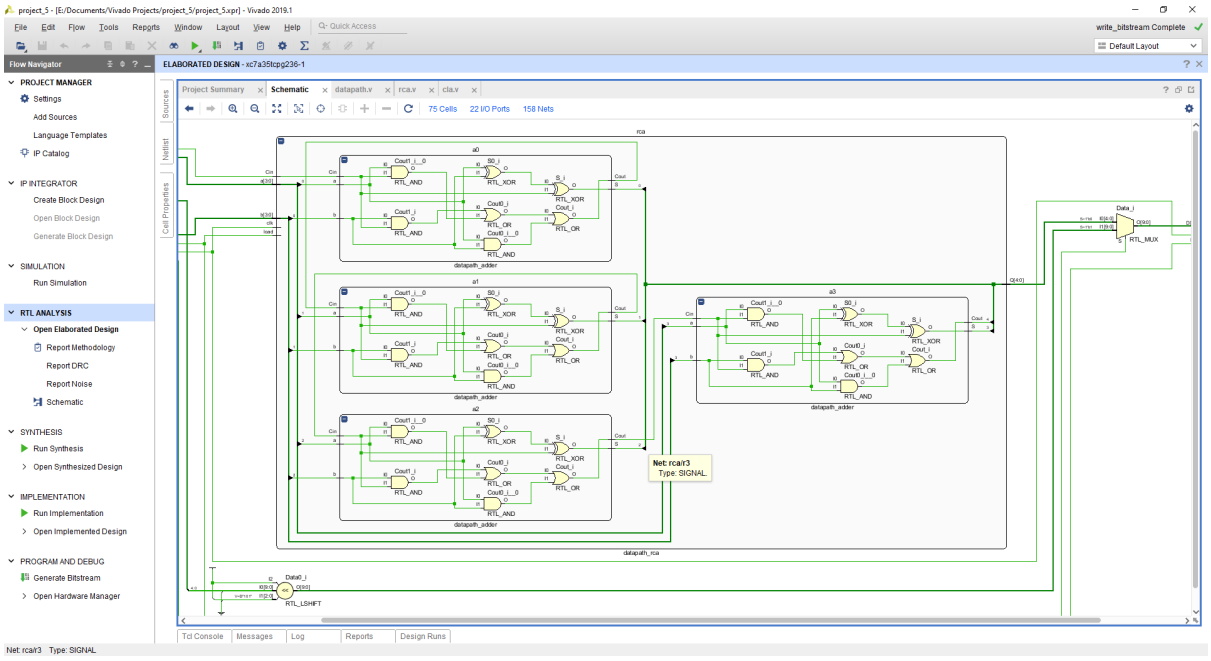
Simulation Waveform:



xii) Screenshot of full circuit and each adder module



RCA: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rca.v
cla.v
75 Cells
22 I/O Ports
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Reports
Design Runs
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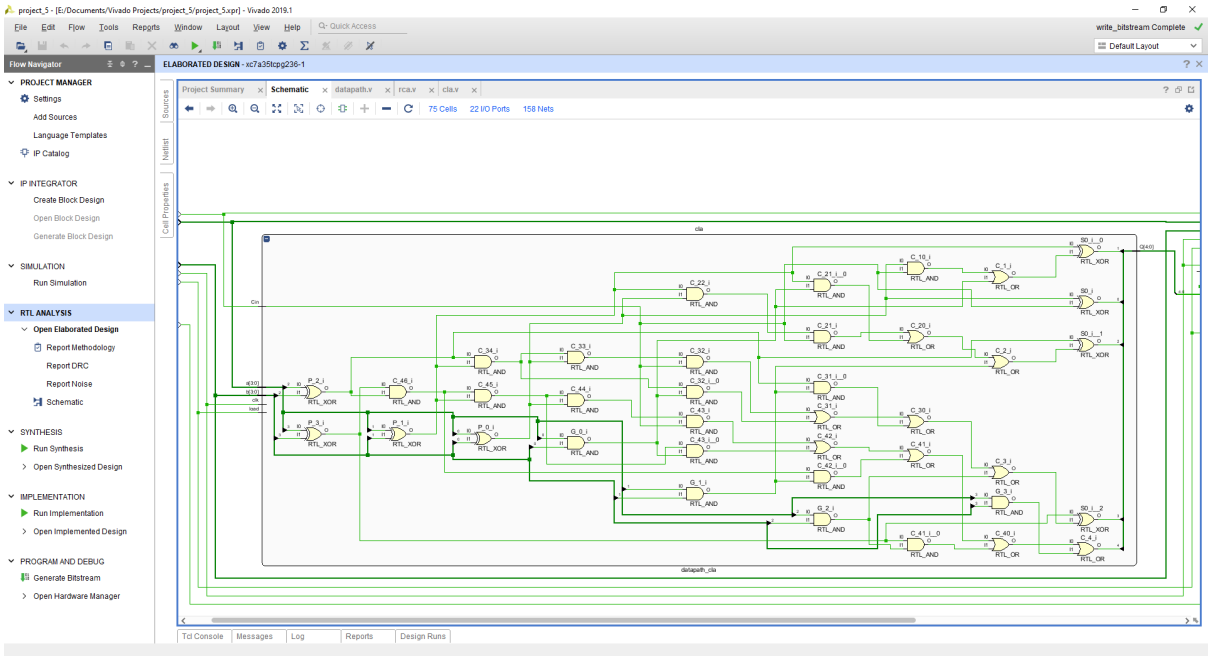
CLA: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xiii) Calculations of delay and area for each adder

RCA:

Critical Path = (3+2+2)*4 = 28 ns

Area = (6(2) + 4(2) + 2(3))*4 = 104

CLA:

Critical Path = 3+3+3+3+3+2+2+2+2 = 23 ns

Area = 10(4) + 8(6) + 20(2) = 128

	Area (area units)	Delay (ns)
RCA	104	28 ns
CLA	128	23 ns