

# Lab 3 Report

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## Checklist:

### Part 2 -

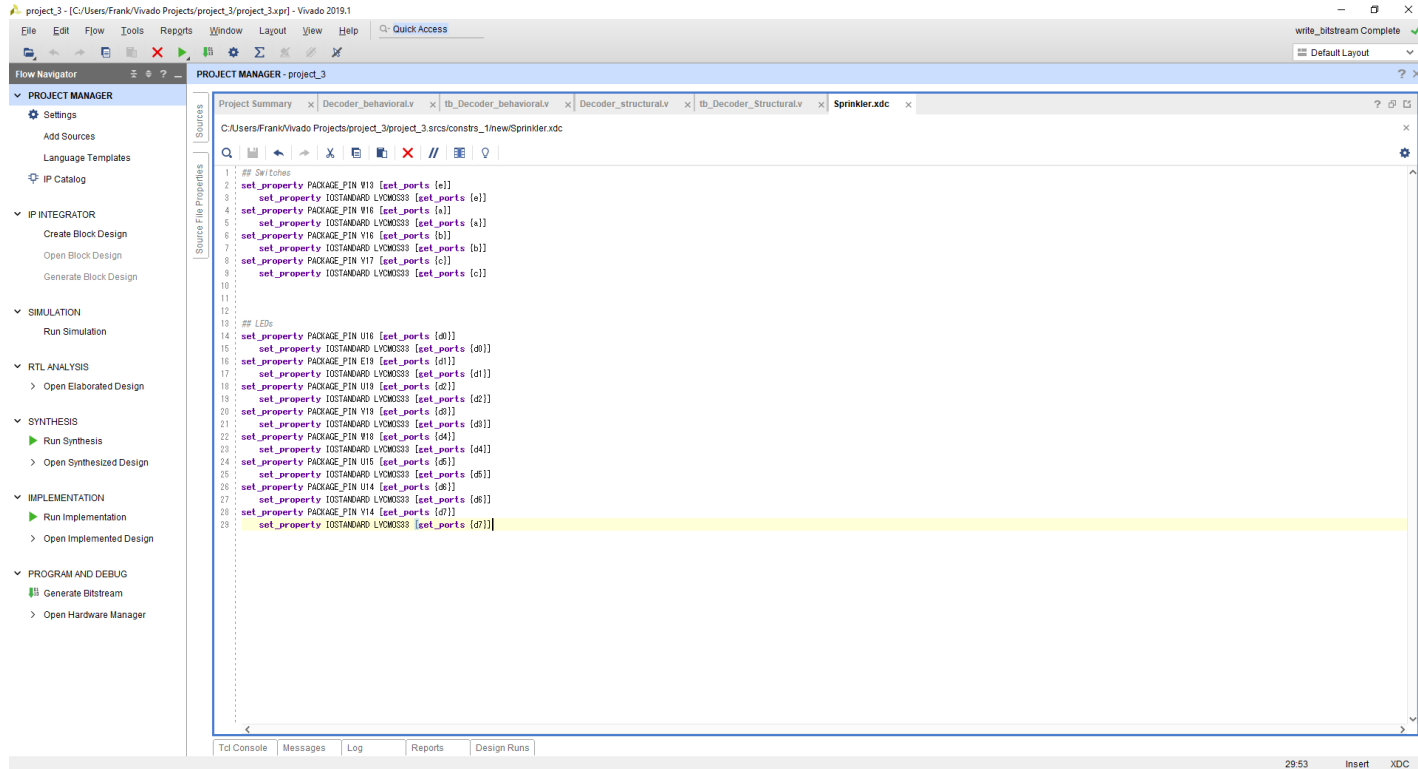
- i. Constraint file (Just the uncommented portion)

### Part 3 -

- ii. Truth table of the function
- iii. K-maps showing minimization of the logic functions (outputs)
- iv. Algebraic expression of the minimized logic functions (outputs)
- v. Verilog codes of module and testbench for structural modelling
- vi. Simulation waveform for structural modelling
- vii. Constraint file (Just the uncommented portion)

**Note** → *The Verilog code and the uncommented portions of the constraint files should be copied in your lab report and the actual Verilog (.v) and constraint (.xdc) files need to be zipped and submitted as well on Canvas. You are not allowed to change your Verilog code after final submission as the TAs may download the submitted codes from Canvas during checkouts. For the truth table, K-maps minimizations and algebraic expressions, you are free to draw them on paper and then put the pictures in your lab report, but please make sure it is legible for the TAs to grade it properly.*

## i) Constraint File Sprinkler



## ii) Truth Table

Inputs (SW[3:0])	Display (an[0])	a	b	c	d	e	f	g
0000	0	0	0	0	0	0	0	1
0001	1	1	0	0	1	1	1	1
0010	2	0	0	1	0	0	1	0
0011	3	0	0	0	0	1	1	0
0100	4	1	0	0	1	1	0	0
0101	5	0	1	0	0	1	0	0
0110	6	0	1	0	0	0	0	0
0111	7	0	0	0	1	1	1	1
1000	8	0	0	0	0	0	0	0
1001	9	0	0	0	0	1	0	0
1010	A	0	0	0	1	0	0	0
1011	b	1	1	0	0	0	0	0
1100	C	0	1	1	0	0	0	1
1101	d	1	0	0	0	0	1	0
1110	E	0	1	1	0	0	0	0
1111	F	0	1	1	1	0	0	0

- iii) K-Maps
- iv) Algebraic Expressions

## SOP & K-Maps

a

AB \ CD	00	01	11	10
00	0	1	0	0
01	1	0	0	0
11	0	1	0	0
10	0	0	1	0

$$a = A'B'C'D + A'BC'D' + ABC'D + AB'CD$$

b

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	1	0	1
11	1	0	1	1
10	0	0	1	0

$$b = A'BC'D + BCD' + ABD' + ACD$$

c

AB \ CD	00	01	11	10
00	0	0	0	1
01	0	0	0	0
11	1	0	1	0
10	0	0	0	0

$$c = A'B'CD' + ABC + ABD'$$

d

AB \ CD	00	01	11	10
00	0	1	0	0
01	1	0	1	0
11	0	0	1	0
10	0	0	0	1

$$d = A'B'C'D + A'BC'D' + BCD + AB'CD'$$

e

AB \ CD	00	01	11	10
00	0	1	1	0
01	1	0	1	0
11	0	0	0	0
10	0	1	0	0

$$e = B'C'D + A'BC' + A'CD$$

f

AB \ CD	00	01	11	10
00	0	1	1	1
01	0	0	1	0
11	0	1	0	0
10	0	0	0	0

$$f = A'B'D + A'B'C + A'CD + ABC'D$$



g

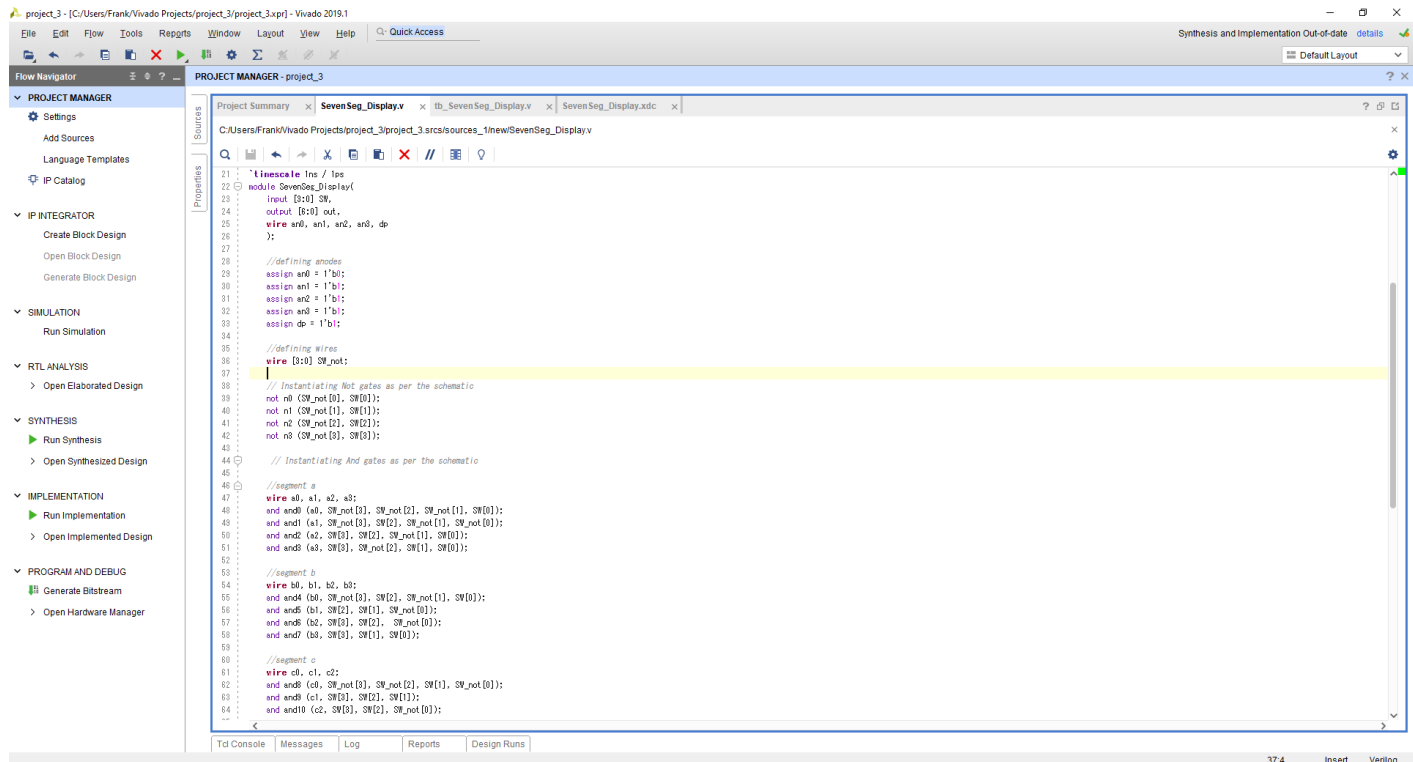
$\leq 10$

AB \ CD	00	01	11	10
00	1	1	0	0
01	0	0	1	0
11	1	0	0	0
10	0	0	0	0

$$g = A'B'C' + A'BCD + ABC'D'$$

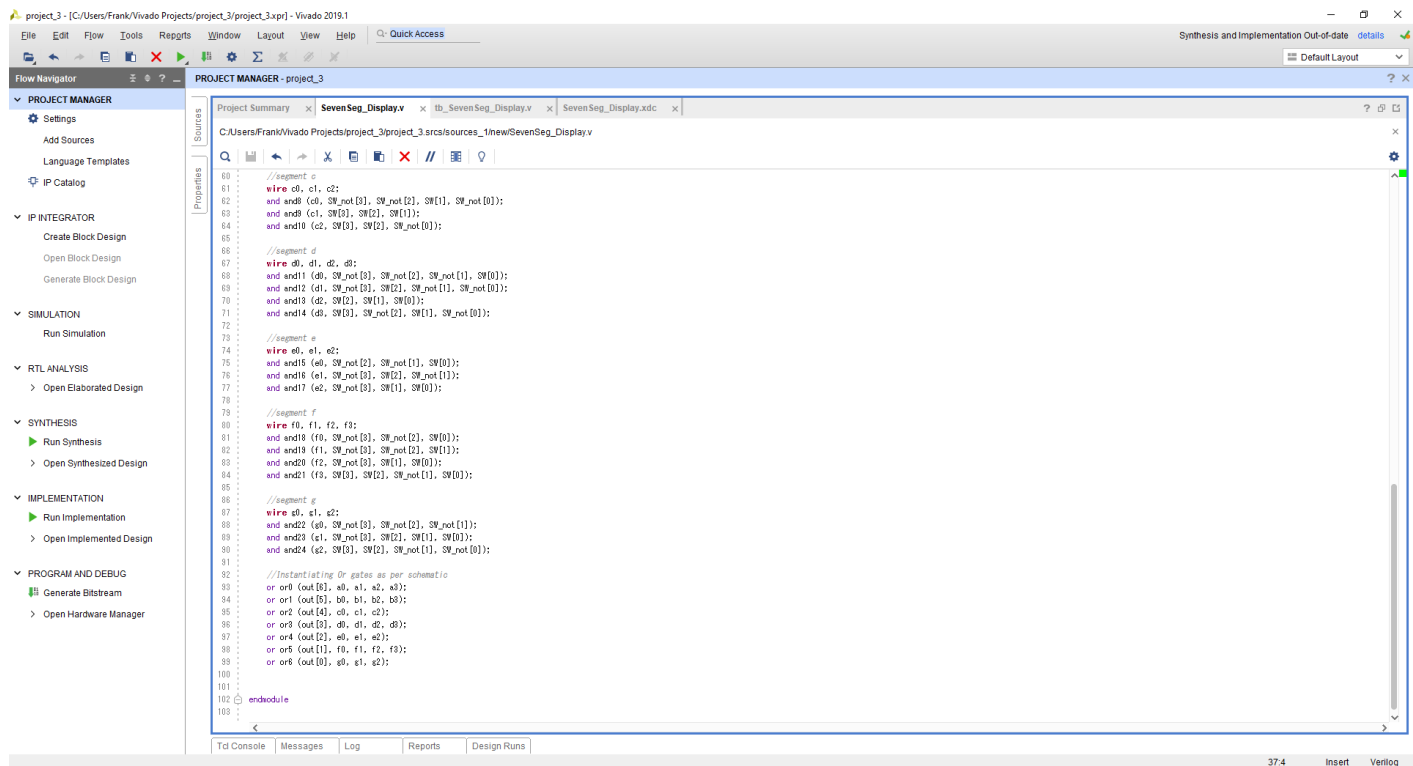
## v) Verilog Code of Module and Testbench

### Structural Module



The screenshot shows the Vivado IDE interface with the project 'project\_3' open. The 'PROJECT MANAGER' pane on the left shows the project structure. The main editor displays the Verilog code for the 'SevenSeg\_Display' module. The code is as follows:

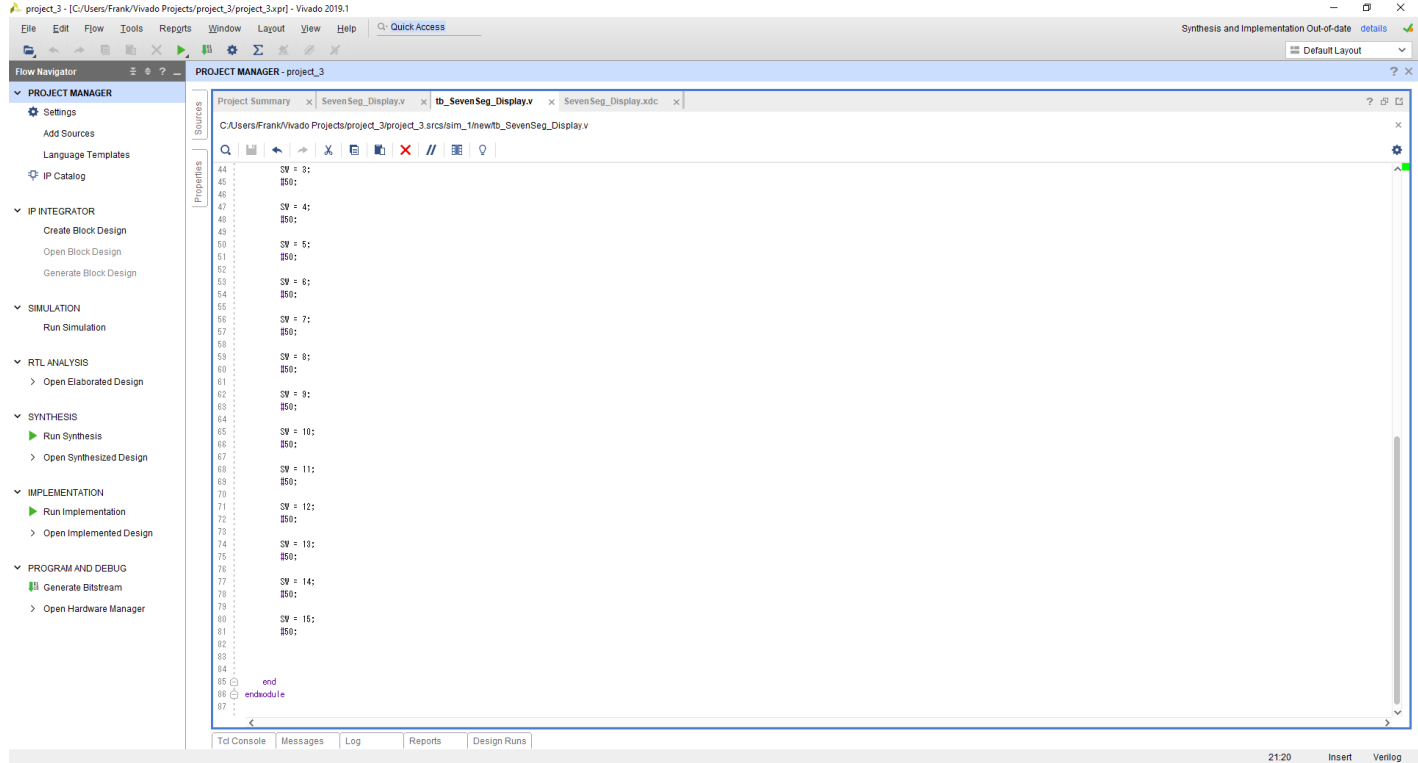
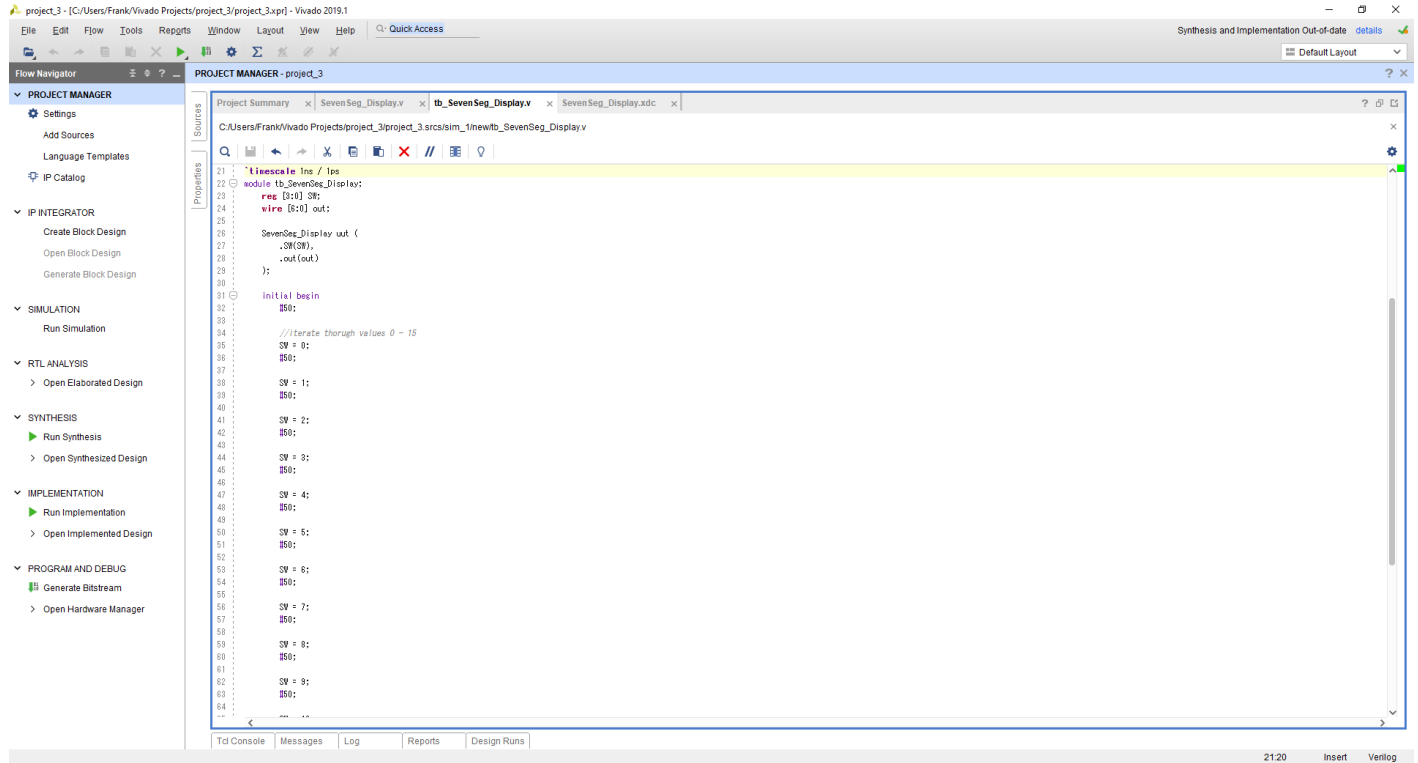
```
1 linescale 1ns / 1ps
22 module SevenSeg_Display(
23     input [3:0] SW,
24     output [6:0] out,
25     wire an0, an1, an2, an3, dp
26 );
27
28 //defining anodes
29 assign an0 = 1'b0;
30 assign an1 = 1'b1;
31 assign an2 = 1'b1;
32 assign an3 = 1'b1;
33 assign dp = 1'b1;
34
35 //defining wires
36 wire [0:0] SW_not;
37
38 //Instantiating Not gates as per the schematic
39 not n0 (SW_not[0], SW[0]);
40 not n1 (SW_not[1], SW[1]);
41 not n2 (SW_not[2], SW[2]);
42 not n3 (SW_not[3], SW[3]);
43
44 //Instantiating And gates as per the schematic
45
46 //segment a
47 wire a0, a1, a2, a3;
48 and0 (a0, SW_not[0], SW_not[2], SW_not[1], SW[0]);
49 and1 (a1, SW_not[0], SW[2], SW_not[1], SW_not[0]);
50 and2 (a2, SW[0], SW[2], SW_not[1], SW[0]);
51 and3 (a3, SW[0], SW_not[2], SW[1], SW[0]);
52
53 //segment b
54 wire b0, b1, b2, b3;
55 and4 (b0, SW_not[0], SW[2], SW_not[1], SW[0]);
56 and5 (b1, SW[2], SW[1], SW_not[0]);
57 and6 (b2, SW[0], SW[2], SW_not[0]);
58 and7 (b3, SW[0], SW[1], SW[0]);
59
60 //segment c
61 wire c0, c1, c2;
62 and8 (c0, SW_not[0], SW_not[2], SW[1], SW_not[0]);
63 and9 (c1, SW[0], SW[2], SW[1]);
64 and10 (c2, SW[0], SW[2], SW_not[0]);
65
66 //segment d
67 wire d0, d1, d2, d3;
68 and11 (d0, SW_not[0], SW_not[2], SW_not[1], SW[0]);
69 and12 (d1, SW_not[0], SW[2], SW_not[1], SW_not[0]);
70 and13 (d2, SW[2], SW[1], SW[0]);
71 and14 (d3, SW[0], SW_not[0], SW[1], SW_not[0]);
72
73 //segment e
74 wire e0, e1, e2;
75 and15 (e0, SW_not[2], SW_not[1], SW[0]);
76 and16 (e1, SW_not[0], SW[2], SW_not[1]);
77 and17 (e2, SW_not[0], SW[1], SW[0]);
78
79 //segment f
80 wire f0, f1, f2, f3;
81 and18 (f0, SW_not[0], SW_not[2], SW[0]);
82 and19 (f1, SW_not[0], SW_not[2], SW[1]);
83 and20 (f2, SW_not[0], SW[1], SW[0]);
84 and21 (f3, SW[0], SW[2], SW_not[1], SW[0]);
85
86 //segment g
87 wire g0, g1, g2;
88 and22 (g0, SW_not[0], SW_not[2], SW_not[1]);
89 and23 (g1, SW_not[0], SW[2], SW[1], SW[0]);
90 and24 (g2, SW[0], SW[2], SW_not[1], SW_not[0]);
91
92 //Instantiating Or gates as per schematic
93 or0 (out[0], a0, a1, a2, a3);
94 or1 (out[0], b0, b1, b2, b3);
95 or2 (out[4], c0, c1, c2);
96 or3 (out[3], d0, d1, d2, d3);
97 or4 (out[2], e0, e1, e2);
98 or5 (out[1], f0, f1, f2, f3);
99 or6 (out[0], g0, g1, g2);
100
101 endmodule
```



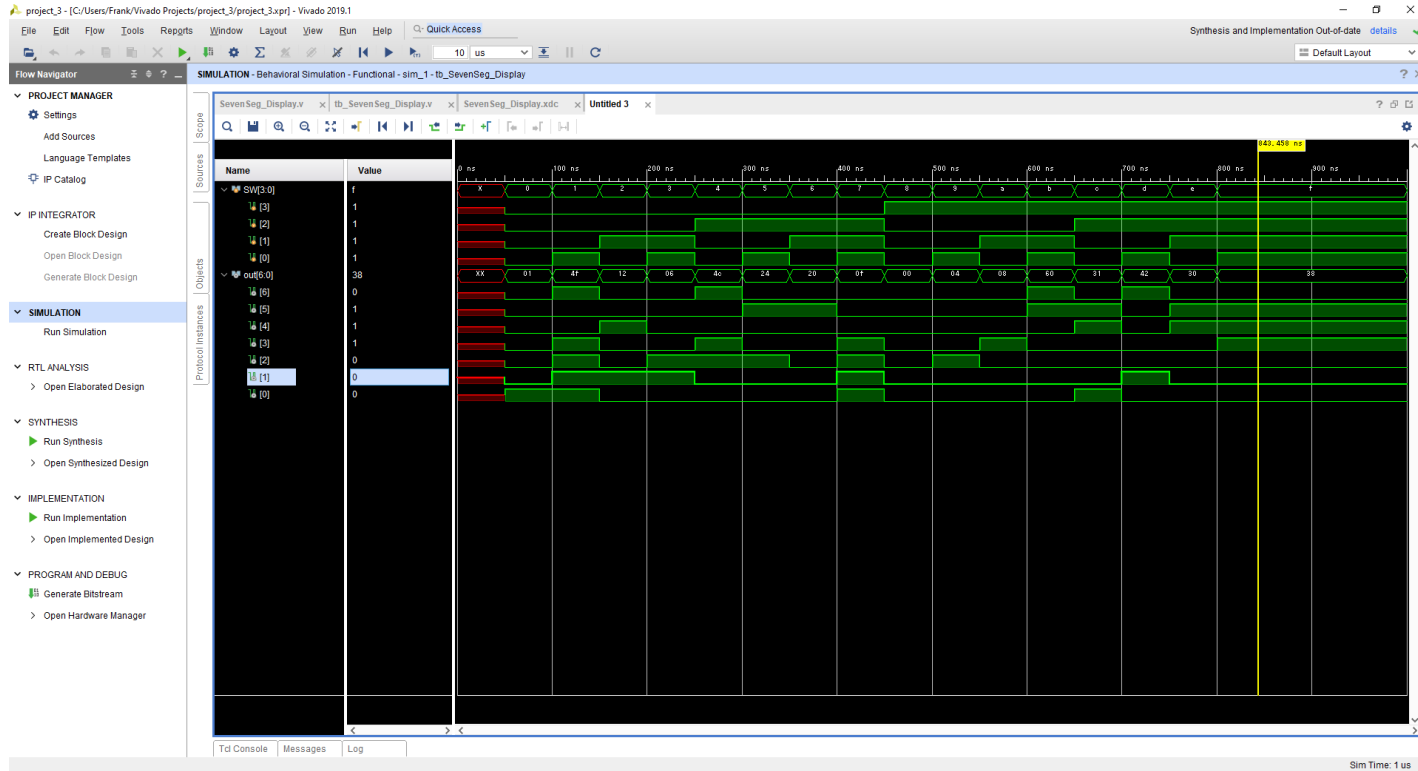
The screenshot shows the Vivado IDE interface with the project 'project\_3' open. The 'PROJECT MANAGER' pane on the left shows the project structure. The main editor displays the Verilog code for the 'SevenSeg\_Display' module, continuing from the previous screenshot. The code is as follows:

```
80 //segment c
81 wire c0, c1, c2;
82 and8 (c0, SW_not[0], SW_not[2], SW[1], SW_not[0]);
83 and9 (c1, SW[0], SW[2], SW[1]);
84 and10 (c2, SW[0], SW[2], SW_not[0]);
85
86 //segment d
87 wire d0, d1, d2, d3;
88 and11 (d0, SW_not[0], SW_not[2], SW_not[1], SW[0]);
89 and12 (d1, SW_not[0], SW[2], SW_not[1], SW_not[0]);
90 and13 (d2, SW[2], SW[1], SW[0]);
91 and14 (d3, SW[0], SW_not[0], SW[1], SW_not[0]);
92
93 //segment e
94 wire e0, e1, e2;
95 and15 (e0, SW_not[2], SW_not[1], SW[0]);
96 and16 (e1, SW_not[0], SW[2], SW_not[1]);
97 and17 (e2, SW_not[0], SW[1], SW[0]);
98
99 //segment f
100 wire f0, f1, f2, f3;
101 and18 (f0, SW_not[0], SW_not[2], SW[0]);
102 and19 (f1, SW_not[0], SW_not[2], SW[1]);
103 and20 (f2, SW_not[0], SW[1], SW[0]);
104 and21 (f3, SW[0], SW[2], SW_not[1], SW[0]);
105
106 //segment g
107 wire g0, g1, g2;
108 and22 (g0, SW_not[0], SW_not[2], SW_not[1]);
109 and23 (g1, SW_not[0], SW[2], SW[1], SW[0]);
110 and24 (g2, SW[0], SW[2], SW_not[1], SW_not[0]);
111
112 //Instantiating Or gates as per schematic
113 or0 (out[0], a0, a1, a2, a3);
114 or1 (out[0], b0, b1, b2, b3);
115 or2 (out[4], c0, c1, c2);
116 or3 (out[3], d0, d1, d2, d3);
117 or4 (out[2], e0, e1, e2);
118 or5 (out[1], f0, f1, f2, f3);
119 or6 (out[0], g0, g1, g2);
120
121 endmodule
```

# Testbench



## vi) Simulation Waveform



## vii) Constraint File Seven Segment Display

The screenshot shows the Vivado Project Manager interface with the 'SevenSeg\_Display.xdc' file open. The file contains Verilog code defining package pins, switches, and segment displays. The code is as follows:

```

1: ## Switches
2: set_property PACKAGE_PIN W17 [set_ports {SW[3]}]
3: set_property IOSTANDARD LVCMOS33 [set_ports {SW[3]}]
4: set_property PACKAGE_PIN W16 [set_ports {SW[2]}]
5: set_property IOSTANDARD LVCMOS33 [set_ports {SW[2]}]
6: set_property PACKAGE_PIN Y16 [set_ports {SW[1]}]
7: set_property IOSTANDARD LVCMOS33 [set_ports {SW[1]}]
8: set_property PACKAGE_PIN W17 [set_ports {SW[0]}]
9: set_property IOSTANDARD LVCMOS33 [set_ports {SW[0]}]
10:
11: ## 7 Segment Display
12: set_property PACKAGE_PIN Y7 [set_ports {out[6]}]
13: set_property IOSTANDARD LVCMOS33 [set_ports {out[6]}]
14: set_property PACKAGE_PIN W6 [set_ports {out[5]}]
15: set_property IOSTANDARD LVCMOS33 [set_ports {out[5]}]
16: set_property PACKAGE_PIN U8 [set_ports {out[4]}]
17: set_property IOSTANDARD LVCMOS33 [set_ports {out[4]}]
18: set_property PACKAGE_PIN V6 [set_ports {out[3]}]
19: set_property IOSTANDARD LVCMOS33 [set_ports {out[3]}]
20: set_property PACKAGE_PIN U5 [set_ports {out[2]}]
21: set_property IOSTANDARD LVCMOS33 [set_ports {out[2]}]
22: set_property PACKAGE_PIN V6 [set_ports {out[1]}]
23: set_property IOSTANDARD LVCMOS33 [set_ports {out[1]}]
24: set_property PACKAGE_PIN U7 [set_ports {out[0]}]
25: set_property IOSTANDARD LVCMOS33 [set_ports {out[0]}]
26:
27: ## Decimal Point
28: set_property PACKAGE_PIN Y7 [set_ports {dp}]
29: set_property IOSTANDARD LVCMOS33 [set_ports {dp}]
30:
31: ## Anodes
32: set_property PACKAGE_PIN U2 [set_ports {an[0]}]
33: set_property IOSTANDARD LVCMOS33 [set_ports {an[0]}]
34: set_property PACKAGE_PIN U4 [set_ports {an[1]}]
35: set_property IOSTANDARD LVCMOS33 [set_ports {an[1]}]
36: set_property PACKAGE_PIN V4 [set_ports {an[2]}]
37: set_property IOSTANDARD LVCMOS33 [set_ports {an[2]}]
38: set_property PACKAGE_PIN W4 [set_ports {an[3]}]
39: set_property IOSTANDARD LVCMOS33 [set_ports {an[3]}]

```