Lab 6 Report

Name: Frank Le
UT EID: fpl227
Section #: 16100

a) <u>Lab Report</u>

When starting on the lab I chose to reuse all of my code from lab 4. By using previous code, all I needed to do to finish this lab was to adjust my previous code and to add another module called stopwatch.

My main approach to implementing the stopwatch functionality was using if-else statements. All 4 of the modes I needed to implement were placed in an always block with if statements that would direct which mode the stopwatch was in currently. I had an input "mode" that would select which mode the stopwatch was in. I also created variables such as startstop and finish to indicate whether the stop button was pushed and to check if the stopwatch finished counting.

I implemented the first mode (counting from 00.00 to 99.99) by first checking to see if both the stopwatch is stopped and reset. By doing so I would load in the starting values such as 0 into the registers to begin counting from 0. Next, I checked to see if the stopwatch was not stopped and if finish was not true. If these conditions were met, then the stopwatch would begin counting from 00.00 to 99.99. This was implemented through nested if-else statements which would check from left most to right most digit to see if the value 9 was reached. If 9 wasn't reached then the register would increment, if it was reached it would

rollover to zero until finally all registers had 9 as their values, signifying the stopwatch reached 99.99. At any point during counting the user could press the stop button to stop counting and press it again to resume. I implemented this by checking to see if stop was pressed and reset was not pressed. Once these conditions were met, I loaded in the current value into the register to ensure no incrementing was occurring.

Once I finished the first mode's functionality the remaining modes to implement were basically the same with minor adjustments. For mode 2, instead of initially loading 0 for all the digits, I loaded the tens and ones digit with the values from the switches. For mode 3, I loaded 9 into all the digits initially and decremented the registers instead of incrementing. The if statements also checked to see if the register reached 0 instead of 9 like the previous modes. Finally, mode 4 was exactly like mode 3 but I loaded the values from the switches into the tens and one place just like mode 2.

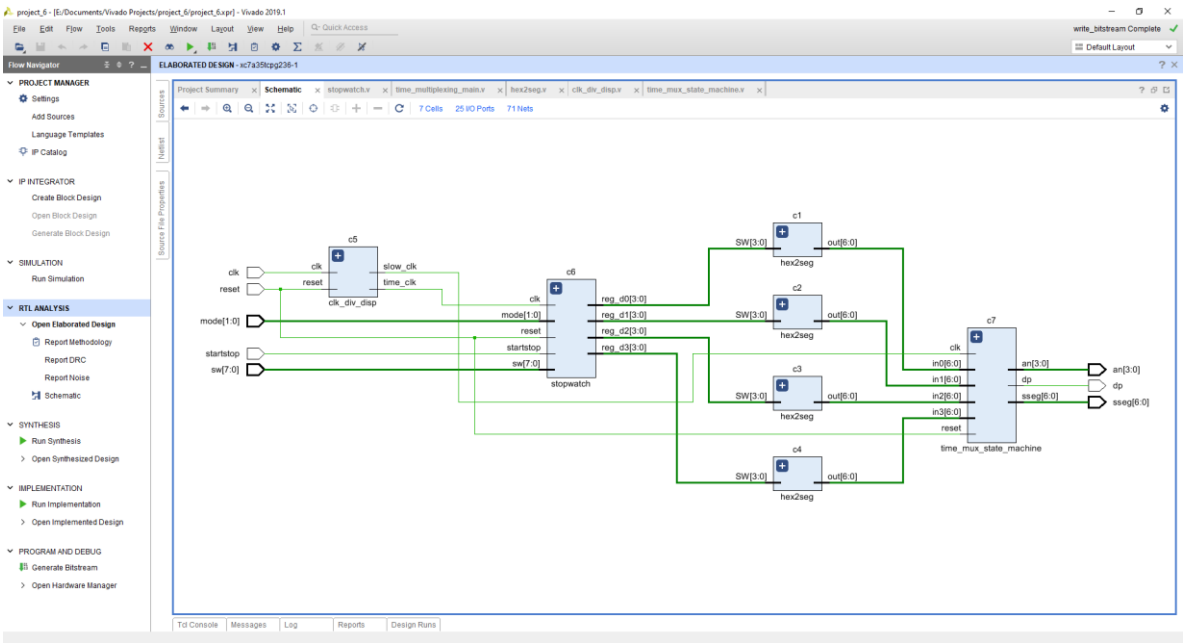
One of the major challenges with this lab was getting mode 2 and mode 4 to function correctly with an input greater than 9. Initially my design caused the stopwatch to rollover incorrectly because it didn't account for this corner case. However, this issue was resolved through if statements to check if the input was greater than 9.

b) <u>Summary of system</u>

This lab is a design for a stopwatch using Verilog and a FPGA board. The stopwatch has 4 different modes depending on the user's input on SW[1:0]: a mode to increment from 00.00 to 99.99, a mode that will increment from an externally loaded value from SW[15:8], a mode to decrement from 99.99 to 00.00, and a mode that will decrement from an

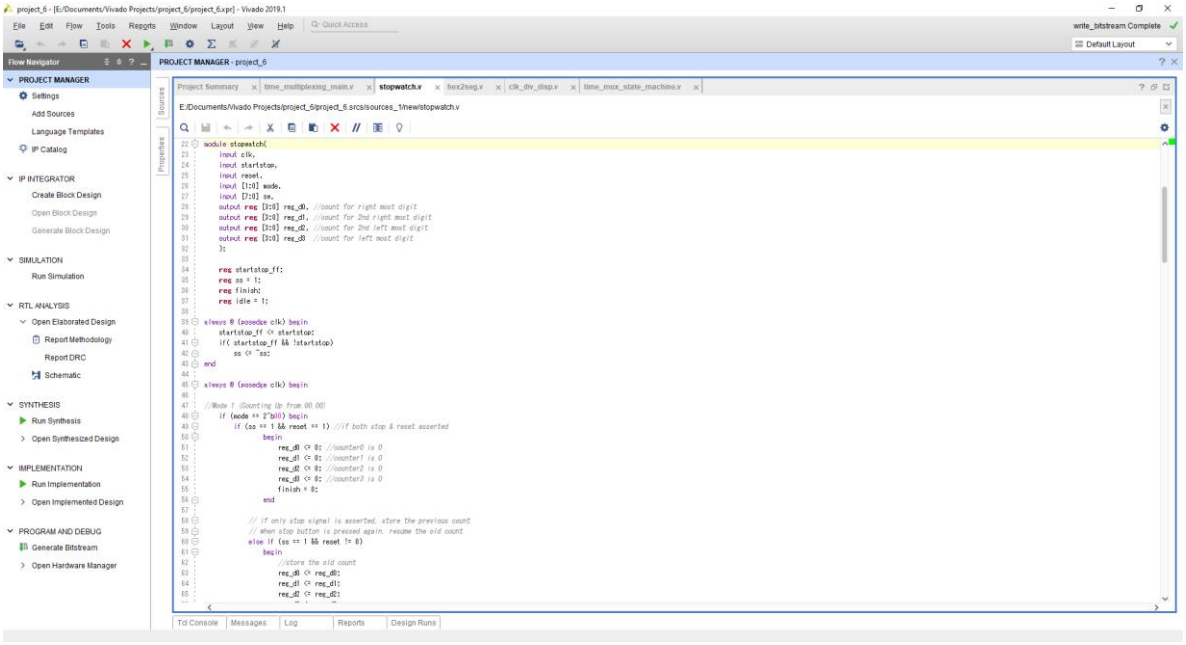
externally loaded value from SW[15:8]. The user can stop and resume the stopwatch by pressing the center button and can also reset the stopwatch by pressing the up button.

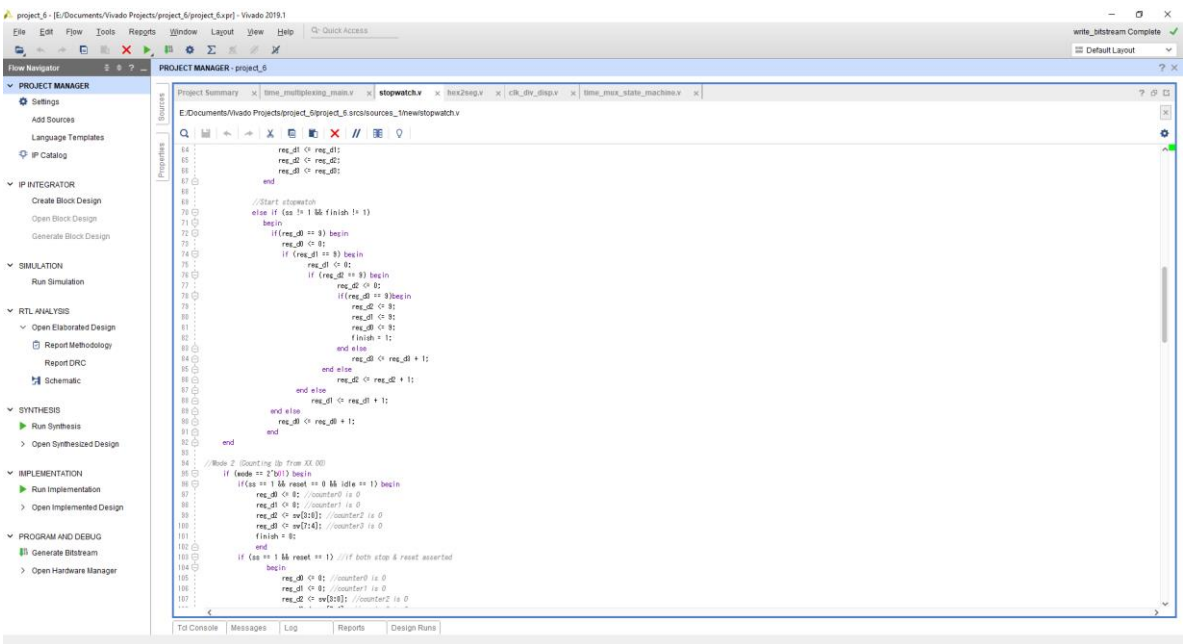
c) <u>High Level Block Diagram</u>

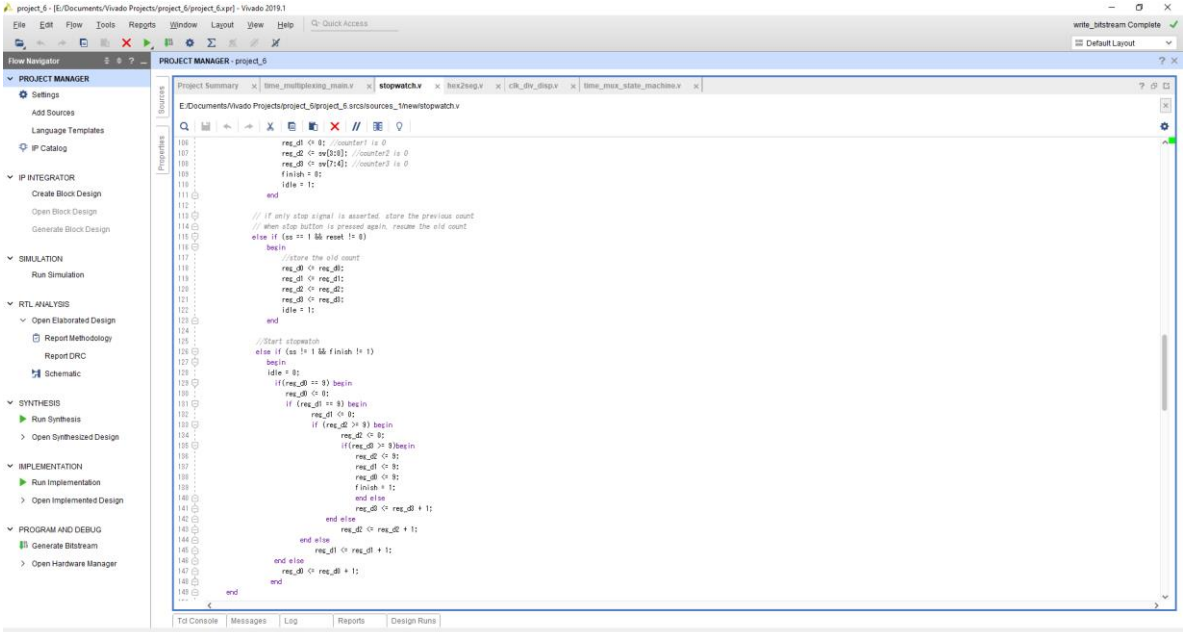


.v Files:

Stopwatch:



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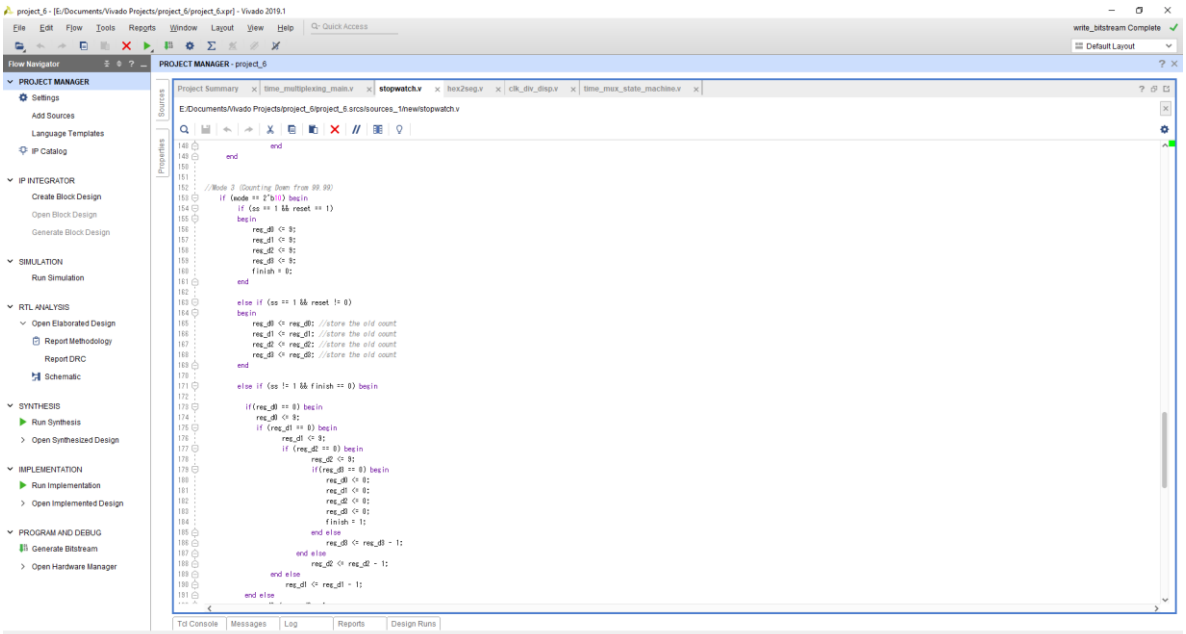
File Edit Flow Tools Reports Window Layout View Help
Quick Access
write_bitstream Complete
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
PROJECT MANAGER - project_6
Project Summary
time_multiplexing_main.v
stopwatch.v
hex2seg.v
clk_div_disp.v
time_mux_state_machine.v
E:/Documents/Vivado Projects/project_6/project_6.srcs/sources_1/new/stopwatch.v
Tcl Console
Messages
Log
Reports
Design Runs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File Edit Flow Tools Reports Window Layout View Help
Quick Access
write_bitstream Complete
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
PROJECT MANAGER - project_6
Project Summary
time_multiplexing_main.v
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clk_div_disp.v
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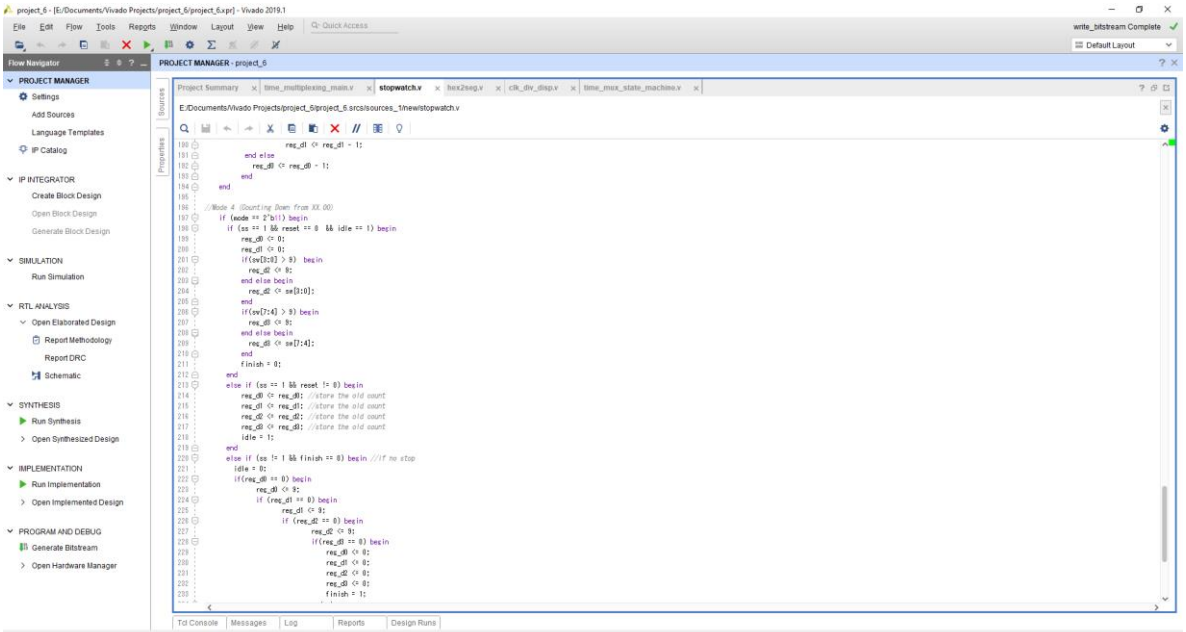
Tcl Console
Messages
Log
Reports
Design Runs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File Edit Flow Tools Reports Window Layout View Help
Quick Access
write_bitstream Complete
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
PROJECT MANAGER - project_6
Project Summary
time_multiplexing_main.v
stopwatch.v
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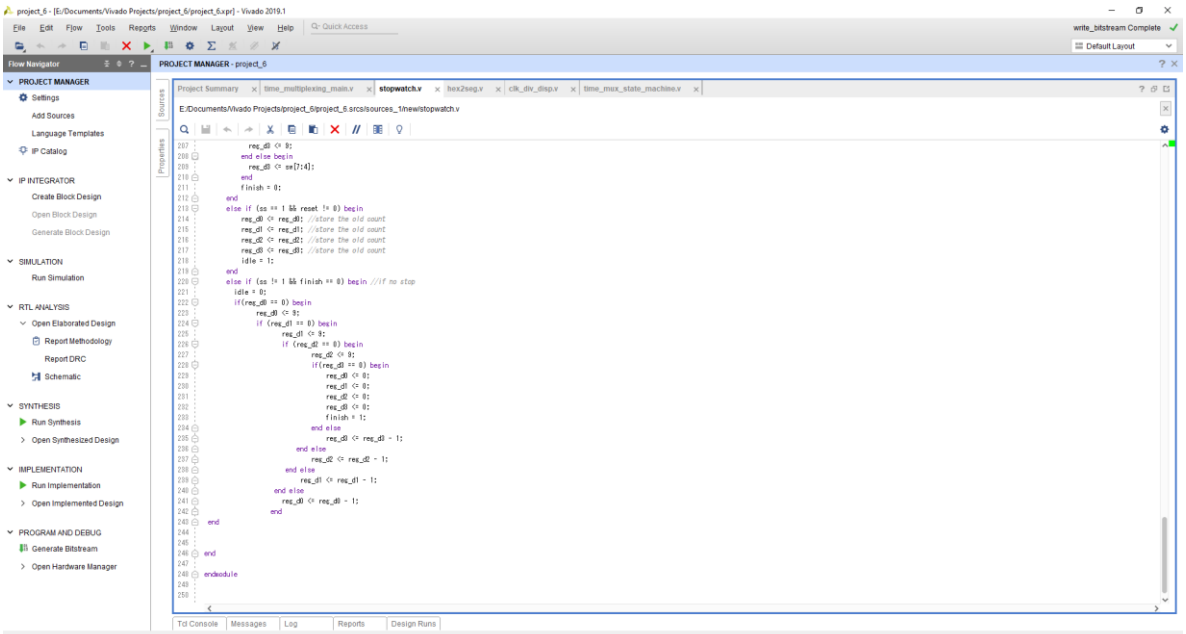
Tcl Console
Messages
Log
Reports
Design Runs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File Edit Flow Tools Reports Window Layout View Help
Quick Access
write_bitstream Complete
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
PROJECT MANAGER - project_6
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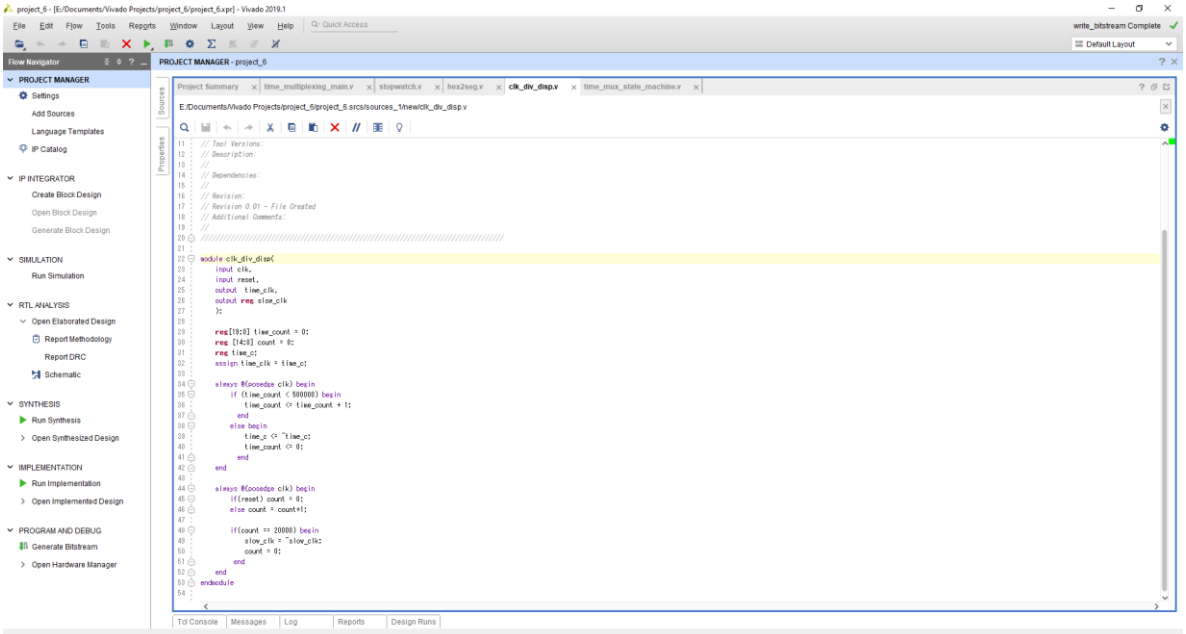
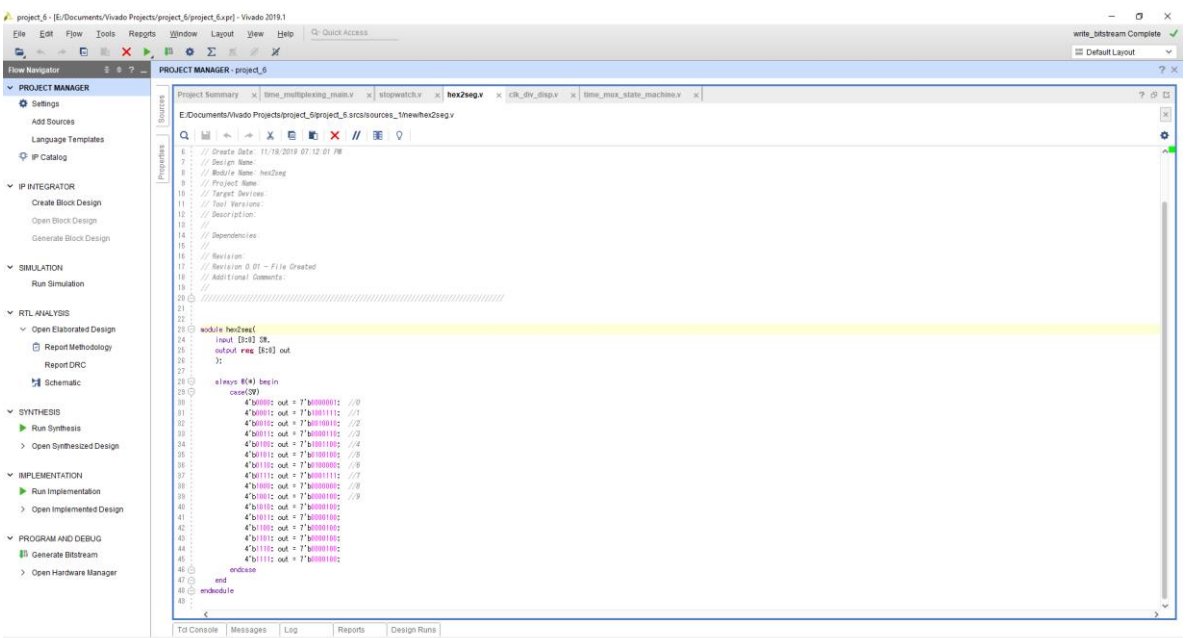
stopwatch.v
hex2seg.v
clk_div_disp.v
time_mux_state_machine.v
E:/Documents/Vivado Projects/project_6/project_6.srcs/sources_1/new/stopwatch.v
Tcl Console
Messages
Log
Reports
Design Runs

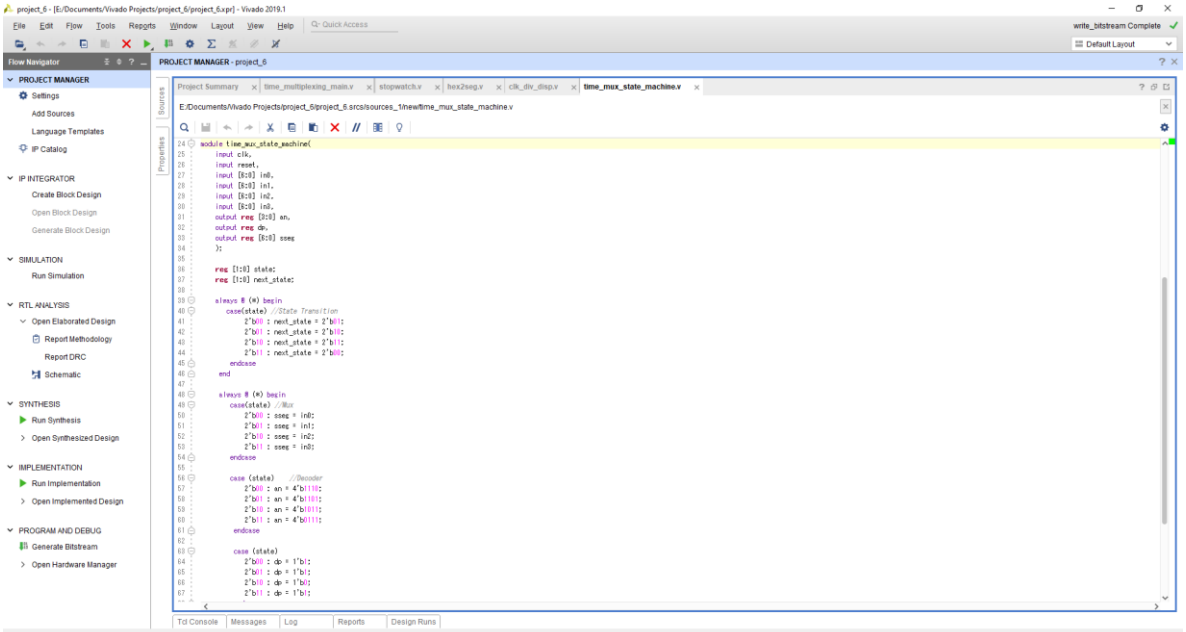
clk_div_disp:

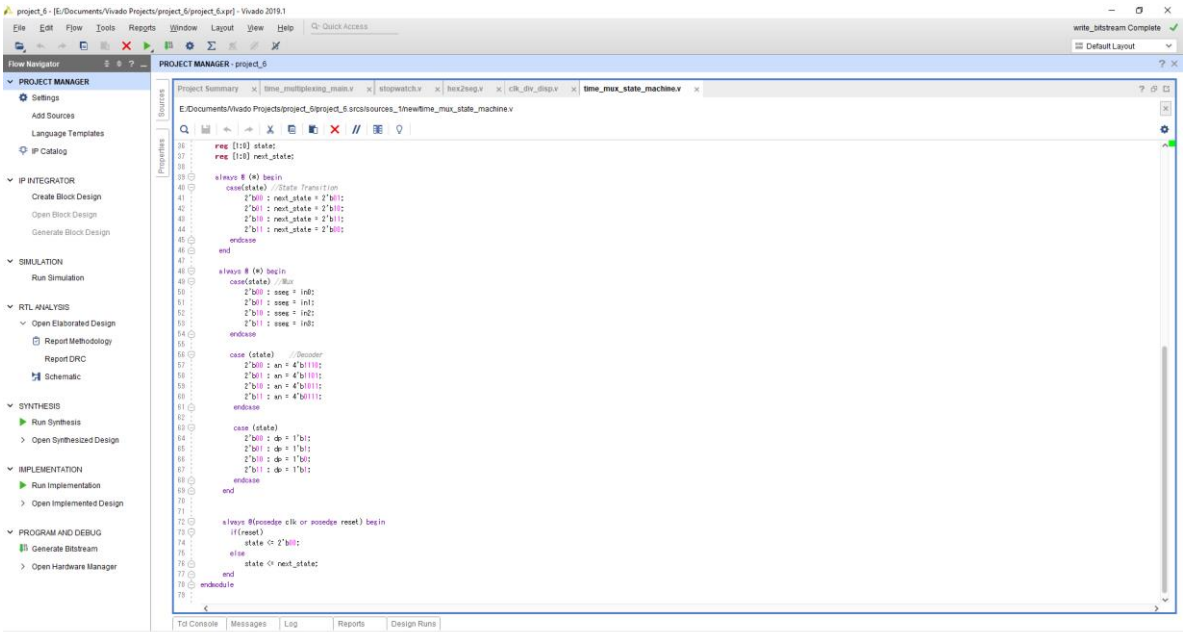


hex2seg:

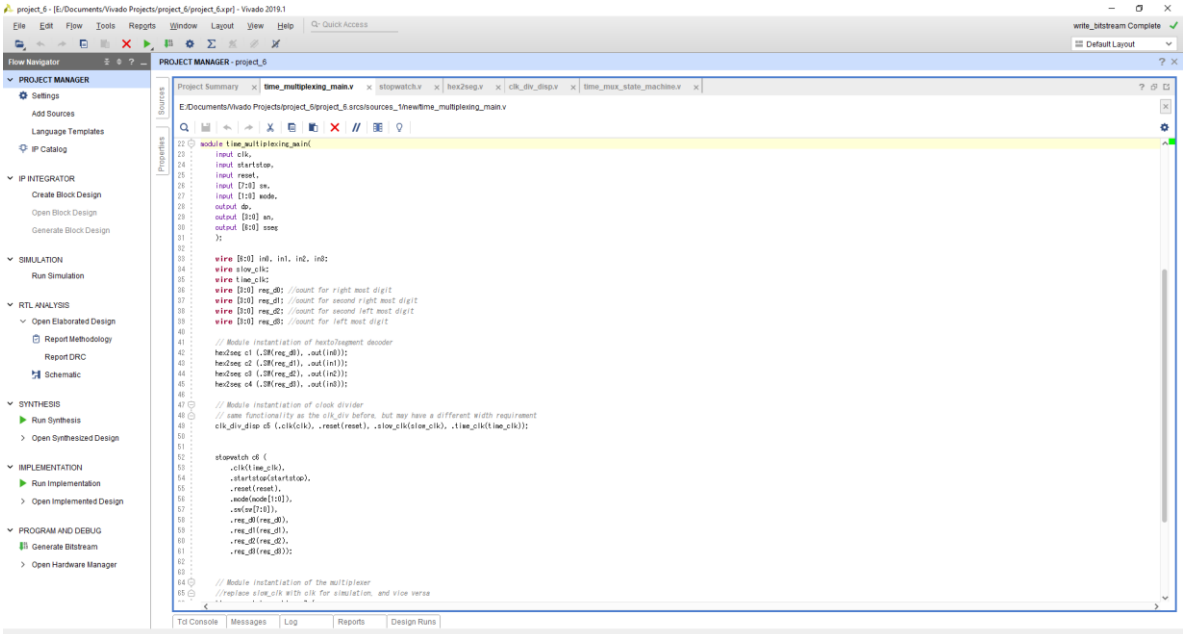


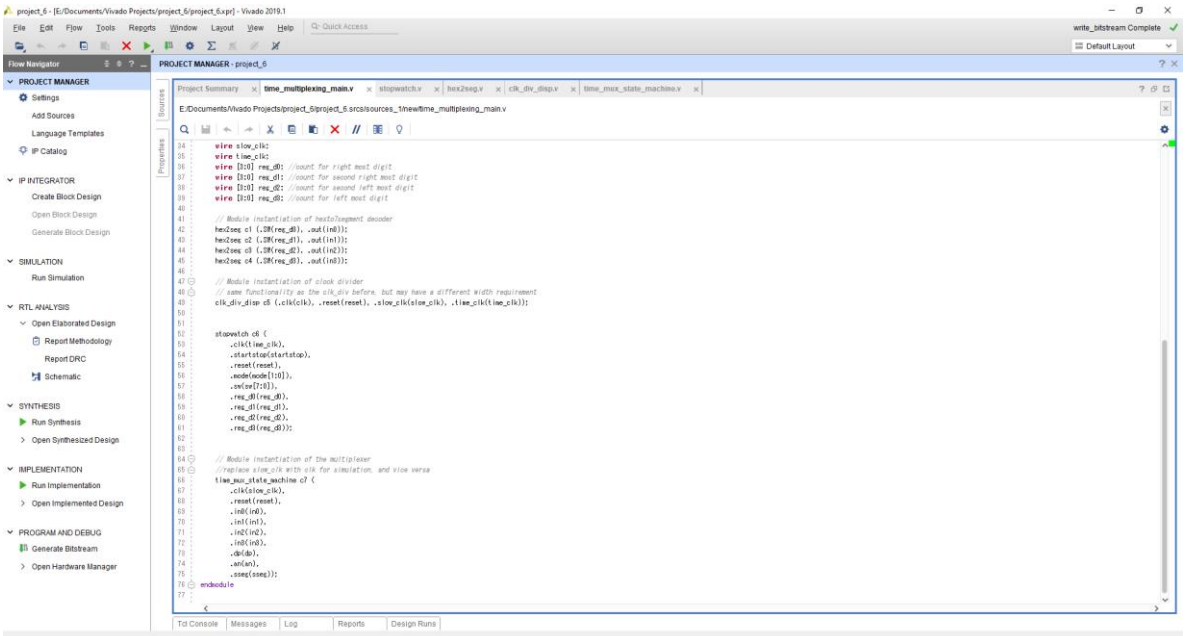
time_mux_state_machine:





time_multiplexing_main:





Testbench:

tb_stopwatch.v

E:/Documents/Vivado Projects/project_6/project_6.srcs/sim_1/new/tb_stopwatch.v

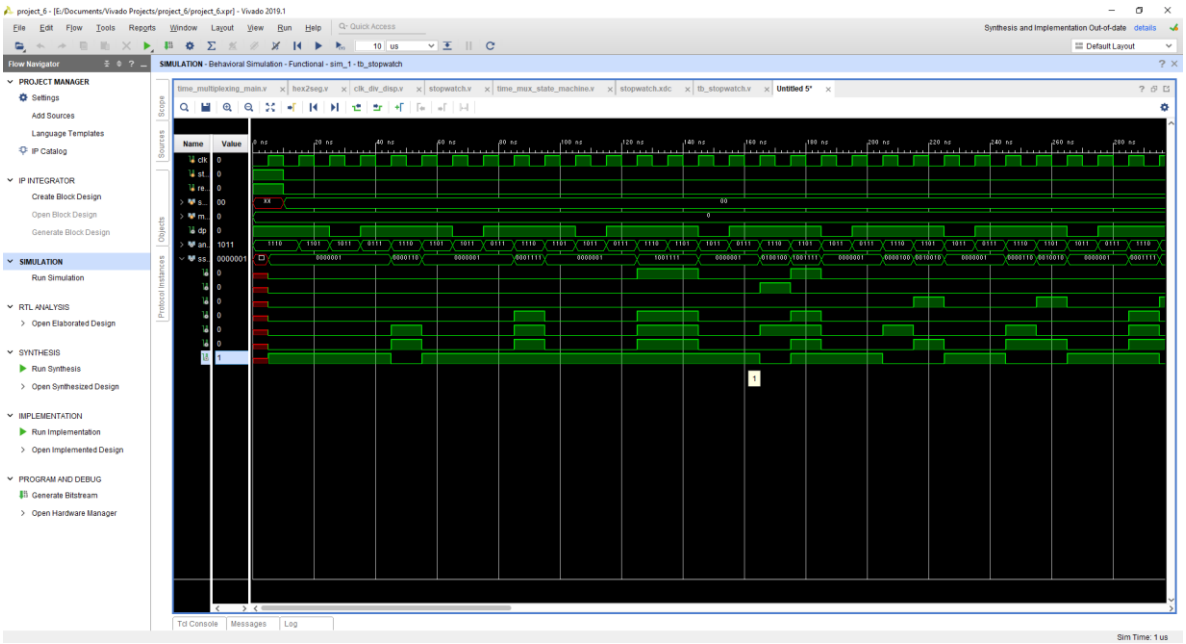
```
module tb_stopwatch;
reg clk;
reg startstop;
reg reset;
reg [7:0] sw;
reg [1:0] mode;
wire dp;
wire [3:0] an;
wire [8:0] sseg;

time_multiplexing_main u1 (
.clk(clk),
.startstop(startstop),
.reset(reset),
.sw(sw),
.mode(mode),
.dp(dp),
.an(an),
.sseg(sseg)
);

initial begin

//Mode 0:
//clk = 0;
//mode = 0;
//startstop = 1;
//reset = 1;
//#10
//startstop = 0;
//reset = 0;
//sw = 8'b00000000;

//Mode 1:
//clk = 0;
//sw = 8'b10001000;
//mode = 1;
//startstop = 1;
//reset = 1;
//#10
//startstop = 0;
//reset = 0;

//Mode 2:
//clk = 0;
//mode = 2;
//startstop = 1;
//reset = 1;
//#10
//startstop = 0;
//reset = 0;

//Mode 3:
```

tb_stopwatch.v

E:/Documents/Vivado Projects/project_6/project_6.srcs/sim_1/new/tb_stopwatch.v

```
.an(an),
.sseg(sseg)
);

initial begin

//Mode 0:
//clk = 0;
//mode = 0;
//startstop = 1;
//reset = 1;
//#10
//startstop = 0;
//reset = 0;
//sw = 8'b00000000;

//Mode 1:
//clk = 0;
//sw = 8'b10001000;
//mode = 1;
//startstop = 1;
//reset = 1;
//#10
//startstop = 0;
//reset = 0;

//Mode 2:
//clk = 0;
//mode = 2;
//startstop = 1;
//reset = 1;
//#10
//startstop = 0;
//reset = 0;

//Mode 3:
//clk = 0;
//sw = 8'b00000001;
//mode = 3;
//startstop = 1;
//reset = 1;
//#10
//startstop = 0;
//reset = 0;

end

always
#5 clk = ~clk;


endmodule
```

Mode 1:


project_6 - [E:/Documents/Vivado Projects/project_6/project_6.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Run Help
Synthesis and Implementation Out-of-date details
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_stopwatch
time_multiplexing_main.v
hex2seg.v
clk_div_disp.v
stopwatch.v
time_mux_state_machine.v
stopwatch.xdc
tb_stopwatch.v
Untitled 5*
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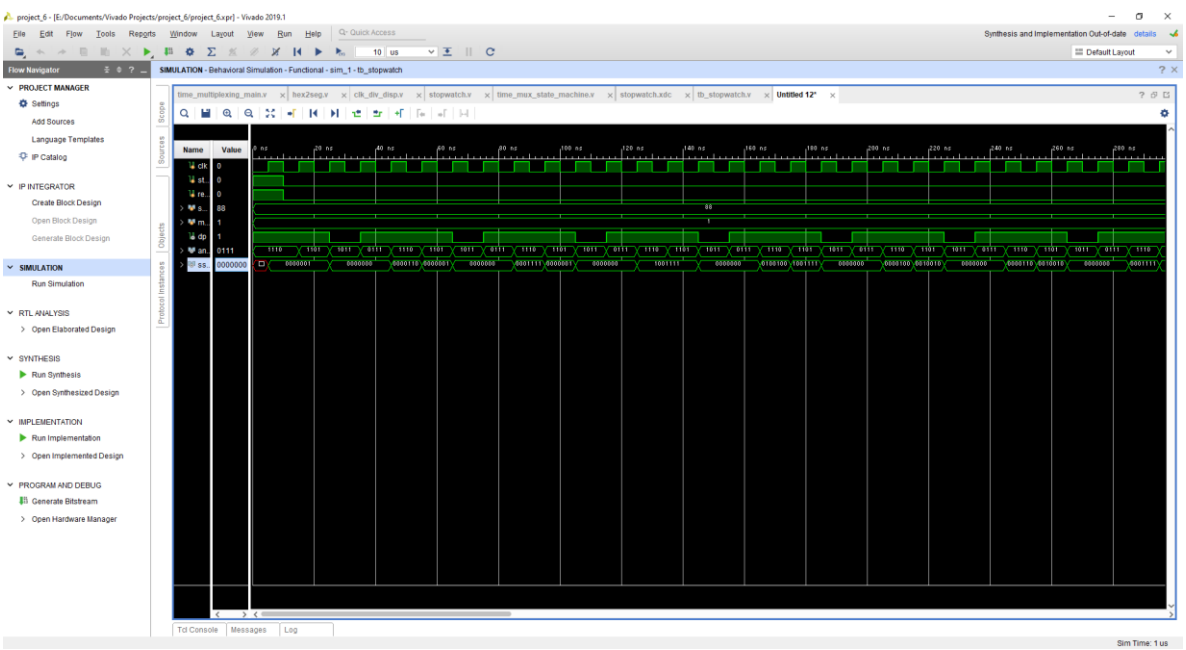
m..
dp
an..
ss..
Tcl Console
Messages
Log
Sim Time: 1 us

Mode 2:


project_6 - [E:/Documents/Vivado Projects/project_6/project_6.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Run Help
Synthesis and Implementation Out-of-date details
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_stopwatch
time_multiplexing_main.v
hex2seg.v
clk_div_disp.v
stopwatch.v
time_mux_state_machine.v
stopwatch.xdc
tb_stopwatch.v
Untitled 12*
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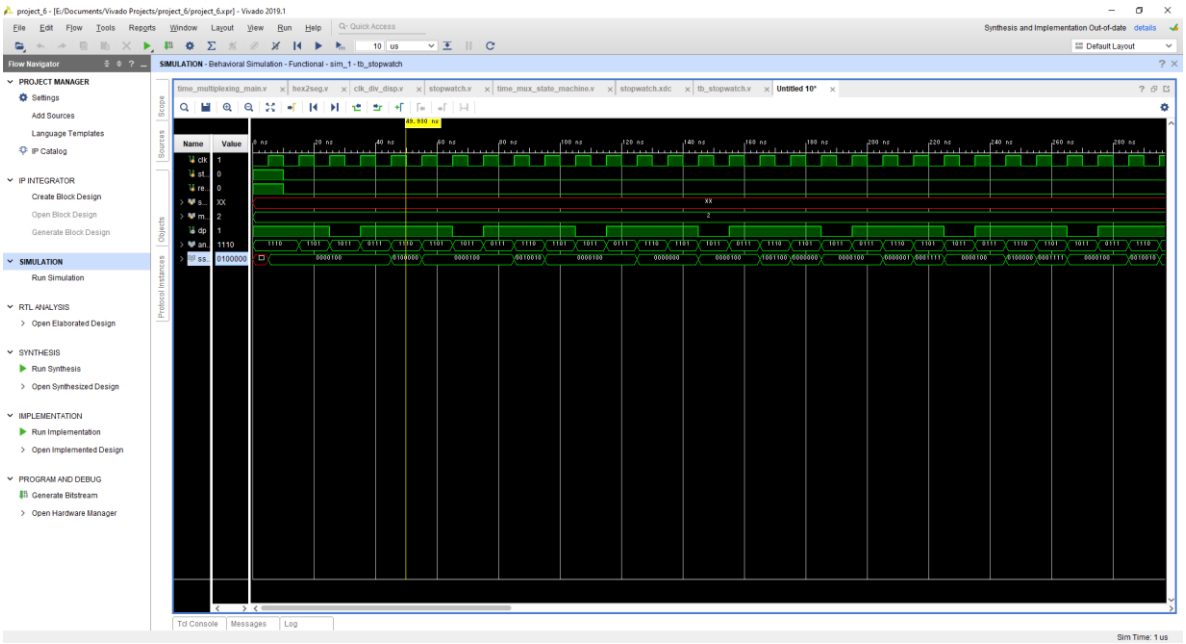
Tcl Console
Messages
Log
Sim Time: 1 us

Mode 3:


project_6 - [E:/Documents/Vivado Projects/project_6/project_6.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Run Help
Synthesis and Implementation Out-of-date details
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_stopwatch
time_multiplexing_main.v
hex2seg.v
clk_div_disp.v
stopwatch.v
time_mux_state_machine.v
stopwatch.xdc
tb_stopwatch.v
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Tcl Console
Messages
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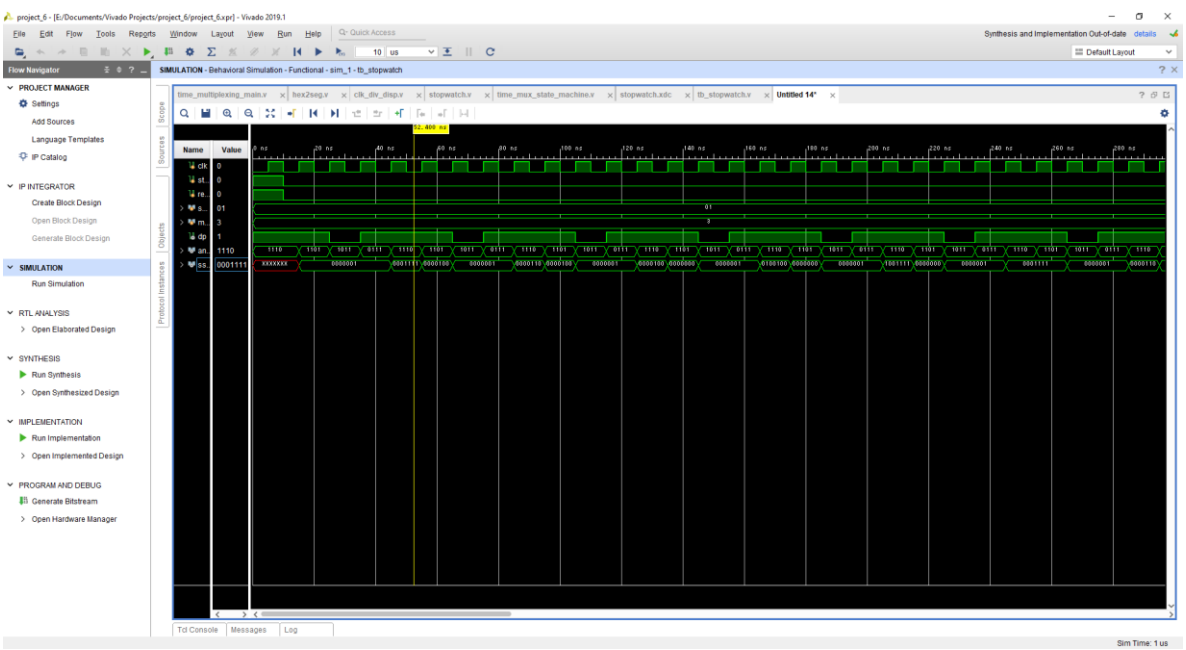
Sim Time: 1 us

Mode 4:


project_6 - [E:/Documents/Vivado Projects/project_6/project_6.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Run Help
Synthesis and Implementation Out-of-date details
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_stopwatch
time_multiplexing_main.v
hex2seg.v
clk_div_disp.v
stopwatch.v
time_mux_state_machine.v
stopwatch.xdc
tb_stopwatch.v
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Tcl Console
Messages
Log
Sim Time: 1 us

Constraints: