

Lab 5 Report

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Section #: 16100

Checklist:

Part 1 –

- i. Design files (.v) for RCA and load register
- ii. Completed testcase table
- iii. Testbench and simulation waveform for the testcases in the table
- iv. Constraints File (Just the uncommented portion)

Part 2 –

- v. All the equations for C_i 's and S_i 's
- vi. Design file (.v) for the CLA
- vii. Constraints File (Just the uncommented portion)
- viii. Simulation waveform for the testcases in the table

Part 3 –

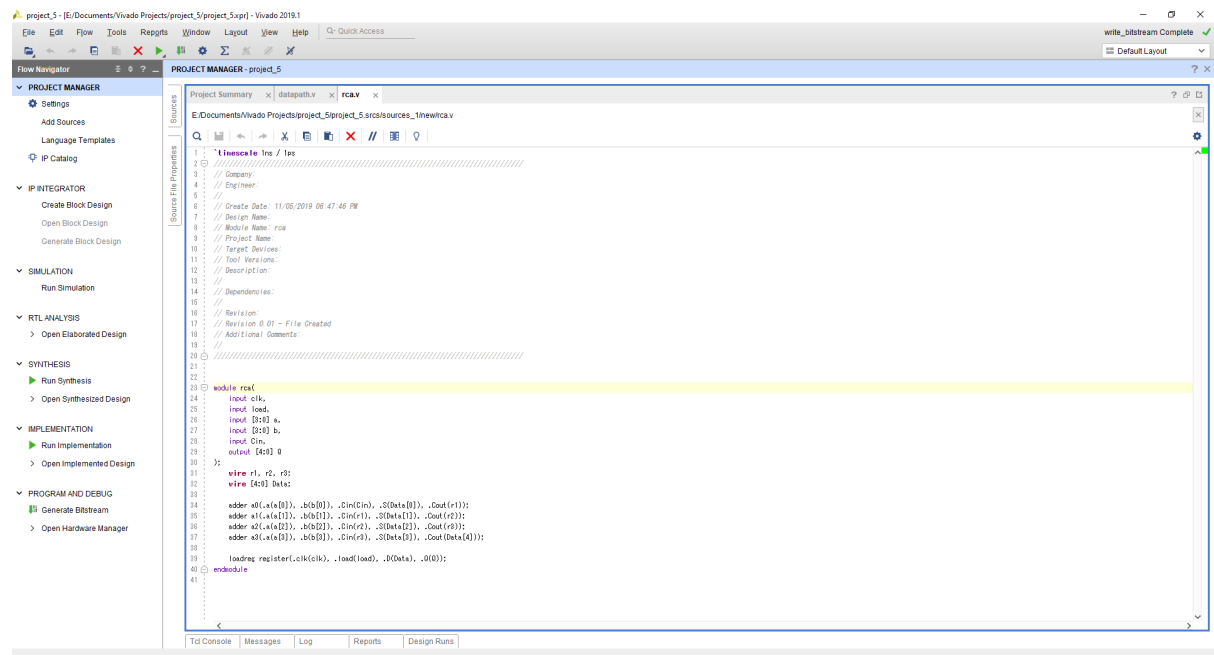
- ix. High-level block diagram of system
- x. Design file for datapath.v
- xi. Testbench and simulation waveform
- xii. Screenshot of full circuit and each adder module
- xiii. Calculations of delay and area for each adder

Note → The Verilog codes and the uncommented portions of the constraint files should be copied in your lab report and the **actual Verilog (.v), Constraint (.xdc) files and Bitstream (.bit) files** need to be zipped and submitted as well on Canvas. You are not allowed to change your codes after final submission as the

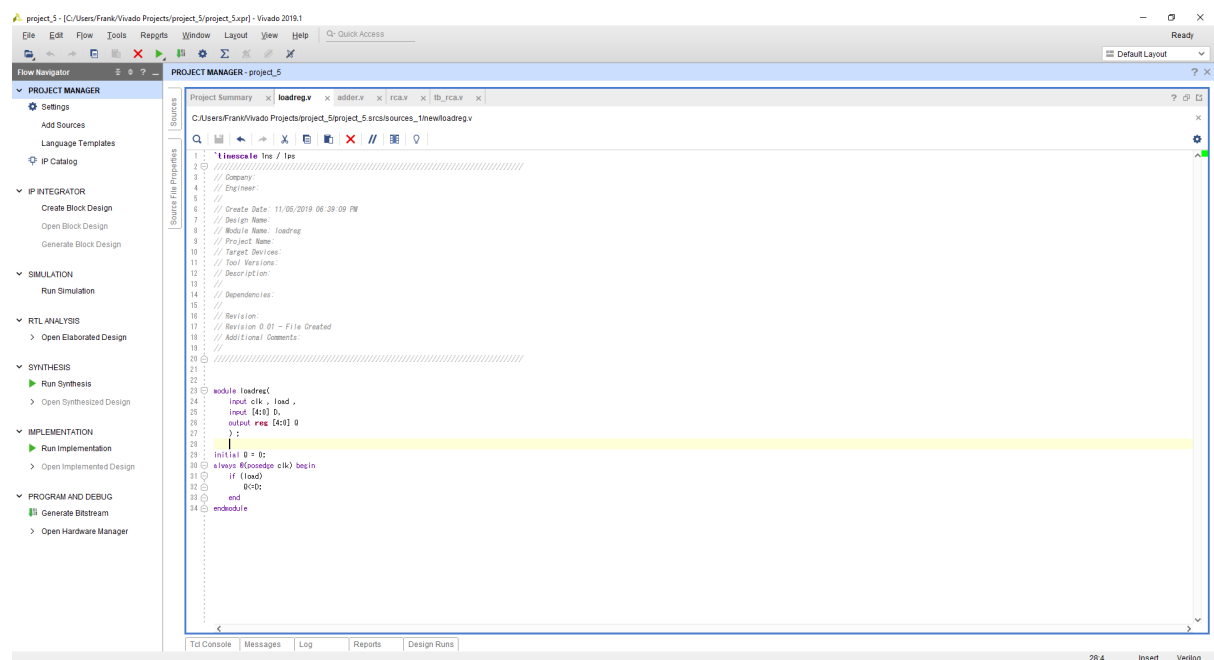
TAs may download the submitted codes or bitstream files from Canvas during checkouts. For the truth Table, K-maps minimizations and algebraic expressions, you are free to draw them on paper and then put the pictures in your lab report, but please make sure it is legible for the TAs to grade it properly.

i) Design files (.v) for RCA and load register

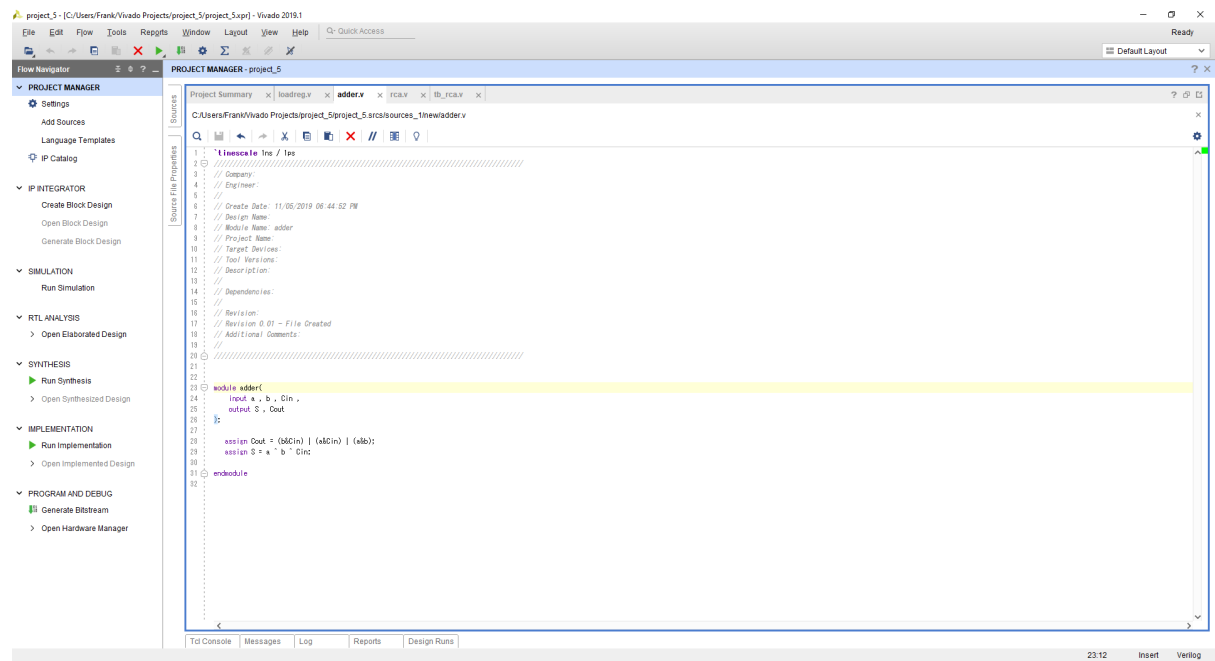
RCA:



Load Register:



Full Adder:

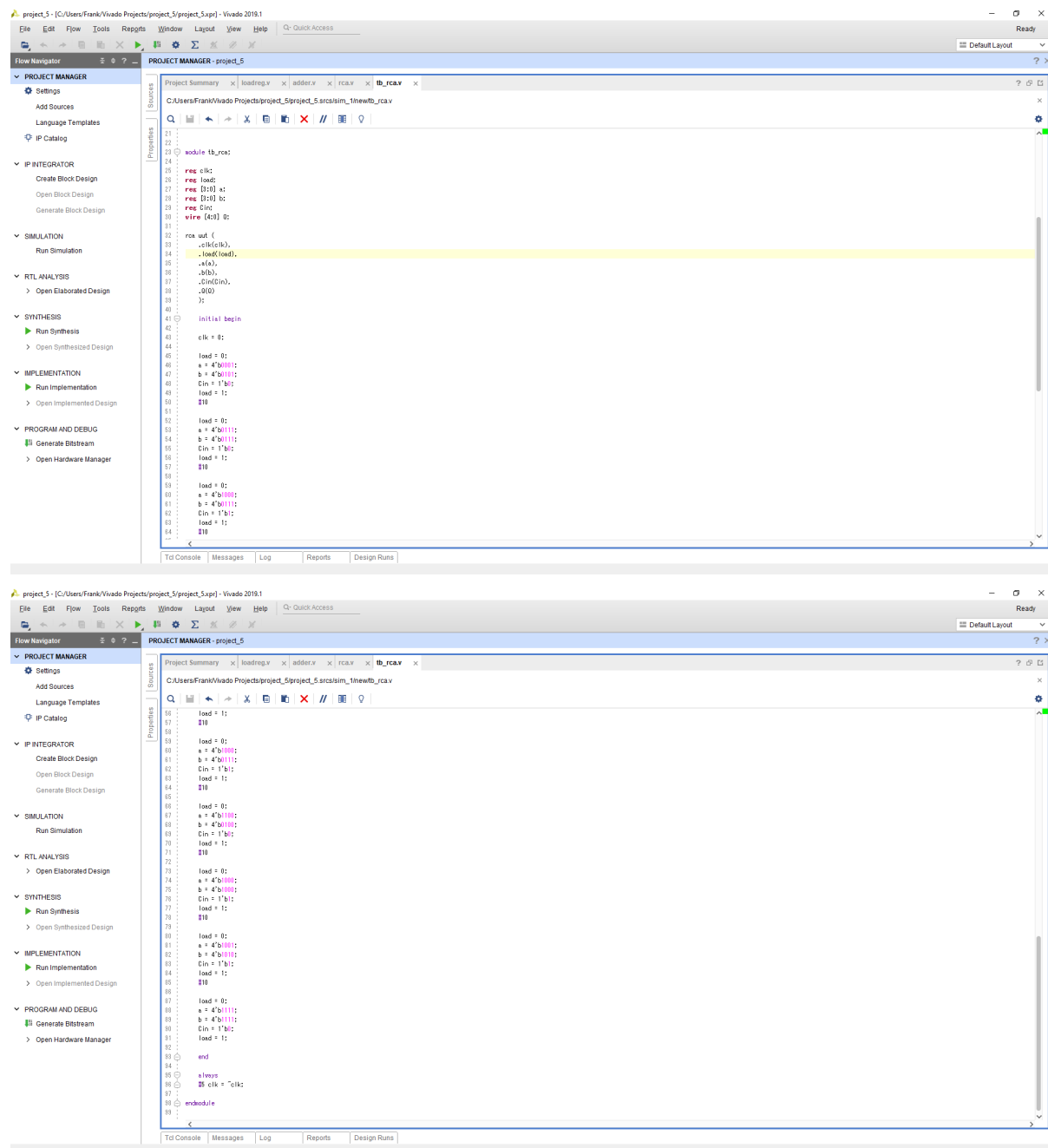


ii) Completed testcase table

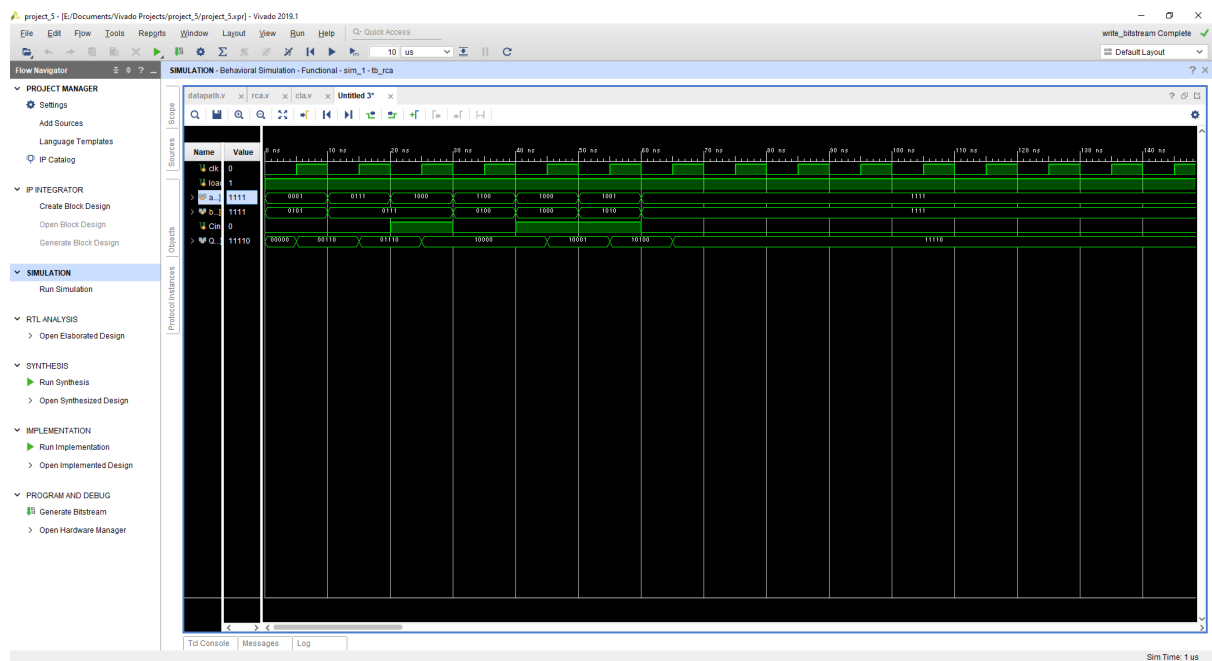
a[3:0]	b[3:0]	Cin	S	Cout
0001	0101	0	0110	0
0111	0111	0	1110	0
1000	0111	1	0000	1
1100	0100	0	0000	1
1000	1000	1	0001	1
1001	1010	1	0100	1
1111	1111	0	1110	1

iii) Testbench and simulation waveform for the testcases in the table

Testbench:



Simulation Waveform:



iv) Constraints File (Just the uncommented portion)

```
1 ## Clock signal
2 set_property PACKAGE_PIN M5 [get_ports clk]
3 set_property IOSTANDARD LVCMOS33 [get_ports clk]
4 create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
5
6 set_property PACKAGE_PIN U10 [get_ports load]
7 set_property IOSTANDARD LVCMOS33 [get_ports load]
8
9 ## LEDs
10 set_property PACKAGE_PIN U10 [get_ports {b[0]}]
11 set_property IOSTANDARD LVCMOS33 [get_ports {b[0]}]
12 set_property PACKAGE_PIN E19 [get_ports {b[1]}]
13 set_property IOSTANDARD LVCMOS33 [get_ports {b[1]}]
14 set_property PACKAGE_PIN U19 [get_ports {b[2]}]
15 set_property IOSTANDARD LVCMOS33 [get_ports {b[2]}]
16 set_property PACKAGE_PIN V19 [get_ports {b[3]}]
17 set_property IOSTANDARD LVCMOS33 [get_ports {b[3]}]
18 set_property PACKAGE_PIN W10 [get_ports {b[4]}]
19 set_property IOSTANDARD LVCMOS33 [get_ports {b[4]}]
20
21 ## Switches
22 set_property PACKAGE_PIN W17 [get_ports {a[0]}]
23 set_property IOSTANDARD LVCMOS33 [get_ports {a[0]}]
24 set_property PACKAGE_PIN Y16 [get_ports {a[1]}]
25 set_property IOSTANDARD LVCMOS33 [get_ports {a[1]}]
26 set_property PACKAGE_PIN W10 [get_ports {a[2]}]
27 set_property IOSTANDARD LVCMOS33 [get_ports {a[2]}]
28 set_property PACKAGE_PIN W17 [get_ports {a[3]}]
29 set_property IOSTANDARD LVCMOS33 [get_ports {a[3]}]
30 set_property PACKAGE_PIN W15 [get_ports {a[0]}]
31 set_property IOSTANDARD LVCMOS33 [get_ports {b[0]}]
32 set_property PACKAGE_PIN W15 [get_ports {a[1]}]
33 set_property IOSTANDARD LVCMOS33 [get_ports {b[1]}]
34 set_property PACKAGE_PIN W14 [get_ports {b[2]}]
35 set_property IOSTANDARD LVCMOS33 [get_ports {b[2]}]
36 set_property PACKAGE_PIN W13 [get_ports {b[3]}]
37 set_property IOSTANDARD LVCMOS33 [get_ports {b[3]}]
38 set_property PACKAGE_PIN W10 [get_ports {cin}]
39 set_property IOSTANDARD LVCMOS33 [get_ports {cin}]
```

v) All the equations for C_i 's and S_i 's

C_i 's:

- $C_0 = C_{in}$
- $C_1 = G_0 + P_0C_0$
- $C_2 = G_1 + P_1G_0 + P_1P_0C_0$
- $C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0$
- $C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_0$

S_i 's:

- $S_0 = P_0 \oplus C_0 = P_0 \oplus (C_{in})$
- $S_1 = P_1 \oplus C_1 = P_1 \oplus (G_0 + P_0C_0)$
- $S_2 = P_2 \oplus C_2 = P_2 \oplus (G_1 + P_1G_0 + P_1P_0C_0)$
- $S_3 = P_3 \oplus C_3 = P_3 \oplus (G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0)$

vi) Design file (.v) for the CLA

```

module cla(
    input clk, load,
    input [3:0] a, b,
    input Cin,
    output [4:0] S,
    output [4:0] Cout);

    wire [4:0] P, G, S;
    wire [4:0] C;

    // P = a ^ b
    // G = a & b
    // S = P ^ C
    // C = P & C

    assign P[0] = a[0] ^ b[0];
    assign P[1] = a[1] ^ b[1];
    assign P[2] = a[2] ^ b[2];
    assign P[3] = a[3] ^ b[3];

    assign G[0] = a[0] & b[0];
    assign G[1] = a[1] & b[1];
    assign G[2] = a[2] & b[2];
    assign G[3] = a[3] & b[3];

    assign C[0] = Cin;
    assign C[1] = (P[0] & G[0]) | G[0];
    assign C[2] = (P[0] & P[1] & G[0]) | (P[1] & G[1]) | G[1];
    assign C[3] = (P[0] & P[1] & P[2] & G[0]) | (P[0] & P[1] & G[1]) | (P[1] & P[2] & G[0]) | (P[2] & G[2]) | G[2];
    assign C[4] = (P[0] & P[1] & P[2] & P[3] & G[0]) | (P[0] & P[1] & P[2] & G[1]) | (P[0] & P[1] & G[2]) | G[3];

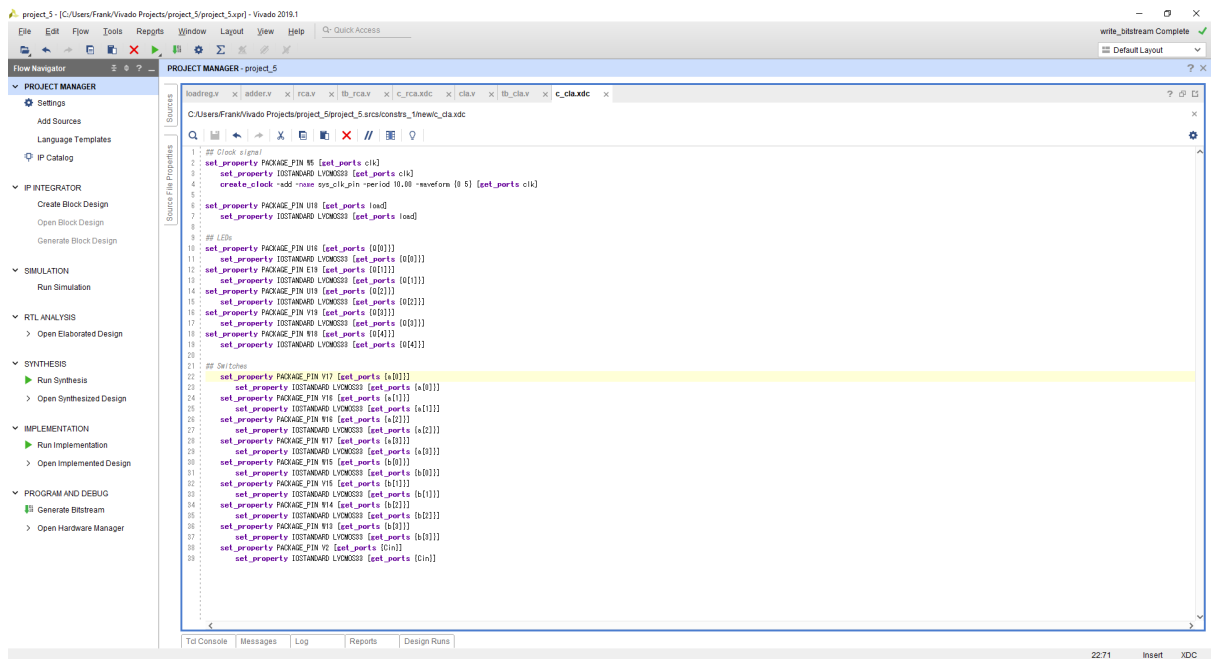
    assign S[0] = P[0] ^ C[0];
    assign S[1] = P[1] ^ C[1];
    assign S[2] = P[2] ^ C[2];
    assign S[3] = P[3] ^ C[3];

    assign Data[4] = C[4];
    assign Data[3:0] = S;

    loadreg register_clk(clk), load(load), .b(Data), .o(Cout);
endmodule

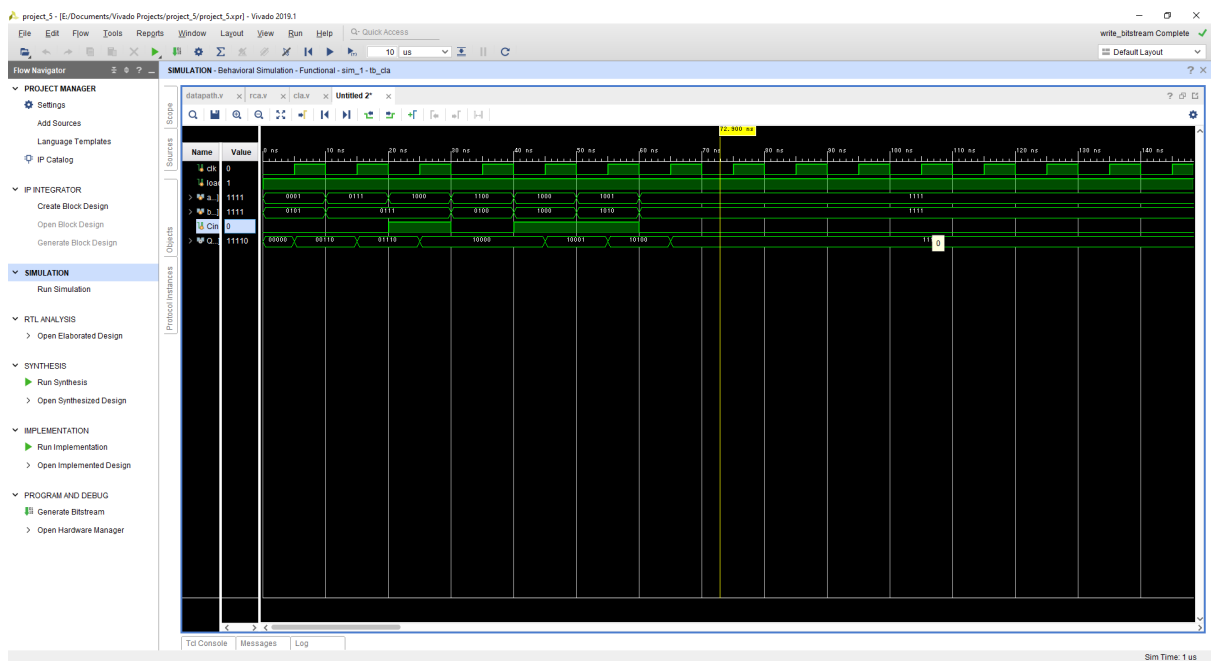
```

vii) Constraints File (Just the uncommented portion)

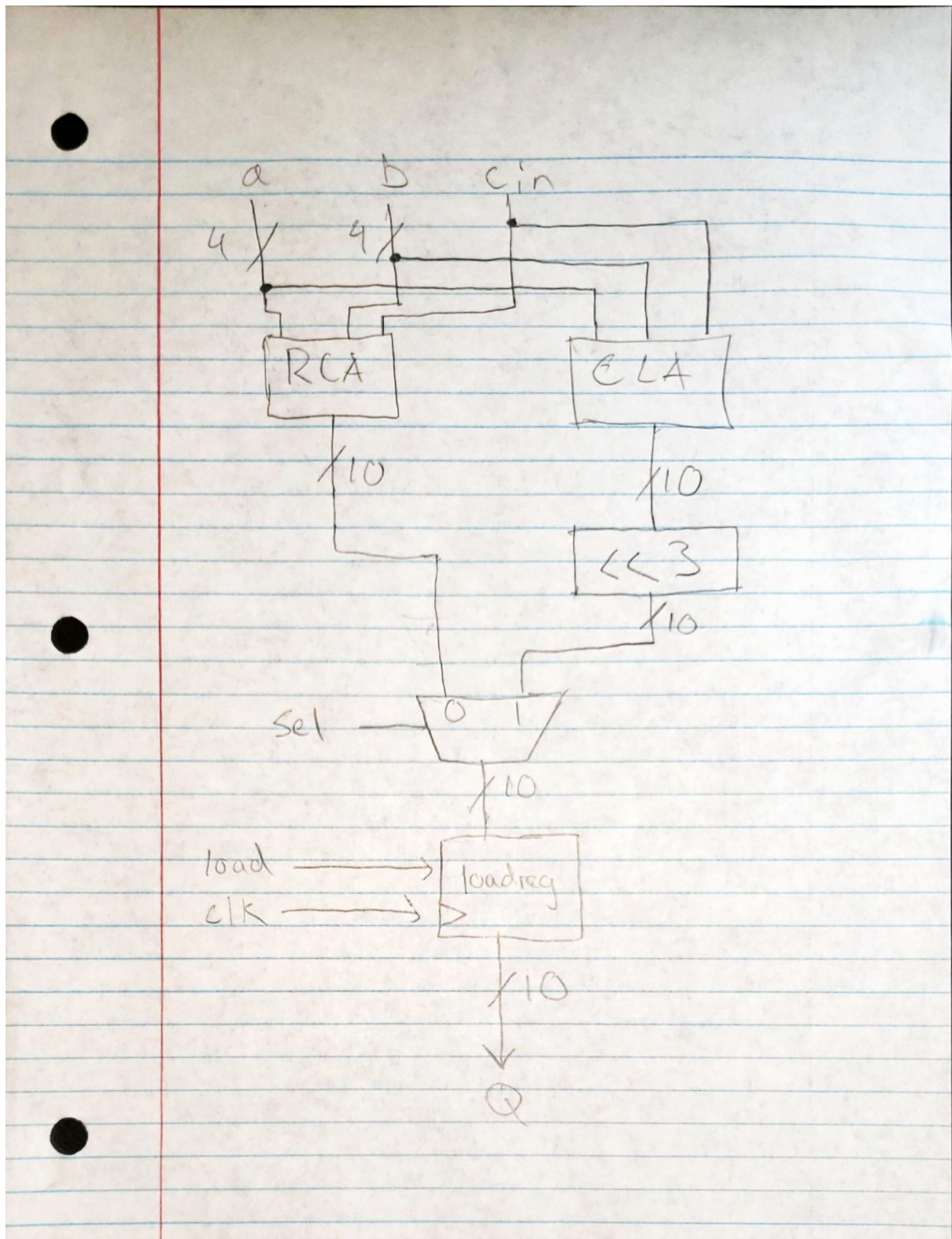


```
1  ## Clock signal
2  set_property PACKAGE_PIN W5 [set_ports clk]
3  set_property IOSTANDARD LVCMOS33 [set_ports clk]
4  create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [set_ports clk]
5
6  set_property PACKAGE_PIN U10 [set_ports load]
7  set_property IOSTANDARD LVCMOS33 [set_ports load]
8
9  ## LEDs
10 set_property PACKAGE_PIN U10 [set_ports {001}]
11 set_property IOSTANDARD LVCMOS33 [set_ports {001}]
12 set_property PACKAGE_PIN E19 [set_ports {011}]
13 set_property IOSTANDARD LVCMOS33 [set_ports {011}]
14 set_property PACKAGE_PIN B19 [set_ports {101}]
15 set_property IOSTANDARD LVCMOS33 [set_ports {101}]
16 set_property PACKAGE_PIN B22 [set_ports {111}]
17 set_property IOSTANDARD LVCMOS33 [set_ports {111}]
18 set_property PACKAGE_PIN B19 [set_ports {014}]
19 set_property IOSTANDARD LVCMOS33 [set_ports {014}]
20
21 ## Switches
22 set_property PACKAGE_PIN Y17 [set_ports {a001}]
23 set_property IOSTANDARD LVCMOS33 [set_ports {a001}]
24 set_property PACKAGE_PIN Y16 [set_ports {a111}]
25 set_property IOSTANDARD LVCMOS33 [set_ports {a111}]
26 set_property PACKAGE_PIN Y16 [set_ports {a211}]
27 set_property IOSTANDARD LVCMOS33 [set_ports {a211}]
28 set_property PACKAGE_PIN Y17 [set_ports {a311}]
29 set_property IOSTANDARD LVCMOS33 [set_ports {a311}]
30 set_property PACKAGE_PIN Y15 [set_ports {b011}]
31 set_property IOSTANDARD LVCMOS33 [set_ports {b011}]
32 set_property PACKAGE_PIN Y15 [set_ports {b111}]
33 set_property IOSTANDARD LVCMOS33 [set_ports {b111}]
34 set_property PACKAGE_PIN Y14 [set_ports {b211}]
35 set_property IOSTANDARD LVCMOS33 [set_ports {b211}]
36 set_property PACKAGE_PIN Y13 [set_ports {b311}]
37 set_property IOSTANDARD LVCMOS33 [set_ports {b311}]
38 set_property PACKAGE_PIN Y10 [set_ports {c011}]
39 set_property IOSTANDARD LVCMOS33 [set_ports {c011}]
```

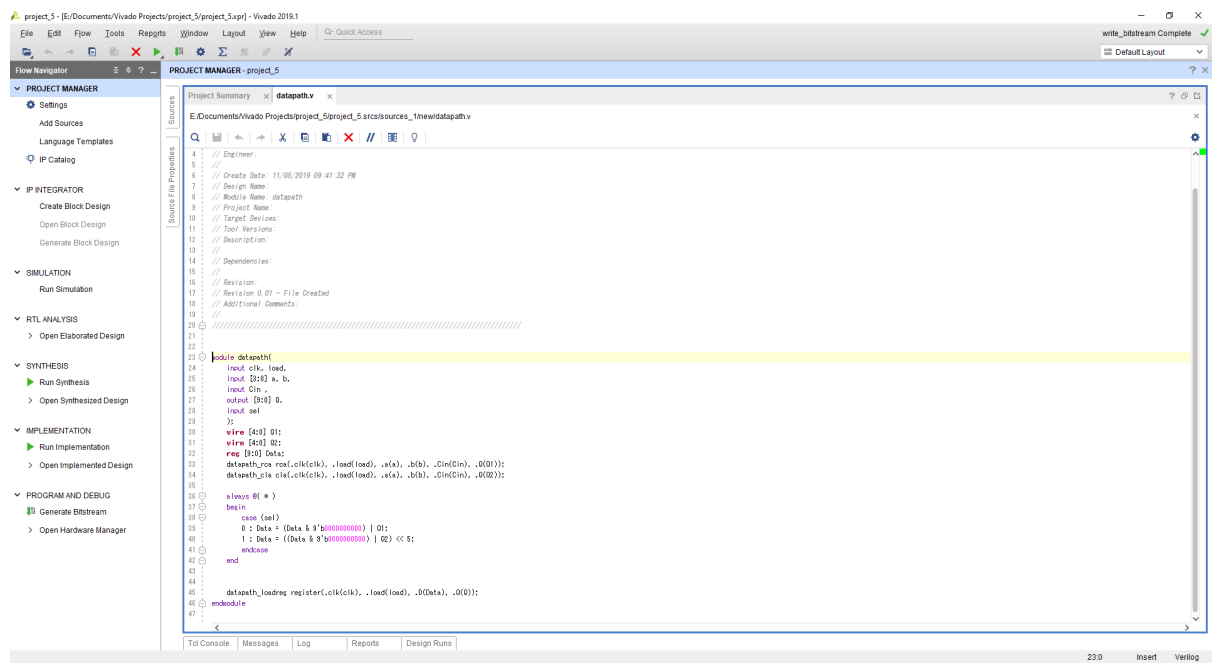
viii) Simulation waveform for the testcases in the table



ix) High-level block diagram of system

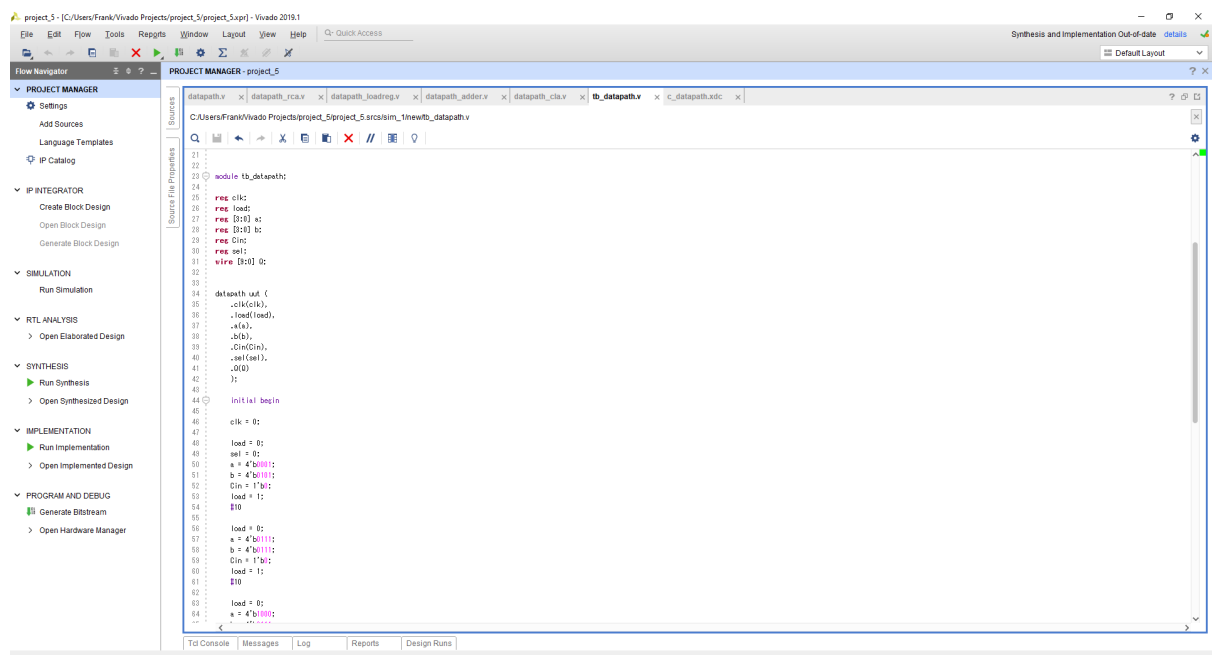


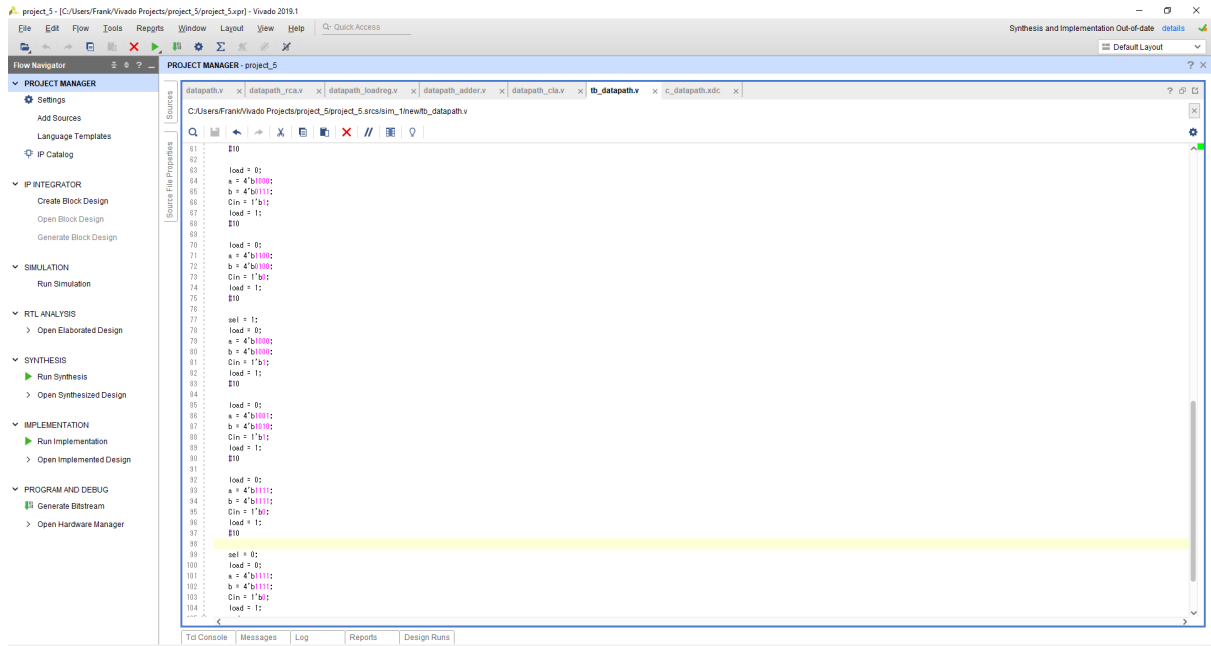
x) Design file for datapath.v



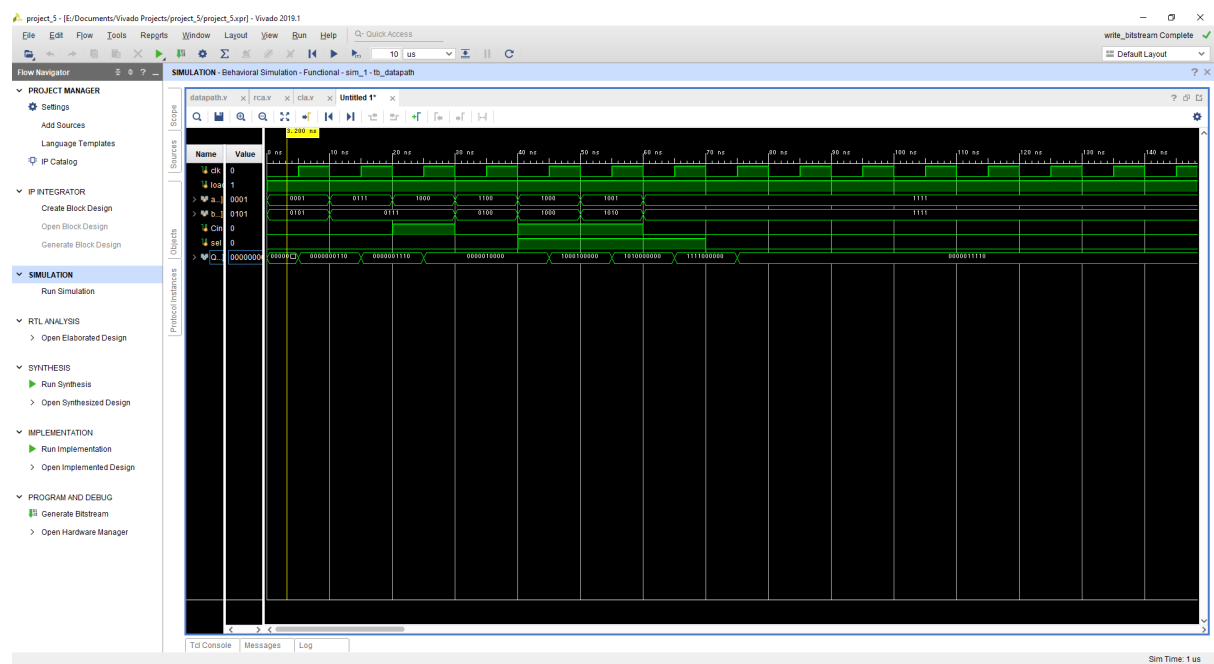
xi) Testbench and simulation waveform

Testbench:

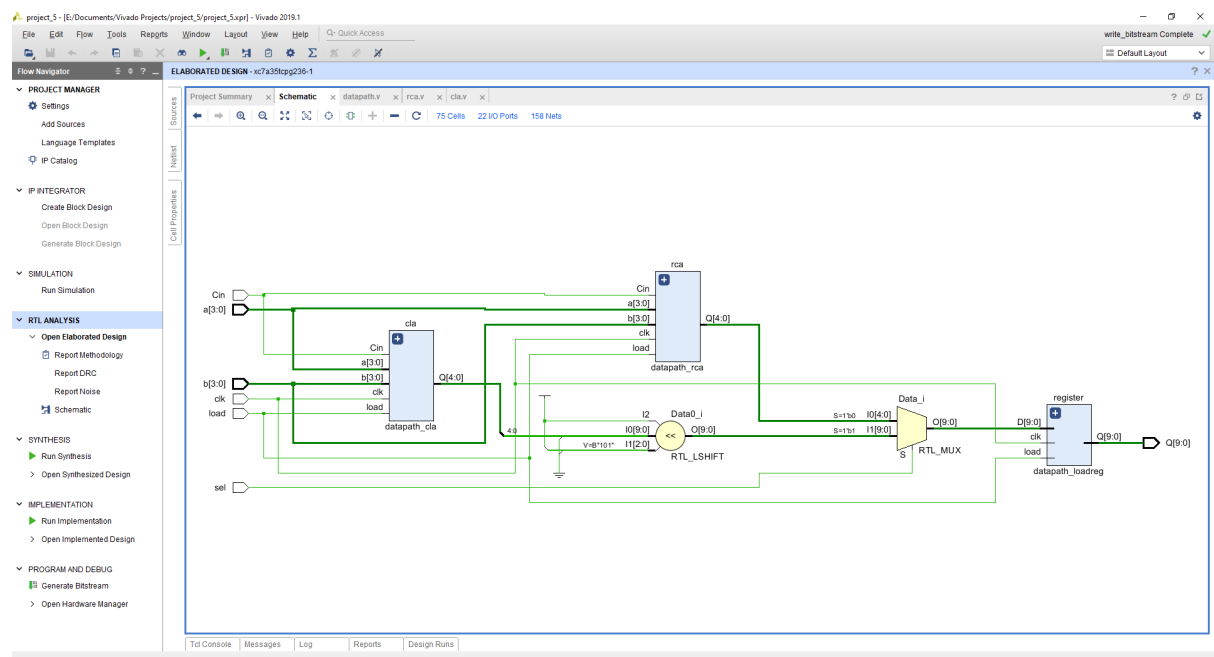




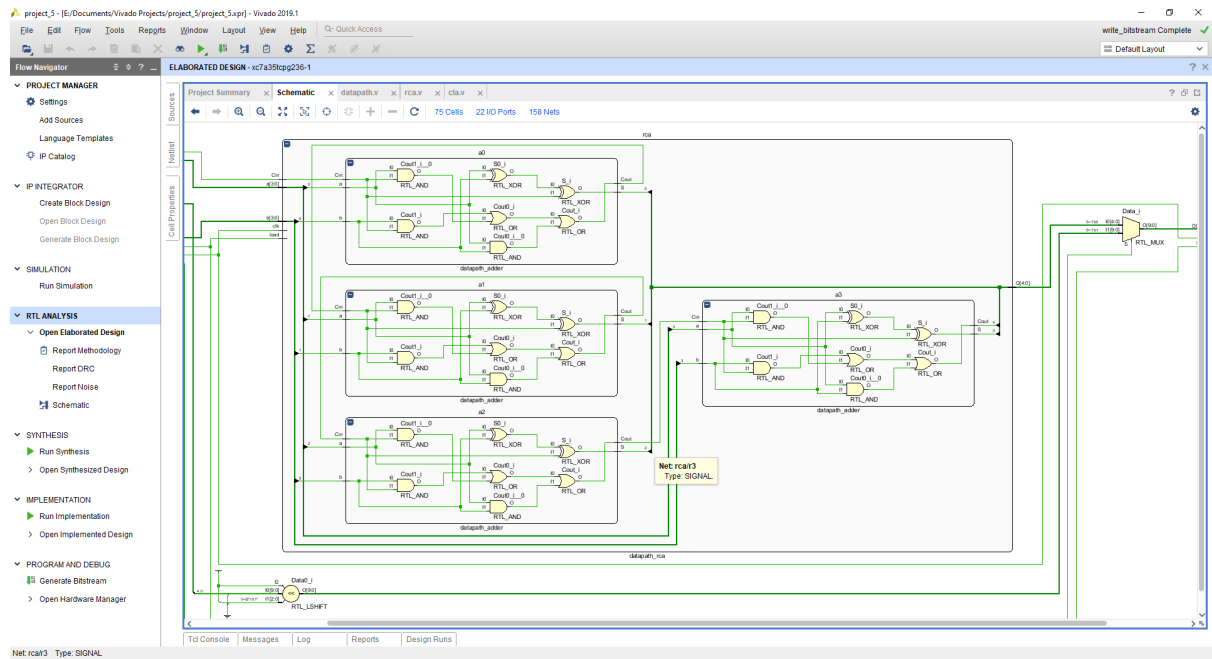
Simulation Waveform:



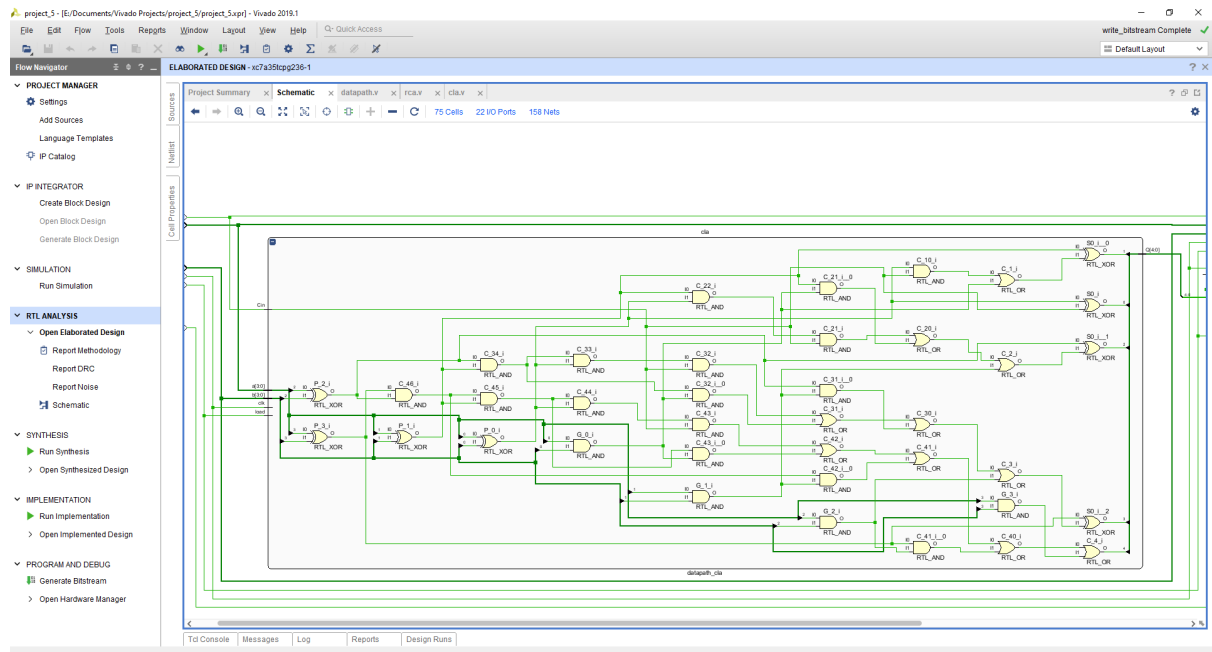
xii) Screenshot of full circuit and each adder module



RCA:



CLA:



xiii) Calculations of delay and area for each adder

RCA:

$$\text{Critical Path} = (3+2+2)*4 = 28 \text{ ns}$$

$$\text{Area} = (6(2) + 4(2) + 2(3))*4 = 104$$

CLA:

$$\text{Critical Path} = 3+3+3+3+3+2+2+2+2 = 23 \text{ ns}$$

$$\text{Area} = 10(4) + 8(6) + 20(2) = 128$$

	Area (area units)	Delay (ns)
RCA	104	28 ns
CLA	128	23 ns