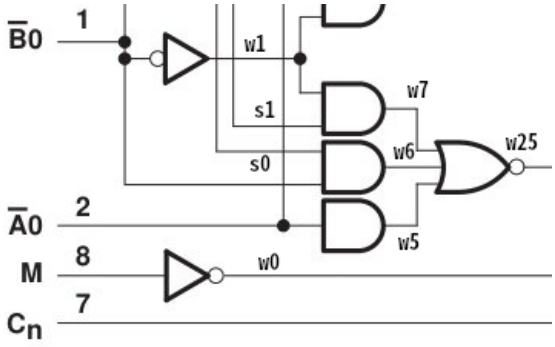
Lab: Specification of Texas Instrument sn74181 ALU

See the background information for the human readable specification of the TI sn74181. The ALU takes two 4-bit inputs, $\overline{A0}$, $\overline{A1}$, $\overline{A2}$, $\overline{A3}$, $\overline{B0}$, $\overline{B1}$, $\overline{B2}$, $\overline{B3}$ plus a carry bit `Cn`, and five selector bits, `S0`, `S1`, `S2`, `S3` and `M`. Depending on the selector bit values, various operations can be performed on the input bits with results appearing on output bits $\overline{G}$, `Cn+4`, $\overline{P}$, `A=B`, $\overline{F0}$. $\overline{F1}$, $\overline{F2}$, $\overline{F3}$. In the following the overbars will not be displayed for simplicity and clarity. In the following a functional specification and a wiring specification for the ALU will be developed and the two will be shown equivalent.

Exercise 1:
Write the specification for the wiring diagram. The following will be a helpful beginning. Consider the following piece of the wiring diagram taken from Page 4 of the TI spec sheet:



Labels have been given to the interconnect points. These labels represent new variables that have logic values as indicated in the wiring specification. For example, `w0` has value `~M` (use `~` for logical not), variable `w1` has value `~B0`, variable `w5` has value `A0` (we remove overbars), variable `w6` has value `s0 /\ B0`, `w7` has value `s1 /\ w1` and `w25` has value `~(w5 \/ w6 \/ w7)`. So, the description of the wiring can begin as a function like this:

```
f74181_netlist c a0 a1 a2 a3 b0 b1 b2 b3 m s0 s1 s2 s3 = [f0,f1,f2,f3,cout,p,g,a_b]
  where
    w0 = ~m
    w1 = ~b0
    w5 = a0
    w6 = s0 /\ b0
    w7 = s1 /\ w1
    w25 = ~(w5 \/ w6 \/ w7)
```

All ALU inputs are the arguments of the function `f74181_netlist`. The output will be a list of ALU outputs in an order that will match the output of a corresponding functional specification. In Cryptol = cannot be a part of a variable label so `a=b` is represent here as `a_b`. Similarly, `cout` is used to represent `Cn+4`. All overbars are removed and lower case letters for variables are used for simplicity and clarity.

Exercise 2:

Write a function `logicStuff` that takes `a0,a1,a2,a3,b0,b1,b2,b3,s0,s1,s2,s3` as input and outputs the results shown in Table 2 of the background human readable specification of the `sn74as181a` for m == True. For example, for

`s=[s3,s2,s1,s0]=[True,True,False,False]=0b1100`,

the output of `logicStuff` is `0b1111`. For `s=0b1010`, and `b=[b3,b2,b1,b0]=0b1110`, the output of `logicStuff` is `b=0b0111`. For `s=0b0111`, `a=0b0011`, and `b=0b1110` the output of `logicStuff` is `0b1000`. Watch out!! Order is critical.

Exercise 3:

Write a function that compares the output of `f74181_spec` with `logicStuff` when `m` is `True` and `c` is `False`. Try it out. Anything not adding up? Watch out!! Order is critical.