Total No. of Pages: 2

Student Name: .....

Enrollment No: .....

Mid-Term Examination – November 2023

Programme: B.Tech (AI-DS/AI-ML/IIOT) **Semester: Fifth Semester (Aug. 2023 - Dec 2023)**

Paper Code: AIDS-307/AIML-307/IIOT-307 **Paper Name: Computer Organization and Architecture**

Time: 1½Hrs. **Maximum Marks: 30**

Note:
- Question No. 1 is compulsory.
- Attempt any two questions from the remaining questions.
- Some questions have internal choice also.
- All questions carry equal marks.
- Only scientific calculator is allowed.

	Question 1	Marks	CO
1(a)	Differentiate between "hit" and "miss" with respect to cache memory	[2.5]	2
1(b)	With the help of a flow chart explain how the interrupts are handled.	[2.5]	1
1(c)	Differentiate between direct and indirect instructions.	[2.5]	1
1(d)	Explain what is virtual memory and what is meant by locality of reference.	[2.5]	2
	Question 2		
2(a)	Represent the following conditional control statement by two register transfer statements with control functions. If (P = 1) then (R1 ← R2) else if (Q = 1) then (R1 ← R3) and draw the block diagram representation for the same. **OR** Register A holds the 8-bit binary 11011001. Determine the B operand and the logic microoperation to be performed in order to change the value in A to: i. 01101101 ii. 11111101	[4]	1
2(b)	A computer uses a memory unit with 512K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 128 registers, and an address part. i. How many bits are there in the operation code, the register code part, and the address part? ii. Draw the instruction word format and indicate the number of bits in each part. iii. How many bits are there in the data and address inputs of the memory?	[6]	1
	Question 3		
3(a)	Explain zero address, one address, two address and three address instructions with the help of an example. **OR**	[4]	2

	Convert the following numerical arithmetic expression into reverse Polish notation and show the stack operations for evaluating the numerical result. $(3 + 4)[10(2 + 6) + 8]$		
3(b)	In detail explain the three different formats for cache mapping.	**[6]**	**2**
	Question 4		**CO**
4(a)	A computer uses RAM chips of 1024×1 capacity. **i.** How many chips are needed, and how should their address lines be connected to provide a memory capacity of 1024 bytes? **ii.** How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus.	**[4]**	**2**
4(b)	The 8-bit registers AR, BR, CR, and DR initially have the following values: AR = 11110010, BR = 11111111, CR = 10111001, DR = 11101010, Determine the 8-bit values in each register after the execution of the following sequence of microoperations. **i.** AR ← AR + BR (Add BR to AR) **ii.** CR ← CR ∧ DR, BR ← BR + 1 (AND DR to CR, increment BR) **iii.** AR ← AR - CR (Subtract CR from AR)	**[6]**	**1**

--XXX--