

## Four 1-Bit, 10MHz, 2nd-Order Delta-Sigma Modulators

### FEATURES

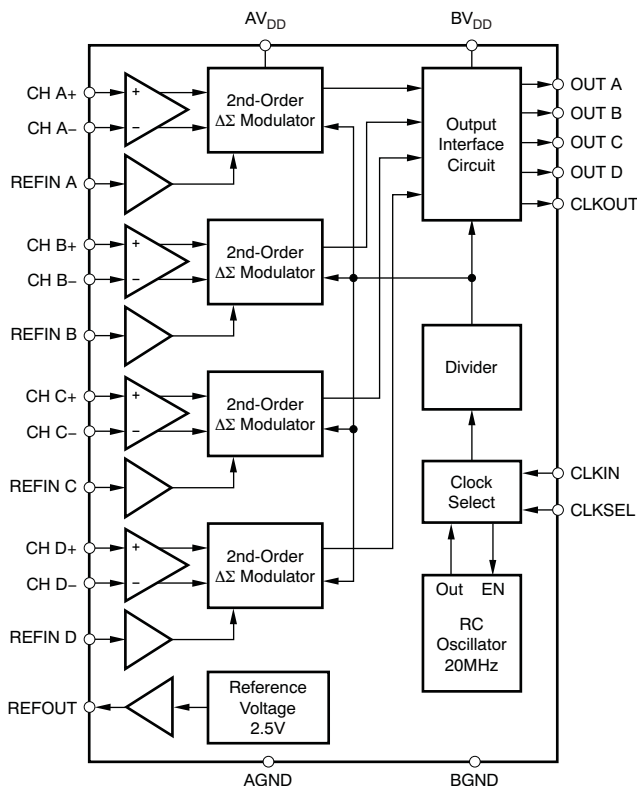
- 16-Bit Resolution
- 14-Bit Linearity
- Resolution/Speed Trade-Off: 10-Bit Effective Resolution with 10 $\mu$ s Signal Delay (12-Bit with 19 $\mu$ s)
- $\pm 2.5$ V Input Range at 2.5V
- Internal Reference Voltage: 2%
- Gain Error: 0.5%
- Four Independent Delta-Sigma Modulators
- Four Input Reference Buffers
- Onboard 20MHz Oscillator
- Selectable Internal or External Clock
- Operating Temperature Range:  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$
- QFN-32 (5x5) Package

### APPLICATIONS

- Motor Control
- Current Measurement
- Industrial Process Control
- Instrumentation
- Smart Transmitters
- Portable Instruments
- Weight Scales
- Pressure Transducers

### DESCRIPTION

The ADS1204 is a four-channel, high-performance device, with four delta-sigma ( $\Delta\Sigma$ ) modulators with 100dB dynamic range, operating from a single +5V supply. The differential inputs are ideal for direct connection to transducers in an industrial environment. With the appropriate digital filter and modulator rate, the device can be used to achieve 16-bit analog-to-digital (A/D) conversion with no missing code. Effective resolution of 12 bits can be obtained with a digital filter data rate of 160kHz at a modulator rate of 10MHz. The ADS1204 is designed for use in medium- to high-resolution measurement applications including current measurements, smart transmitters, industrial process control, weight scales, chromatography, and portable instrumentation. It is available in a QFN-32 (5x5) package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MAXIMUM GAIN ERROR (%)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS1204	±3	±0.5	QFN-32	RHB	–40°C to +105°C	ADS1204I	ADS1204IRHBT	Tape and Reel, 250
							ADS1204IRHBR	Tape and Reel, 3000

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range, unless otherwise noted.

	ADS1204	UNIT
Supply voltage, $AV_{DD}$ to AGND	–0.3 to 6	V
Supply voltage, $BV_{DD}$ to BGND	–0.3 to 6	V
Analog input voltage with respect to AGND	AGND – 0.3 to $AV_{DD} + 0.3$	V
Reference input voltage with respect to AGND	AGND – 0.3 to $AV_{DD} + 0.3$	V
Digital input voltage with respect to BGND	BGND – 0.3 to $BV_{DD} + 0.3$	V
Ground voltage difference, AGND to BGND	±0.3	V
Voltage differences, $BV_{DD}$ to AGND	–0.3 to 6	V
Input current to any pin except supply	±10	mA
Power dissipation	See <a href="#">Dissipation Ratings</a> table	
Operating virtual junction temperature range, $T_J$	–40 to +150	°C
Storage temperature range, $T_{STG}$	–65 to +150	°C
Lead temperature (1.6mm or 1/16" from case for 10s)	260	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, $AV_{DD}$ to AGND	4.75	5	5.25	V
Supply voltage, $BV_{DD}$ to BGND	Low-voltage levels		3.6	V
	5V logic levels		5.5	V
Reference input voltage	0.5	2.5	2.6	V
Operating common-mode signal	0		$AV_{DD}$	V
Analog inputs	+IN – (–IN)		±REFIN	V
External clock <sup>(1)</sup>	16	20	24	MHz
Operating free-air temperature range, $T_A$	–40		+125	°C
Specified free-air temperature range, $T_A$	–40		+105	°C

- (1) With reduced accuracy, clock can go from 1MHz up to 32MHz; see [Typical Characteristic](#) curves.

## DISSIPATION RATINGS

PACKAGE	$T_A \leq +25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A =$ $+25^\circ\text{C}^{(1)}$	$T_A = +70^\circ\text{C}$ POWER RATING	$T_A = +85^\circ\text{C}$ POWER RATING	$T_A = +105^\circ\text{C}$ POWER RATING
QFN-32 (5x5)	3406mW	27.25mW/°C	2180mW	1771mW	1226mW

(1) This is the inverse of the traditional junction-to-ambient thermal resistance ( $R_{\theta JA}$ ). Thermal resistances are not production tested and are for informational purposes only.

## ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$ ,  $AV_{DD} = 5\text{V}$ ,  $BV_{DD} = 3\text{V}$ ,  $CH\ x+ = 0.5\text{V}$  to  $4.5\text{V}$ ,  $CH\ x- = 2.5\text{V}$ ,  $REFIN = REFOUT = \text{internal } +2.5\text{V}$ ,  $CLKIN = 20\text{MHz}$ , and 16-bit Sinc<sup>3</sup> filter with decimation by 256, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS1204			UNIT
			MIN	TYP <sup>(1)</sup>	MAX	
RESOLUTION			16			Bits
DC ACCURACY						
INL	Integral linearity error <sup>(2)</sup>		±1		±3	LSB
			±0.001		±0.005	% FSR
	Integral linearity match				±6	LSB
					±0.009	% FSR
DNL	Differential nonlinearity <sup>(3)</sup>				±1	LSB
V <sub>OS</sub>	Input offset error		−1.4		±3	mV
	Input offset error match				±2	mV
TCV <sub>OS</sub>	Input offset error drift		±2		±8	μV/°C
G <sub>ERR</sub>	Gain error <sup>(4)</sup>	Referenced to V <sub>REF</sub>	±0.08		±0.5	% FSR
	Gain error match		±0.185		±0.5	% FSR
TCG <sub>ERR</sub>	Gain error drift		±2			ppm/°C
PSRR	Power-supply rejection ratio	4.75V < AV <sub>DD</sub> < 5.25V	78			dB
ANALOG INPUT						
FSR	Full-scale differential range	(CH x+) − (CH x−); CH x− = 2.5V			±2.5	V
	Specified differential range	(CH x+) − (CH x−); CH x− = 2.5V			±2	V
	Maximum operating input range <sup>(3)</sup>		0		AV <sub>DD</sub>	V
	Input capacitance	Common-mode	1.5			pF
	Input leakage current	CLK turned off			±1	nA
	Differential input resistance		100			kΩ
	Differential input capacitance		2.5			pF
CMRR	Common-mode rejection ratio	At DC	100			dB
		V <sub>IN</sub> = ±1.25V <sub>PP</sub> at 40kHz	110			dB
BW	Bandwidth	FS sine wave, −3dB	50			MHz
SAMPLING DYNAMICS						
	Internal clock frequency	CLKSEL = 1	8	10	12	MHz
CLKIN	External clock frequency	CLKSEL = 0	1	20	24	MHz

(1) All typical values are at  $T_A = +25^\circ\text{C}$ .

(2) Integral nonlinearity is defined as the maximum deviation of the line through the end points of the specified input range of the transfer curve for  $CH\ x+ = -2\text{V}$  to  $+2\text{V}$  at  $2.5\text{V}$ , expressed either as the number of LSBs or as a percent of measured input range (4V).

(3) Specified by design.

(4) Maximum values, including temperature drift, are specified over the full specified temperature range.

## ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating free-air temperature range at  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $\text{AV}_{\text{DD}} = 5\text{V}$ ,  $\text{BV}_{\text{DD}} = 3\text{V}$ ,  $\text{CH x+} = 0.5\text{V}$  to  $4.5\text{V}$ ,  $\text{CH x-} = 2.5\text{V}$ ,  $\text{REFIN} = \text{REFOUT} = \text{internal } +2.5\text{V}$ ,  $\text{CLKIN} = 20\text{MHz}$ , and 16-bit Sinc<sup>3</sup> filter with decimation by 256, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS1204			UNIT
			MIN	TYP <sup>(1)</sup>	MAX	
AC ACCURACY						
THD	Total harmonic distortion	V <sub>IN</sub> = ±2V <sub>PP</sub> at 5kHz; –40°C ≤ T <sub>A</sub> ≤ +85°C		–96	–88	dB
		V <sub>IN</sub> = ±2V <sub>PP</sub> at 5kHz; –40°C ≤ T <sub>A</sub> ≤ +105°C		–96	–87	dB
SFDR	Spurious-free dynamic range	V <sub>IN</sub> = ±2V <sub>PP</sub> at 5kHz	92	100		dB
SNR	Signal-to-noise ratio	V <sub>IN</sub> = ±2V <sub>PP</sub> at 5kHz	86	89		dB
SINAD	Signal-to-noise + distortion	V <sub>IN</sub> = ±2V <sub>PP</sub> at 5kHz	85	89		dB
	Channel-to-channel isolation <sup>(5)</sup>	V <sub>IN</sub> = ±2V <sub>PP</sub> at 50kHz		85		dB
ENOB	Effective number of bits		14	14.5		Bits
VOLTAGE REFERENCE OUTPUT						
V <sub>OUT</sub>	Reference voltage output		2.450	2.5	2.550	V
dV <sub>OUT</sub> /dT	Output voltage temperature drift			±20		ppm/°C
	Output voltage noise	f = 0.1Hz to 10Hz, C <sub>L</sub> = 10μF		10		μVrms
		f = 10Hz to 10kHz, C <sub>L</sub> = 10μF		12		μVrms
PSRR	Power-supply rejection ratio			60		dB
I <sub>OUT</sub>	Output current			10		μA
I <sub>SC</sub>	Short-circuit current			0.5		mA
	Turn-on settling time	to 0.1% at C <sub>L</sub> = 0		100		μs
VOLTAGE REFERENCE INPUT						
V <sub>IN</sub>	Reference voltage input		0.5	2.5	2.6	V
	Reference input resistance			100		MΩ
	Reference input capacitance			5		pF
	Reference input current				1	μA
DIGITAL INPUTS <sup>(6)</sup>						
	Logic family		CMOS with Schmitt Trigger			
V <sub>IH</sub>	High-level input voltage		0.7 × BV <sub>DD</sub>	BV <sub>DD</sub> + 0.3		V
V <sub>IL</sub>	Low-level input voltage		–0.3	0.3 × BV <sub>DD</sub>		V
I <sub>IN</sub>	Input current	V <sub>I</sub> = BV <sub>DD</sub> or GND		±50		nA
C <sub>I</sub>	Input capacitance			5		pF
DIGITAL OUTPUTS <sup>(6)</sup>						
	Logic family		CMOS			
V <sub>OH</sub>	High-level output voltage	BV <sub>DD</sub> = 4.5V, I <sub>OH</sub> = –100μA	4.44			V
V <sub>OL</sub>	Low-level output voltage	BV <sub>DD</sub> = 4.5V, I <sub>OL</sub> = +100μA		0.5		V
C <sub>O</sub>	Output capacitance			5		pF
C <sub>L</sub>	Load capacitance			30		pF
	Data format		Bit stream			

(5) Specified by design.

(6) Applicable for 5.0V nominal supply:  $\text{BV}_{\text{DD}}(\text{min}) = 4.5\text{V}$  and  $\text{BV}_{\text{DD}}(\text{max}) = 5.5\text{V}$ .

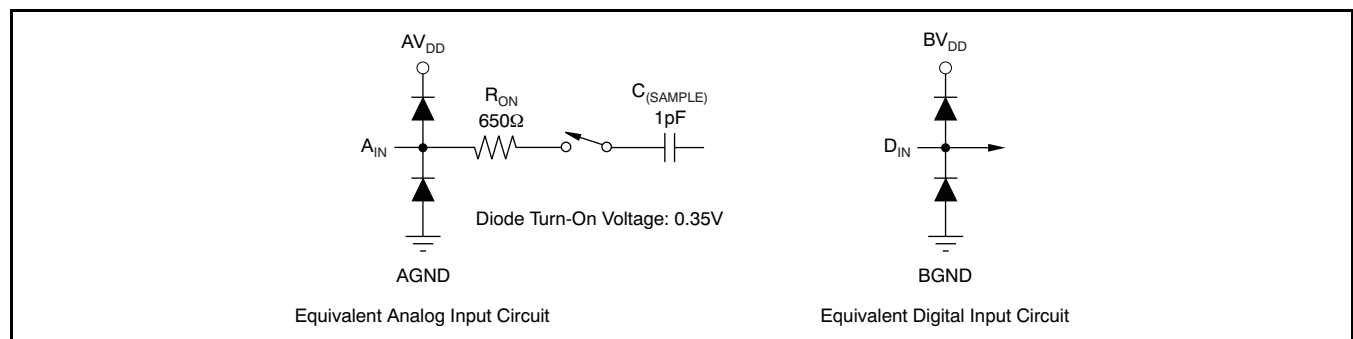
## ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating free-air temperature range at  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $\text{AV}_{\text{DD}} = 5\text{V}$ ,  $\text{BV}_{\text{DD}} = 3\text{V}$ ,  $\text{CH x+} = 0.5\text{V}$  to  $4.5\text{V}$ ,  $\text{CH x-} = 2.5\text{V}$ ,  $\text{REFIN} = \text{REFOUT} = \text{internal } +2.5\text{V}$ ,  $\text{CLKIN} = 20\text{MHz}$ , and 16-bit Sinc<sup>3</sup> filter with decimation by 256, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS1204			UNIT
			MIN	TYP <sup>(1)</sup>	MAX	
DIGITAL INPUTS <sup>(7)</sup>						
	Logic family		LVCMOS			
V <sub>IH</sub>	High-level input voltage	BV <sub>DD</sub> = 3.6V	2	BV <sub>DD</sub> + 0.3		V
V <sub>IL</sub>	Low-level input voltage	BV <sub>DD</sub> = 2.7V	−0.3	0.8		V
I <sub>IN</sub>	Input current	V <sub>I</sub> = BV <sub>DD</sub> or GND		±50		nA
C <sub>I</sub>	Input capacitance		5			pF
DIGITAL OUTPUTS <sup>(7)</sup>						
	Logic family		LVCMOS			
V <sub>OH</sub>	High-level output voltage	BV <sub>DD</sub> = 2.7V, I <sub>OH</sub> = −100μA	BV <sub>DD</sub> − 0.2			V
V <sub>OL</sub>	Low-level output voltage	BV <sub>DD</sub> = 2.7V, I <sub>OL</sub> = +100μA	0.2			V
C <sub>O</sub>	Output capacitance		5			pF
C <sub>L</sub>	Load capacitance		30			pF
	Data format		Bit stream			
POWER SUPPLY						
AV <sub>DD</sub>	Analog supply voltage		4.5	5.5		V
BV <sub>DD</sub>	Buffer I/O supply voltage	Low-voltage levels	2.7	3.6		V
		5V logic levels	4.5	5.5		V
AI <sub>DD</sub>	Analog operating supply current	CLKSEL = 1	22.5		30	mA
		CLKSEL = 0	22.4		29	mA
BI <sub>DD</sub>	Buffer I/O operating supply current	BV <sub>DD</sub> = 3V, CLKOUT = 10MHz			4	mA
		BV <sub>DD</sub> = 5V, CLKOUT = 10MHz			4	mA
	Power dissipation	CLKSEL = 0	122		145	mW
		CLKSEL = 1	112.5		150	mW

(7) Applicable for 3.0V nominal supply:  $\text{BV}_{\text{DD}}$  (min) = 2.7V and  $\text{BV}_{\text{DD}}$  (max) = 3.6V.

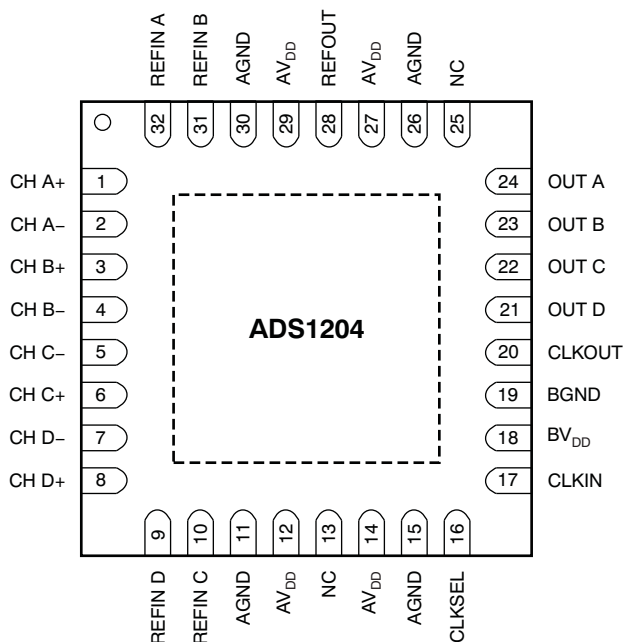
## EQUIVALENT INPUT CIRCUITS



NOTE: The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

## PIN ASSIGNMENTS

**RHB PACKAGE<sup>(1)</sup>**  
**QFN-32**  
**(TOP VIEW)**



(1) The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

## TERMINAL FUNCTIONS

TERMINAL		I/O <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
CH A+	1	AI	Analog input of channel A: noninverting input
CH A–	2	AI	Analog input of channel A: inverting input
CH B+	3	AI	Analog input of channel B: noninverting input
CH B–	4	AI	Analog input of channel B: inverting input
CH C–	5	AI	Analog input of channel C: inverting input
CH C+	6	AI	Analog input of channel C: noninverting input
CH D–	7	AI	Analog input of channel D: inverting input
CH D+	8	AI	Analog input of channel D: noninverting input
REF IN D	9	AI	Reference voltage input of channel D: pin for external reference voltage
REF IN C	10	AI	Reference voltage input of channel C: pin for external reference voltage
AGND	11	—	Analog ground
AVDD	12	P	Analog power supply; nominal 5V
NC	13	—	No connection; this pin is left unconnected
AV <sub>DD</sub>	14	P	Analog power supply; nominal 5V
AGND	15	—	Analog ground
CLKSEL	16	I	Clock select between internal clock (CLKSEL = 1) or external clock (CLKSEL = 0)
CLKIN	17	I	External clock input
BV <sub>DD</sub>	18	P	Digital interface power supply; from 2.7V to 5.5V
BGND	19	—	Interface ground
CLKOUT	20	O	System clock output

(1) AI = Analog Input; AO = Analog Output; I = Input; O = Output; P = Power Supply.

**TERMINAL FUNCTIONS (continued)**

TERMINAL		I/O <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
OUT D	21	O	Bit stream from channel D modulator
OUT C	22	O	Bit stream from channel C modulator
OUT B	23	O	Bit stream from channel B modulator
OUT A	24	O	Bit stream from channel A modulator
NC	25	—	No connection; this pin is left unconnected
AGND	26	—	Analog ground
AV <sub>DD</sub>	27	P	Analog power supply; nominal 5V
REFOUT	28	AO	Reference voltage output: output pin of the internal reference source; nominal 2.5V
AV <sub>DD</sub>	29	P	Analog power supply; nominal 5V
AGND	30	—	Analog ground
REFIN B	31	AI	Reference voltage input of channel B: pin for external reference voltage
REFIN A	32	AI	Reference voltage input of channel A: pin for external reference voltage

## PARAMETER MEASUREMENT INFORMATION

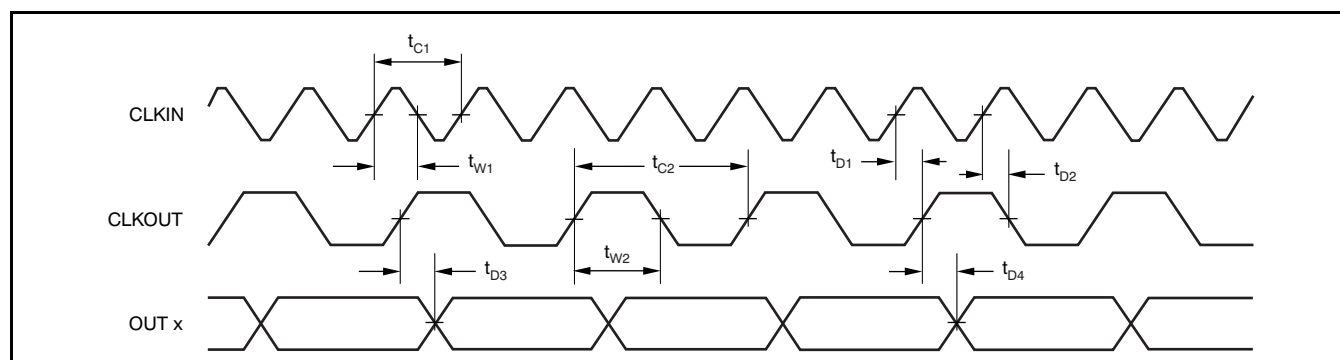


Figure 1. ADS1204 Timing Diagram

### TIMING REQUIREMENTS: 5.0V<sup>(1)</sup>

Over recommended operating free-air temperature range at  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $\text{AV}_{\text{DD}} = 5\text{V}$ , and  $\text{BV}_{\text{DD}} = 5\text{V}$ , unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
$t_{\text{C1}}$	CLKIN period	41.6	1000	ns
$t_{\text{W1}}$	CLKIN high time	10	$t_{\text{C1}} - 10$	ns
$t_{\text{C2}}$	CLKOUT period using internal oscillator (CLKSEL = 1)	83	125	ns
	CLKOUT period using external clock (CLKSEL = 0)	$2 \times t_{\text{C1}}$		ns
$t_{\text{W2}}$	CLKOUT high time	$(t_{\text{C2}}/2) - 5$	$(t_{\text{C2}}/2) + 5$	ns
$t_{\text{D1}}$	CLKOUT rising edge delay after CLKIN rising edge	0	10	ns
$t_{\text{D2}}$	CLKOUT falling edge delay after CLKIN rising edge	0	10	ns
$t_{\text{D3}}$	Data valid delay after rising edge of CLKOUT (CLKSEL = 1)	$(t_{\text{C2}}/4) - 8$	$(t_{\text{C2}}/4) + 8$	ns
$t_{\text{D4}}$	Data valid delay after rising edge of CLKOUT (CLKSEL = 0)	$t_{\text{W1}} - 3$	$t_{\text{W1}} + 7$	ns

(1) Applicable for 5.0V nominal supply:  $\text{BV}_{\text{DD}}(\text{min}) = 4.5\text{V}$  and  $\text{BV}_{\text{DD}}(\text{max}) = 5.5\text{V}$ . All input signals are specified with  $t_{\text{R}} = t_{\text{F}} = 5\text{ns}$  (10% to 90% of  $\text{BV}_{\text{DD}}$ ) and timed from a voltage level of  $(V_{\text{IL}} + V_{\text{IH}})/2$ . See Figure 1.

### TIMING REQUIREMENTS: 3.0V<sup>(1)</sup>

Over recommended operating free-air temperature range at  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $\text{AV}_{\text{DD}} = 5\text{V}$ , and  $\text{BV}_{\text{DD}} = 5\text{V}$ , unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
$t_{\text{C1}}$	CLKIN period	41.6	1000	ns
$t_{\text{W1}}$	CLKIN high time	10	$t_{\text{C1}} - 10$	ns
$t_{\text{C2}}$	CLKOUT period using internal oscillator (CLKSEL = 1)	83	125	ns
	CLKOUT period using external clock (CLKSEL = 0)	$2 \times t_{\text{C1}}$		ns
$t_{\text{W2}}$	CLKOUT high time	$(t_{\text{C2}}/2) - 5$	$(t_{\text{C2}}/2) + 5$	ns
$t_{\text{D1}}$	CLKOUT rising edge delay after CLKIN rising edge	0	10	ns
$t_{\text{D2}}$	CLKOUT falling edge delay after CLKIN rising edge	0	10	ns
$t_{\text{D3}}$	Data valid delay after rising edge of CLKOUT (CLKSEL = 1)	$(t_{\text{C2}}/4) - 8$	$(t_{\text{C2}}/4) + 8$	ns
$t_{\text{D4}}$	Data valid delay after rising edge of CLKOUT (CLKSEL = 0)	$t_{\text{W1}} - 3$	$t_{\text{W1}} + 7$	ns

(1) Applicable for 3.0V nominal supply:  $\text{BV}_{\text{DD}}(\text{min}) = 2.7\text{V}$  and  $\text{BV}_{\text{DD}}(\text{max}) = 3.6\text{V}$ . All input signals are specified with  $t_{\text{R}} = t_{\text{F}} = 5\text{ns}$  (10% to 90% of  $\text{BV}_{\text{DD}}$ ) and timed from a voltage level of  $(V_{\text{IL}} + V_{\text{IH}})/2$ . See Figure 1.



## TYPICAL CHARACTERISTICS

$AV_{DD} = 5V$ ,  $BV_{DD} = 3V$ ,  $CH_{x+} = +0.5V$  to  $+4.5V$ ,  $CH_{x-} = +2.5V$ ,  $REFIN$  = external,  $CLKSEL = 0$ , and 16-bit Sinc<sup>3</sup> filter, with  $OSR = 256$ , unless otherwise noted.

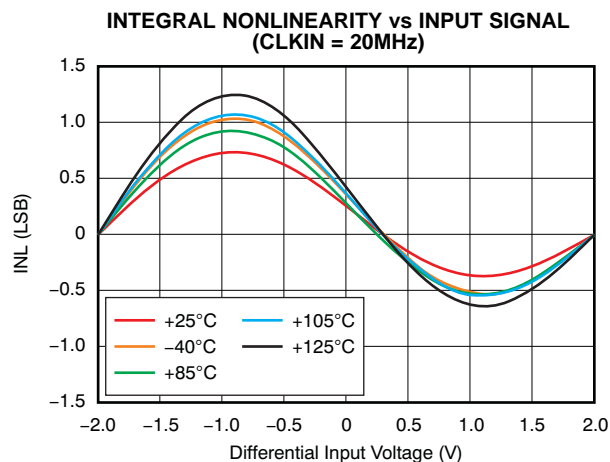


Figure 2.

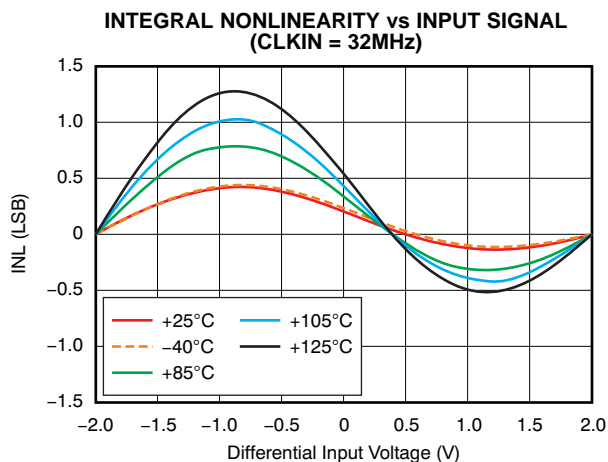


Figure 3.

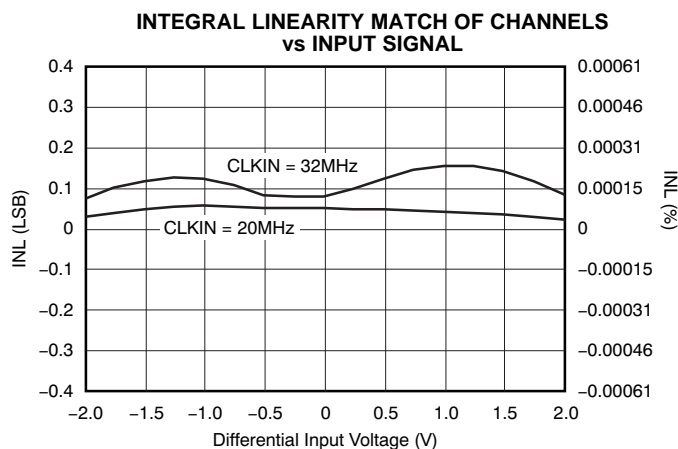


Figure 4.

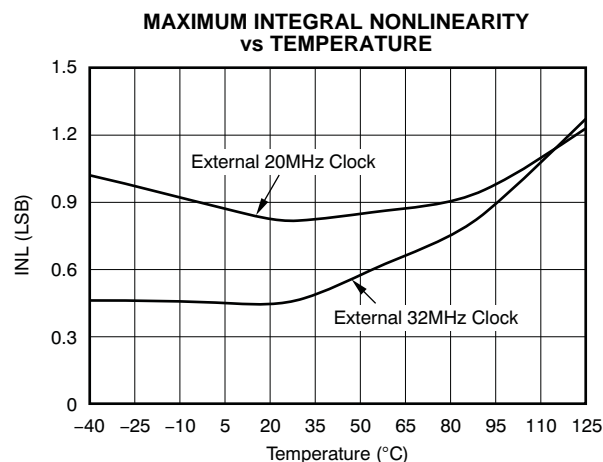


Figure 5.

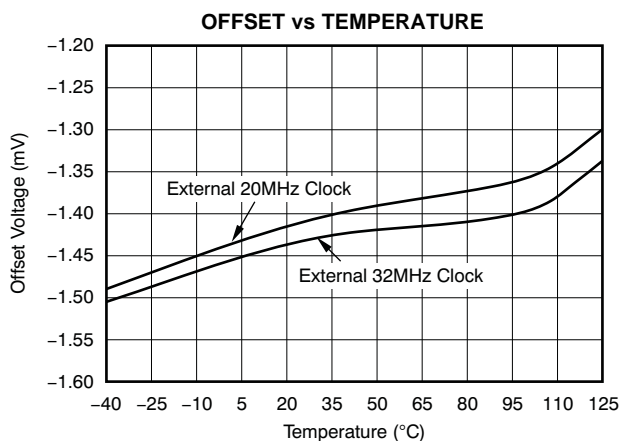


Figure 6.

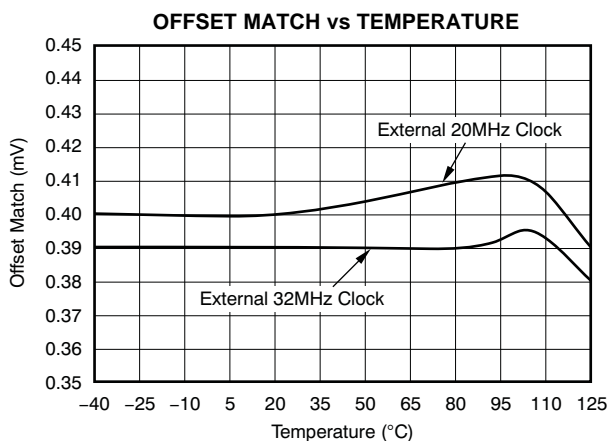


Figure 7.

## TYPICAL CHARACTERISTICS (continued)

$AV_{DD} = 5V$ ,  $BV_{DD} = 3V$ ,  $CH\ x+ = +0.5V$  to  $+4.5V$ ,  $CH\ x- = +2.5V$ ,  $REFIN = \text{external}$ ,  $CLKSEL = 0$ , and 16-bit Sinc<sup>3</sup> filter, with  $OSR = 256$ , unless otherwise noted.

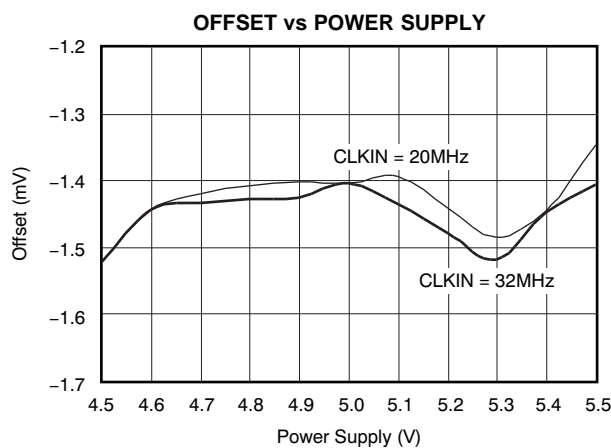


Figure 8.

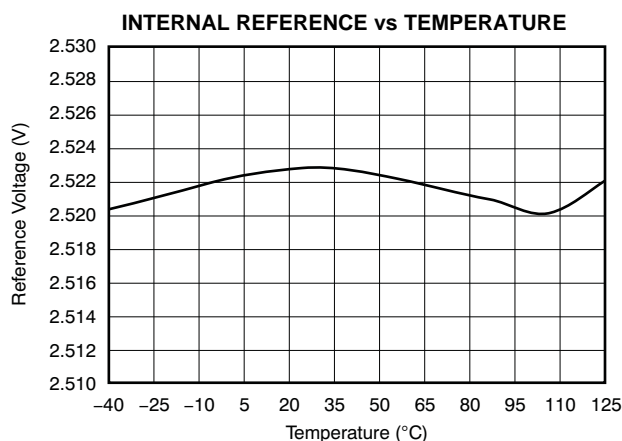


Figure 9.

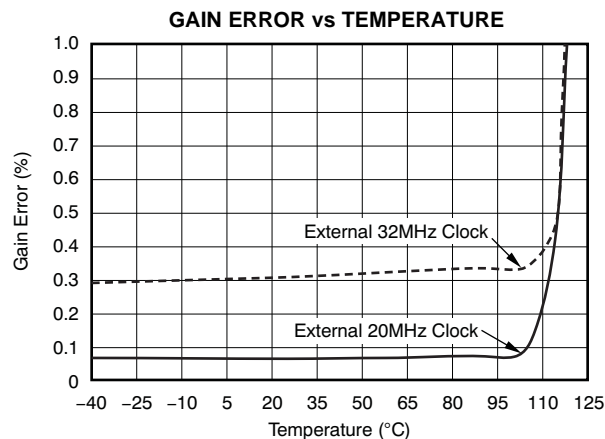


Figure 10.

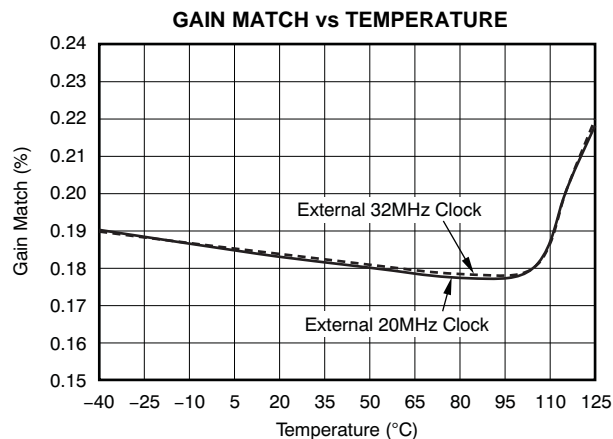


Figure 11.

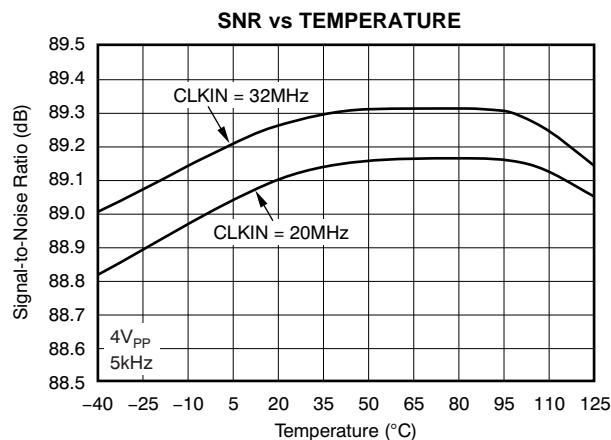


Figure 12.

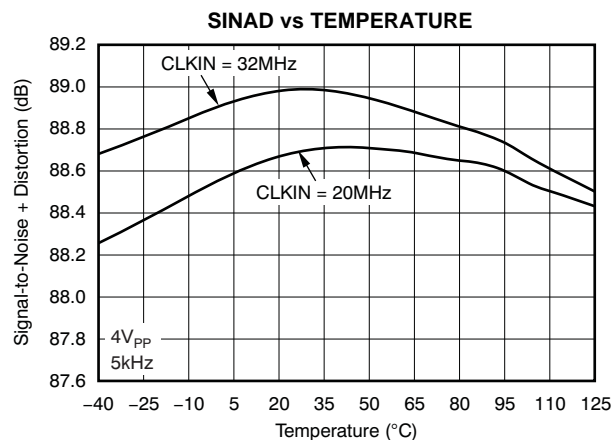
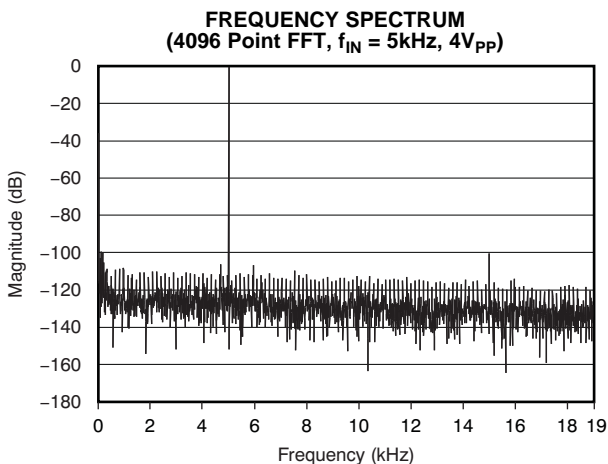
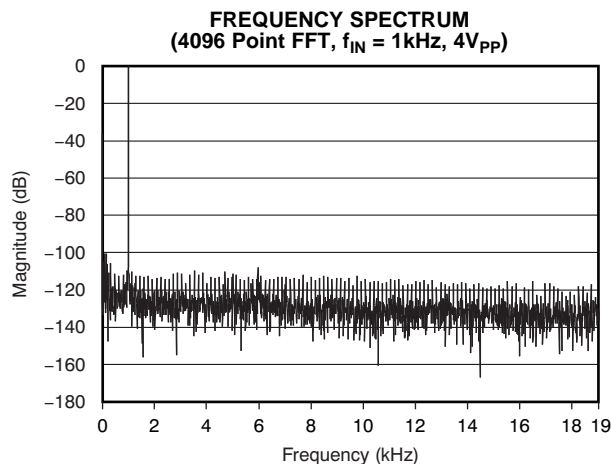
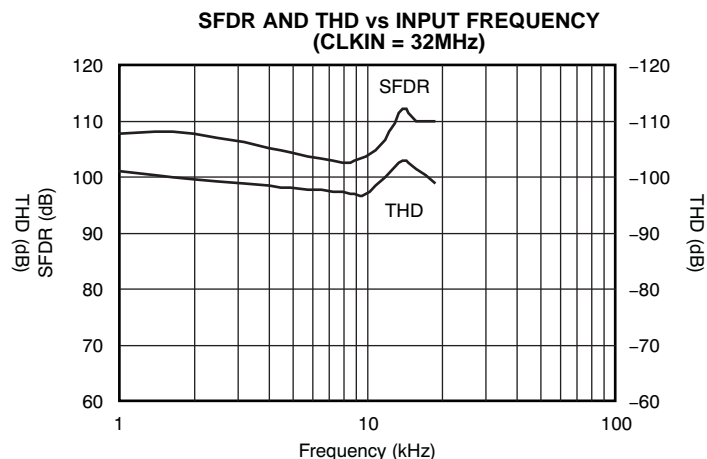
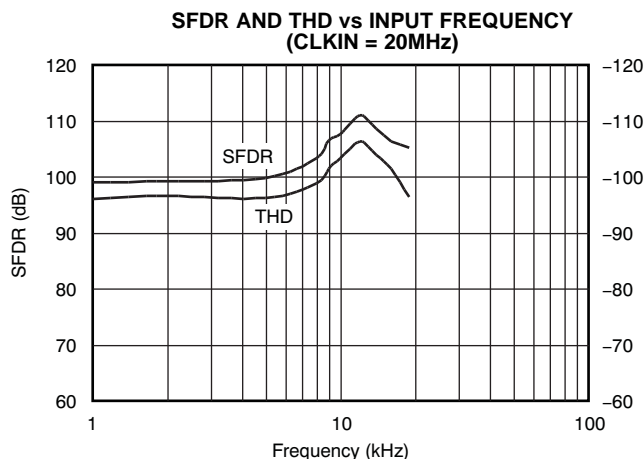
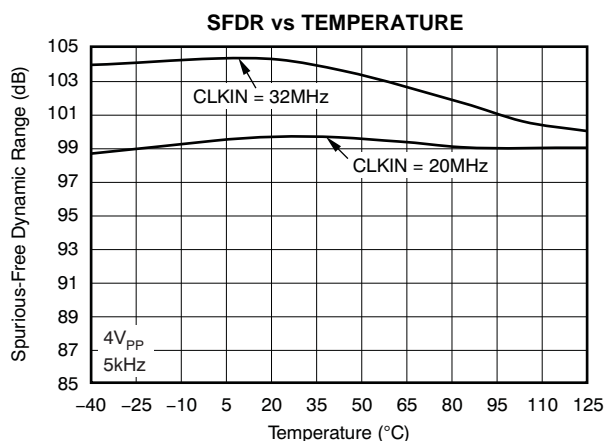
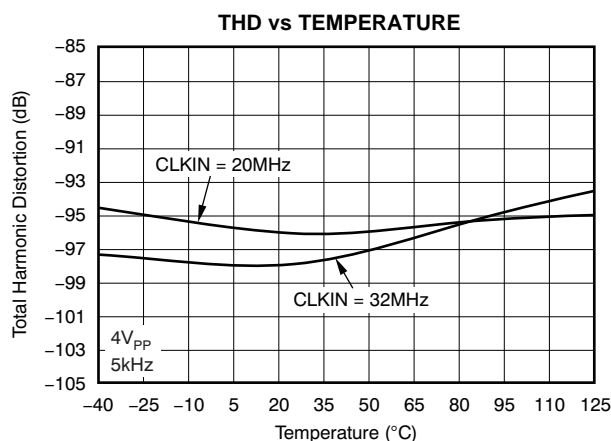


Figure 13.

## TYPICAL CHARACTERISTICS (continued)

$AV_{DD} = 5V$ ,  $BV_{DD} = 3V$ ,  $CH\ x+ = +0.5V$  to  $+4.5V$ ,  $CH\ x- = +2.5V$ ,  $REFIN = \text{external}$ ,  $CLKSEL = 0$ , and 16-bit Sinc<sup>3</sup> filter, with  $OSR = 256$ , unless otherwise noted.



## TYPICAL CHARACTERISTICS (continued)

$AV_{DD} = 5V$ ,  $BV_{DD} = 3V$ , CH  $x+ = +0.5V$  to  $+4.5V$ , CH  $x- = +2.5V$ , REFIN = external, CLKSEL = 0, and 16-bit Sinc<sup>3</sup> filter, with OSR = 256, unless otherwise noted.

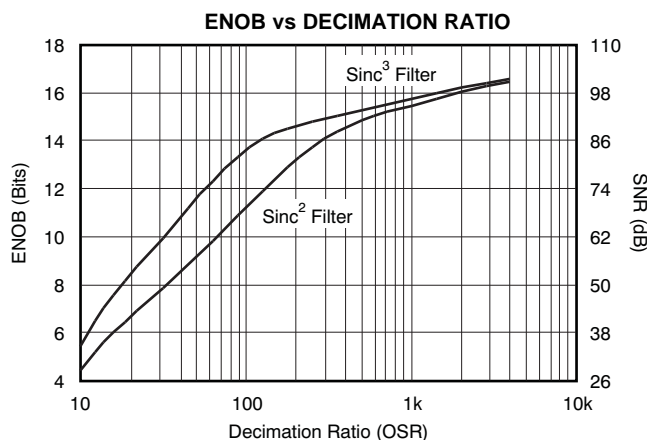


Figure 20.

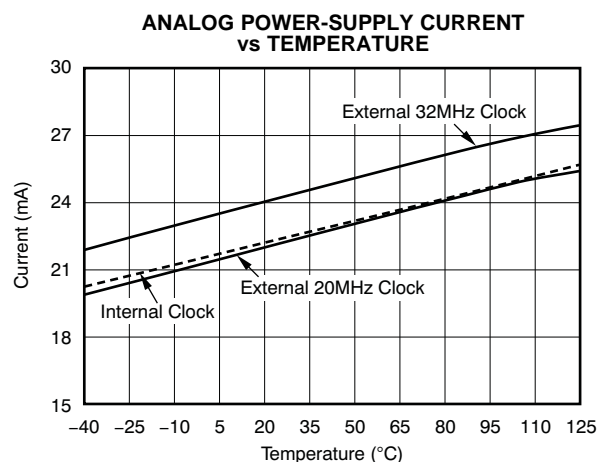


Figure 21.

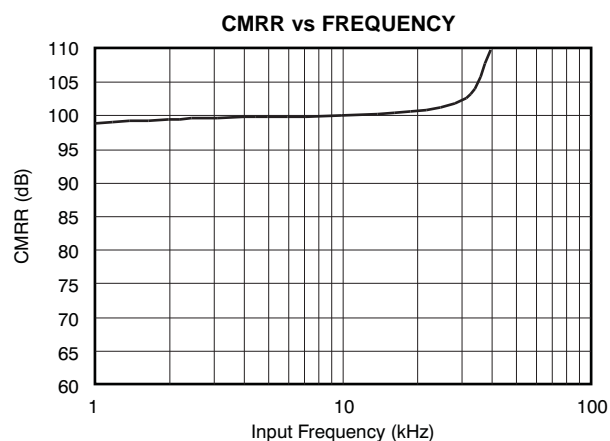


Figure 22.

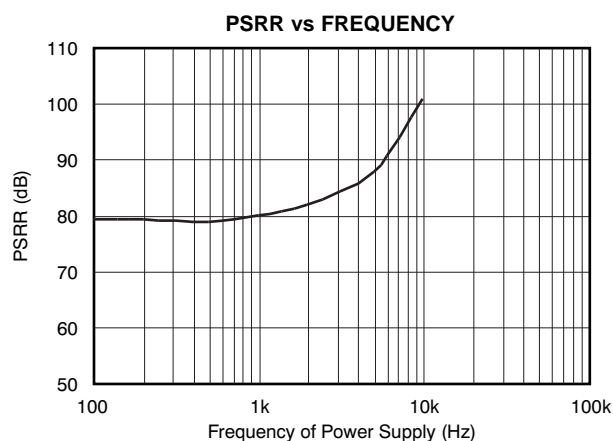


Figure 23.

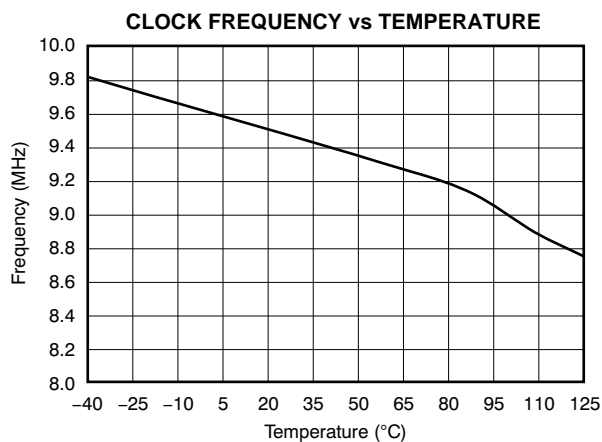


Figure 24.

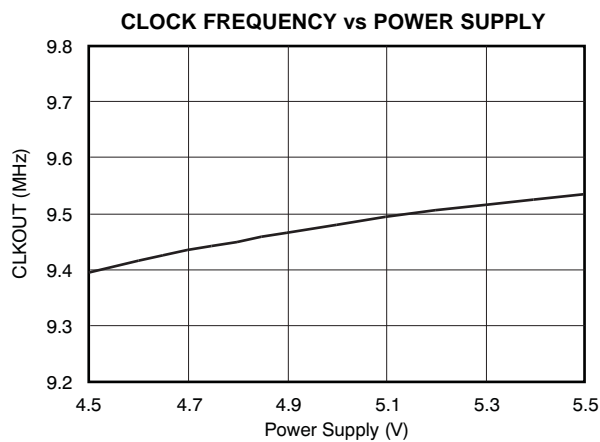


Figure 25.

## GENERAL DESCRIPTION

The ADS1204 is a four-channel, second-order, CMOS device with four delta-sigma ( $\Delta\Sigma$ ) modulators, designed for medium- to high-resolution A/D signal conversions from dc to 39kHz (filter response  $-3\text{dB}$ ) if an oversampling ratio (OSR) of 64 is chosen. The output of the converter (OUTX) provides a stream of digital ones and zeros. The time average of this serial output is proportional to the analog input voltage.

The modulator shifts the quantization noise to high frequencies. A low-pass digital filter should be used at the output of the  $\Delta\Sigma$  modulator. The filter serves two functions. First, it filters out high-frequency noise. Second, the filter converts the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation).

An application-specific integrated circuit (ASIC) or field-programmable gate array (FPGA) could be used to implement the digital filter. Figure 26 and Figure 27 show typical application circuits with the ADS1204 connected to an FPGA.

The overall performance (that is, speed and accuracy) depends on the selection of an appropriate OSR and filter type. A higher OSR produces greater output accuracy while operating at a lower refresh rate. Alternatively, a lower OSR produces lower output accuracy, but operates at a higher refresh rate. This system allows flexibility with the digital filter design and is capable of A/D conversion results that have a dynamic range exceeding 100dB with an OSR equal to 256.

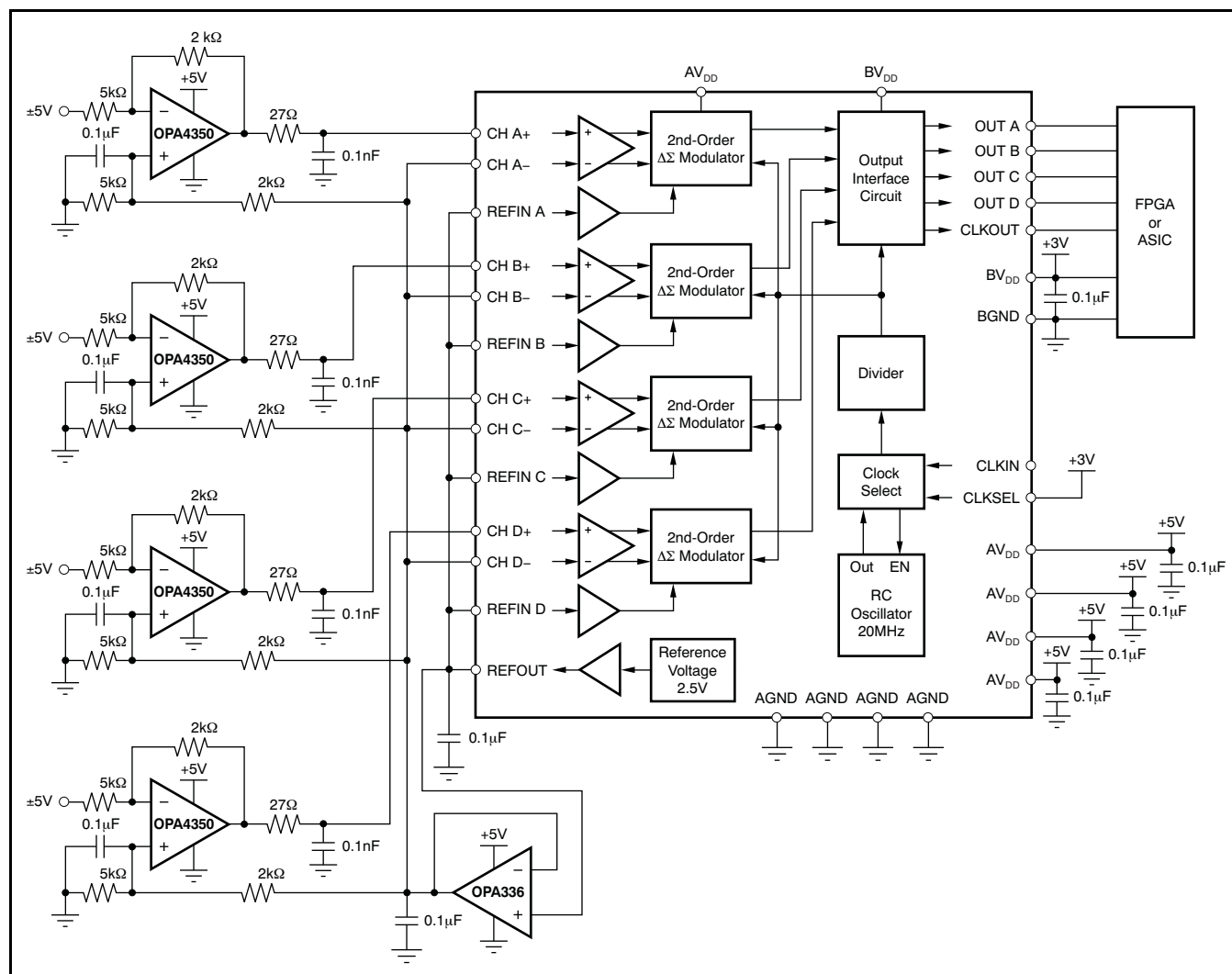
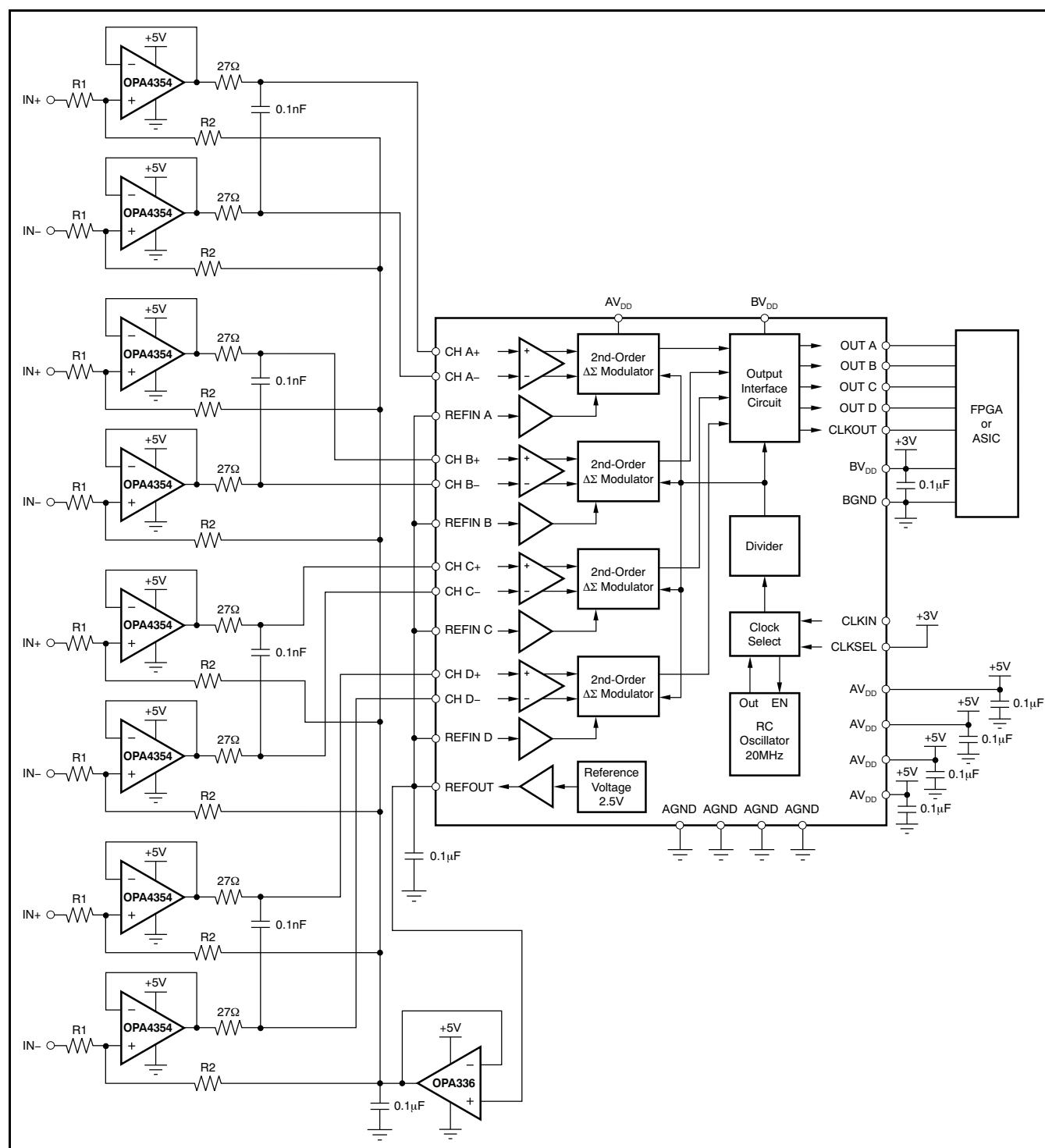


Figure 26. Single-Ended Connection Diagram for the ADS1204  $\Delta\Sigma$  Modulator



**Figure 27. Differential Connection Diagram for the ADS1204  $\Delta\Sigma$  Modulator**

## THEORY OF OPERATION

The differential analog input of the ADS1204 is implemented with a switched-capacitor circuit. This circuit implements a second-order modulator stage, which digitizes the analog input signal into a 1-bit output stream. The clock source can be internal as well as external. Different frequencies for this clock allow for a variety of solutions and signal bandwidths. Every analog input signal is continuously sampled by the modulator and compared to a reference voltage that is applied to the REFINx pin. A digital stream, which accurately represents the analog input voltage over time, appears at the output of the corresponding converter.

## ANALOG INPUT STAGE

### Analog Input

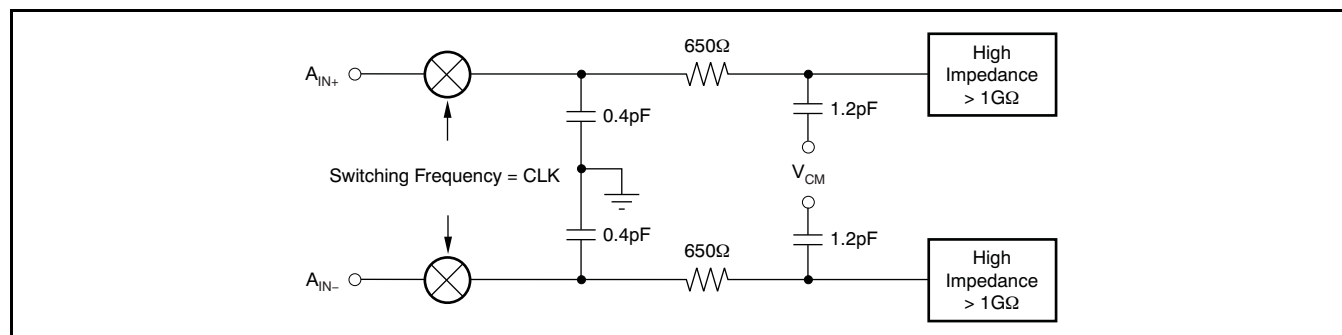
The topology of the analog inputs of ADS1204 is based on fully differential switched-capacitor architecture. This input stage provides the mechanism to achieve low system noise, high common-mode rejection (100dB), and excellent power-supply rejection.

The input impedance of the analog input is dependent on the modulator clock frequency ( $f_{CLK}$ ),

which is also the sampling frequency of the modulator. Figure 28 shows the basic input structure of one channel of the ADS1204. The relationship between the input impedance of the ADS1204 and the modulator clock frequency is shown in Equation 1:

$$Z_{IN} = \frac{100k\Omega}{f_{MOD}/10MHz} \quad (1)$$

The input impedance becomes a consideration in designs where the source impedance of the input signal is high. This high impedance may cause degradation in gain, linearity, and THD. The importance of this effect depends on the desired system performance. There are two restrictions on the analog input signals, CH x+ and CH x-. If the input voltage exceeds the range ( $GND - 0.3V$ ) to ( $V_{DD} + 0.3V$ ), the input current must be limited to 10mA because the input protection diodes on the front end of the converter will begin to turn on. In addition, the linearity and the noise performance of the device are ensured only when the differential analog voltage resides within  $\pm 2V$  (with  $V_{REF}$  as a midpoint); however, the FSR input voltage is  $\pm 2.5V$ .



**Figure 28. Input Impedance of the ADS1204**

## Modulator

The ADS1204 can be operated in two modes. When CKLSEL = 1, the four modulators operate using the internal clock, which is fixed at 20MHz. When CKLSEL = 0, the modulators operate using an external clock. In both modes, the clock is divided by two internally and functions as the modulator clock. The frequency of the external clock can vary from 1MHz to 32MHz to adjust for the clock requirements of the application.

The modulator topology is fundamentally a second-order, switched-capacitor,  $\Delta\Sigma$  modulator, such as the one conceptualized in Figure 29. The analog input voltage and the output of the 1-bit digital-to-analog converter (DAC) are differentiated, providing analog voltages at X2 and X3. The voltages at X2 and X3 are presented to their individual integrators. The output of these integrators progresses in a negative or positive direction. When the value of the signal at X4 equals the comparator reference voltage, the output of the comparator switches from negative to positive, or positive to negative, depending on its original state. When the output value of the comparator switches from high to low or vice versa, the 1-bit DAC responds on the next

clock pulse by changing its analog output voltage at X6, causing the integrators to progress in the opposite direction. The feedback of the modulator to the front end of the integrators forces the value of the integrator output to track the average of the input.

## DIGITAL OUTPUT

A differential input signal of 0V will ideally produce a stream of ones and zeros that are high 50% of the time and low 50% of the time. A differential input of +2V produces a stream of ones and zeros that are high 80% of the time. A differential input of -2V produces a stream of ones and zeros that are high 20% of the time. The input voltage versus the output modulator signal is shown in Figure 30.

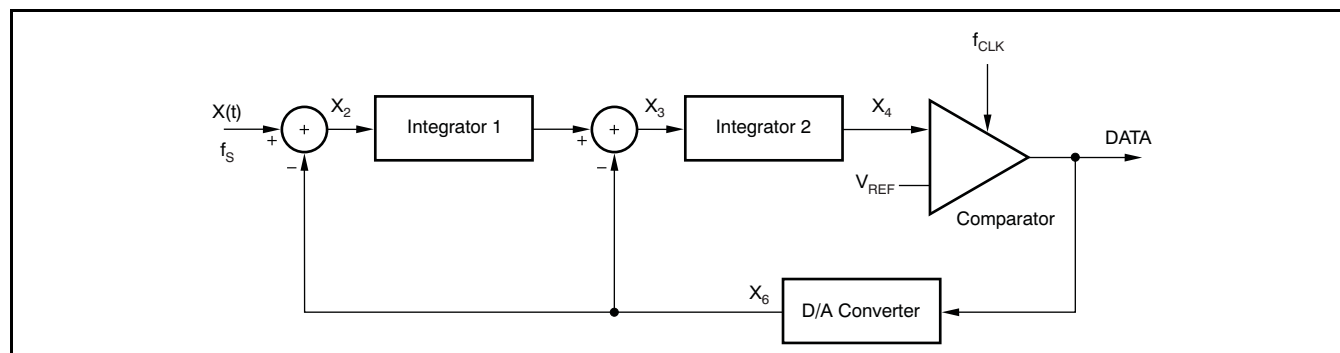


Figure 29. Block Diagram of the Second-Order Modulator

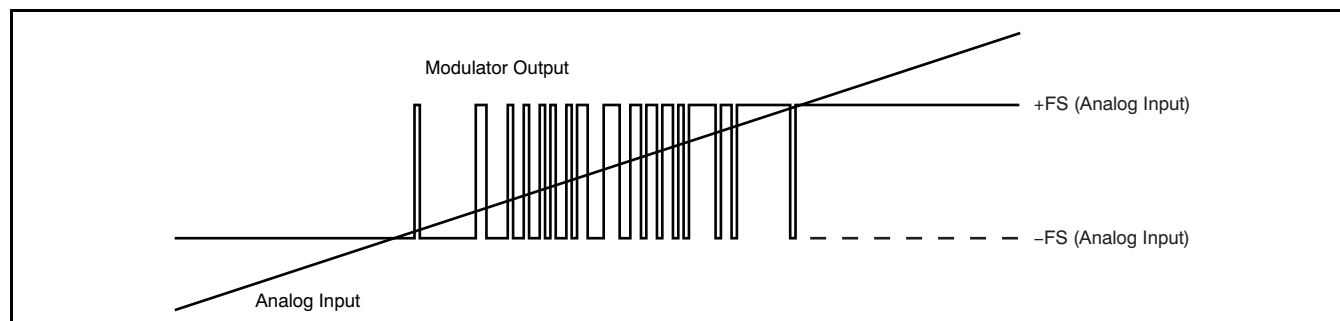


Figure 30. Analog Input vs Modulator Output of the ADS1204



## DIGITAL INTERFACE

### INTRODUCTION

The analog signal connected to the input of the  $\Delta\Sigma$  modulator is converted using the clock signal applied to the modulator. The result of the conversion, or modulation, is generated and sent to the OUTx pin from the  $\Delta\Sigma$  modulator. In most applications where a direct connection is realized between the  $\Delta\Sigma$  modulator and an ASIC or FPGA (each with an implemented filter), the two standard signals per modulator (CLKOUT and OUTx) are provided from the modulator. The output clock signal is equal for all four modulators. If CLKSEL = 1, CLKIN must always be set either high or low.

### MODES OF OPERATION

The system clock of the ADS1204 is 20MHz by default. The system clock can be provided either from the internal 20MHz RC oscillator or from an external clock source. For this purpose, the CLKIN pin is provided; it is controlled by the mode setting, CLKSEL.

The system clock is divided by two for the modulator clock. Therefore, the default clock frequency of the modulator is 10MHz. With a possible external clock range of 1MHz to 32MHz, the modulator operates between 500kHz and 16MHz.

### FILTER USAGE

The modulator generates only a bitstream, which does not output a digital word like an A/D converter. In order to output a digital word equivalent to the analog input voltage, the bitstream must be processed by a digital filter.

A very simple filter, built with minimal effort and hardware, is the Sinc<sup>3</sup> filter shown in Equation 2:

$$H(z) = \left[ \frac{1 - z^{-OSR}}{1 - z^{-1}} \right]^2 \quad (2)$$

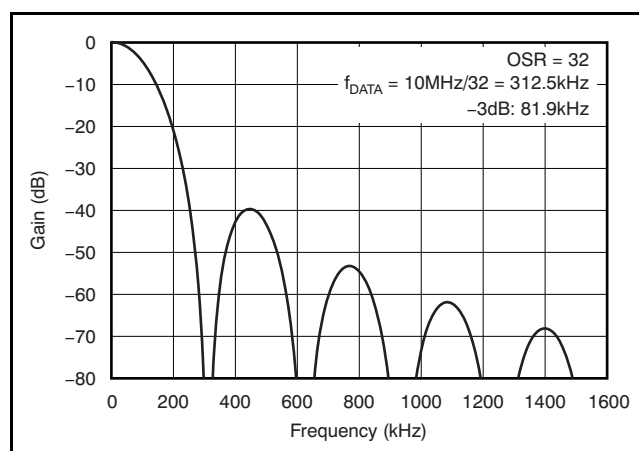
This filter provides the best output performance at the lowest hardware size (for example, a count of digital gates). For oversampling ratios in the range of 16 to 256, this is a good choice. All the characterizations in the data sheet are also done using a Sinc<sup>3</sup> filter with an oversampling ratio of OSR = 256 and an output word width of 16 bits.

In a Sinc<sup>3</sup> filter response (shown in Figure 31 and Figure 32), the location of the first notch occurs at the

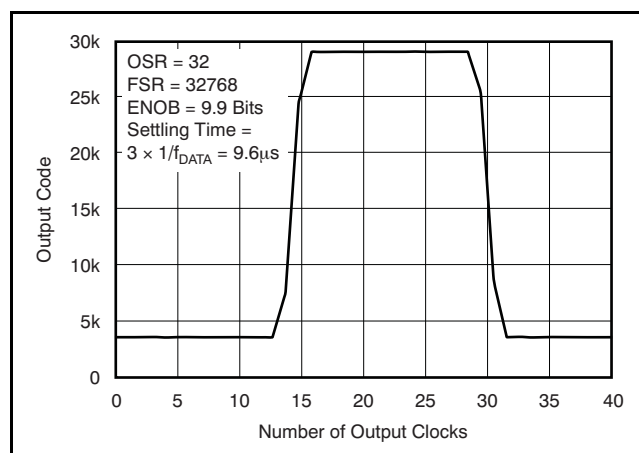
frequency of output data rate  $f_{DATA} = f_{CLK}/OSR$ . The -3dB point is located at half the Nyquist frequency or  $f_{DATA}/4$ . For some applications, it may be necessary to use another filter type for better frequency response.

This performance can be improved, for example, by a cascaded filter structure. The first decimation stage can be a Sinc<sup>3</sup> filter with a low OSR and the second stage a high-order filter.

For more information, see application note SBAA094, *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications*, available for download at [www.ti.com](http://www.ti.com).



**Figure 31. Frequency Response of Sinc<sup>3</sup> Filter**



**Figure 32. Pulse Response of Sinc<sup>3</sup> Filter  
( $f_{MOD} = 10\text{MHz}$ )**

The effective number of bits (ENOB) can be used to compare the performance of A/D converters and  $\Delta\Sigma$  modulators. Figure 33 shows the ENOB of the ADS1204 with different filter types. In this data sheet, the ENOB is calculated from the SNR as shown in Equation 3:

$$\text{SNR} = 1.76\text{dB} + 6.02\text{dB} \times \text{ENOB} \quad (3)$$

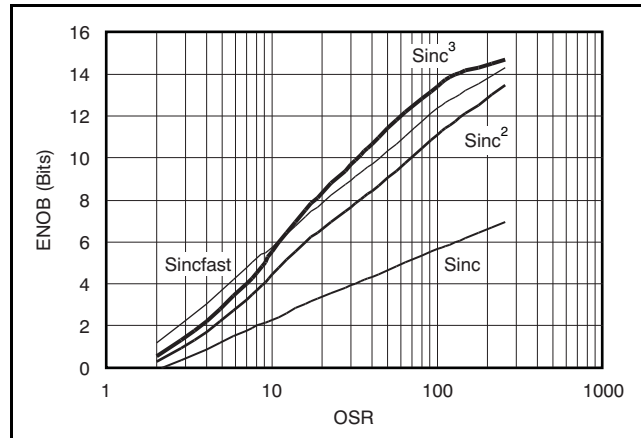


Figure 33. Measured ENOB vs OSR

In motor control applications, a very fast response time for overcurrent detection is required. There is a constraint between  $1\mu\text{s}$  and  $5\mu\text{s}$  with 3 bits to 7 bits resolution. The time for full settling is dependent on the filter order. Therefore, the full settling of the  $\text{Sinc}^3$  filter needs three data clocks and the  $\text{Sinc}^2$  filter needs two data clocks. The data clock is equal to the modulator clock divided by the OSR. For overcurrent

protection, filter types other than  $\text{Sinc}^3$  might be a better choice. A simple example is a  $\text{Sinc}^2$  filter. Figure 34 compares the settling time of different filter types. The Sincfast is a modified  $\text{Sinc}^2$  filter as Equation 4 shows:

$$H(z) = \left( \frac{1 - z^{-\text{OSR}}}{1 - z^{-1}} \right)^2 (1 + z^{-2 \times \text{OSR}}) \quad (4)$$

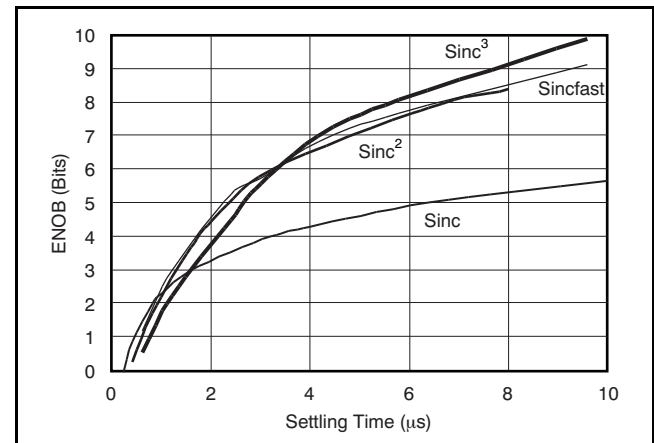


Figure 34. Measured ENOB vs Settling Time

For more information, see application note SBAA094, *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications*, available for download at [www.ti.com](http://www.ti.com).

## LAYOUT CONSIDERATIONS

### POWER SUPPLIES

An applied external digital filter rejects high-frequency noise. PSRR and CMRR improve at higher frequencies because the digital filter suppresses high-frequency noise.

However, the suppression of the filter is not infinite, so high-frequency noise still influences the conversion result. Inputs to the ADS1204, such as CH x+, CH x–, and CLKIN, should not be present before the power supply is on. Violating this condition could cause latch-up. If these signals are present before the supply is on, series resistors should be used to limit the input current to a maximum of 10mA. Experimentation may be the best way to determine the appropriate connection between the ADS1204 and different power supplies.

### GROUNDING

Analog and digital sections of the design must be carefully and cleanly partitioned. Each section should have its own ground plane with no overlap between them. Do not join the ground planes; instead, connect the two with a moderate signal trace underneath the converter. However, for different applications with DSPs and switching power supplies, this process might be different.

For multiple converters, connect the two ground planes as close as possible to one central location for all of the converters. In some cases, experimentation may be required to find the best point to connect the two planes together.

### DECOUPLING

Good decoupling practices must be used for the ADS1204 and for all components in the design. All decoupling capacitors, specifically the 0.1μF ceramic capacitors, must be placed as close as possible to the pin being decoupled. A 1μF and 10μF capacitor, in parallel with the 0.1μF ceramic capacitor, can be used to decouple AV<sub>DD</sub> to AGND as well as BV<sub>DD</sub> to BGND. At least one 0.1μF ceramic capacitor must be used to decouple every AV<sub>DD</sub> to AGND and BV<sub>DD</sub> to BGND, as well as for the digital supply on each digital component.

The digital supply sets the I/O voltage for the interface and can be set within a range of 2.7V to 5.5V.

In cases where both the analog and digital I/O supplies share the same supply source, an RC filter of 10Ω and 0.1μF can be used to help reduce the noise in the analog supply.

## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2007) to Revision C	Page
• Updated document format .....	1
• Extended operating temperature range from +85°C to +105°C throughout document .....	1
• Deleted operating free-air temperature range row from <i>Absolute Maximum Ratings</i> table .....	2
• Added free-air temperature range ratings to <i>Recommended Operating Conditions</i> table .....	2
• Changed <i>Dissipation Ratings</i> table .....	3
• Changed typical specification in <i>Input capacitance</i> row of <i>Analog Input</i> section of <i>Electrical Characteristics</i> table .....	3
• Added additional specification for Total Harmonic Distortion in <i>AC Accuracy</i> section of <i>Electrical Characteristics</i> table ....	3
• Deleted test condition of $V_{OUT}$ row in <i>Voltage Reference Output</i> section of <i>Electrical Characteristics</i> table .....	3
• Updated typical characteristic graphs to reflect extended temperature range .....	9
<hr/>	
Changes from Revision A (June 2004) to Revision B	Page
• Added note to QFN package .....	6

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
ADS1204IRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS1204IRHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS1204IRHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS1204IRHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

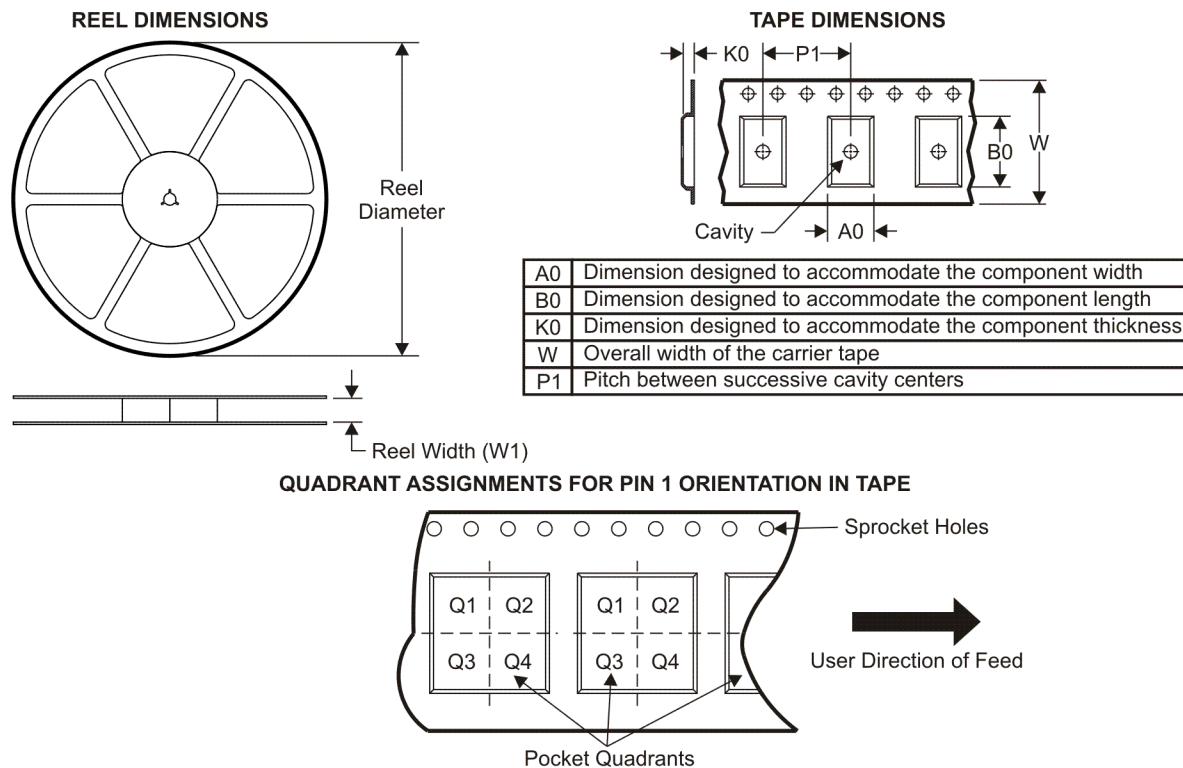
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

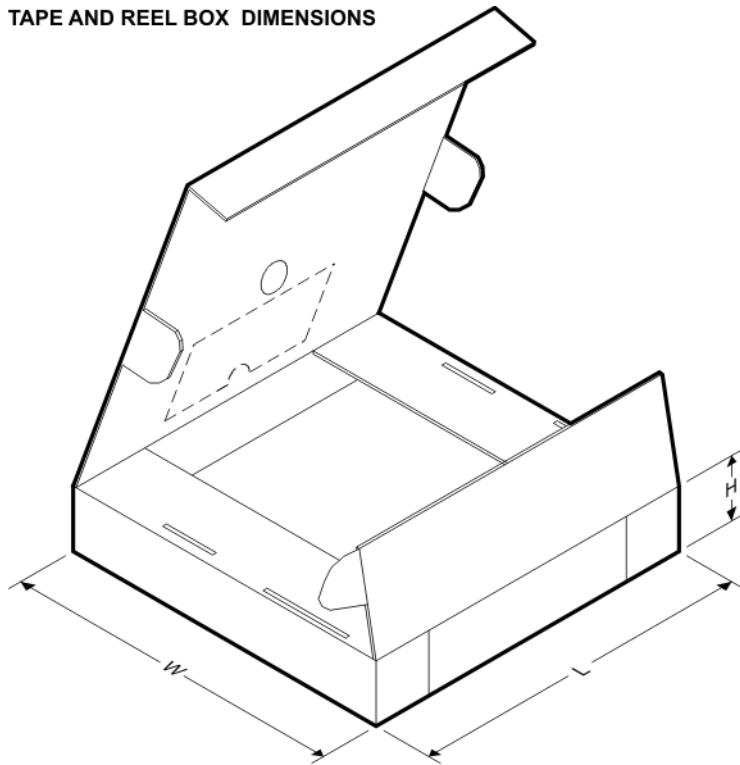
**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1204IRHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS1204IRHBT	QFN	RHB	32	250	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS

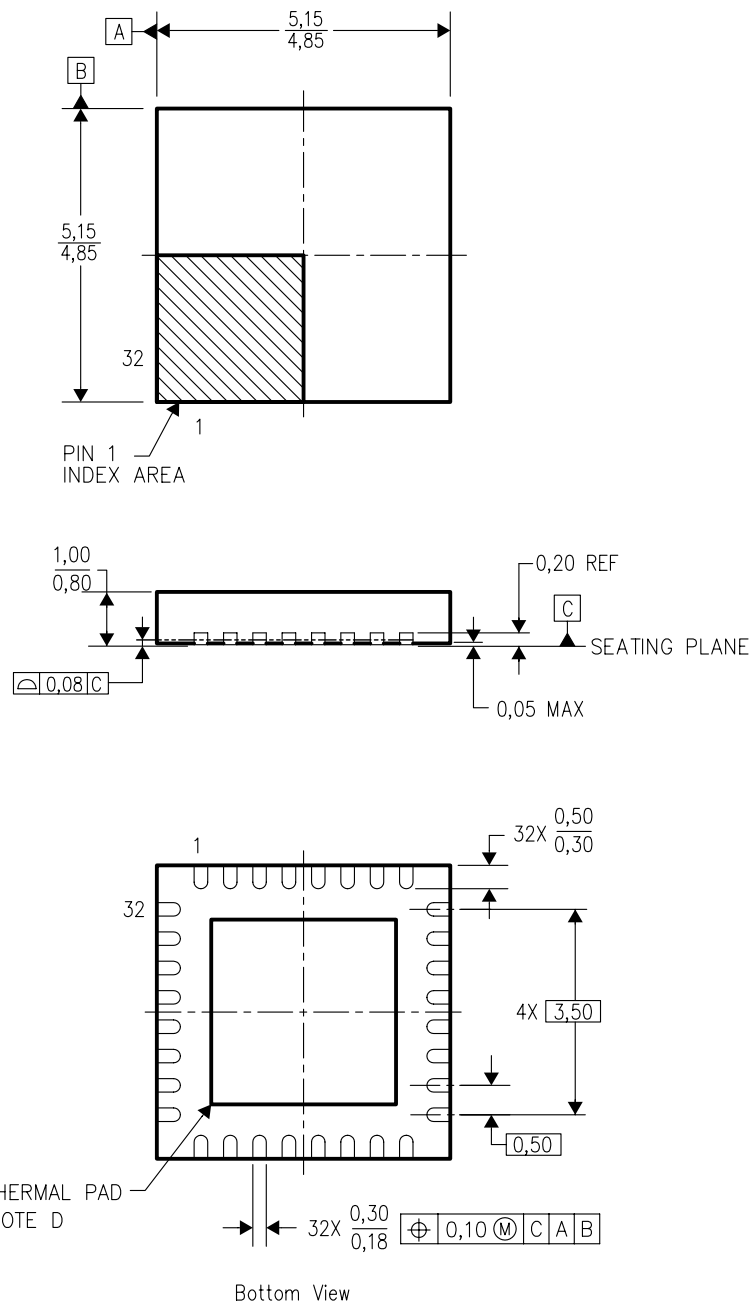


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1204IRHBR	QFN	RHB	32	3000	340.5	333.0	20.6
ADS1204IRHBT	QFN	RHB	32	250	340.5	333.0	20.6

RHB (S-PQFP-N32)

PLASTIC QUAD FLATPACK



4204326/C xx/04

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) Package configuration.
  - The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
  - Falls within JEDEC MO-220.

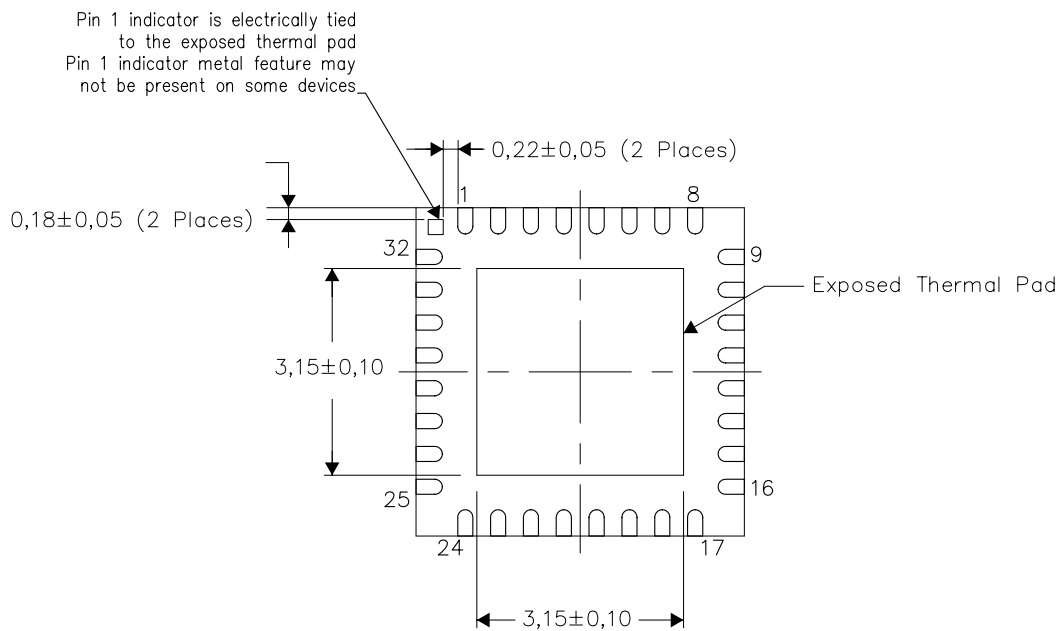


### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

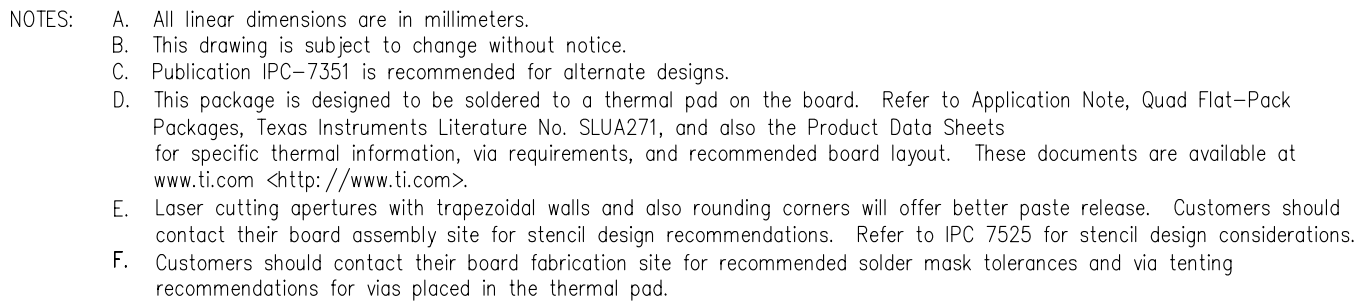


Bottom View

Exposed Thermal Pad Dimensions

4206356-3/Q 11/10

NOTE: A. All linear dimensions are in millimeters



RHB (S-PVQFN-N32)

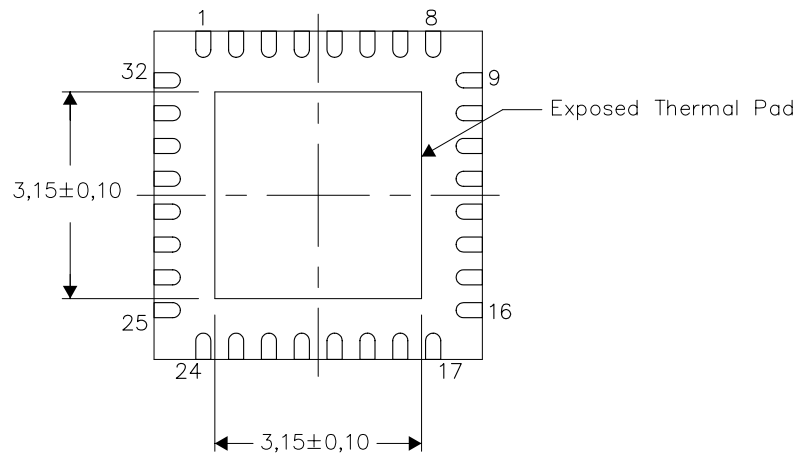
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

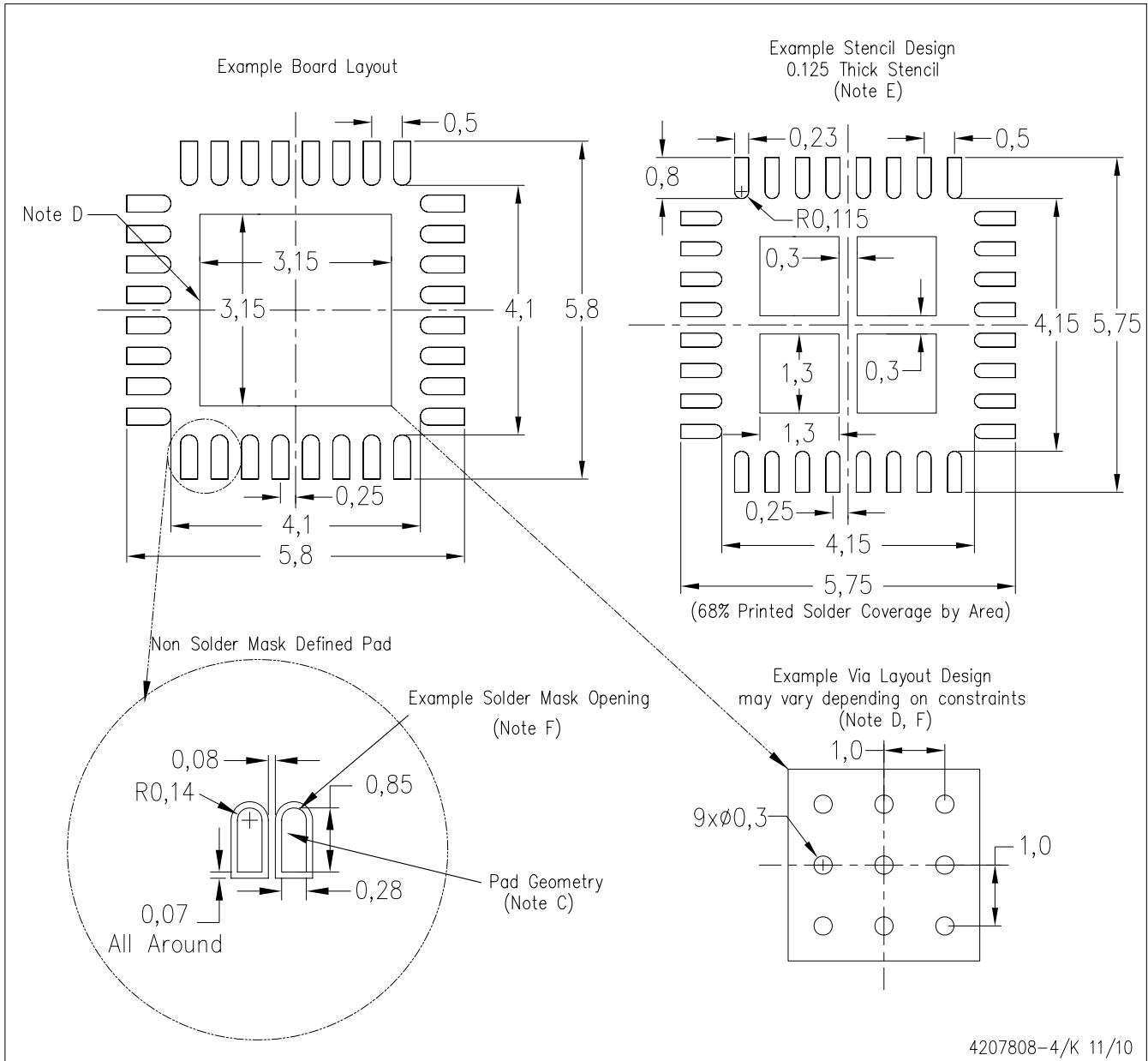
Exposed Thermal Pad Dimensions

4206356-4/Q 11/10

NOTE: A. All linear dimensions are in millimeters

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



4207808-4/K 11/10

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>	Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>	Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Energy	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>	Space, Avionics & Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>	Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless-apps">www.ti.com/wireless-apps</a>