

## UNIT - 5

### THE LINK LAYER: LINKS, ACCESS NETWORKS and LANs

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#### 1) The Services provided by the link layer:

##### 1) Framing:

- \* Almost all link-layer protocols encapsulate each network-layer datagram within a link-layer frame before transmission over the link.
- \* The structure of the frame is specified by the link layer.

##### 2) Link access:

- \* A medium access control (MAC) protocol specifies the rules by which a frame is transmitted onto the link.
- \* For point-to-point links that have a single sender at one end of the link and a single receiver at the other end of the link, the MAC protocol is simple. The sender can send a frame whenever the link is idle.

- \* The more interesting case is when multiple nodes share a single broadcast link—the so-called multiple access problem.

##### 3) Reliable Delivery:

- \* When a link layer protocol provides reliable delivery service, it guarantees to move each network-layer datagram across the link without

error.

- \* A link layer reliable delivery service can be achieved with acknowledgements and transmissions.

#### 4) Error detection and correction:

- \* Errors are introduced by signal attenuation and electromagnetic noise.

- \* Many link-layer protocols provide a mechanism to detect such bit errors.

- \* This is done by having the transmitting node include error detection bits in the frame & having the receiving node performs an error check.

- \* Receiver identifies and corrects bit error(s) without resorting to retransmission.

#### 5) Flow control:

- \* Pacing b/w adjacent sending and receiving nodes.

#### 6) Half duplex and full duplex:

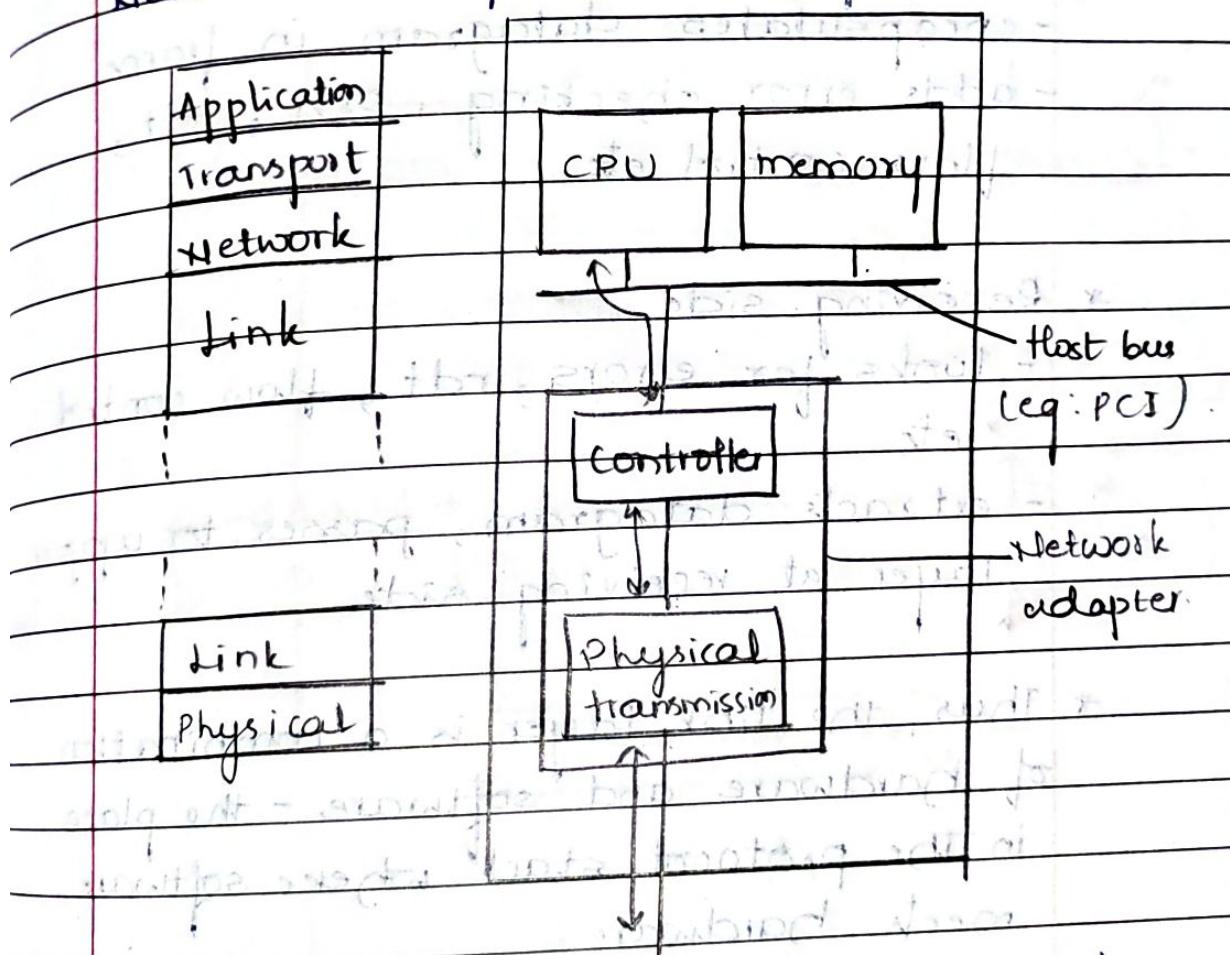
- \* In half duplex, nodes at both ends of link can transmit, but not at the same time.

\* Full duplex protocol allows an application program to send and receive information concurrently.

2) Where is the link layer implemented?

\* It is implemented in each and every host.

\* The link layer is implemented in a network adapter, also sometimes known as a Network Interface Card (NIC).

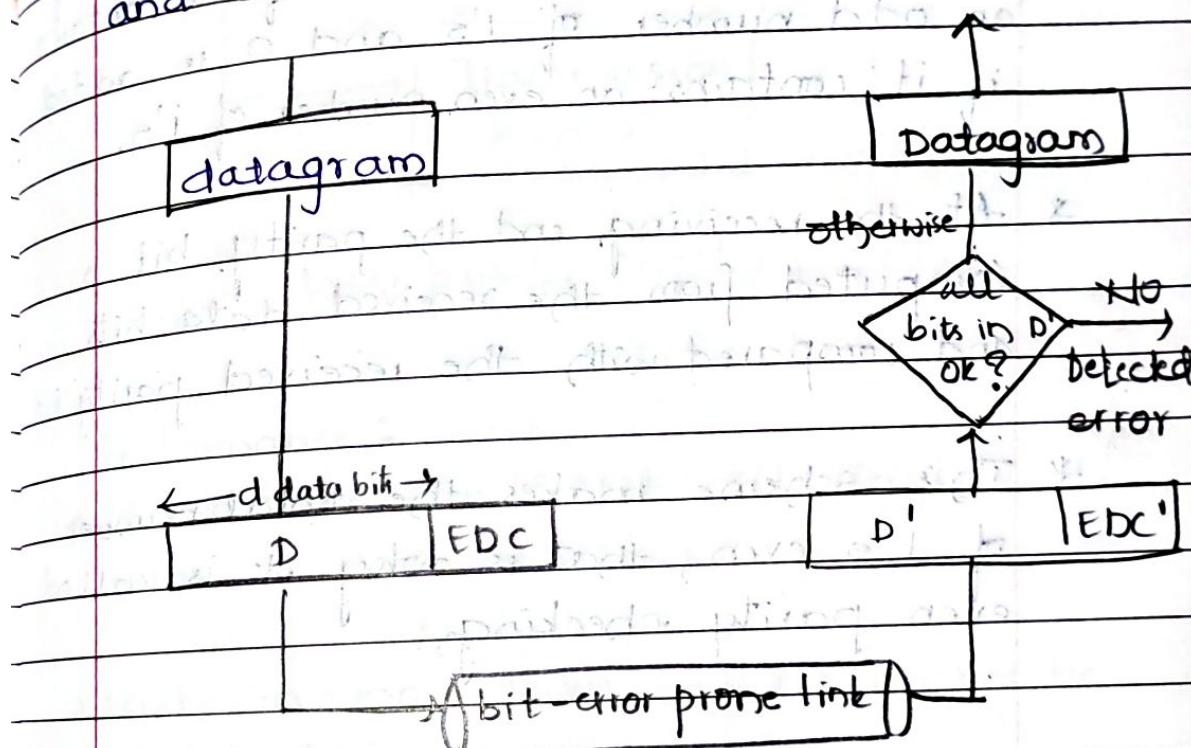


Network Adapter: its relationship to other host components & to protocol stack functionally.

- \* Figure shows a network adapter attaching to a host's bus (e.g.: PCI), where it looks much like any other I/O device to other host components.
- \* Figure also shows that while most of the link layer is implemented in hardware, part of the link layer is implemented in software that runs on the host's CPU.
- \* Sending side:
  - encapsulates datagram in frame
  - adds error checking, bits, rdt, flow control etc.
- \* Receiving side:
  - looks for errors, rdt, flow control etc.
  - extracts datagram, passes to upper layer at receiving side.
- \* Thus, the link layer is a combination of hardware and software - the place in the protocol stack where software meets hardware.

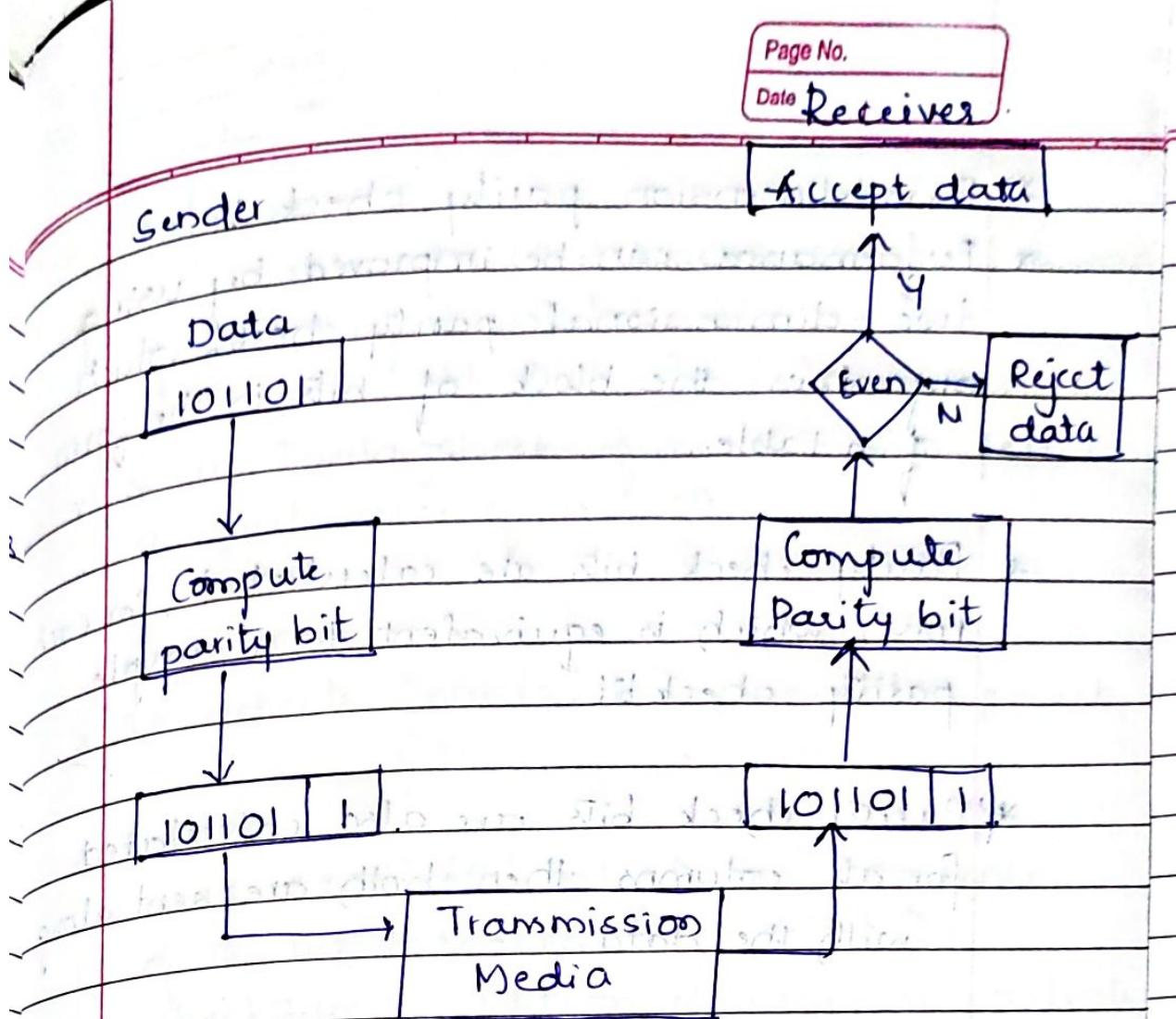
### 3) Error detection:

- \* EDC - Error detection and correction bits (redundancy)
- \* D - Data protected by error checking, may include header fields
- \* Error detection is not 100% reliable
  - Protocol may miss some errors, but rarely
  - larger EDC field yields better detection and correction



#### 4) Parity checks:

- \* In this technique, a redundant bit called parity bit, is appended to every data unit so that the number of 1's in the unit including the parity becomes even.
- \* Block of data from the source are subjected to a check bit or Parity bit generator form, where a parity of 1 is added to the block if it contains an odd number of 1's and 0 is added if it contains an even number of 1's.
- \* At the receiving end the parity bit is computed from the received data bits and compared with the received parity bit.
- \* This scheme makes the total number of 1's even, that is why it is called even parity checking.



Even parity checking sum.

### Performance:

- \* A receiver can detect all single bit errors in each code word.
- \* Errors in more than one bit cannot be detected.

\* Two-dimension parity check :

\* Performance can be improved by using two-dimensional parity check, which organizes the block of bits in the form of a table.

\* Parity check bits are calculated for each row, which is equivalent to a simple parity check bit.

\* Parity check bits are also calculated for all columns then both are sent along with the data.

\* At the receiving end these are compared with the parity bits calculated on the received data.

Original	1011011   1010101   01011010   11010101
Column parities	10110011   1 10101011   1 01011010   0 11010101   1
Row parities	

Data to be sent	1011011   10101011   01011010   11010101 10010111
-----------------	------------------------------------------------------

Performance :

- \* 2-D Parity checking increases the likelihood of detecting burst errors
- \* 2-D Parity check of n-bits can detect a burst error of n-bits

5) Checksums :

- \* It detects "errors" in transmitted packet.

\* Sender :

- treat segment contents as sequence of 16 bit integers.
- checksum: addition of segment contents
- sender puts checksum value into VDP checksum field.

\* Receiver :

- compute checksum of received segment.
- check if computed checksum equals checksum field value;  
No - error detected
- YES - error detected.

\* Performance :

- It detects all errors involving an odd no. of bits.
- It also detects most errors involving even number of bits.

$$\begin{array}{r} 10110011 \\ 10101011 \\ \hline \end{array}$$

$$\begin{array}{r} 101011110 \\ \hline \end{array}$$

$$\begin{array}{r} 01011111 \\ \hline \end{array}$$

$$\begin{array}{r} 01011010 \\ \hline \end{array}$$

$$\begin{array}{r} 10111001 \\ \hline \end{array}$$

$$\begin{array}{r} 11010101 \\ \hline \end{array}$$

$$\begin{array}{r} 010001110 \\ \hline \end{array}$$

sum: 10001111

compliment: 01010000

Received data: 10110011

$$\begin{array}{r} 10110011 \\ 10101011 \\ \hline \end{array}$$

$$\begin{array}{r} 101011110 \\ \hline \end{array}$$

$$\begin{array}{r} 01011111 \\ \hline \end{array}$$

$$\begin{array}{r} 01011010 \\ \hline \end{array}$$

$$\begin{array}{r} 10111001 \\ \hline \end{array}$$

$$\begin{array}{r} 11010101 \\ \hline \end{array}$$

$$\begin{array}{r} 010001110 \\ \hline \end{array}$$

sum: 10001111

compliment: 01110000

sum: 11111111

compliment: 00000000

## 6) Cyclic Redundancy checks :

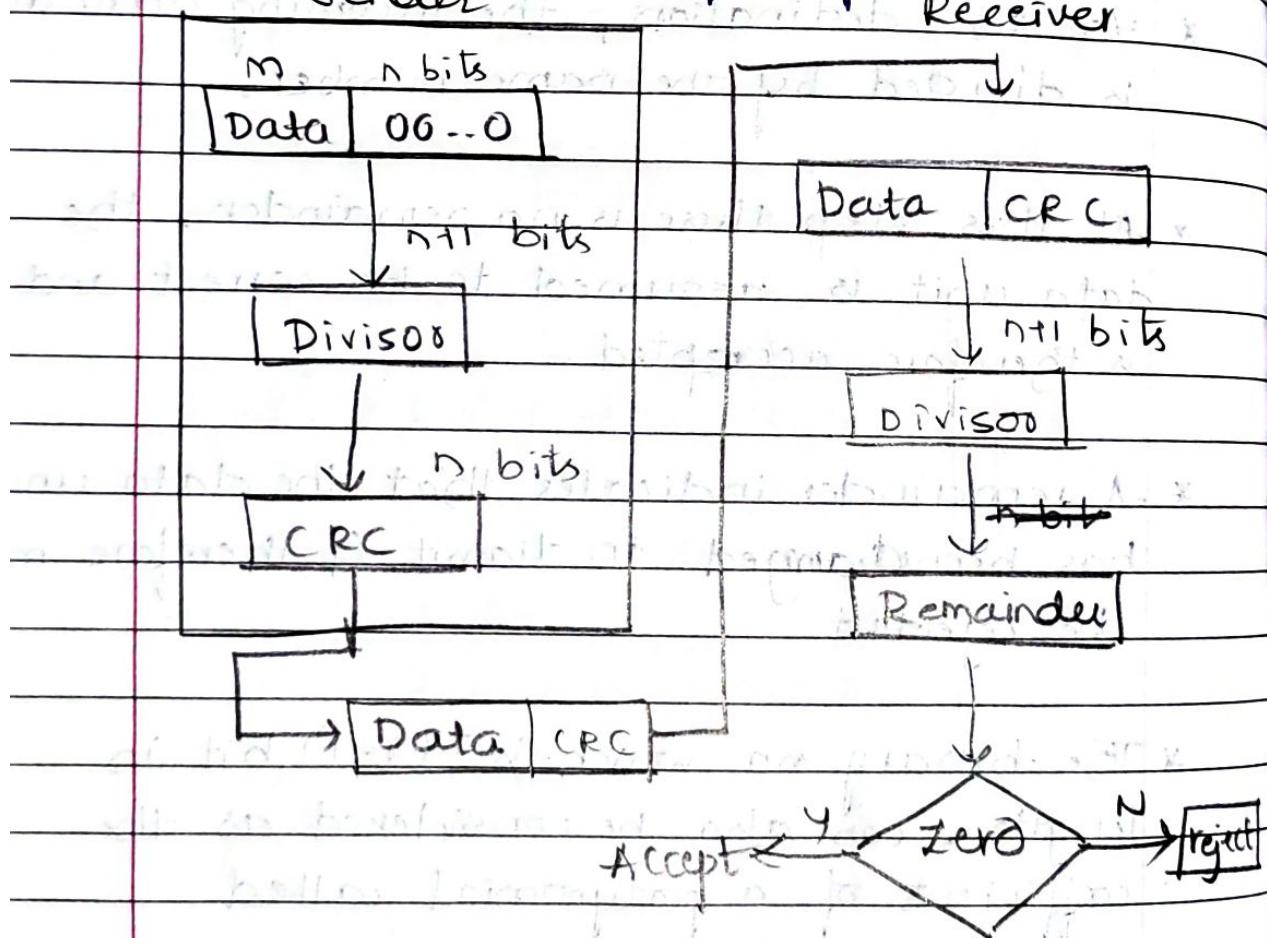
- \* CRC is the most powerful and easy to implement technique.
- \* CRC is based on binary division.
- \* In CRC, a sequence of redundant bits are appended to the end of data unit so that the resulting data unit becomes exactly divisible by second, predetermined binary number.
- \* At the destination, the incoming data unit is divided by the same number.
- \* At this step there is no remainder, the data unit is assumed to be correct and is therefore accepted.
- \* A remainder indicates that the data unit has been changed in transit & therefore must be rejected.
- \* The binary no. which is  $(r+1)$  bit in length, can also be considered as the coefficients of a polynomial called Generator polynomial.

## Performance:

\* CRC is very effective in error detection

\* If the divisor is chosen according to the previously mentioned rules, its performance can be summarized as follows.

- CRC can detect all single-bit errors.
- CRC can detect all double-bit errors.
- CRC can detect any odd-number of errors.
- CRC can detect all burst errors of less than the degree of polynomial.



Basic scheme for CRC.

each.

same - 0  
diff - 1

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A      B      A XOR B

0      0      0

0      1      1

1      0      1 (1's complement)

1      1      0

111101

divisor ← 1101 ) 100100000

L = 4

L-1 = 3

3's are

appended to the message.

1101 ↓

⊗ 1000

0101 ↓

⊗ 10010

11101 ↓

110010

111010

1100101

10000110

10000000

0100001100

100000001101

10100000001

001

00000

11010

Remainder

CRC : 001

Data transmitted : 100100001 frame CRC

$$x^7 + x^5 + x^2 + x + 1$$

$$x^6 \quad x^4 \quad x^3$$

↓    ↓    ↓

1 0 1 0 0 1 1

2) Frame : 1101011011

Generator : 10011

message, after appending 4 zero bits :

11010110110000

1100001010

10011 ) 11010110110000

10011↓

0110011

1010011↓

01000001

000000000↓

00110000010

1011 0.0000↓

100 00101

00000↓

01011

00000↓

11000010101110

10110

10011

001010

00000↓

10100

10011

01110

00000

1110

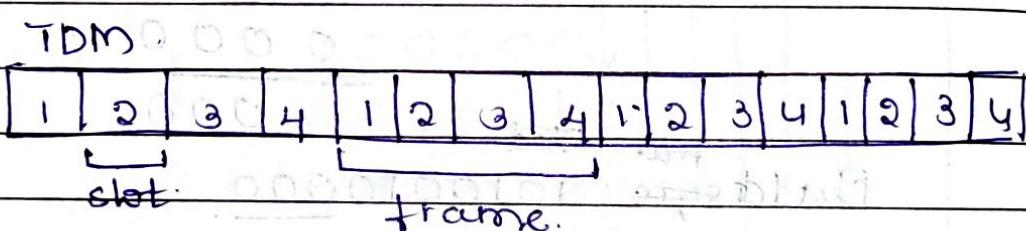
### f) TDMA : Time Division Multiple Access

\* Suppose the channel supports  $N$  nodes, & that the transmission rate of the channel is  $R$  bps.

\* TDM divides time into time frames & further divides each time frame into  $N$  time slots.

\* Each time slot is then assigned to one of the  $N$  nodes.

\* Typically, slot sizes are chosen so that a single packet can be transmitted during a slot time.



key :

2 All slots labeled "2" are dedicated to a specific sender receiver pair.

\* TDM is attractive because it eliminates collisions and perfectly fair.

\* 2 Drawbacks :

1) A node is limited to an avg. rate of  $R/N$  bps when it is the only node with

- packets to send.
- 2) A node must always wait for its turn in the transmission sequence again, even when it is the only node with a frame to send.

## 8) FDMA : Frequency Division Multiple Access

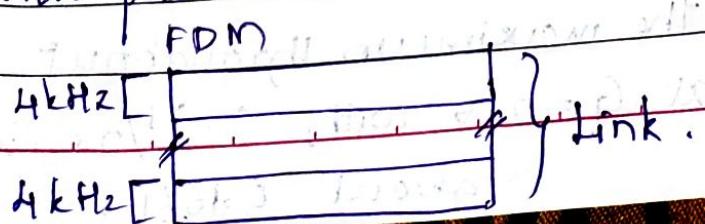
\* FDMA divides the  $R$  bps channel into different frequencies (each with a bandwidth of  $R/N$ ) & assigns each frequency to one of the  $N$  nodes.

\* FDMA thus creates  $N$  smaller channels of  $R/N$  bps out of the single, larger  $R$  bps channel.

\* FDMA shares both advantages & disadvantages of TDM.

\* It avoids collisions & divides the bandwidth fairly among the  $N$  nodes.

\* FDMA also shares a principal disadvantage with TDM - a node is limited to a bandwidth of  $R/N$ , even when it is the only node with packets to send.



### 9) Pure ALOHA:

\* Pure ALOHA allows users to transmit whenever they have data to be sent.

\* Senders wait to see if a collision occurred.

\* If a collision occurs, each station involved waits a random amount of time then tries again.

\* Systems in which multiple users share a common channel in a way that can lead to conflicts are widely known as contention systems.

\* Whenever 2 frames try to occupy the channel at the same time, there will be a collision.

\* If the first bit of a new frame overlaps with just the last bit of a frame almost finished, both frames will be totally destroyed & both will have to be transmitted later.

\* The maximum throughput occurs

at  $G=0.5$  with  $S=1/2e$ , which is

about 0.184.

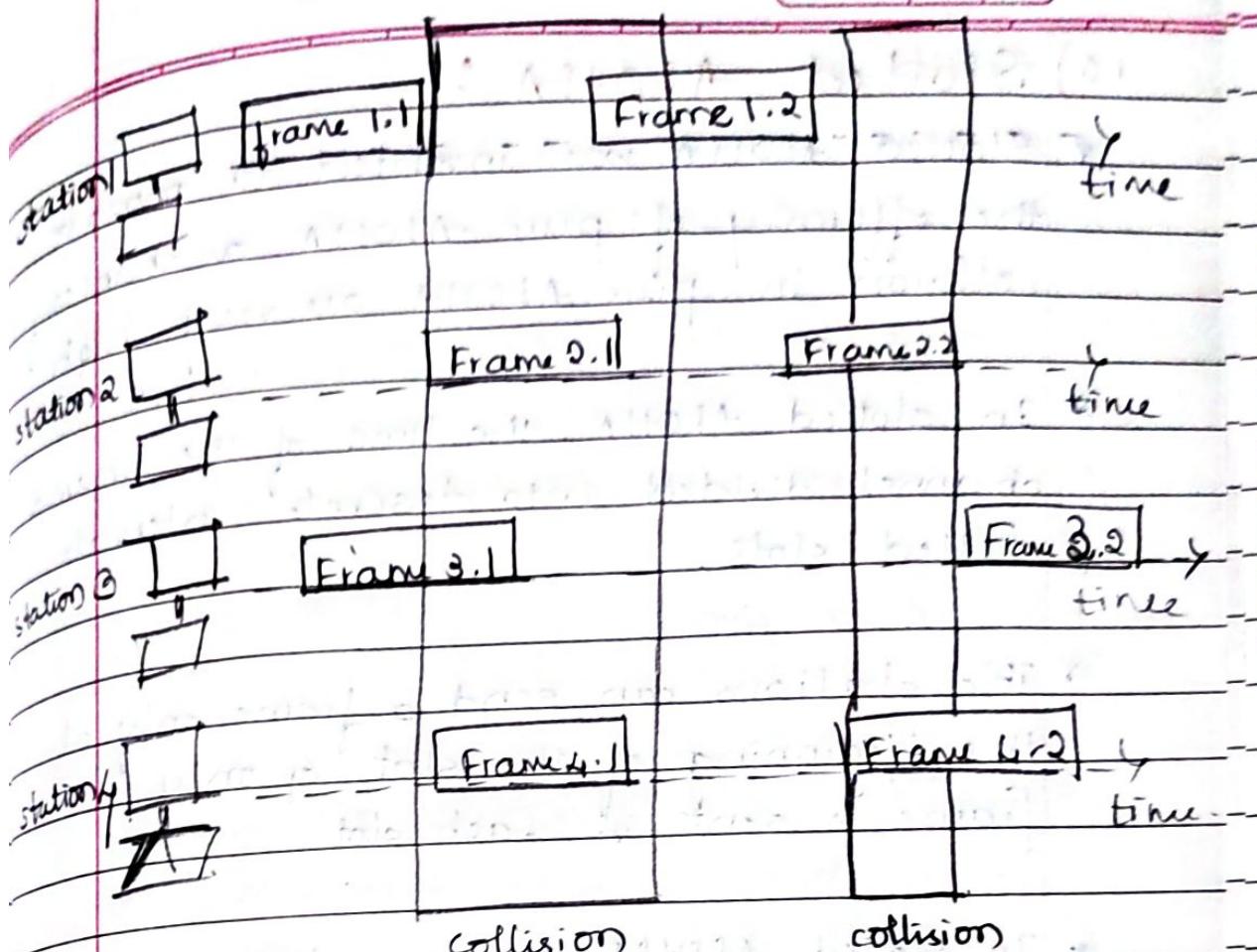


Figure: In pure ALOHA, frames are transmitted at completely arbitrary times.

- \* The probability that  $k$  frames are generated during a given frame time is given by the Poisson Distribution:

$$\textcircled{2} \quad P_r[k] = \frac{G^k e^{-G}}{k!}$$

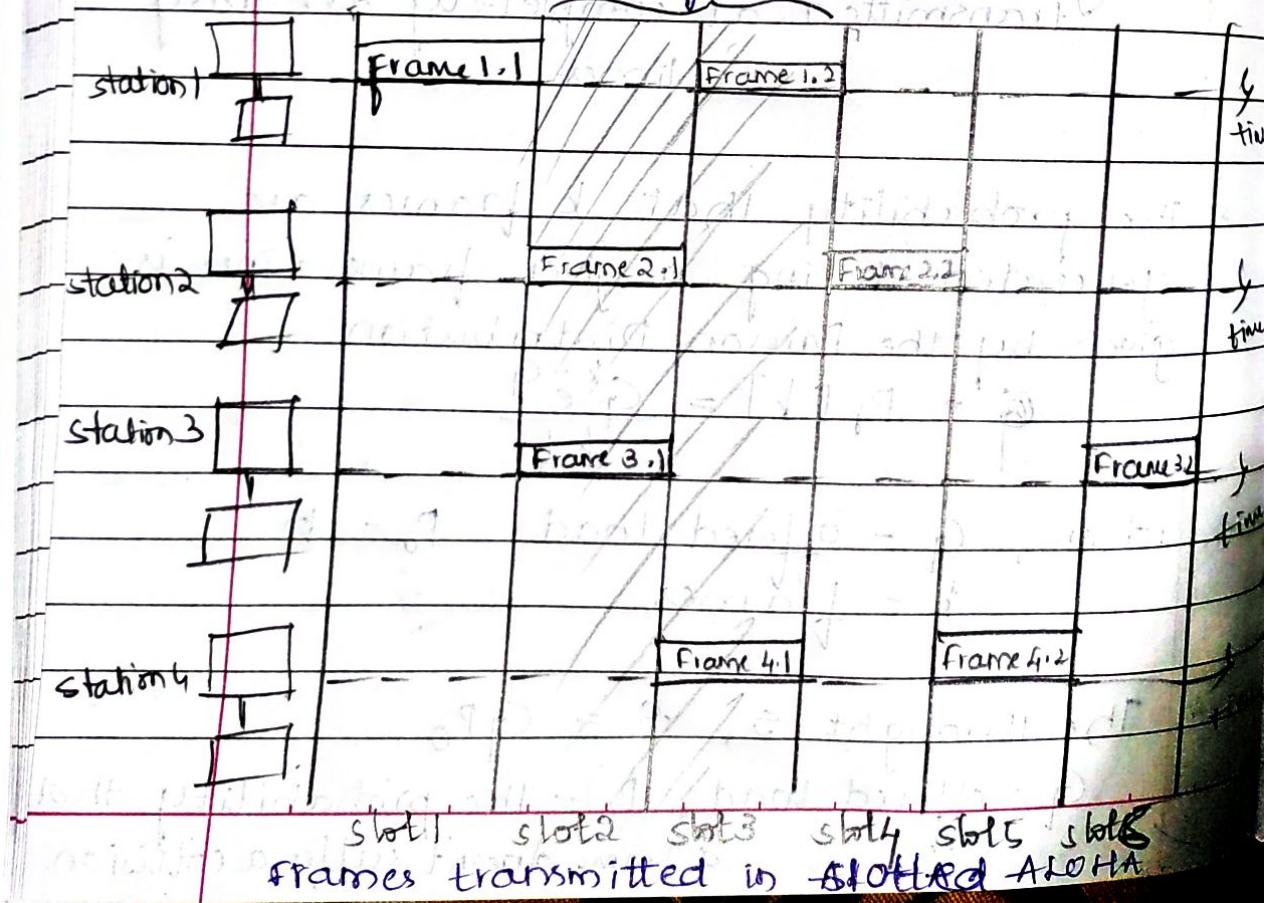
where,  $G$  - offered load     $P_0$  - ~~probability that a frame doesn't suffer a collision~~  
 $k$  - frames

- \* The throughput  $S$ ,  $S = G P_0$ .

~~G = offered load,  $P_0$  = the probability that a frame doesn't suffer a collision.~~

## 10) Slotted ALOHA :

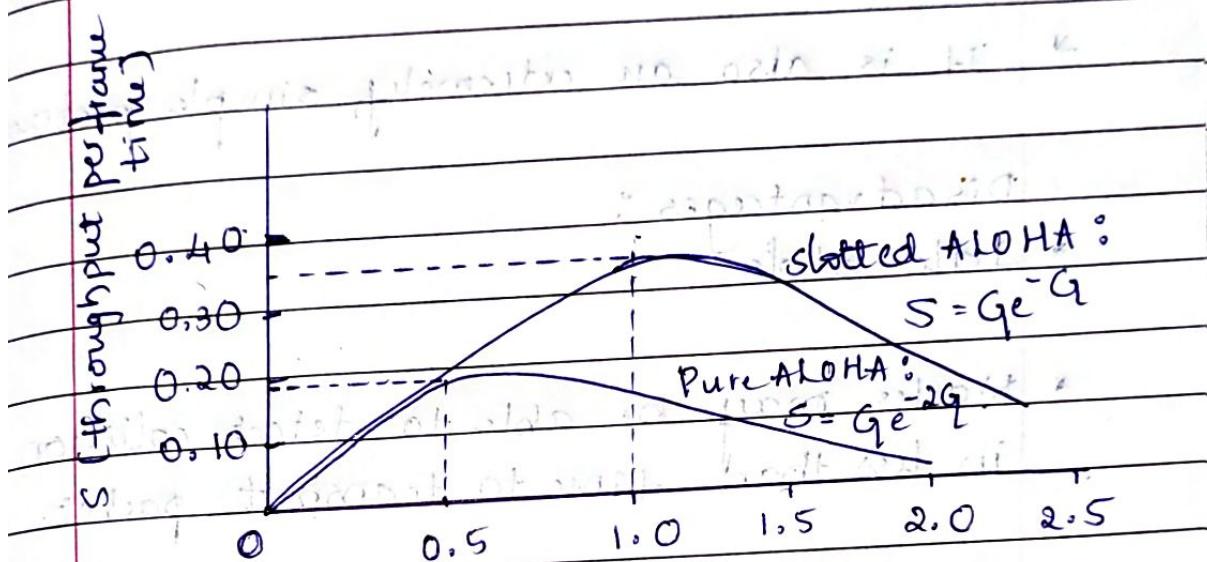
- \* Slotted ALOHA was invented to improve the efficiency of pure ALOHA as channel collision in pure ALOHA are very high.
- \* In slotted ALOHA, the time of the channel divided into discrete intervals called slots.
- \* The stations can send a frame only at the beginning of the slot & only one frame is sent in each slot.
- \* In slotted ALOHA, if any station is not able to place the frame onto the channel at the beginning of the slot, then ~~collision duration~~



\* What is the efficiency of an ALOHA channel?

- Pure ALOHA  $\rightarrow S = Ge^{-2G}$

- Slotted ALOHA  $\rightarrow S = Ge^{-G}$



Throughput v/s offered traffic for ALOHA systems.

\* Maximum for pure ALOHA occurs at  $G = 0.5$  for which  $S = \frac{1}{2}e = 0.184$  which means the rate of successful transmission is  $\approx 18.4\%$ .

\* For slotted ALOHA,  $G = 1$ ,  $S = \frac{1}{2}e = 0.368$   $36.8\%$ .

Advantages :

- \* A single active node can continuously transmit at full rate of channel
- \* Slotted Aloha is also decentralized
- \* It is also an extremely simple protocol

Disadvantages :

- \* Idle slots
- \* Nodes may be able to detect collision in less than time to transmit packet.
- \* Clock synchronization