

QuadGlide F4 REV B1

A Features:

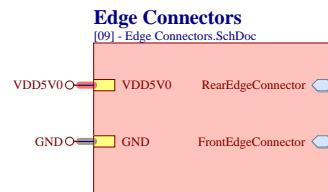
- STM32F4 processor running at 168MHz
- ICM-20689 Gyro / Accelerometer
- 32MB Flash memory
- Switched regulator
 - Max 6S (28V)
 - Max 0.4A for 5V pin on edge connector
 - Reverse polarity protection on battery input
- All I/O on edge connectors are ESD protected
- Bidirectional level shifters 3V <> 5V on ESC ports (1-4)
- Button to enable DFU bootloader

B Physical:

- Standard 36.5x36.5 Board (30.5x30.5 mounting)
- I/O:s placed to be easy accessed for Alien frame (4"-6")

C Connectivity:

- Two 18-pin edge connectors
 - Three hardware serial ports 3V (5V tollerant) ports (UART2, UART5 and UART6)
 - Serial port inverter allows S.BUS receivers to be used without external inverter.
 - Telemetry 1-wire port is not inverted. X4R can be modified to be non-inverting.
 - Four PWM outputs for ESC. Selectable 3V or 5V
 - Four 1-wire ports for ESC telemetry.
 - Buzzer port
 - IR LED
 - 5V power from battery or USB
- USB 2.0 connector with trough hole pins for robustness
 - Bihami passthrough via USB
- JTAG debug port



This schematic is *NOT SUPPORTED* and DOES NOT constitute a reference design. Only "community" support is allowed via resources at [github](#) or [flighttronics.se](#)

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A Microprocessor

[02] - MCU.SchDoc

VDD3V0O --- VDD3V0
VDD5V0O --- VDD5V0
GNDO --- GND

GYRO

A Gyro and Accelerometer

[03] - Gyro.SchDoc

VDD3V0O --- VDD3V0
GNDO --- GND

GYRO

A USB Interface

[06] - USB.SchDoc

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USB --- GND
GND --- VBUS

A Voltage regulators

[04] - Power.SchDoc

VBUS --- VBAT
VIN_FILTERED --- VIN

VIN --- VIN_FILTERED

VDD3V0O --- VDD3V0
VDD5V0O --- VDD5V0
GNDO --- GND

A NOR Flash memory

[07] - Flash.SchDoc

VDD3V0O --- VDD3V0
GNDO --- GND

NOR_FLASH

D LED:s

[08] - LED.SchDoc

VDD5V0O --- VDD5V0
GNDO --- GND

LED

Design QuadGlide F4

Page 1.

Size A3 Revision B1 Author ANDKI

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File [01] - COVER PAGE.SchDoc



The STM32F405/415 lines are designed for medical, industrial and consumer applications where the high level of integration and performance.

Performance: At 168 MHz, the STM32F405/415 deliver 210 MFIPS/566 CoreMark performance executing from Flash memory, with 0-wait states using ST's ART Accelerator. The DSP instructions and the floating point unit enlarge the range of addressable applications.

Rich connectivity: Superior and innovative peripherals

2x USB OTG (one with HS support)
Audio: dedicated audio PLL and 2 full duplex I^SS

USB: 2x high speed interfaces (including 6x USARTs running at up to 10.5 Mbit/s, 3x SPI running at up to 42 Mbit/s,

3x I^C, 2x CAN, SDIO)

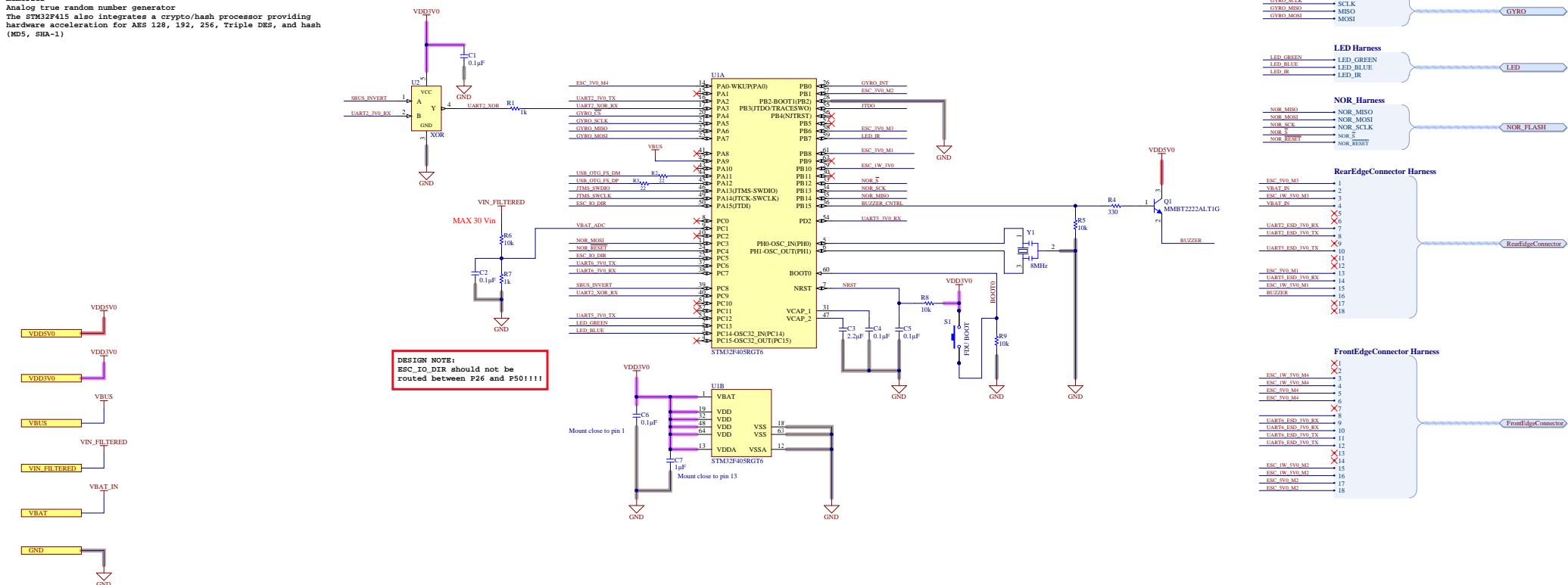
Analog: two 12-bit DACs, three 12-bit ADCs reaching 2.4 MSPS or 7.2 MSPS in interleaved mode

Up to 17 timers: 16- and 32-bit running at up to 168 MHz

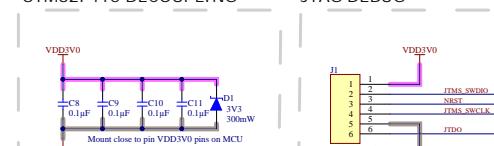
Easily extendable memory range using the flexible static memory controller supporting Compact Flash, SRAM, PSRAM, NOR and NAND memories

Analog true random number generator

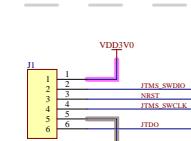
The STM32F415 also integrates a crypto/hash processor providing hardware acceleration for AES 128, 192, 256, Triple DES, and hash (MD5, SHA-1)



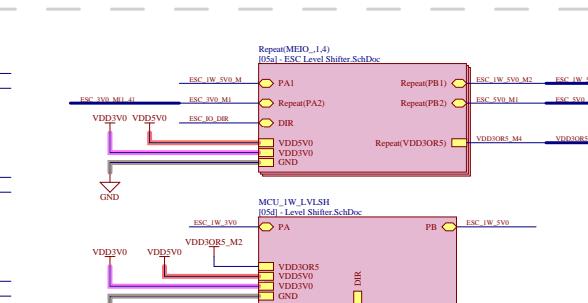
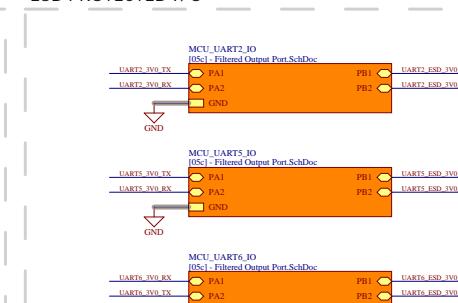
STM32F415 DECOUPLING



JTAG DEBUG



ESD PROTECTED I/O



Design QuadGlide F4			
Page 2		Author ANDKI	
Size A2	Revision B1	Date 2017-01-22	Time 09:29:56
File 021 - MCU.SchDoc	Sheet 2 of 16		

A

A

B

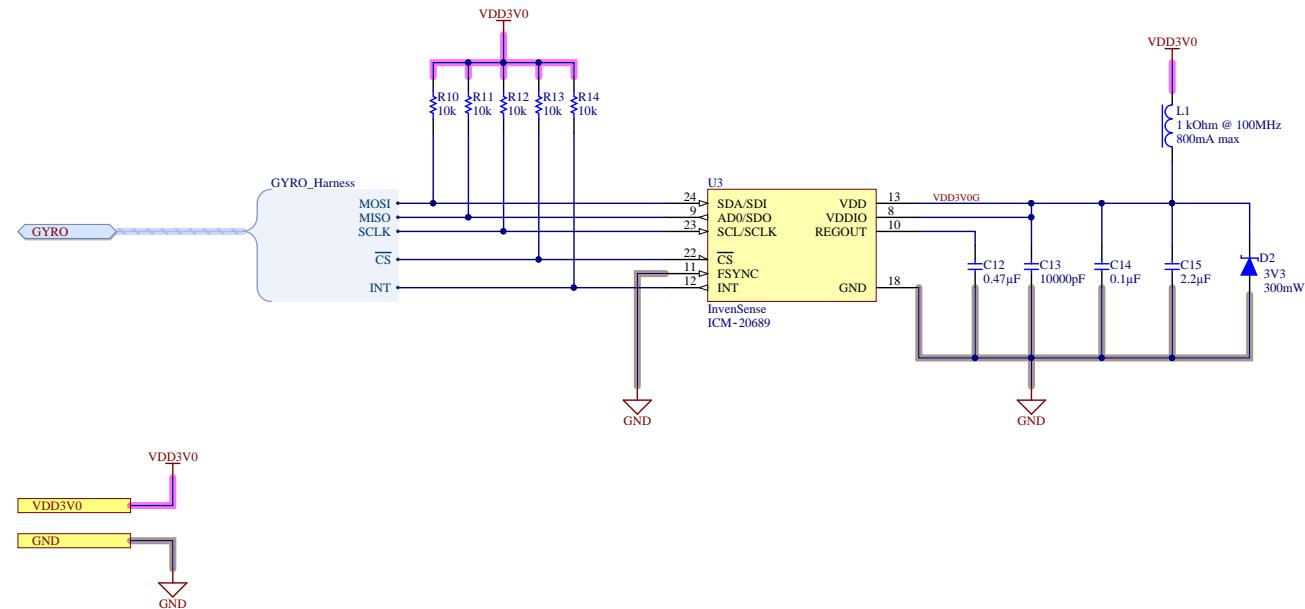
B

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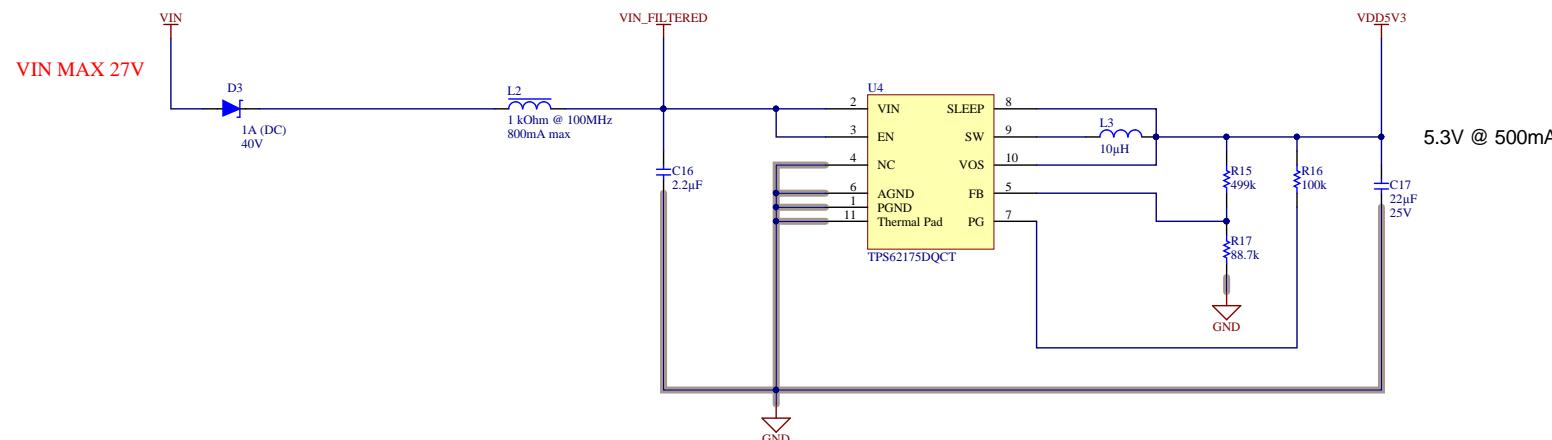
The ICM-20689 is a 6-axis MotionTracking device that combines a 3-axis gyroscope, 3-axis accelerometer, in a small 4x4x0.9mm (24-pin QFN) package.

- * Large 4K-byte FIFO to reduce traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode
- * Gyroscope programmable FSR of ±250dps, ±500dps, ±1000dps and ±2000dps
- * Accelerometer with Programmable FSR of ±2g, ±4g, ±8g and ±16g
- * EIS FSYNC support

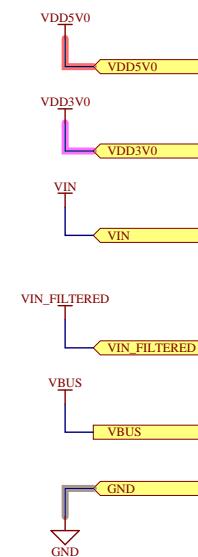
ICM-20689 includes on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features an operating voltage range down to 1.71 V. Communication ports include I²C and high speed SPI at 8 MHz.

Design Page	QuadGlide F4 3.			
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File [03] - Gyro.SchDoc		Sheet 3 of 16		

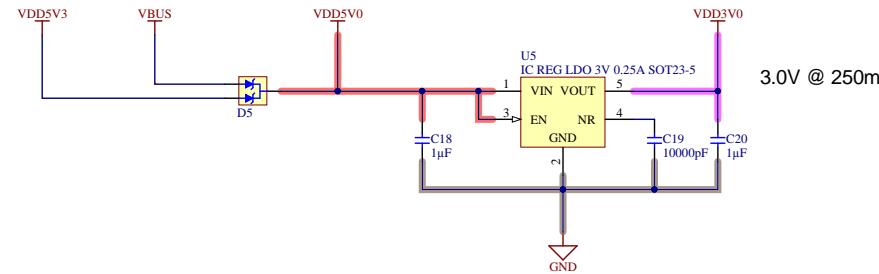
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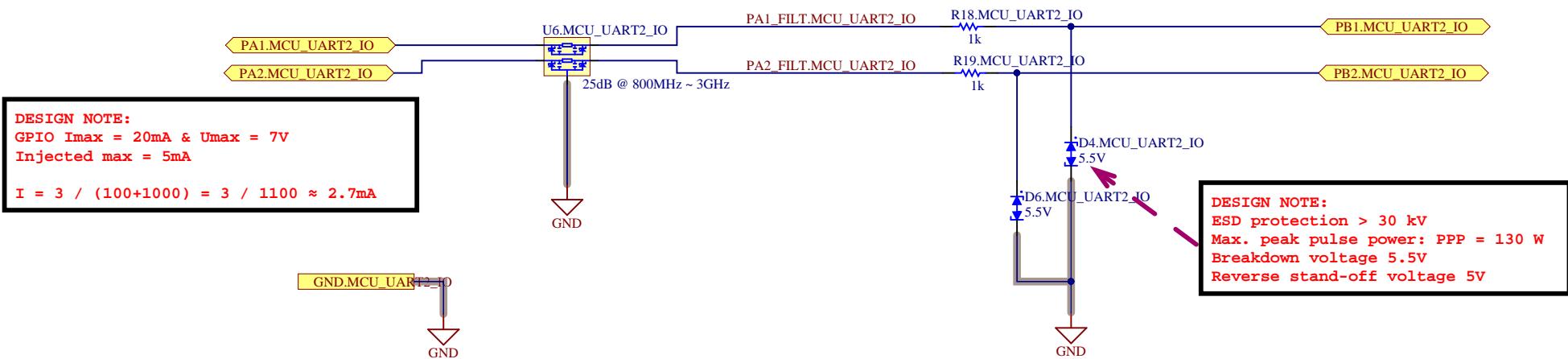


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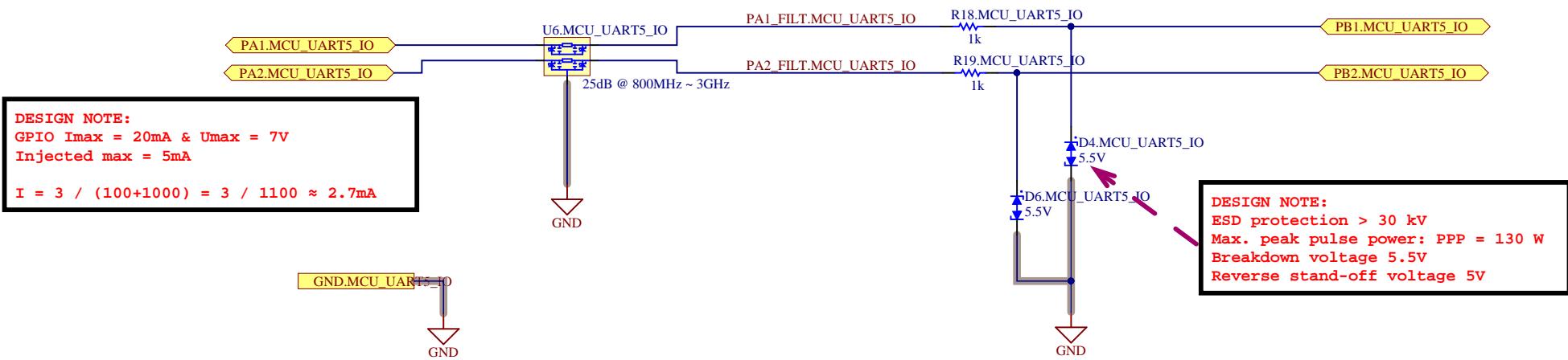


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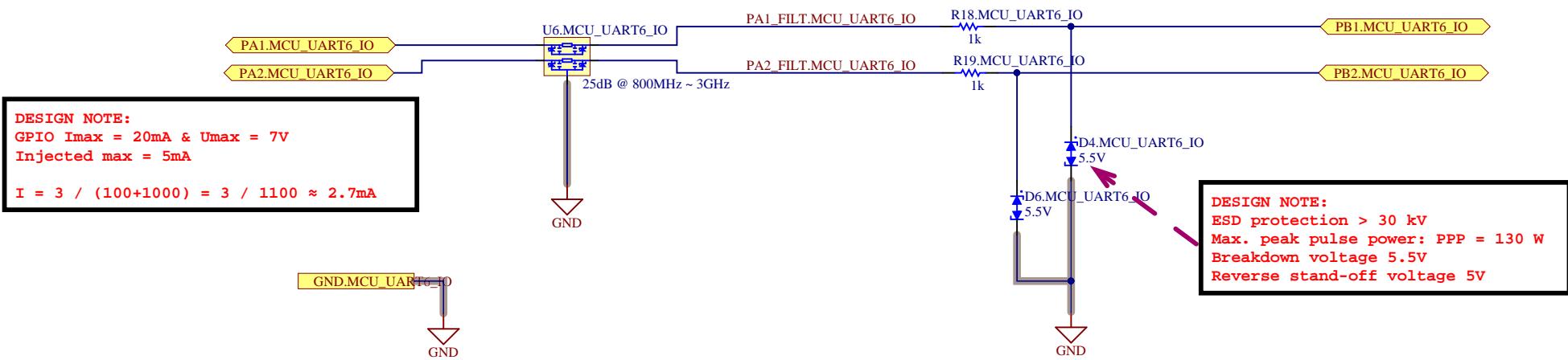
Design QuadGlide F4		
Page 4.		
Size A3	Revision B1	Author ANDKI
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File [04] - Power.SchDoc		Right-click for All



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File	[05c] - Filtered Output Port.SchDoc	Sheet 5.1 of 16

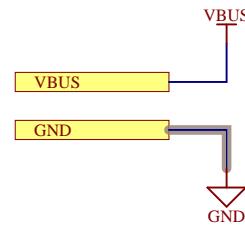


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Size	A4	Revision B1
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File	[05c] - Filtered Output Port.SchDoc	Sheet 5.2 of 16

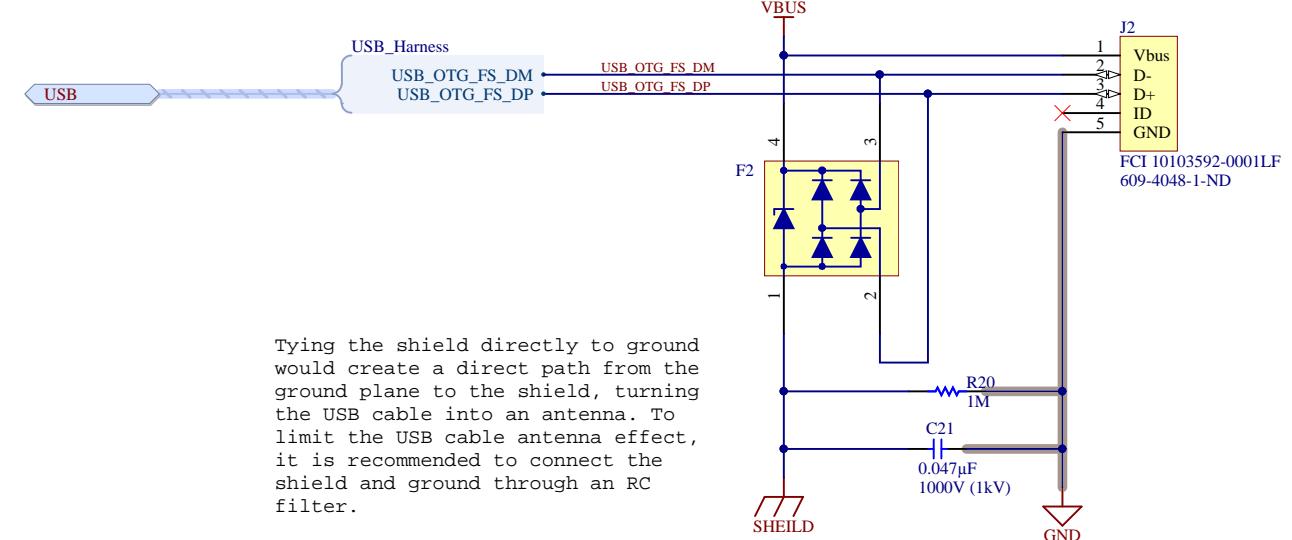


Design Page	QuadGlide F4 5.3	
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File	[05c] - Filtered Output Port.SchDoc	Sheet 5.3 of 16

A



B



Tying the shield directly to ground would create a direct path from the ground plane to the shield, turning the USB cable into an antenna. To limit the USB cable antenna effect, it is recommended to connect the shield and ground through an RC filter.

C

D

Design Page	QuadGlide F4 6.	
Size A4	Revision B1	Author ANDKI
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File [06] - USB.SchDoc		

A

A

B

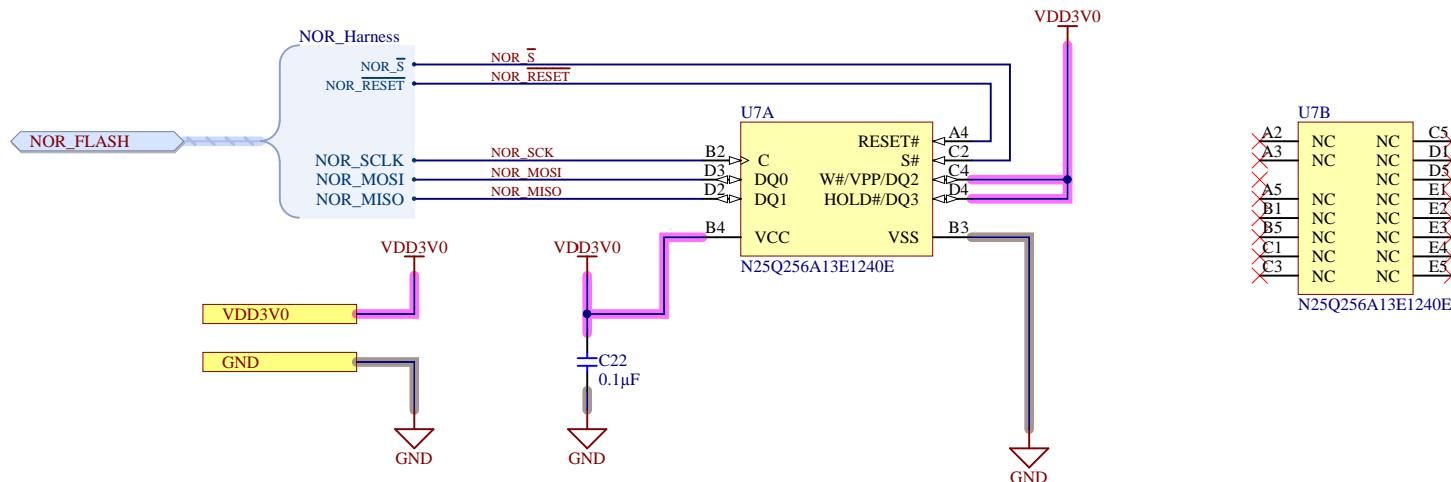
B

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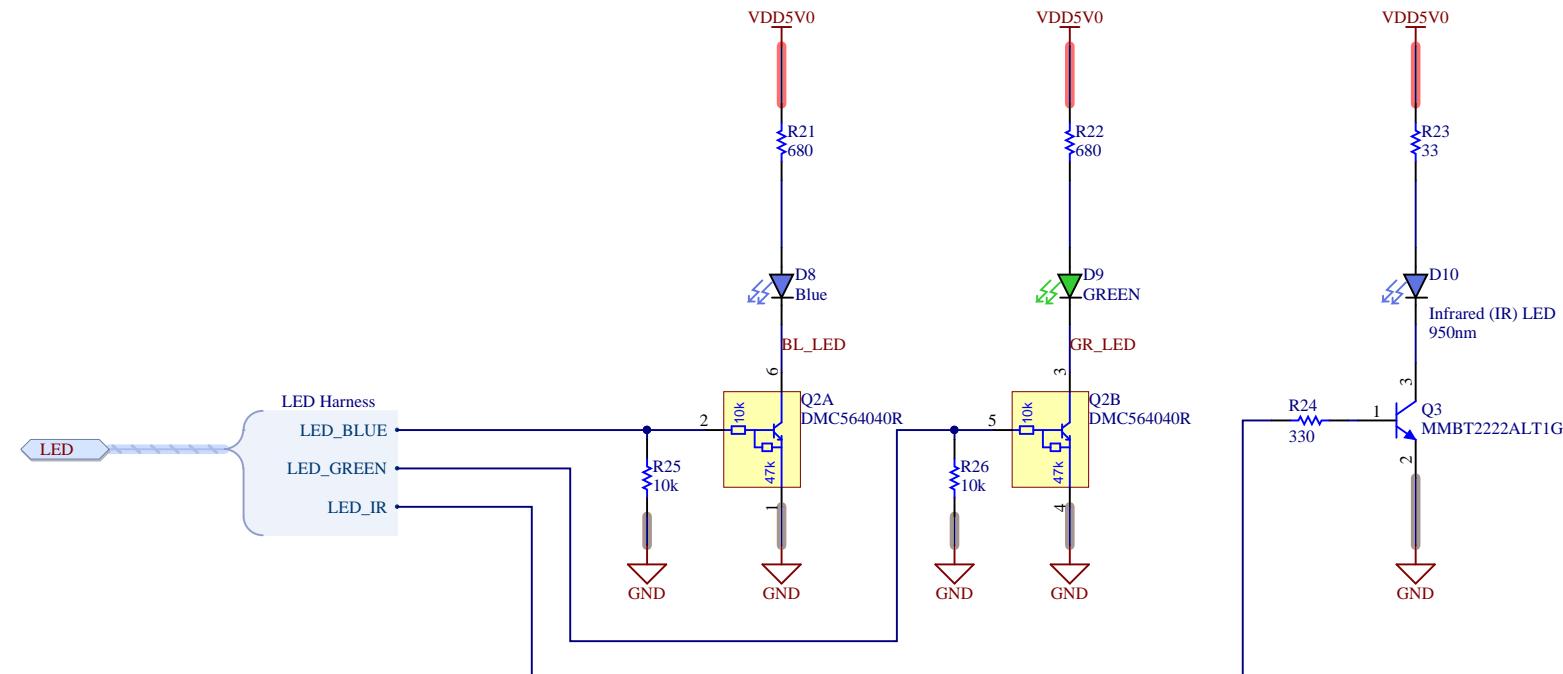
**Micron Serial NOR Flash Memory
3V, Multiple I/O, 4KB Sector Erase**

The N25Q is the first high-performance multiple input/output serial Flash memory device manufactured on 65nm NOR technology. It features execute-in-place (XIP) functionality, advanced write protection mechanisms, and a high-speed SPI-compatible bus interface. The innovative, high-performance, dual and quad input/output instructions enable double or quadruple the transfer bandwidth for READ and PROGRAM operations.

- * Memory Size 256M (64Mx4)
- * Speed 108MHz
- * Interface SPI Serial
- * Voltage - Supply 2.7 V 3.6 V
- * Operating Temperature -40°C 85°C (TA)

Design Page	QuadGlide F4 7.	
Size	A4	Revision B1
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File	[07] - Flash.SchDoc	Sheet 7 of 16

A



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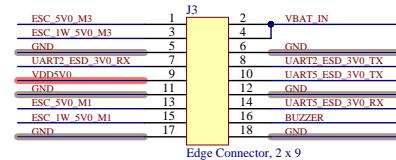
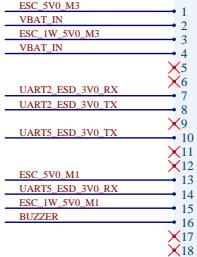
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Size	A4	Revision	B1
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File	[08] - LED.SchDoc	Sheet	8 of 16



A

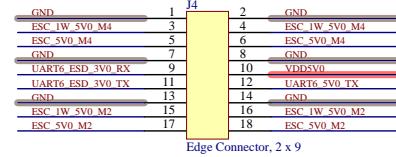
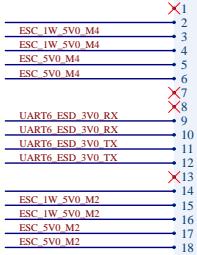
A

Rear Edge Connector**RearEdgeConnector Harness**

RearEdgeConnector

B

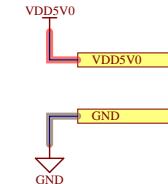
B

Front Edge Connector**FrontEdgeConnector Harness**

FrontEdgeConnector

C

C



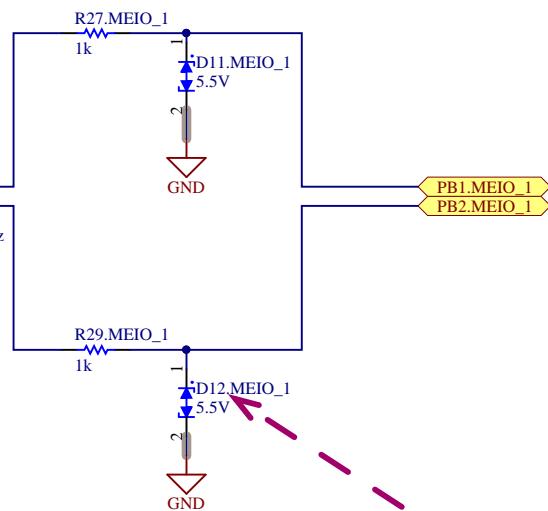
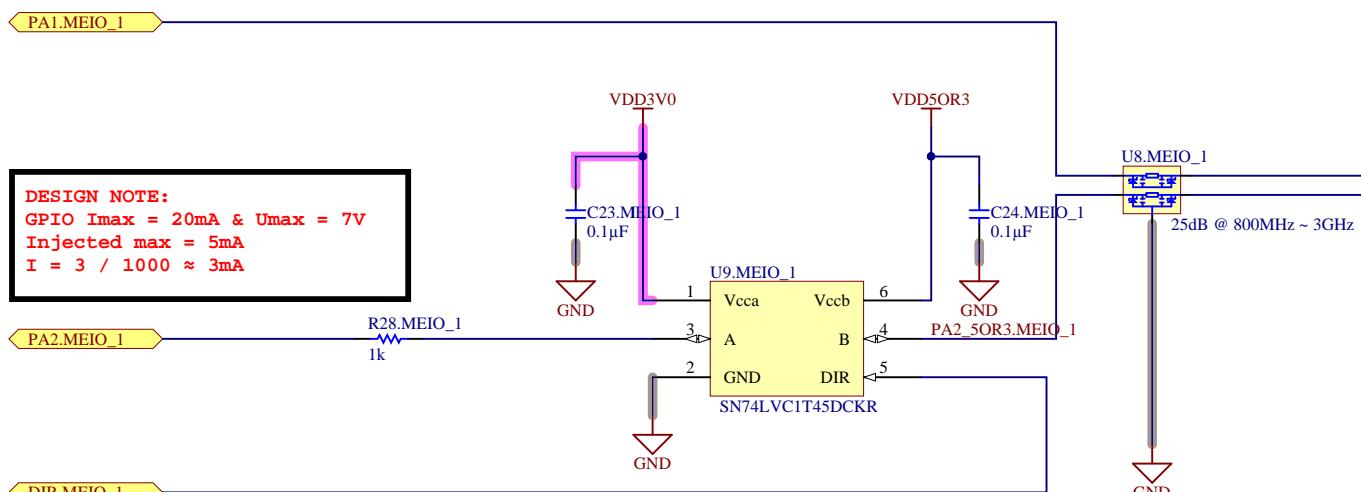
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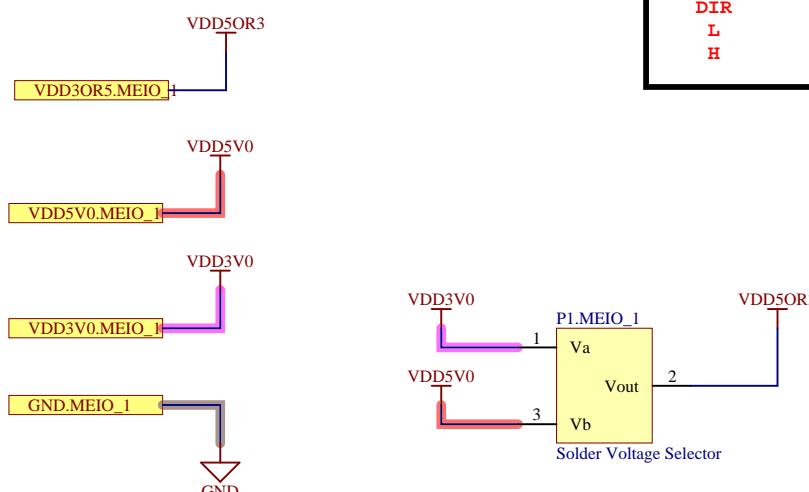
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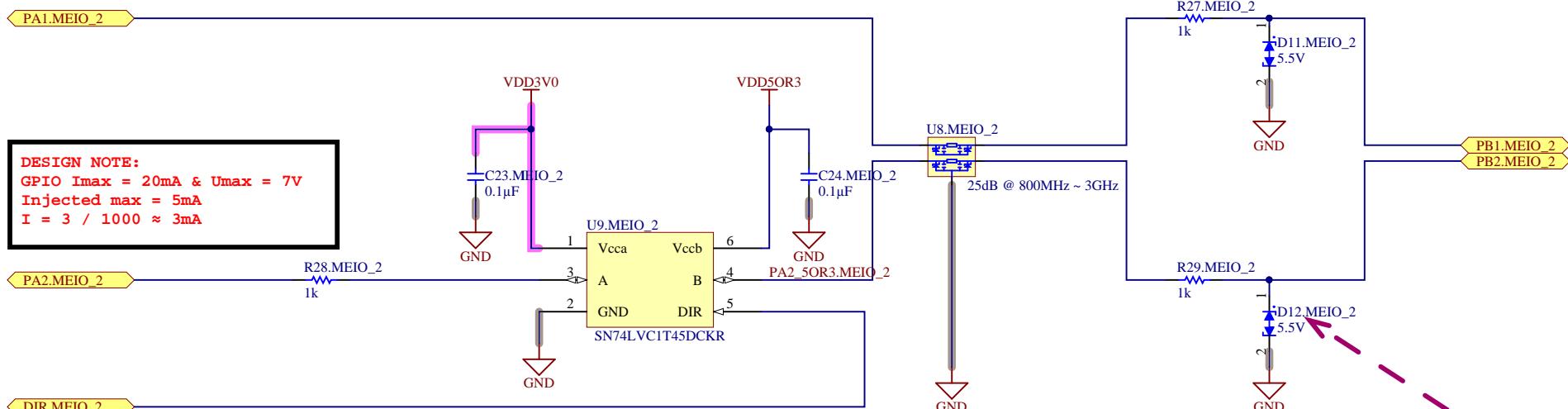
DESIGN NOTE:
DIR OPERATION
L B data to A bus
H A data to B bus

DESIGN NOTE:
ESD protection > 30 kV
Max. peak pulse power: PPP = 130 W
Breakdown voltage 5.5V
Reverse stand-off voltage 5V



Design Page			QuadGlide F4
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File [05a] - ESC Level Shifter.SchDoc			

A



B

A

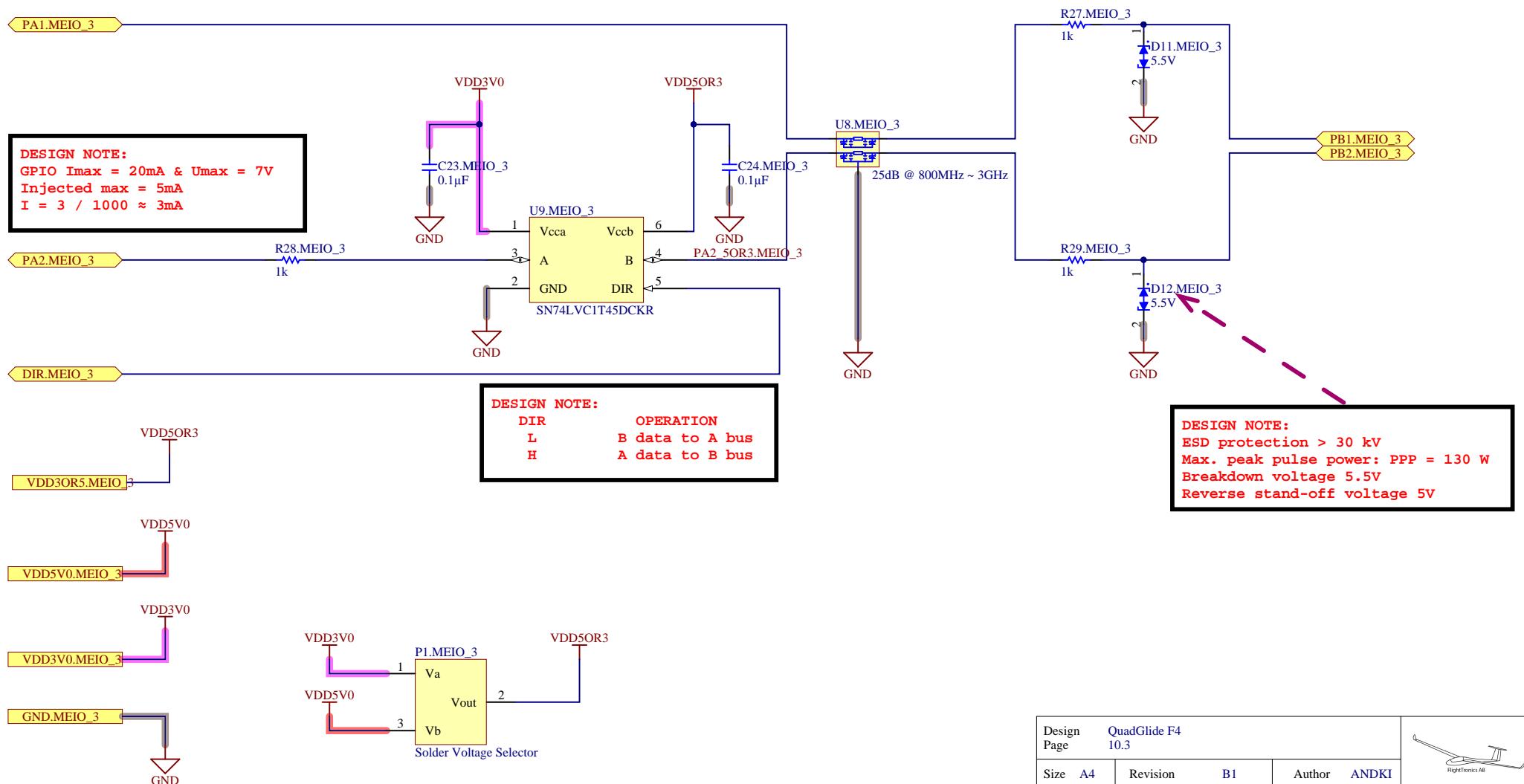
C

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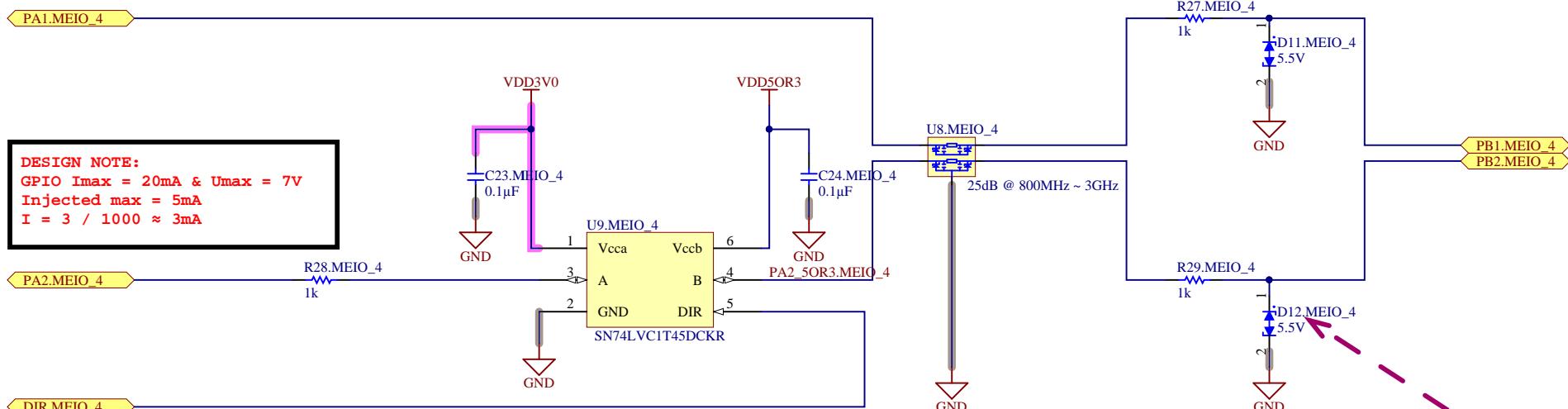
C





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File	[05a] - ESC Level Shifter.SchDoc			

A



B

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D

A

B

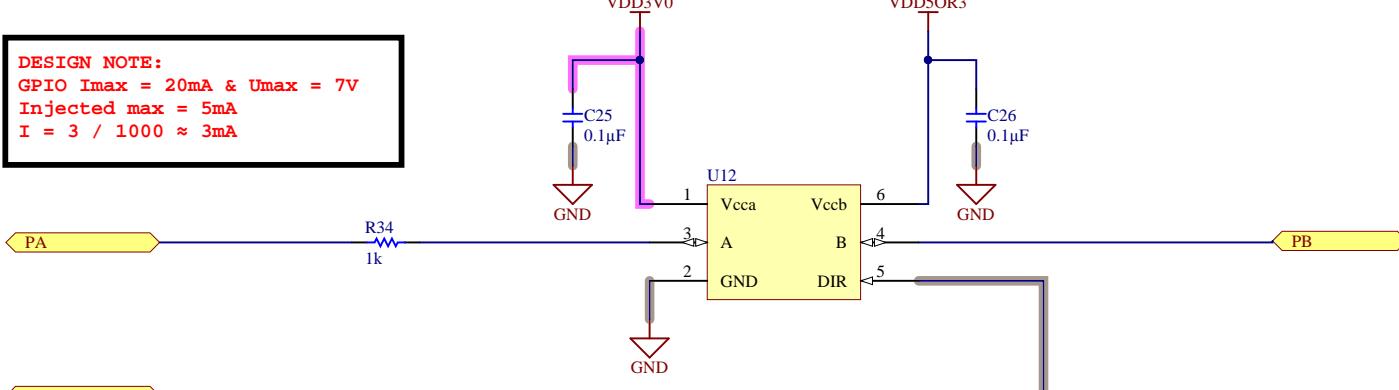
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Design Page			QuadGlide F4 10.4
Size A4	Revision B1	Author ANDKI	
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File [05a] - ESC Level Shifter.SchDoc			

A

A



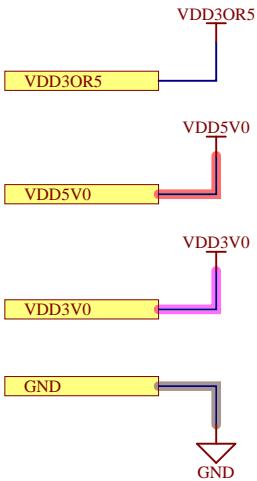
B

B

DESIGN NOTE:
DIR OPERATION
L B data to A bus
H A data to B bus

C

C



D

D

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