The following table shows how the entire indirect and program address space is allocated.CPU registers belong to the direct address space, which is separate from data and program memory address spaces.

All memories use byte addressing, although all accesses to instruction memory and registers are in 32-bit word multiples, 32-bit word-aligned. Data accesses vary in width, depending on instruction. Operand addressing in data memory is big-endian – i.e., the most significant byte has the lowest address. Bit numbering within registers and instruction and data memory is little-endian, with bit 0 being the least significant bit.

Indirect and Program Space Address Map

Address Range	Function
Mapped Space	
0000 0000–AFFF FFFC	Translated by MMU
Unmapped Space	
B000 0000–B0FF FFFC	External Flash (16 MB)
B100 0000–B800 07FC	*Reserved*
B800 0800–B800 083C	HRT Table 0.
B800 0840–B800 08FC	*Reserved*
B800 0900–B800 093C	HRT Table 1.
B800 0940–B8FF FFFC	*Reserved*
B900 0000–B900 0FFC	On-chip peripherals (includes timers and debug port). For data (indirect) space, these on-chip peripherals occupy 4 KB. For Debug Port instruction space, there is 16 MB available at this block of addresses.
B900 1000–B9FF FFFC	*Reserved*
BA00 0000–BAFF FFFC	I/O controllers (16 MB).
BB00 0000–BFFB FFFC	*Reserved*
BFFC 0000–BFFF FFFC	On-chip SRAM (256 KB)*
C000 0000–FFFF FFFC	External DRAM (1024 MB)

Application Note

Ubicom®, Inc.

Ubicom develops networking and media processor solutions that address the unique demands of real-time interactive applications and multimedia content delivery in the digital home. The company provides optimized system-level solutions for a wide range of products including wireless routers, access points, bridges, VoIP gateways, networked digital photo frames, and streaming media players.

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