DesignWare Cores MIPI D-PHY Bidir 4L for TSMC 40-nm LP /2.5V

Databook

July 21, 2011

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Contents

Revision History

Date	Description
April 12, 2011	Initial version
July 21, 2011	Corrected the PHY + PLL macro size (required for Master configuration) to be 1.005 mm^2 in Table 11-1.

Preface

This document describes the DesignWare Cores MIPI D-PHY Bidir 4L —Synopsys's Mobile Industry Processor Interface (MIPI) physical layer IP. The MIPI D-PHY Bidir 4L macro implements the physical layer of bidirectional universal lanes for the MIPI D-PHY interface. The DesignWare Cores MIPI D-PHY Bidir 4L is a reusable IP solution for both master-side and slave-side applications, targeted at the TSMC 40-nm LP /2.5V fabrication process.

MIPI D-PHY Bidir 4L for TSMC 40-nm LP /2.5V can be found on the Synopsys Web site at:

https://www.synopsys.com/dw/dwdl.php?id=dwc_mipi_dphy_bd_4l_tsmc40lp25

Databook Organization

This Databook is organized as follows:

- Chapter 1, Product Overview, provides an introduction to DWC D-PHY Bidir 4L and its features.
- Chapter 2, Deliverables, describes the DWC D-PHY Bidir 4L deliverables database for a full-package release.
- Chapter 3, Signal Descriptions, describes the DWC D-PHY Bidir 4L top-level signals.
- Chapter 4, Functional Description, provides a functional overview of the DWC D-PHY Bidir 4L and describes its various operating modes and test mode.
- Chapter 5, PLL Programming, discusses PLL programming details.
- Chapter 6, External Software Calibration Requirements, describes the software virtual calibration machine.
- Chapter 7, Timing Model Usage Guidelines, provides the guidelines for timing model usage.
- Chapter 8, Test and Configuration Modes, describes the subset of features that can be used during characterization stage and production testing.
- Chapter 9, Assembly Guidelines, describes the general guidelines regarding the IP integration.
- Chapter 10, PCB Guidelines, provides general recommendations for PCB layout common to most high speed digital communication environments.
- Chapter 11, Process-Specific Specifications, provides specifications that are specific to the fabrication process.
- Appendix A, Timing Diagrams, shows some important timing diagrams.

Web Resources

- DesignWare IP product information: http://www.designware.com
- Your custom DesignWare IP page: http://www.mydesignware.com
- Documentation through SolvNet: https://solvnet.synopsys.com (Synopsys password required)
- Synopsys Common Licensing (SCL): http://www.synopsys.com/keys

Reference Documentation

- MIPI Alliance Specification for D-PHY Version 1.00.00 – 14 May 2009
- MIPI Alliance Test Program, D-PHY Physical Layer Conformance Test Suite Version v1.00

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To obtain support for your product, contact Support Center using one of the following methods:

- *For fastest response*, use the SolvNet website. If you fill in your information as explained below, your issue is automatically routed to a support engineer who is experienced with your product. The **Sub Product** entry is critical for correct routing.

  Go to http://solvnet.synopsys.com/EnterACall and click on the link to enter a call.
  Provide the requested information, including:

  - **Product:** DesignWare Cores
  - **Sub Product:** MIPI D-PHY
  - **Tool Version:** <product_version_number>
  - **Problem Type**:
  - **Priority**:
  - **Title:** MIPI D-PHY for TSMC 40-nm LP /2.5V
  - **Description:** Support would like you to provide a short summary of the issue or error message you have encountered.

    For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood.

- Or, send an e-mail message to support_center@synopsys.com (your e-mail will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
  - Include the Product name, Sub Product name, process, and Tool Version number in your e-mail (as identified above) so it can be routed correctly.
  - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood.
  - Attach any debug files you created.
- Or, telephone your local support center:
  - North America:

    Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
  - All other countries:

    http://www.synopsys.com/Support/GlobalSupportCenters

1 Product Overview

1.1 General Product Description

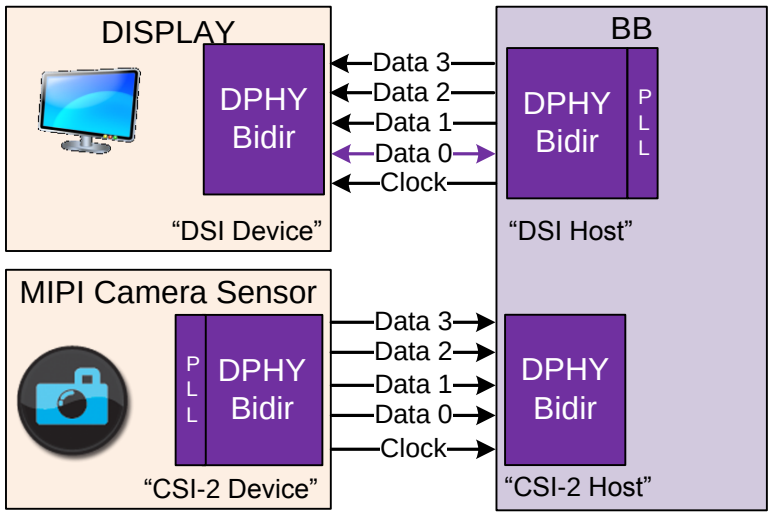
The DWC D-PHY Bidir 4L macro implements the physical layer of bidirectional universal lanes for the MIPI D-PHY interface, stacked in a four data lane and one clock lane configuration. This IP is reusable for both master and slave applications. The lane modules are full-featured, bi-directional modules with HS-TX, HS-RX, LP-TX, LP-RX, and LP-CD functions, but with no support for HS reverse communication.

DWC D-PHY Bidir 4L also includes a clock multiplier PLL for HS clock generation needed in a master-side application. It is targeted for digital data transmission between a host processor and display drivers or camera interfaces in mobile applications, supporting a maximum effective bit rate of 1 Gbps (per lane). The assembled four data lane system enables up to 4 Gbps aggregate communication throughputs, delivering the bandwidth needed for high throughput data transfer.

Given its dual master/slave reusability, DWC D-PHY Bidir 4L builds a highly reliable bidirectional high-speed differential interface for serial data transmission with an additional reduced throughput low-power data transfer mode in the same differential pair-reducing line count and minimizing cable wires and EMI shielding requirements.

Figure 1-1 shows a typical application for DWC D-PHY Bidir 4L.

Figure 1-1 Typical Application for DWC D-PHY Bidir 4L



1.2 Standards Compliance

The DWC D-PHY Bidir 4L is compliant with the MIPI D-PHY interface specification, revision 1.0.

1.3 Features

The DWC D-PHY Bidir 4L has the following features:

- Attachable PLL clock multiplication unit for master-side functionality
- Flexible input clock reference 17 MHz to 27 MHz
- 50% DDR output clock duty-cycle
- Lane operation ranging from 80 to 1000 Mbps in forward direction
- Aggregate throughput up to 4 Gbps with four data lanes
- Protocol peripheral interface (PPI) for clock and data lanes
- Low-power escape modes and ultra low-power state
- 2.5 V ± 10% Analog supply operation
- 1.1 V ± 10% Digital supply operation
- Core Area:
  - For Slave configuration: 0.81 mm^2
  - For Master configuration: 1.005 mm^2

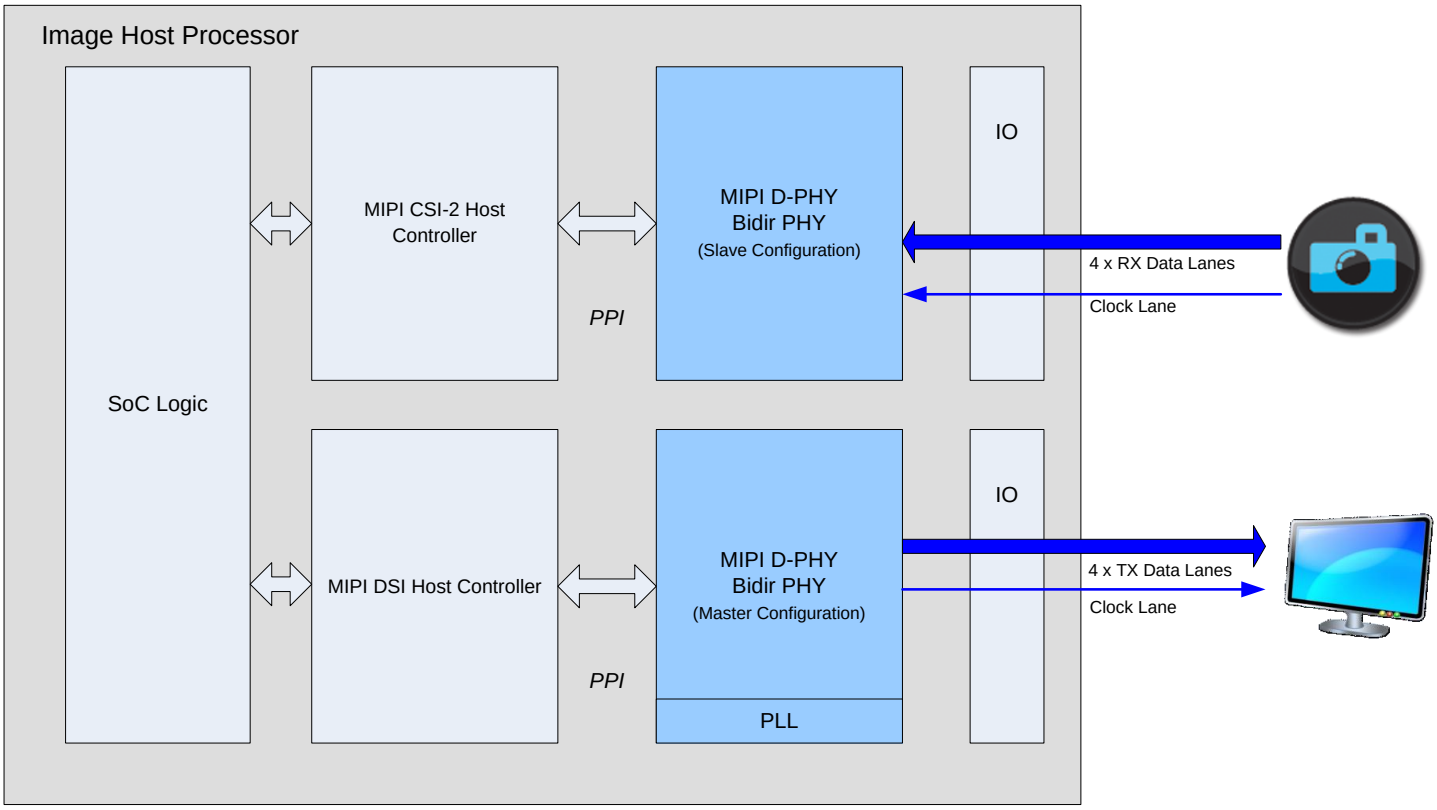
1.4 DWC D-PHY Bidir 4L System-Level Overview

This section provides a system-level overview of DWC D-PHY Bidir 4L.

1.4.1 System-Level Block Diagram

Figure 1-2 shows a system-level block diagram of DWC D-PHY Bidir 4L.

Figure 1-2 DWC D-PHY Bidir 4L System-Level Block Diagram



The MIPI D-PHY macro interfaces with a CSI-2 or DSI Host controller. The CSI-2 or DSI Host controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 or DSI specifications, providing an interface between the System and the MIPI D-PHY, allowing the communication with a compliant MIPI Camera Sensor or Display. I/O block is responsible for interface with the analog physical world.

1.4.2 DWC D-PHY Bidir 4L

DWC D-PHY Bidir 4L is the physical layer of a MIPI CSI-2/DSI capable Host/Device.

For a functional block diagram and a functional description of the DWC D-PHY Bidir 4L, refer to Functional Description.

1.4.2.1 Interfaces

The DWC D-PHY features both an inter-chip and an intra-chip interface. The first relies on four data lanes and one clock lane which can be configured in TX or RX direction. The second interface is defined between the D-PHY and the higher protocol layers of a communication stack and comprises parallel TX and RX data. This interface complies with informative Logical PHY-Protocol Interface (PPI) description in Annex A of D-PHY specification.

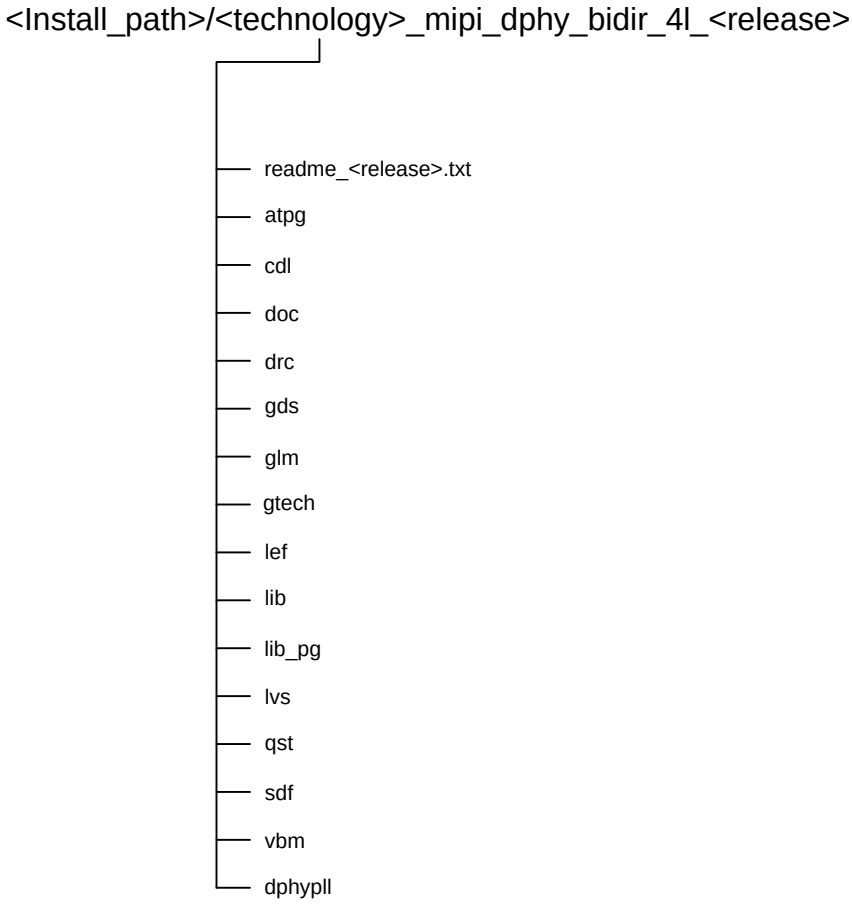
2 Deliverables

2.1 Directory Structure

This section describes the DWC D-PHY Bidir 4L deliverables database for a full-package release—its directory structure and contents.

Figure 2-1 shows the directory structure of the DWC D-PHY Bidir 4L database deliverables for a full-package release.

Figure 2-1 Database Deliverables Directory Structure



2.2 Directory Contents

Table 2-1 describes the contents of each directory in the database deliverables.

Note If any of the deliverables under the directories in Table 2-1 are metal-dependent, one or more <metal option> directories will reside within the main view directory to differentiate the deliverables.

Table 2-1 Database Deliverables Contents

Directory	Contents
-	Readme file[1]: readme_<version>.txt
atpg	Automatic Test Pattern Generation (ATPG) model and coverage report: ■ mipi_4_bidir_dphy_atpg.v ■ mipi_4_bidir_dphy_atpg_coverage.log
cdl[2]	Circuit Design Language (CDL) netlist for LVS: mipi_4_bidir_dphy.cdl
doc	Databook: This document
drc[b]	Design Rule Check (DRC) reports
gds	GDSII layout file: mipi_4_bidir_dphy.gds.gz Layer map table: mipi_4_bidir_dphy_layer_map.txt
glm	Gate-level model: mipi_4_bidir_dphy_glm_<tool>.vp
gtech	Unencrypted GTECH Verilog model: mipi_4_bidir_dphy_gtech.v
lef	Layout abstract files: ■ mipi_4_bidir_dphy.lef ■ mipi_4_bidir_dphy_ant.lef ■ mipi_4_bidir_dphy_both.lef
lib	Synopsys timing file: mipi_4_bidir_dphy_<corner>_<mode>.lib
lib_pg	Synopsys timing file (UPF-compliant): mipi_4_bidir_dphy_<corner>_<mode>_pg.lib
lvs[b]	Layout Versus Schematic (LVS) report
qst	Quick-start test bench : mipi_4_bidir_dphy_qst.v Simulation script: mipi_4_bidir_dphy_qst_vcs_run
sdf	Standard Delay Format (SDF) file: mipi_4_bidir_dphy_<corner>.sdf
vbm	Encrypted Verilog model: Encrypted Verilog model: mipi_4_bidir_dphy_vbm_<tool>.vp
dphypll[3]	D-PHY PLL Library (used for Master configuration): DWC_DPHYPLL_<technology, device>_<version>.tar.gz

[1] For details about release contents, refer to readme file, “Contents” section.
[2] Includes both Calibre and Hercules, if available (differentiated by directories with associated tool names).
[3] Includes all PLL views, including GDSII.

3 Signal Descriptions

3.1 Top-Level I/O Diagram

Figure 3-1 shows the DWC D-PHY Bidir 4L top-level signals.

Figure 3-1 Top-Level I/O Diagram

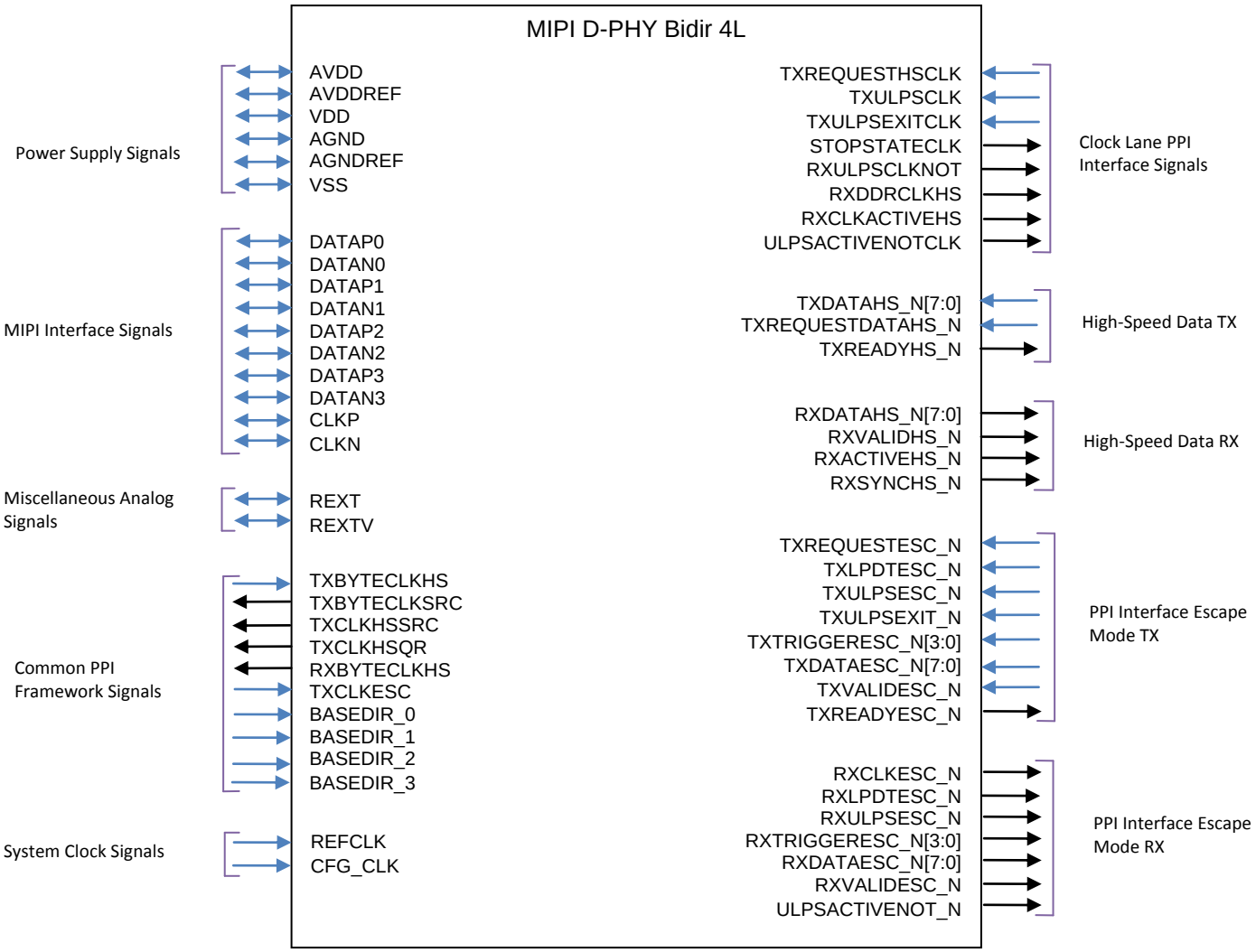
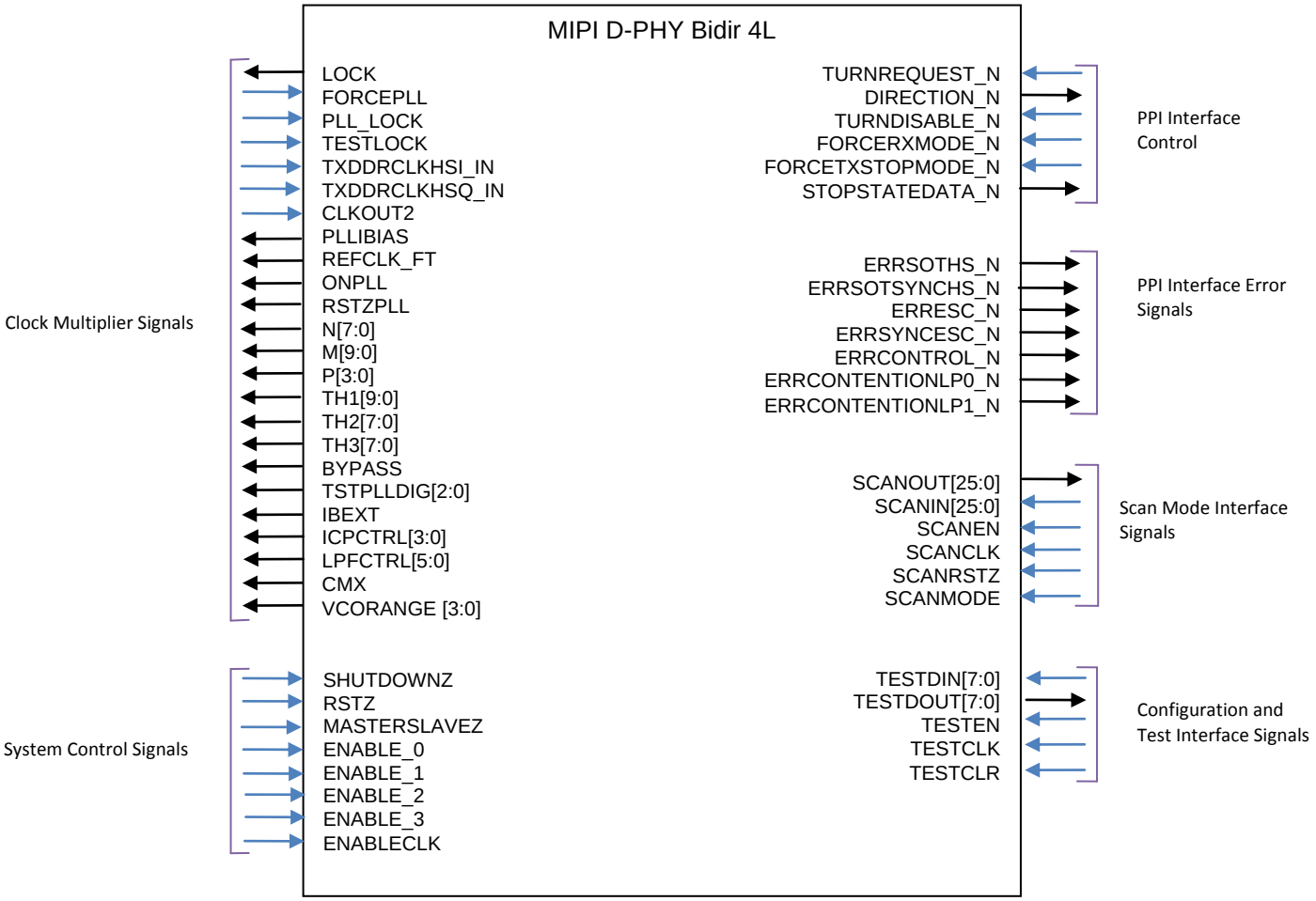


Figure 3-2 Top-Level I/O Diagram (continued)



3.2 Signal Descriptions

This section describes the top-level signals.

In addition to describing the function of each signal, the signal descriptions include the following information:

- **Voltage range:** Describes the voltage range expected on this pin.
- **Synchronous:** Indicates that the signal is asserted or de-asserted with respect to a clock edge.
- **Asynchronous:** Indicates that the signal is not asserted or de-asserted with respect to a clock edge.

All digital signals are active high unless stated otherwise.

3.2.1 Power Supply Signals

Table 3-1 describes the power supply signals.

Table 3-1 Power Supplies

Signal	I/O	Type	Description
AVDD	I/O	Power	**Function:** Analog 2.5 V power supply. **Voltage range:** ± 10% **Active state:** N/A **Synchronous to:** N/A
AVDDREF	I/O	Power	**Function:** Analog 2.5 V supply for reference generator. Should be tied directly to 2.5 V supply pad at chip level. **Voltage range:** ± 10% **Active state:** N/A **Synchronous to:** N/A
VDD	I/O	Power	**Function:** Digital 1.1 V power supply. **Voltage range:** ± 10% **Active state:** N/A **Synchronous to:** N/A
AGND	I/O	Ground	**Function:** Analog supply ground return. **Voltage range:** 0 V **Active state:** N/A **Synchronous to:** N/A
AGNDREF	I/O	Ground	**Function:** Analog supply ground return for reference generator. Should be tied directly to ground pad at chip level. **Voltage range:** 0 V **Active state:** N/A **Synchronous to:** N/A
VSS	I/O	Ground	**Function:** Digital supply ground return. **Voltage range:** 0 V **Active state:** N/A **Synchronous to:** N/A

3.2.2 MIPI Interface Signals

Table 3-2 describes the MIPI interface signals.

Table 3-2 MIPI Interface

Signal	I/O	Type	Description
DATAP0	I/O	Analog	**Function:** Positive D-PHY differential data line transceiver output, Lane 0 **Active state:** N/A **Synchronous to:** N/A
DATAN0	I/O	Analog	**Function:** Negative D-PHY differential data line transceiver output, Lane 0 **Active state:** N/A **Synchronous to:** N/A
DATAP1	I/O	Analog	**Function:** Positive D-PHY differential data line transceiver output, Lane 1 **Active state:** N/A **Synchronous to:** N/A
DATAN1	I/O	Analog	**Function:** Negative D-PHY differential data line transceiver output, Lane 1 **Active state:** N/A **Synchronous to:** N/A
DATAP2	I/O	Analog	**Function:** Positive D-PHY differential data line transceiver output, Lane 2 **Active state:** N/A **Synchronous to:** N/A
DATAN2	I/O	Analog	**Function:** Negative D-PHY differential data line transceiver output, Lane 2 **Active state:** N/A **Synchronous to:** N/A
DATAP3	I/O	Analog	**Function:** Positive D-PHY differential data line transceiver output, Lane 3 **Active state:** N/A **Synchronous to:** N/A
DATAN3	I/O	Analog	**Function:** Negative D-PHY differential data line transceiver output, Lane 3 **Active state:** N/A **Synchronous to:** N/A
CLKP	I/O	Analog	**Function:** Positive D-PHY differential clock line transceiver output. **Active state:** N/A **Synchronous to:** N/A
CLKN	I/O	Analog	**Function:** Negative D-PHY differential clock line transceiver output. **Active state:** N/A **Synchronous to:** N/A

3.2.3 Miscellaneous Analog Signals

Table 3-3 describes other analog signals.

Table 3-3 Miscellaneous Analog Signals

Signal	I/O	Type	Description
REXT	I/O	Analog	**Function:** External resistor connection (REXT and REXTV should be shorted together at the chip pad connection). Use a 6.04 KΩ E96 resistor. **Active state:** N/A **Synchronous to:** N/A
REXTV	I/O	Analog	**Function:** External resistor connection (REXT and REXTV should be shorted together at the chip pad connection). Use a 6.04 KΩ E96 resistor. **Active state:** N/A **Synchronous to:** N/A

3.2.4 Common PPI Framework Signals

Table 3-4 describes the common PPI framework signals.

Table 3-4 Common PPI Framework

Signal	I/O	Type	Description
TXBYTECLKHS	I	Digital	**Function:** High Speed Transmit byte clock. This is used to synchronize PPI signals in the High-Speed transmit clock domain. The frequency of TXBYTECLKHS is 1/8 of the serial bit rate. **Active state:** High **Synchronous to:** N/A
TXBYTECLKSRC	O	Digital	**Function:** Possible sources for the High Speed transmit byte clock TXBYTECLKHS. TXBYTECLKHS can be generated from TXBYTECLKSRC or optionally from the provided TXCLKHSSRC/TXCLKHSQR signals. No other source is allowed as the signal must be frequency and phase-locked to the internal high-speed clock signal. This signal is bypassed with SCANCLK when scan mode is enabled. **Active state:** High **Synchronous to:** N/A
TXCLKHSSRC	O	Digital	**Function:** Possible sources for the High Speed transmit byte clock TXBYTECLKHS. **Note:** The fundamental frequency of this signal is identical to the line data rate (for example, TXCLKHSSRC is 1000 MHz for an interface operating at 1000 Mb/s). This signal is bypassed with SCANCLK when scan mode is enabled. **Active state:** High **Synchronous to:** N/A

Signal	I/O	Type	Description
TXCLKHSQR	O	Digital	**Function:** Possible sources for the High Speed transmit byte clock TXBYTECLKHS. **Note:** The fundamental frequency of this signal is one quarter of the line data rate (for example, TXCLKHSQR is 250 MHz for an interface operating at 1000 Mb/s). This signal is bypassed with SCANCLK when scan mode is enabled. **Active state:** High **Synchronous to:** N/A
RXBYTECLKHS	O	Digital	**Function:** High Speed Receive byte clock. This is used to synchronize PPI signals in the high-speed receive clock domain. The frequency of RXBYTECLKHS is 1/8 of the serial bit rate. This signal is bypassed with SCANCLK when scan mode is enabled. **Active state:** High **Synchronous to:** N/A
TXCLKESC	I	Digital	**Function:** Escape mode transmit clock. This clock is directly used to generate escape sequences. The period of this clock determines the symbol time for low power signals. **Active state:** High **Synchronous to:** N/A
BASEDIR_0	I	Digital	**Function:** Configures the base direction for Lane 0. ■ BASEDIR_0 = 1: configures the Lane 0 as RX upon startup of the macro ■ BASEDIR_0 = 0: configures the Lane 0 as TX **Active state:** High **Synchronous to:** TXCLKESC
BASEDIR_1	I	Digital	**Function:** Configures the base direction for Lane 1. ■ BASEDIR_1 = 1: configures the Lane 1 as RX upon startup of the macro ■ BASEDIR_1 = 0: configures the Lane 1 as TX **Active state:** High **Synchronous to:** TXCLKESC
BASEDIR_2	I	Digital	**Function:** Configures the base direction for Lane 2. ■ BASEDIR_2 = 1: configures the Lane 2 as RX upon startup of the macro ■ BASEDIR_2 = 0: configures the Lane 2 as TX **Active state:** High **Synchronous to:** TXCLKESC
BASEDIR_3	I	Digital	**Function:** Configures the base direction for Lane 3. ■ BASEDIR_3 = 1: configures the Lane 3 as RX upon startup of the macro ■ BASEDIR_3 = 0: configures the Lane 3 as TX **Active state:** High **Synchronous to:** TXCLKESC

3.2.5 Clock Lane PPI Interface Signals

Table 3-5 describes the clock lane PPI interface signals.

Table 3-5 Clock Lane PPI Interface

Signal	I/O	Type	Description
TXREQUESTHSCLK	I	Digital	**Function:** High-speed transmit clock request signal. This signal causes the clock lane to start transmitting DDR clock on the lane interconnect. **Active state:** High **Synchronous to:** TXBYTECLKHS
TXULPSCLK	I	Digital	**Function:** Transmit Ultra Low Power on Clock Lane. This signal is asserted to cause the clock lane module to enter the ultra low-power state. The lane module remains in this mode until TXULPSEXITCLK is asserted. This signal is clocked by TXCLKESC. **Active state:** High **Synchronous to:** TXCLKESC
TXULPSEXITCLK	I	Digital	**Function:** This active-high signal is asserted to cause the clock lane module to transmit the Ultra Low Power (ULP) exit sequence and return to the “11” stop state. This signal is clocked by TXCLKESC. While TXCLKESC can be gated during ULP state, it must be reactivated so that the TXULPSEXITCLK command can be processed. **Active state:** High **Synchronous to:** TXCLKESC
STOPSTATECLK	O	Digital	**Function:** Clock Lane in Stop state. This signal indicates the clock lane module is in Stop state. **Note:** This is valid for both master and slave side. This signal is asynchronous to any clock in the PPI interface. **Active state:** High **Synchronous to:** Asynchronous
RXULPSCLKNOT	O	Digital	**Function:** This signal indicates that the clock lane module has entered the Ultra Low-Power state. This signal is kept low until a Stop state is sent or detected on the lane interconnect. **Active state:** Low **Synchronous to:** RXCLKESC
RXDDRCLKHS	O	Digital	**Function:** DDR clock signal received by the clock lane. This signal is bypassed with SCANCLK when scan mode is enabled. **Active state:** High **Synchronous to:** N/A
RXCLKACTIVEHS	O	Digital	**Function:** Indicates that the clock lane is actively receiving a DDR clock. **Active state:** High **Synchronous to:** RXDDRCLKHS

Signal	I/O	Type	Description
ULPSACTIVENOTCLK	O	Digital	**Function:** Indicates that the lane is in the Ultra Low Power (ULP) state. For a TX lane, this signal is asserted some time after TXULPSCLK. TXCLKESC must be supplied to the macro until ULPSACTIVENOTCLK is asserted. In order to leave ULP state, the transmitter first drives TXULPSEXIT high, then waits for ULPSACTIVENOT to become high (inactive). At that point, the macro is active and has started transmitting a Mark-1 on the Lines. The protocol waits for a time Twakeup and then drives TXULPSCLK inactive to return the lane to Stop state. For an RX lane, this signal indicates that the lane is in ULP state. At the beginning of ULP state, ULPSACTIVENOT is asserted together with RXCLKULPSNOT; at the end of the ULP state, this signal becomes inactive to indicate that the Mark-1 state has been observed. Later, after a period of time Twakeup, the RXULPSCLKNOT signal is de-asserted. **Active state:** Low **Synchronous to:** CFG_CLK

3.2.6 Lane *N* PPI Interface Signals

Table 3-6 describes the high-speed data TX signals.

Table 3-6 High-Speed Data TX

Signal	I/O	Type	Description
TXDATAHS_N[7:0][4]	I	Digital	**Function:** High-speed transmit data. This is an 8-bit data bus input that receives data to be transmitted. TXDATAHS[0] is transmitted first. TXDATAHS is synchronous to the rising edge of TXBYTECLKHS. **Active state:** High **Synchronous to:** TXBYTECLKHS
TXREQUESTDATAHS_N	I	Digital	**Function:** High-speed transmit request and data valid signal. When TXREQUESTHS is sampled high by TXBYTECLKHS, the lane module initiates a Start-of-Transmission (SOT) sequence. When TXREQUESTHS is sampled low while TXREADYHS is asserted, the lane module initiates an End-of-Transmission (EOT) sequence. **Active state:** High **Synchronous to:** TXBYTECLKHS
TXREADYHS_N	O	Digital	**Function:** High-speed transmit ready. This signal indicates that TXDATAHS is accepted by the lane module to be serially transmitted. TXREADYHS and the other high-speed data TX signals are synchronous with the rising edge of TXBYTECLKHS. **Active state:** High **Synchronous to:** TXBYTECLKHS

Table 3-7 describes the high-speed data RX signals.

Table 3-7 High-Speed Data RX

Signal	I/O	Type	Description
RXDATAHS_N[7:0][5]	O	Digital	**Function:** High-speed receive data. This is the output 8-bit data bus for the received data by the lane. RXDATAHS[0] is received first in the lane interconnect. Data is transferred on the rising edges of RXBYTECLKHS. **Active state:** High **Synchronous to:** RXBYTECLKHS

[4] *N* represents the lane ID: 0, 1, 2, and 3
[5] *N* represents the lane ID: 0, 1, 2, and 3

Signal	I/O	Type	Description
RXVALIDHS_N	O	Digital	**Function:** High-speed receive data valid. This signal indicates that the lane module is driving valid data to protocol layer on the RXDATAHS data bus. **Note:** There is no “RXdatareadyhs” signal, and the protocol layer is expected to capture data on RXDATAHS on every rising edge of RXBYTECLKHS where RXVALIDHS is asserted. There is no provision for the macro to slow down or throttle the received data. **Active state:** High **Synchronous to:** RXBYTECLKHS
RXACTIVEHS_N	O	Digital	**Function:** High-speed reception active. This signal indicates that the lane module is actively receiving a high-speed data transmission from lane interconnect. **Active state:** High **Synchronous to:** RXBYTECLKHS
RXSYNCHS_N	O	Digital	**Function:** Receiver synchronization observed. This signal indicates that the lane module has seen an appropriate synchronization event. In a typical high-speed transmission RXSYNCHS is high for one cycle of RXBYTECLKHS at the beginning of a high-speed transmission when RXACTIVEHS is first asserted. **Active state:** High **Synchronous to:** RXBYTECLKHS

Table 3-8 describes the PPI interface Escape mode TX signals.

Table 3-8 PPI Interface Escape Mode TX

Signal	I/O	Type	Description
TXREQUESTESC_N[6]	I	Digital	**Function:** Escape Mode Transmit Request. This signal together with TXLPDTESC_N, TXULPSESC_N and TXTRIGGERESC_N [3:0] is used to request the entry into any escape mode. Once in escape mode, the lane stays in escape mode until TXREQUESTESC is de-asserted. **Note:** It can only be asserted by the protocol layer while TXREQUESTDATAHS is at low level. **Active state:** High **Synchronous to:** TXCLKESC

[6] *N* represents the lane ID: 0, 1, 2, and 3

Signal	I/O	Type	Description
TXLPDTESC_N	I	Digital	**Function:** Escape Mode Transmit Low Power Data. This signal is asserted with TXREQUESTESC to cause the lane module to enter Low Power data transmission mode. The lane module remains in this mode until TXREQUESTESC is de-asserted. **Note:** TXULPSESC and all bits of TXTRIGGERESC must be at low level when TXLPDTESC is at high level. **Active state:** High **Synchronous to:** TXCLKESC
TXULPSESC_N	I	Digital	**Function:** Escape Mode Transmit Ultra Low Power. This signal is asserted with TXREQUESTESC to cause the lane module to enter the Ultra Low Power State. The lane module remains in this state until TXULPSEXIT is asserted and TXREQUESTESC is de-asserted. **Note:** TXLPDTESC and all bits of TXTRIGGERESC must be at low level when TXULPSESC is at high level. **Active state:** High **Synchronous to:** TXCLKESC
TXULPSEXIT_N	I	Digital	**Function:** Initiate transmission of the Ultra Low Power (ULP) exit sequence. When this signal is asserted while the lane is in Ultra Low Power State, the macro leaves ULP state and begins driving a Mark-1 symbol on the line interconnect. Afterwards, upon de-assertion of TXREQUESTESC, the macro drives the LP-11 Stop state. **Note:** this signal is ignored when the macro is not in ULP state. **Active state:** High **Synchronous to:** TXCLKESC
TXTRIGGERESC_N[3:0]	I	Digital	**Function:** Escape Mode Transmit Trigger 0-3. One of these signals is asserted with TXREQUESTESC to cause the lane module to send the associated trigger across the lane interconnect. TXTRIGGERESC is synchronous with the rising edge of TXCLKESC. **Note:** Only one of the TXTRIGGERESC is asserted at any given time, and only when TXLPDTESC and TXULPSESC are both at low level. **Active state:** High **Synchronous to:** TXCLKESC
TXDATAESC_N[7:0]	I	Digital	**Function:** Escape Mode Transmit Data bus. This is the eight-bit bus data input to be transmitted in low-power data transmission mode. The LSB is transmitted first. TXDATAESC is synchronous with the rising edge of TXCLKESC. **Active state:** High **Synchronous to:** TXCLKESC

Signal	I/O	Type	Description
TXVALIDESC_N	I	Digital	**Function:** Escape Mode Transmit Data Valid. This signal indicates that the protocol layer is driving valid data on TXDATAESC bus, to be transmitted. **Note:** The lane module accepts data when TXREQUESTESC, TXVALIDESC, and TXREADYESC are all active on the same rising edge of TXCLKESC. **Active state:** High **Synchronous to:** TXCLKESC
TXREADYESC_N	O	Digital	**Function:** Escape Mode Transmit Ready. This signal indicates that data is accepted by the lane module to be serially transmitted. TXREADYESC is synchronous with the rising edge of TXCLKESC **Active state:** High **Synchronous to:** TXCLKESC

Table 3-9 describes the PPI interface Escape mode RX signals.

Table 3-9 PPI Interface Escape Mode RX

Signal	I/O	Type	Description
RXCLKESC_N[7]	O	Digital	**Function:** Escape Mode Receive Clock. This clock is used to transfer received data to protocol layer. Unlike the other clocks in the macro, a specific RXCLKESC is provided for each data lane. **Note:** This clock is generated from the two low power signals in the lane interconnect. Because of the asynchronous nature of Escape Mode Data Transmission, this clock may not be periodic, and is available only during LP data reception. This signal is bypassed with SCANCLK when scan mode is enabled. **Active state:** High **Synchronous to:** N/A
RXLPDTESC_N	O	Digital	**Function:** Escape Low Power Data Receive Mode. This signal is asserted to indicate that the lane module is now in Low Power Data Receive Mode. While in this mode, received data is driven onto RXDATAESC output bus when RXVALIDESC is active. RXLPDTESC remains asserted until a STOP state is detected on the lane interconnect. **Active state:** High **Synchronous to:** RXCLKESC

[7] *N* represents the lane ID: 0, 1, 2, and 3

Signal	I/O	Type	Description
RXULPSESC_N	O	Digital	**Function:** Escape Ultra Low Power Receive Mode. This signal is asserted to indicate that the lane module has entered the Ultra Low Power State. The lane module remains in this mode with RXULPSESC asserted until a STOP state is detected on the lane interconnect. **Active state:** High **Synchronous to:** RXCLKESC
RXTRIGGERESC_N[3:0]	O	Digital	**Function:** Escape Mode Receive Trigger 0-3. This signal indicates that a trigger event has been received in the lane interconnect. The asserted RXTRIGGERESC signal remain active until a STOP state is detected on the lane interconnect. **Active state:** High **Synchronous to:** RXCLKESC
RXDATAESC_N[7:0]	O	Digital	**Function:** Escape Mode Receive Data bus. This is the 8-bit bus data output received by the lane interconnect. The signal RXDATAESC[0] was received first. Data is transferred on rising edges of RXCLKESC. **Active state:** High **Synchronous to:** RXCLKESC
RXVALIDESC_N	O	Digital	**Function:** Escape Mode Receive Data Valid. This signal indicates that the lane module is driving valid data to the protocol layer on the RXDATAESC bus. **Note:** There is no RXREADYESC signal and the protocol layer is expected to process received data on every rising edge of the RXCLKESC where RXVALIDESC is asserted. There is no provision in the macro to slow down or throttle the received data. **Active state:** High **Synchronous to:** RXCLKESC

Signal	I/O	Type	Description
ULPSACTIVENOT_N	O	Digital	**Function:** Indicates that the lane is in the Ultra Low Power (ULP) state. For a TX lane, this signal is asserted some time after TXULPSESC and TXREQUESTESC (or TXULPSCLK) are asserted. TXCLKESC must be supplied to the macro until ULPSACTIVENOT is asserted. In order to leave ULP state, the transmitter first drives TXULPSEXIT high, then waits for ULPSACTIVENOT to become high (inactive). At that point, the macro is active and has started transmitting a Mark-1 on the Lines. The protocol waits for a time Twakeup and then drives TXREQUESTESC or TXULPSCLK inactive to return the lane to Stop state. For a RX lane, this signal indicates that the lane is in ULP state. At the beginning of ULP state, ULPSACTIVENOT is asserted; at the end of the ULP state, this signal becomes inactive to indicate that the Mark-1 state has been observed. Later, after a period of time Twakeup, the RXULPSESC (or RXULPSCLKNOT) signal is de-asserted. **Active state:** Low **Synchronous to:** TXCLKESC for a Tx lane and RXCLKESC for a RX lane

Table 3-10 describes the PPI interface control signals.

Table 3-10 PPI Interface Control

Signal	I/O	Type	Description
TURNREQUEST_N[8]	I	Digital	**Function:** Turn around Request. This signal is used to indicate the protocol layer needs to turn the lane around, allowing for the other side to start transmitting data. TURNREQUEST is valid on rising edges of TXCLKESC. **Note**: TURNREQUEST is only meaningful for a lane that is currently transmitting data (DIRECTION = 0). If the data lane module is in receive mode (DIRECTION =1), this signal is ignored. **Active state:** High **Synchronous to:** TXCLKESC
DIRECTION_N	O	Digital	**Function:** Transmit/Receive Direction. This signal is used to indicate the current direction of the lane interconnect. When DIRECTION is at low level, the lane interconnect is in transmit mode. When DIRECTION is at high level, the lane interconnect is in receive mode. **Active state:** High **Synchronous to:** TXCLKESC
TURNDISABLE_N	I	Digital	**Function:** Disable Turn around. This signal is used to prevent the bi-directional lane from processing a turn-around request in the lane interconnect. **Note:** This is useful to prevent a potential “lock-up” situation when a unidirectional lane module is connected to a bi-directional lane module. **Active state:** High **Synchronous to:** Asynchronous
FORCERXMODE_N	I	Digital	**Function:** Force lane module into receive mode/Wait for stop state. This signal allows protocol layer to initialize a lane module or force a bi-directional lane module into receive mode. This signal is used to solve a contention situation. When this signal is at high level, the lane module immediately transitions into HS receive mode. **Active state:** High **Synchronous to:** TXCLKESC
FORCETXSTOPMODE_N	I	Digital	**Function:** Force lane module into transmit mode / Generate Stop state. This signal allows the protocol layer to force a bi-directional lane module into transmit mode and Stop state following an error indication (for example, Expired Timeout). When this signal is at high level, the lane module immediately transitions into transmit mode and the module state machine is forced into the Stop state. **Active state:** High **Synchronous to:** TXCLKESC

[8] *N* represents the lane ID: 0, 1, 2, and 3

Signal	I/O	Type	Description
STOPSTATEDATA_N	O	Digital	**Function:** Data Lane in Stop state. This signal indicates the lane module is in Stop state. Note: This is valid for both Master and Slave applications. This signal is asynchronous to any clock in the PPI interface. **Active state:** High **Synchronous to:** Asynchronous

Table 3-11 describes the PPI interface error signals.

Table 3-11 PPI Interface Error Signals

Signal	I/O	Type	Description
ERRSOTHS_N[9]	O	Digital	**Function:** Start of Transmission Error. If the high-speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this error signal is asserted for one cycle of RXBYTECLKHS. **Note:** This is considered to be a “soft error” in the leader sequence and confidence in the payload data is reduced. **Active state:** High **Synchronous to:** RXBYTECLKHS
ERRSOTSYNCHS_N	O	Digital	**Function:** Start of Transmission Synchronization Error. If the high-speed SoT leader sequence is corrupted in a way that proper synchronization cannot be expected, this error signal is asserted for one cycle of RXBYTECLKHS. **Active state:** High **Synchronous to:** RXBYTECLKHS
ERRESC_N	O	Digital	**Function:** Escape Entry Error. In an unrecognized escape entry command is received, this signal is asserted and remains high until the line returns to Stop state. **Active state:** High **Synchronous to:** RXCLKESC
ERRSYNCESC_N	O	Digital	**Function:** Low Power Data Transmission Synchronization Error. If the number of bits received during low power data transmission mode is not a multiple of eight when the transmission ends, this signal is asserted and remains high until the line returns to Stop state. **Active state:** High **Synchronous to:** RXCLKESC

[9] *N* represents the lane ID: 0, 1, 2, and 3

Signal	I/O	Type	Description
ERRCONTROL_N	O	Digital	**Function:** Control Error. This signal is asserted when an incorrect line state sequence is detected (for example, if a turnaround request or escape mode request is immediately followed by a Stop state instead of the required Bridge state, this signal is asserted and remains at high level until the line returns to Stop state). **Active state:** High **Synchronous to:** RXCLKESC
ERRCONTENTIONLP0_N	O	Digital	**Function:** LP0 Contention Error. This signal is asserted when a lane module functioning as TX while its base direction is RX detects a contention situation on a line while trying to drive the line low. **Active state:** High **Synchronous to:** TXCLKESC
ERRCONTENTIONLP1_N	O	Digital	**Function:** LP1 Contention Error. This signal is asserted when a lane module functioning as TX while its base direction is RX detects a contention situation on a line while trying to drive the line high. **Active state:** High **Synchronous to:** TXCLKESC

3.2.7 System Clock Signals

Table 3-12 describes the system clock signals.

Table 3-12 System Clock Signals

Signal	I/O	Type	Description
REFCLK	I	Digital	**Function:** Reference clock. This is the clock used for master-side serial clock generation in the Clock Multiplying Unit. It is the system clock input. For details, refer to the section 5.1 PLL Programming. **Active state:** High **Synchronous to:** N/A
CFG_CLK	I	Digital	**Function:** Configuration clock. This is the clock used for the initialization of the PHY by sequencing the different blocks power up, performing calibrations, and so on. In addition it is also used for exiting Ultra Low Power state. **Active state:** High **Synchronous to:** N/A

3.2.8 Clock Multiplier Signals

Table 3-13 describes the clock multiplier signals.

The PHY and the PLL blocks are prepared in such a way that when both are used no routing is needed between them as they abut perfectly. When the PHY is used without the PLL (slave application), ensure that all PHY inputs usually connected to the PLL are tied low while the outputs may be left open. For additional information, refer to chapter 9 Assembly Guidelines.

Table 3-13 Clock Multiplier Signals

Signal	I/O	Description	
LOCK	O	**Function:** PLL lock signal. When set signals PLL acquired lock with input REFCLK. **Active state:** High **Synchronous to:** Asynchronous	
FORCEPLL	I	**Function:** By default, the PLL clock multiplier will be switched off both during power down, ULP operation, and in a Slave-side configured macro. Should the PLL functionality be required from system perspective in any of these conditions, FORCEPLL allows the macro to be operated with the PLL active at all times, regardless of other configurations or states. **Active state:** High **Synchronous to:** Asynchronous	
PHY		**Interface between PHY and PLL**	**PLL**
PLL_LOCK	I	**Function:** Lock state signaling 0: PLL is not locked 1: PLL is locked **Active state:** High **Synchronous to:** Asynchronous	lock
TESTLOCK	I	**Function:** Testability output for observability **Active state:** High **Synchronous to:** Asynchronous	testlock
TXDDRCLKHSI_IN	I	**Function:** In phase high speed clock from the PLL **Active state:** N/A **Synchronous to:** Asynchronous	clkout1
TXDDRCLKHSQ_IN	I	**Function:** Inverted high speed clock from **Active state:** N/A **Synchronous to:** Asynchronous	clkout1n
CLKOUT2	O	**Function:** Clock signal with dedicated post divider **Active state:** N/A **Synchronous to:** Asynchronous	clkout2
PLLIBIAS	O	**Function:** Biasing current for PLL **Active state:** N/A **Synchronous to:** N/A	ipll

Signal	I/O	Description	
REFCLK_FT	O	**Function:** Reference clock signal **Active state:** N/A **Synchronous to:** Asynchronous	clkin
ONPLL	O	**Function:** PLL power down mode ■ 1: PLL active ■ 0: PLL stopped **Active state:** High **Synchronous to:** Asynchronous	onpll
RSTZPLL	O	**Function:** Digital reset for PLL **Active state:** Low **Synchronous to:** Asynchronous	rstz
N[7:0]	O	**Function:** Control of the input frequency division ratio N (N – 1 = 0 to 255) **Active state:** N/A **Synchronous to:** Asynchronous	n[7:0]
M[9:0]	O	**Function:** Control of the feedback multiplication ratio M (M – 1 = 11 to 999) **Active state:** N/A **Synchronous to:** Asynchronous	m[9:0]
P[3:0]	O	**Function:** Control of the output frequency division ratio P (P – 1 = 0 to 15) **Active state:** N/A **Synchronous to:** Asynchronous	p[3:0]
TH1[9:0]	O	**Function:** Lock detector phase error threshold **Active state:** N/A **Synchronous to:** Asynchronous	th1[9:0]
TH2[7:0]	O	**Function:** Lock filter length **Active state:** N/A **Synchronous to:** Asynchronous	th2[7:0]
TH3[7:0]	O	**Function:** Unlock filter length **Active state:** N/A **Synchronous to:** Asynchronous	th3[7:0]
BYPASS	O	**Function:** PLL bypass mode ■ 0: fclkout = PLL output ■ 1: fclkout = fclkin **Active state:** High **Synchronous to:** Asynchronous	bypass

Signal	I/O	Description	
TSTPLLDIG[2:0]	O	**Function:** Digital testability selector **Active state:** N/A **Synchronous to:** Asynchronous	tstplldig[2:0]
IBEXT	O	**Function:** External current source enable ■ 1:enabled ■ 0:disabled **Active state:** N/A **Synchronous to:** Asynchronous	ibext
ICPCTRL[3:0]	O	**Function:** Charge pump current control **Active state:** N/A **Synchronous to:** Asynchronous	icpctrl[3:0]
LPFCTRL[5:0]	O	**Function:** Loop filter zero control **Active state:** N/A **Synchronous to:** Asynchronous	lpfctrl[5:0]
CMX	O	**Function:** Not used **Active state:** N/A **Synchronous to:** Asynchronous	-
VCORANGE [3:0]	O	**Function:** VCO range selection **Active state:** N/A **Synchronous to:** Asynchronous	vcorange[3:0]

3.2.9 System Control Signals

Table 3-14 describes the system control signals.

Table 3-14 System Control Signals

Signal	I/O	Type	Description
SHUTDOWNZ	I	Digital	**Function:** Shutdown input. This line is used to place the complete macro in power down. All analog blocks are in power down mode and digital logic is reset. **Active state:** Low **Synchronous to:** Asynchronous
RSTZ	I	Digital	**Function:** Reset input. This line is used to place the digital section of macro in reset state. **Active state:** Low **Synchronous to:** Asynchronous
MASTERSLAVEZ	I	Digital	**Function:** Master/Slave configuration signal. This signal controls whether the PHY functionalities are configured for a Master-side D-PHY implementation (MASTERSLAVEZ=1) or for a Slave-side D-PHY implementation (MASTERSLAVEZ=0). **Note:** this signal configures all the PHY lanes (data and clock). **Active state:** High **Synchronous to:** Asynchronous
ENABLE_0	I	Digital	**Function:** Enable Lane 0 Module. All lane drivers, receivers, terminations, and contention detectors are turned off when ENABLE is low. Furthermore, all other lane PPI inputs are ignored and all lane PPI outputs are driven to the default value. ENABLE is level sensitive and asynchronous. **Active state:** High **Synchronous to:** Asynchronous
ENABLE_1	I	Digital	**Function:** Enable Lane 1 Module. All lane drivers, receivers, terminations, and contention detectors are turned off when ENABLE is low. Furthermore, all other lane PPI inputs are ignored and all lane PPI outputs are driven to the default value. ENABLE is level sensitive and asynchronous. **Active state:** High **Synchronous to:** Asynchronous
ENABLE_2	I	Digital	**Function:** Enable Lane 2 Module. All lane drivers, receivers, terminations, and contention detectors are turned off when ENABLE is low. Furthermore, all other lane PPI inputs are ignored and all lane PPI outputs are driven to the default value. ENABLE is level sensitive and asynchronous. **Active state:** High **Synchronous to:** Asynchronous

Signal	I/O	Type	Description
ENABLE_3	I	Digital	**Function:** Enable Lane 3 Module. All lane drivers, receivers, terminations, and contention detectors are turned off when ENABLE is low. Furthermore, all other lane PPI inputs are ignored and all lane PPI outputs are driven to the default value. ENABLE is level sensitive and asynchronous. **Active state:** High **Synchronous to:** Asynchronous
ENABLECLK	I	Digital	**Function:** Enable Clock Lane Module. All lane drivers, receivers, terminations, and contention detectors are turned off when ENABLE is low. Furthermore, all other lane PPI inputs are ignored and all lane PPI outputs are driven to the default value. ENABLE is level sensitive and asynchronous. **Active state:** High **Synchronous to:** Asynchronous

3.2.10 Scan Mode Interface Signals

Table 3-15 describes the Scan mode interface signals.

Table 3-15 Scan Mode Interface

Signal	I/O	Type	Description
SCANOUT[25:0]	O	Digital	**Function:** Scan out. Used as serial data stream output, when macro is in Scan mode. Macro contains 26 independent scan chains: four for each bidirectional lane, and six for the common digital logic. **Active state:** High **Synchronous to:** SCANCLK
SCANIN[25:0]	I	Digital	**Function:** Scan in. Used as serial data stream input, when macro is in Scan mode. Macro contains 26 independent scan chains: four for each bidirectional lane, and six for the common digital logic. **Active state:** High **Synchronous to:** SCANCLK
SCANEN	I	Digital	**Function:** Scan enable. Used to select scan operation mode. 1: Shift mode 0: Capture mode **Active state:** High **Synchronous to:** SCANCLK
SCANMODE	I	Digital	**Function:** Scan mode. Places the PHY in scan mode when asserted. **Active state:** High **Synchronous to:** SCANCLK
SCANCLK	I	Digital	**Function:** Scan clock. Clock source for scan mode. **Active state:** High **Synchronous to:** N/A
SCANRSTZ	I	Digital	**Function:** Scan reset. Reset signal for scan mode. **Active state:** Low **Synchronous to:** Asynchronous

3.2.11 Configuration and Test Interface Signals

Table 3-16 describes the configuration and test interface signals.

Table 3-16 Configuration and Test Interface

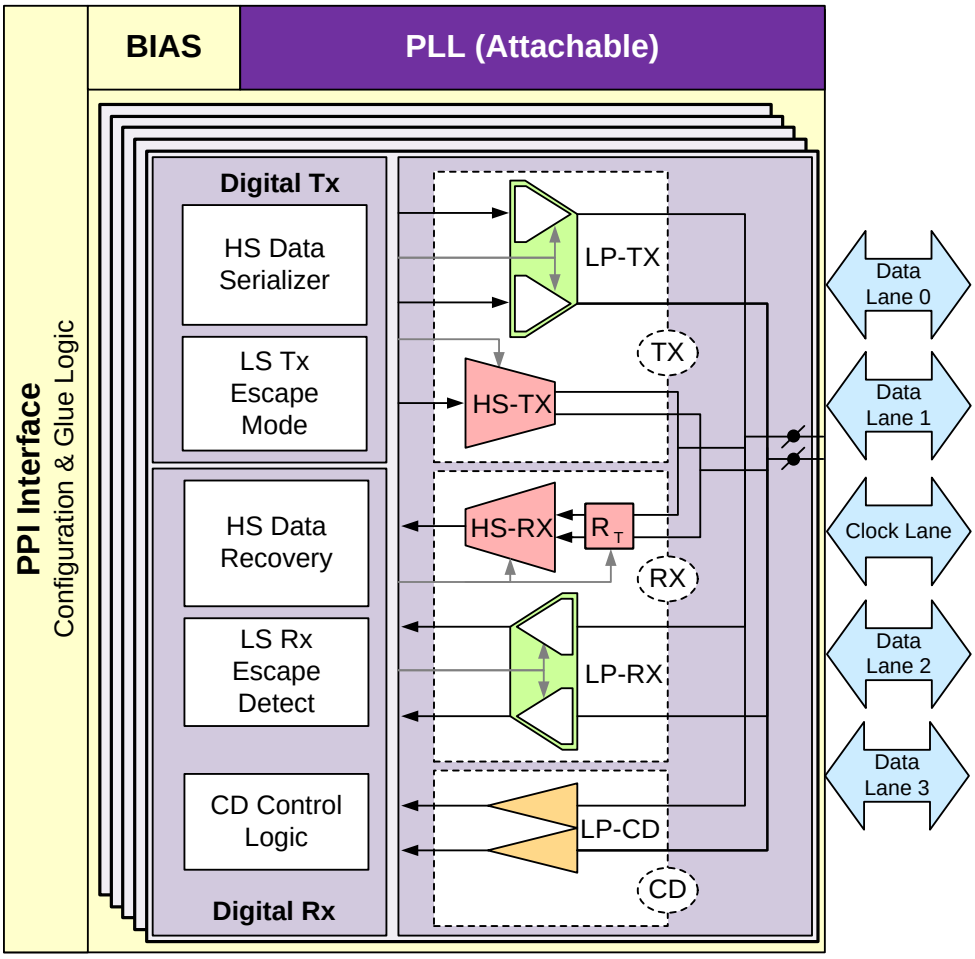
Signal	I/O	Type	Description
TESTDIN[7:0]	I	Digital	**Function:** Vendor-specific input eight-bit data bus for internal register programming and test functionalities access. **Active state:** High **Synchronous to:** TESTCLK
TESTDOUT[7:0]	O	Digital	**Function:** Vendor-specific output eight-bit data bus for read-back and internal probing functionalities. **Active state:** High **Synchronous to:** TESTCLK
TESTEN	I	Digital	**Function:** Vendor Specific interface operation type selector. When asserted, configures an address write operation on the falling edge of strobe signal (TESTCLK). When asserted low, configures a data write operation on the rising edge of strobe signal (TESTCLK). **Active state:** High **Synchronous to:** TESTCLK
TESTCLK	I	Digital	**Function:** Vendor Specific interface operation strobe signal. Used to clock TESTDIN bus contents into the macro. In conjunction with TESTEN signal, controls the operation selection. **Active state:** High **Synchronous to:** N/A
TESTCLR	I	Digital	**Function:** Vendor Specific interface clear signal. When active, performs vendor specific interface initialization. **Note:** This line needs an initial high pulse after power up for analog programmability default values preset. **Active state:** High **Synchronous to:** Asynchronous

4 Functional Description

4.1 Functional Overview

Figure 4-1 shows a functional block diagram of DWC D-PHY Bidir 4L.

Figure 4-1 DWC D-PHY Bidir 4L Functional Block Diagram



The DWC D-PHY Bidir 4L has the following main blocks:

- HS Driver/Receiver
  - Implements High Speed TX and RX functionalities
  - Replicated for each lane

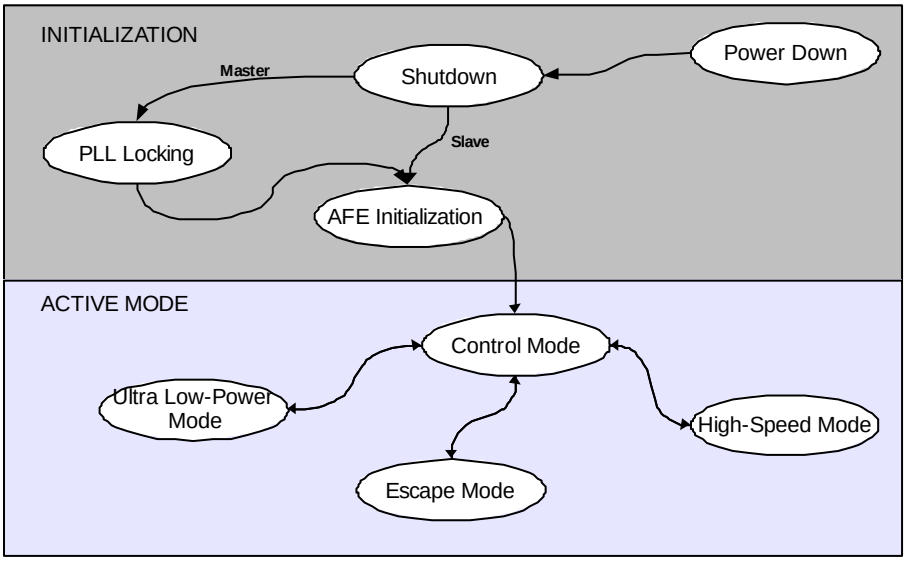
- LP Driver/Receiver
  - Implements Low Power TX and RX functionalities
  - Replicated for each lane
- Contention Detectors
  - Used for contention detector when there's a direction change in Low power mode
  - Replicated for each lane
- PLL
  - Generates High Speed clocks required in Master mode
  - Can be attached to the PHY for Master applications
- Digital Block : Includes all control logic as well as PPI interface

4.2 Operating Modes

This section describes the various operating modes of the DWC D-PHY Bidir 4L.

Figure 4-2 illustrates the various modes of the DWC D-PHY Bidir 4L during initialization and active operating mode.

Figure 4-2 PHY Initialization from Shutdown to Idle Modes



4.2.1 Initialization

4.2.1.1 Power Down Mode

This is the mode characterized by the inexistence of any supply voltage applied to the IP. In order to get to the powered modes proper voltages should be applied sequentially to the IP, this task is usually ensured by the SoC PMU or eventually by global powering up sequence.

The recommended powering up sequence determines that core voltage (VDD) must power up first and the I/O voltage (AVDD) powers up second. Failing to do so may result in excessive current consumption and die heating which can potentially lead to performance and reliability issues.

It is also assumed that RESETZ and SHUTDOWNZ are kept at logic level low prior or immediately after those events.

4.2.1.2 Shut Down Mode

This mode is characterized as the lowest power consumption mode, all analog blocks are disabled and digital logic reset. Current consumption is given by the analog stand-by current and the digital logic leakage current. It is entered asynchronously when RESETZ and SHUTDOWNZ are in low state. It should also be ensured that TESTCLR signal is asserted by default, as it acts as an active high reset to the control block responsible for the configuration values preset.

Depending on the PHY usage some additional steps may be performed. By default the PHY is configured to work only on the lower operation range of 80-110 Mbps. If higher bit rate operation is required the user should set the register hsRXfreqrange with the proper code. If D-PHY is expected to work always at the same bit rate this additional step can be performed while in Shutdown mode as the control interface is independent of the rest of the PHY. Conversely, if D-PHY is expected to change bit rate after initialization, hsRXfreqrange should be updated while in Idle mode. Refer to section 4.2.2 Active Modes, for further information on these options.

In addition, when working in Master mode, the PLL must be configured in order to select the proper input frequency and the desired output frequency, which determines the bit rate on the transmission path. Refer to the section 5.1 PLL Programming, for details.

Once RESETZ and SHUTDOWN are set to logic high level, the PHY leaves this state and starts an initialization procedure.

4.2.1.3 PLL Locking Mode and AFE Initialization

This IP comprises four data lanes but applications exist where just one of the data lanes would be used. In such cases, the user is granted access to individual enabling signals (ENABLE_N) that control which lanes should be used and evolve through all necessary initialization steps. It is assumed that such configurations are static or at least are stable prior to leaving the Shutdown Mode.

After the reset signals (RESETZ and SHUTDOWNZ) are released, the PHY begins an initialization sequence that allows its correct operation. Sequencing between which signal gets released first is not that critical but it is recommended that SHUTDOWNZ precedes RESETZ. It is also assumed that CFG_CLK is available and stable by that time.

TESTCLR signal can be kept at logic high level if no test/configuration operation is intended. If that is not the case then TESTCLR must be de-asserted to bring the control logic out of reset and allow for the necessary configuration steps through the control interface.

The D-PHY specification has a myriad of timing intervals which need to be respected to ensure proper operation. The fact that those timing intervals often have both a relative (UI) and absolute timing components, makes it difficult to meet the maximum and minimum values across the complete data rate range (80 Mbps-1 Gbps) by just using default settings. To cope with this, the macro implements a set of frequency ranges that needs to be configured prior to starting normal operation. Those ranges, when in Master operation, also define the operating bit rate assuming REFCLK is equal to 27 MHz. If the desired bit rate or REFCLK frequencies are different, the user must directly configure the PLL as described in chapter 5 PLL Programming. All these steps fall under the category of configurations that need to be performed through the control interface with TESTCLR de-asserted.

The different ranges allowed are shown in Table 4-1

Table 4-1 Frequency Ranges

RANGES (Mbps)	hsfreqrange[5:0]	Default bit rate (Mbps)
80-90 (default)	000000	90
90-100	010000	99
100-110	100000	108
110-125	000001	123
125-140	010001	135
140-150	100001	150
150-160	000010	159
160-180	010010	180
180-200	100010	198
200-210	000011	210
210-240	010011	240
240-250	100011	249
250-270	000100	270
270-300	010100	300
300-330	000100	330
330-360	010101	360
360-400	100101	399
400-450	000110	450
450-500	010110	486
500-550	000111	549
550-600	010111	600

RANGES (Mbps)	hsfreqrange[5:0]	Default bit rate (Mbps)
600-650	001000	648
650-700	011000	699
700-750	001001	750
750-800	011001	783
800-850	001010	849
850-900	011010	900
900-950	101010	972
950-1000	111010	999

hsfreqrange is accessible through control code 0x44 when testdin[7] = 0 and testdin[0] = 0. hsfreqrange[5:0] is programmed with the contents of testdin[6:1] at every rising edge of TESTCLK.

If the PHY is configured to work as a MASTER (MASTERSLAVEZ=1'b1), the PLL becomes active and the PHY goes through PLL Locking Mode, in which PHY waits for PLL to acquire lock, indicated by the LOCK output going high. A valid REFCLK (FREFCLK) should be provided.

Following the PLL lock, the rest of the AFE is initialized leading ultimately to the Low Power drivers enable. After completing these transitory state, lines goes to Stop State (LP = 11) and TX achieves active mode.

In the case of a SLAVE configuration (MASTERSLAVEZ = 1'b0), PLL is inactive so only the rest of AFE initialization takes place.

The initialization sequence determines that bandgap and biasing blocks are enabled first. After the related voltage and current references get settled, a second step is triggered where the internal calibrations are performed, and this can include internal resistors, receivers offset compensation, and so on.

Once this second step is complete, the control is passed to the lanes which handle the power management for LP/HS requests, enabling/disabling the corresponding drivers/receivers.

All initialization steps have been performed once STOPSTATE_X outputs get asserted.

A final note is in order regarding initialization period as per definition under D-PHY specification. Initialization period (TINIT) is a protocol dependent parameter with a minimum 100 µs defined by the specification. The current PHY implementation does not set any limit to the initialization period, meaning it immediately drives a Stop State (LP-11) after AFE initialization and PLL lock when in Master Mode, or alternatively starts decoding LP commands after AFE initialization in Slave mode. It is up to the controller or upper layers to ensure the proper initialization times through the correct handling of D-PHY control signals; this time must conform to D-PHY specification and so obey to the minimum specified 100 µs value.

Figure 4-3 shows a possible power up sequence for a Slave application when default settings used is 80-110 Mbps operation.

If the desired operation mode is different from the default one, additional configuration steps can be performed during T2+T3 time window.

Figure 4-3 Example Power-Up Sequence for Slave Operation

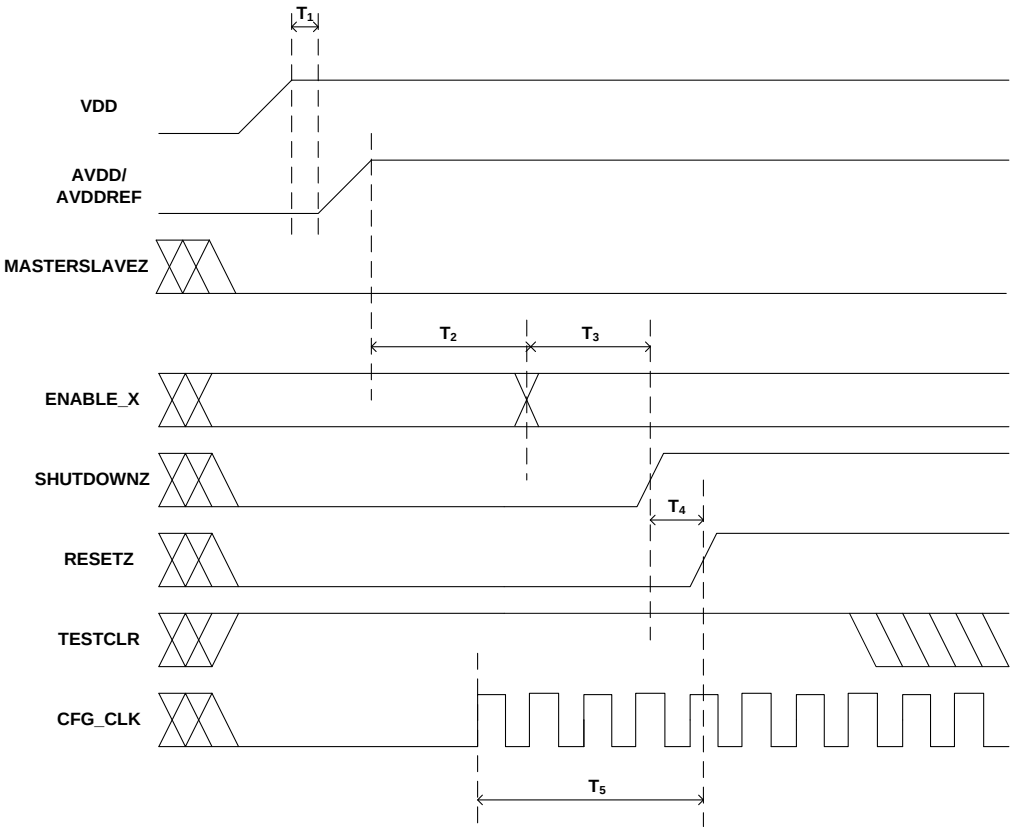


Table 4-2 Power-Up Sequence Timings

Parameters	Symbol	Minimum	Typical	Maximum	Units
Delay from stable VDD to AVDD/AVDDREF start	T1	0		1	us
Delay from stable AVDD/AVDDREF to ENABLE_X definition	T2	0			ns
Delay for assertion of SHUTDOWNZ after ENABLE_X definition	T3	5			ns
Delay from SHUTDOWNZ assertion to RESETZ assertion	T4	5			ns
Time for CFG_CLK settling before assertion of RESETZ	T5	1			CFG_ CLK

4.2.2 Active Modes

4.2.2.1 Idle Mode

Idle mode is the default operating mode. After initialization is complete (analog calibrations and PLL locking for MASTER configurations), the PHY remains in this default mode until some request is done (which is done either by the protocol layer for TX, or directly through the sequence of low-power signals in the lanes in case of RX). While in control mode, the transmitter side sets LP-11 state in the lines - this is called the stop state. The receiver side remains in control mode while receiving LP-11 in the lines. Any request must start from and end in stop state. Following a request, a lane can leave control mode for either high speed data transfer mode, escape mode or ultra low-power state.

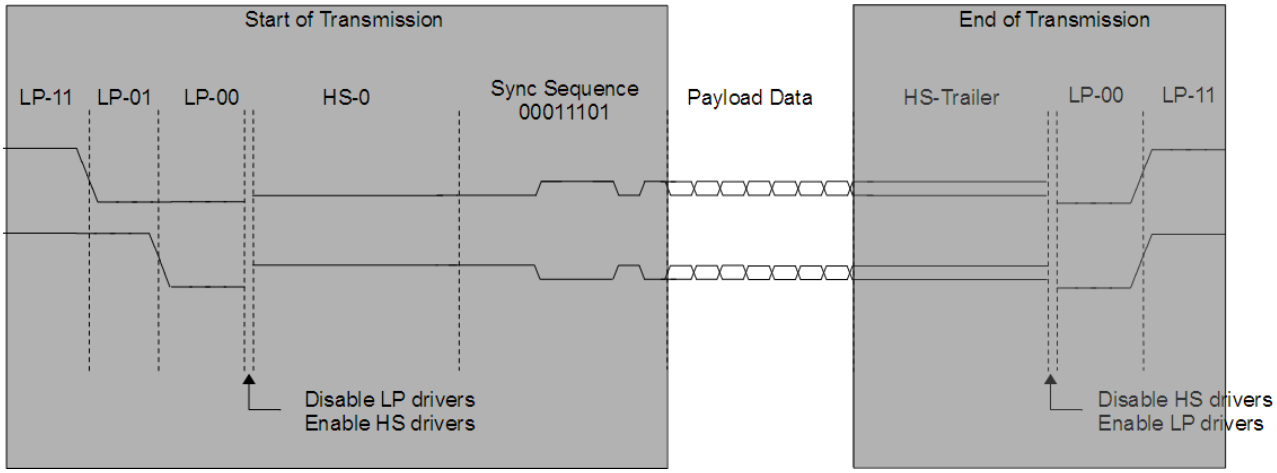
4.2.2.2 High-Speed Data Transfer Mode

Once the initialization sequence is done, the PHY remains in control mode, which is the default operating mode, until some request appears. High speed is one of the possible requests at this point. High Speed data transfer occurs in bursts. Only during these bursts the lane is in high speed mode - a high speed burst must start from and return to a stop state (control mode). A high-speed burst allows for the transmission of payload data by the data lanes. Inherent to such data transmission is the existence of a valid DDR clock in the clock lane.

High-speed data bursts are independent for each lane, which means that each data lane can start and end a high-speed transmission independently of the state of the remaining data lanes. Still, if the application requires multi-lane synchronicity, the lanes must be kept in STOP state during 26 byte clock cycles after STOPSTATE signals are observed in PPI, only then a new burst request in lanes are issued.

A burst contains the low-power initialization sequence, the high speed data payload and also the end of transmission sequence.

Figure 4-4 HS Data Transfer Sequence



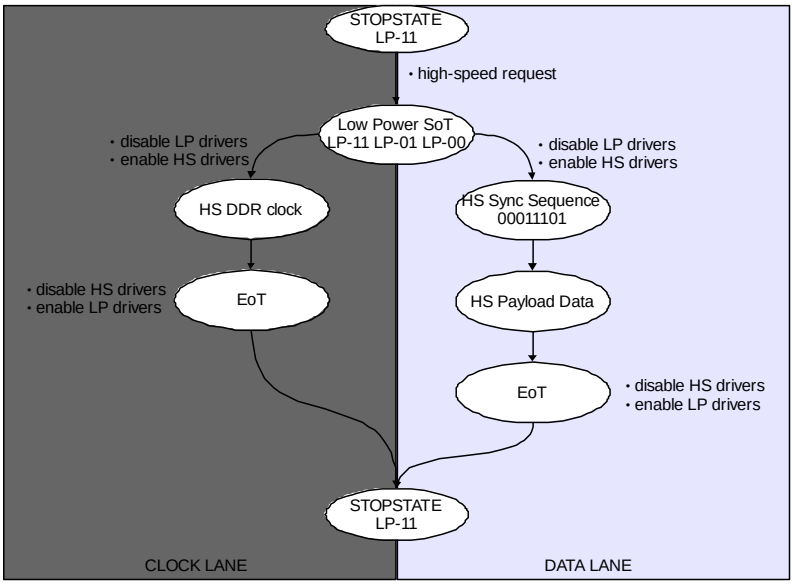
From the transmitter side, high-speed mode is entered when the correspondent TXREQUESTHS input is set high (assuming that the PHY is in stop state). This request is processed in a slightly different way for clock and data lanes. For a clock lane, the high speed request is followed by the transmission of a low-power sequence that represents this request for the receiver side (a lane high-speed request). Only after generating this sequence the low-power driver is disabled, and the high-speed driver enabled. Given the time necessary to settle, the transmission of the high-speed DDR clock starts. For a data lane, the high-speed request also starts a lane high-speed request, and in addition, extend the payload data with a leader

and a trailer sequence that allow for the receiver synchronization. The transmission of such sequence requires the existence of a valid high speed clock signal in the clock lane.

When the high-speed request input is disabled, each lane leaves the high-speed data transmission mode. It is important to note that a clock lane must be in high speed mode during the complete high-speed data transmission state of all the lanes - it must enter high speed mode before a high speed data transmission begins and it must not leave this state before all the lanes finish their respective high-speed data transmission bursts. The operation sequence when leaving high-speed mode is also slightly different for data and clock lanes. For a clock lane, the high-speed transmission will always end with a HS-0 state, followed by the disable of the high-speed driver, and enabling of low-power driver. As for a data lane, the transmission ends with the differential state opposite to the last bit transmitted, followed by the disable of the high-speed driver, and enabling of low-power driver.

The receiver side will enter high speed mode following the sequence of low-power states in the lines: LP-11, LP-01, and LP-00. This sequence is seen as a high speed mode request, and toggles the enabling oh the high speed receivers. The synchronization is then achieved through the identification of the leader sequence in the received differential high-speed data. Once synchronization is achieved, the PHY outputs the received bytes trough the protocol layer, until a stop state (LP-11) is detected in the lane.

Figure 4-5 HS Data Transfer State Diagram



The current implementation features no EoT processing for which it should be done at the controller level. This affects the behavior of RXActiveHs and RXValidHS signals as per Annex A (PPI Description).

4.2.2.3 Escape Mode

Escape mode is a special mode of operation that uses Data Lanes to communicate asynchronously using low power states at low speed; PHY supports this mode in both directions. A Data Lane shall enter Escape mode via an Escape Mode Entry procedure (LP-11, LP-10, LP-00, LP-01, LP-00), if an LP-11 is detected before reaching LP-00 state, the entry will be aborted and the receiver returns to Stop State. Once the sequence is correctly finished the transmitter sends an 8-bit command to indicate a requested action. Table 4-3 shows Escape mode supported actions. If the entry command is not valid it will be ignored, ERRESC error flag will go high and the receiver waits until transmitter returns to Stop state. The PHY applies

Spaced-One-Hot encoding (a Mark state is interleaved with a Space state) on commands and data. Each symbol consists of the following two parts:

- One-Hot phase
- Space state

To transmit one bit, a Mark-1 should be sent followed by Space state; in the case of a zero bit a Mark-0 should be sent followed by Space state.

Table 4-3 Possible Escape Mode Sequences for Data Lanes

Escape Mode Action	Entry Command Pattern (first bit to last bit to be transmitted)	Command Type
Low-Power Data Transmission	8'b11100001	mode
Ultra- Lower Power State	8'b00011110	mode
Reset Trigger	8'b01100010	trigger
Unknown -3	8'b01011101	trigger
Unknown -4	8'b00100001	trigger
Unknown -4	8'b10100000	trigger

4.2.2.3.1 Low Power Data Transmission (LPDT)

In this mode Data can be transmitted by the protocol at low speed in Low Power mode (High Speed drivers/receivers are off and Lower Power drivers/receivers are on). During LPDT the Lane can pause by maintaining a Space state on the Lines. The last state before exiting Escape mode is a Mark-1, not considered as a one-bit, because it is followed by the Stop state.

4.2.2.3.2 Remote Trigger

This mode allows the protocol to send a flag to the receiving side, on request of the transmitting side.

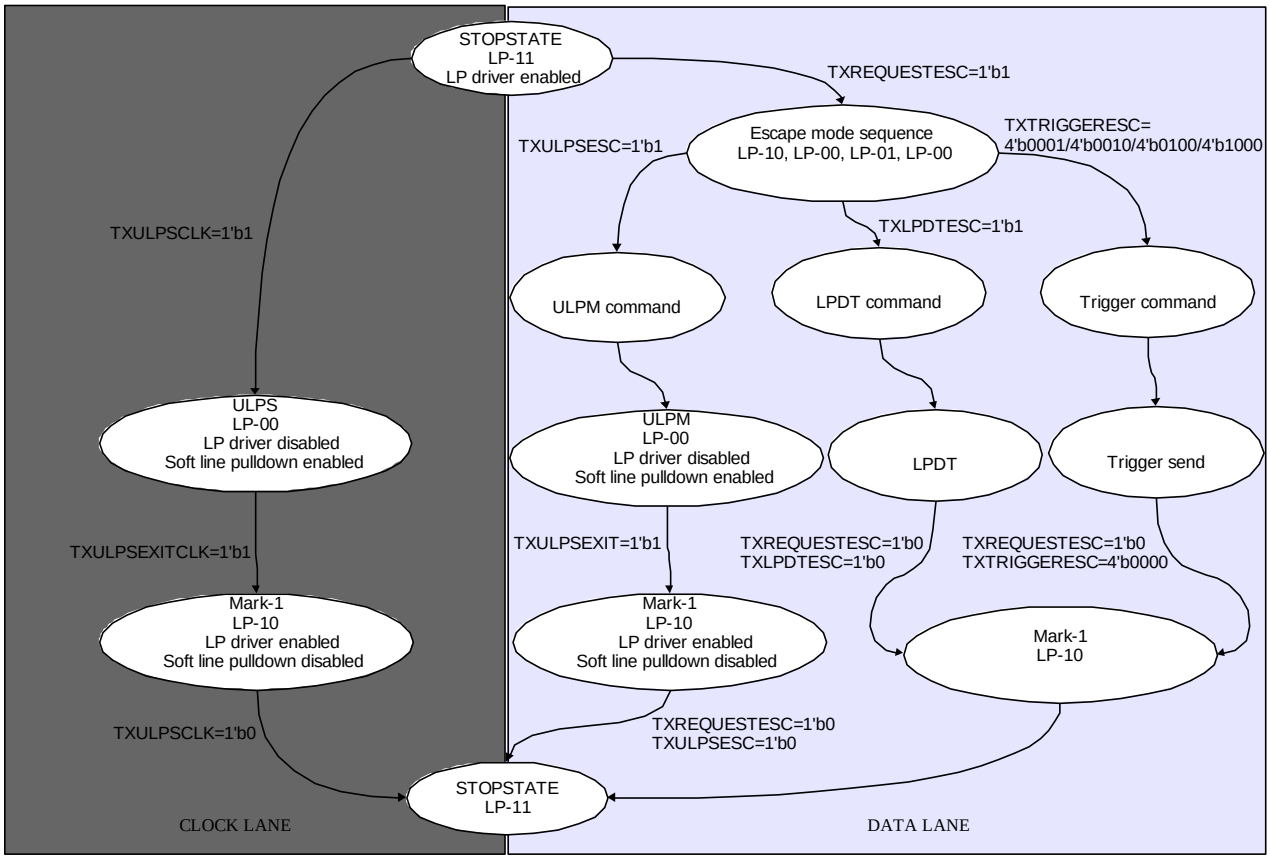
The Spaced-One-Hot encoding allows the asynchronous communication between the Lanes (does not depend on Clock Lane), because at receiver the clock RXCLKESC is generated using the XOR of the lines. It is however important to note that because of the asynchronous nature of the Escape mode transmission, the RXCLKESC can stop at anytime in either low or high state. The Escape mode transition sequencing from state to state is presented in Figure 4-6.

4.2.3 Ultra Low Power State (ULPS)

This mode is characterized for being the one with lowest power consumption, excluding shutdown mode.

For Data Lanes this mode is entered by sending an Ultra lower power state entry command, after the Escape mode entry command. During this mode the Lines are in the Space state (LP-00). Although Clock Lane does not support regular Escape mode, the Clock Lane supports ULPS. If the PHY is in MASTER mode and all lanes are set to ULPS, PLL is turned off. Figure 4-6 shows the ULPS state diagram for Clock and Data Lanes.

Figure 4-6 Escape Mode Sequences State Diagram



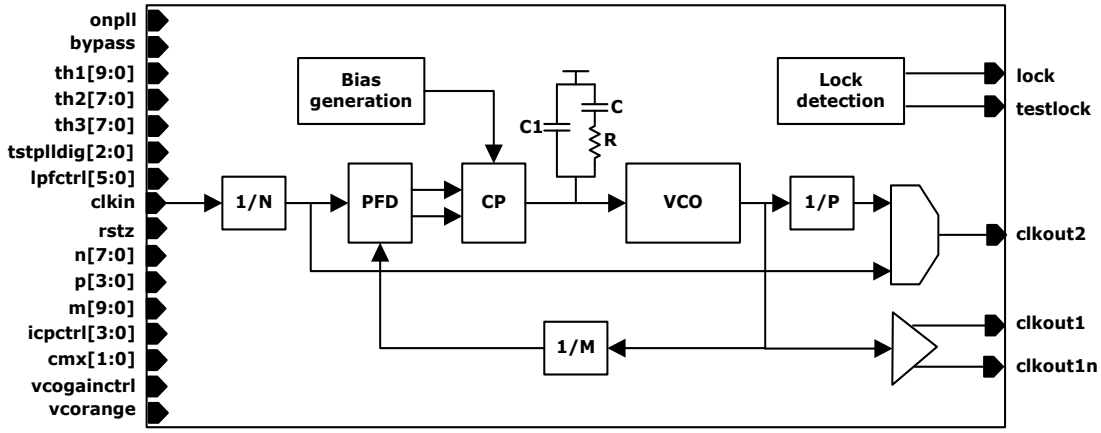
To exit ULPS, the transmitter side drives a Mark-1 for a minimum time of 1 ms (T_{wakeup}) followed by a Stop State. The T_{wakeup} time must be ensured by the protocol layer possibly using TXUlpsExit and TXRequestEsc/TXUlpsClk control signals.

5 PLL Programming

5.1 PLL Programming

As D-PHY is expected to be used in applications where the lane bit rate requirements can change dramatically from system to system, this IP features a very flexible PLL architecture, fully programmable through the PHY tester interface.

Figure 5-1 PLL



The VCO oscillating frequency is a function of the input reference frequency and of the multiplication/division ratios. It can be determined as follows:

$$f_{VCO} = \frac{M}{N} \quad f_{REFCLK}$$

Where:

- M is Feedback Multiplication Ratio
- N is Input Frequency Division Ratio.

However, some limits apply:

$$40\ MHz \geqslant \frac{f_{REFCLK}}{N} \geqslant 1\ MHz$$

For vcorange = 0001:

$$80\ MHz \leqslant f_{VCO} (= \frac{M}{N} \quad f_{REFCLK}) \leqslant 160\ MHz$$

For vcorange = 0011:

$$160\ MHz \leqslant f_{VCO}\left(= \frac{M}{N} \quad f_{REFCLK}\right) \leqslant 250\ MHz$$

For vcorange = 0111:

$$250\ MHz \leqslant f_{VCO}\left(= \frac{M}{N} \quad f_{REFCLK}\right) \leqslant 500\ MHz$$

For vcorange = 1111:

$$500\ MHz \leqslant f_{VCO}\left(= \frac{M}{N} \quad f_{REFCLK}\right) \leqslant 1000\ MHz$$

f_{VCO} is the output, full rate clock used for bit serialization. A 1000 Mbps bit rate on the data lanes assumes f_{VCO} to be equal to 1000 MHz.

Table 5-1 details the selection bit correspondence.

Table 5-1 Division Ratios for the Attachable PLL

m<9..0> = M - 1	M	n<7..0> = N - 1	N
10'hB	12	8'h0	1
10'hC	13	8'h1	2
…	…	…	…
10'h3E5	998	8'hFD	254
10'h3E6	999	8'hFE	255
10'h3E7	1000	8'hFF	256

Note that some combinations of N and M are not allowed, since they violate the limits of operation of the VCO and/or the minimum allowed comparison frequency.

These values should be programmed on the meaningful Control registers as presented in section 8.6 Control/Test Codes.

To ensure proper operation of PLL, the loop bandwidth should be configured depending on the selected frequency. The user is granted control over the CP current (icpctrl[3:0]), the LPF characteristics (lpfctrl[5..0]) and vcorange control signals. Table 5-2 presents the bits correspondence.

Table 5-2 PLL CP and LPF Control Bits

M	ipctrl[3..0]	lpfctrl[5..0]
12-32	0110	010000
33-64	0110	010000
65-128	1100	001000
129-256	0100	000100
257-512	0000	000001
513-768	0001	000001
769-1000	0010	000001

Default value for input clock is 27 MHz.

Table 5-3 shows the default internal setup of the PLL for the different hsfreqrange[5:0] frequency ranges selectable through control code 0x44 (refer to Table 4-1).

Table 5-3 PLL Settings for 27 MHz Reference Clock and Selectable Ranges

Ranges (MHz)	m[9:0]	n[7:0]	icpctrl[3:0]	lpfctrl[5:0]	vcorange[3:0]	fout (MHz)
80-90	29	8	0110	010000	0001	90
90-100	32	8	0110	010000	0001	99
100-110	35	8	0110	010000	0001	108
110-125	40	8	0110	010000	0001	123
125-140	14	2	0110	010000	0001	135
140-150	49	8	0110	010000	0001	150
150-160	52	8	0110	010000	0001	159
160-180	19	2	0110	010000	0011	180
180-200	21	2	0110	010000	0011	198
200-210	69	8	1100	001000	0011	210
210-240	79	8	1100	001000	0011	240
240-250	82	8	1100	001000	0011	249
250-270	29	2	0110	010000	0111	270
270-300	99	8	1100	001000	0111	300
300-330	109	8	1100	001000	0111	330
330-360	39	2	0110	010000	0111	360

Ranges (MHz)	m[9:0]	n[7:0]	icpctrl[3:0]	lpfctrl[5:0]	vcorange[3:0]	fout (MHz)
360-400	132	8	0100	000100	0111	399
400-450	49	2	0110	010000	0111	450
450-500	17	0	0110	010000	0111	486
500-550	60	2	0110	010000	1111	549
550-600	199	8	0100	000100	1111	600
600-650	23	0	0110	01000	1111	648
650-700	232	8	0100	000100	1111	699
700-750	249	8	0100	000100	1111	750
750-800	28	0	0110	000001	1111	783
800-850	282	8	0000	000001	1111	849
850-900	99	2	1100	001000	1111	900
900-950	35	0	0110	010000	1111	972
950-1000	36	0	0110	010000	1111	999

For reference clock frequencies other than 27MHz, it is required to configure PLL using control codes described in chapter 8 Test and Configuration Modes.

- PLL Input divider ratio (N): Register 0x17
- PLL loop divider ratio (M): Register 0x18
- Make previously configured N and M factors effective: Register 0x19 : bit 5:4 = 11

hsfreqrange[5:0] must always be correctly configured irrespective of the PLL reference clock (REFCLK) value.

6 External Software Calibration Requirements

6.1 Introduction

A software virtual calibration machine is required to be implemented outside PHY macro, in order to guarantee that the following PHY parameters meet the specification throughout silicon corners:

- LP transmitter output impedance - Z_{OLP}
- LP output signal slew rate - $\partial V/\partial t_{SR}$
- HS differential input impedance - Z_{ID}
- HS single ended output impedance - Z_{OS}

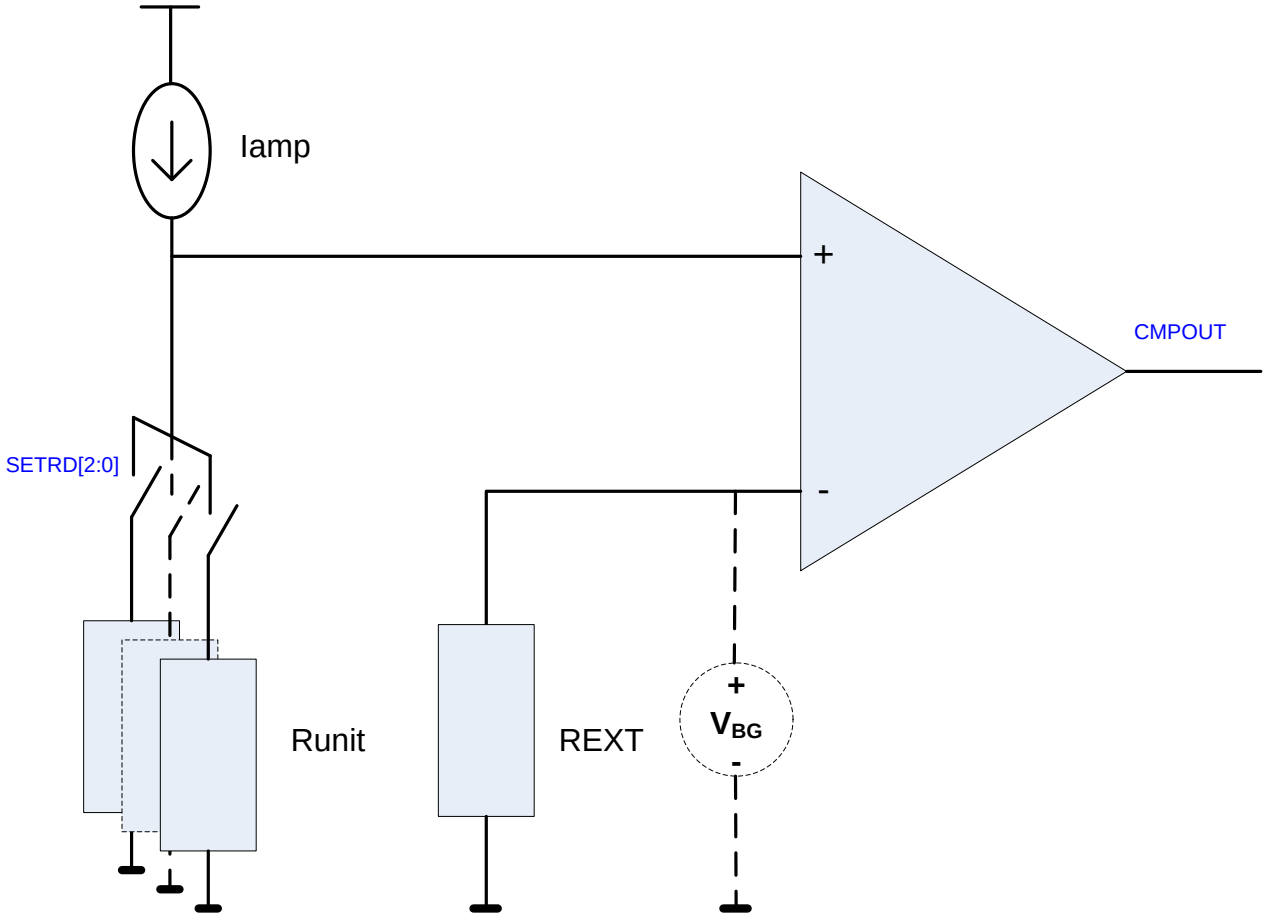
This calibration machine relies on an internal replica resistor that is matched to the external REXT high precision resistor. This is done by a set of switches, controlled by SETRD bus, that are progressively enabled and disabled resulting in an overall internal resistance value higher or lower than REXTscan mode. The results “higher than” and “lower than” are actually the output of internal OTA comparator as illustrated below.

After a complete sweep of all settings, the algorithm selects the optimum setting as the one that yields the internal resistor value closer to REXT. This setting is then used throughout the complete AFE for tuning of internal circuitry to compensate for process variation.

The default setting used in the absence of this calibration machine is sufficient to ensure proper functionality of all circuitry within the PHY but fails some D-PHY performance parameters across PVT corner variation.

Attention	Include the software calibration machine, if the product that uses D-PHY is expected to be fully compliant with MIPI specification.

Figure 6-1 Resistor Tuning Circuitry



6.2 Calibration Machine Algorithm

Software calibration machine should be implemented controlling input pins TESTDIN[4:0] and observing output pin TESTDOUT[7] of Control Code 0x21. The mapping is as follows:

- TESTDIN[4:2] – SETRD: internal termination resistor value control
- TESTDIN[1] – RTUNPON_EN: termination resistor power override enable
- TESTDIN[0] – RTUNPON: termination resistor power on
- TESTDOUT[7] – CMPOUT: Output of internal resistor comparator

Every access to TESTDIN shall be followed by the corresponding rising edge in TESTCLK while TESTEN=0. This will ensure that TESTDIN contents are latched internally and applied to the relevant circuitry. These additional steps are not included on the subsequent description for the sake of clarity.

6.2.1 Procedure

6.2.1.1 Initial Conditions

Enter CONTROL CODE 0x21 as defined in 8.6.24 Termination Resistor Control.

Set TESTDIN[1] and TESTDIN[0] to high and TESTDIN[7:5] to 000 during the entire calibration process.

6.2.1.2 Steps

1. Set TESTDIN[4:2] to 000 and wait for 100 ns (settling time).

   Check TESTDOUT[7] and store the value as AUX_TRIPU. It is expected that the value in typical case is 1;

Note Observe TESTDOUT[6:0] to ensure correct controllability.

2. Sweep TESTDIN[4:2] from 001 to 111.

   Wait for 100 ns between every control word change.

3. Check TESTDOUT[7].

   If TESTDOUT[7] is different from AUX_TRIPU, then set:

   - AUX_A = TESTDIN[4:2]
   - AUX_TRIPU = TESTDOUT[7]

   It is possible that the output of comparator TESTDOUT[7] will not change its value during this sweep depending on the process corner. In such a case:

   - If TESTDOUT[7] = 1 throughout the complete sweep, then set TESTDOUT[4:2] to 111
   - If TESTDOUT[7]= 0 throughout the complete sweep, then set TESTDOUT[4:2] to 000

4. Once TESTDIN[4:2] =111, check TESTDOUT[7] and store the value as AUX_TRIPD.

   It is not expected that TESTDOUT[7] toggles more than once during a sweep.

   If AUX_TRIPD ≠ AUX_TRIPU, then TESTDIN[4:2] = 011; Flag an error.

5. Sweep TESTDIN[4:2] from 110 down to 000.

   Wait for 100 ns between every control word change.

   Check TESTDOUT[7]. If TESTDOUT[7] is different from AUX_TRIPD, then set:

   - AUX_B = TESTDIN[4:2]
   - AUX_TRIPD = TESTDOUT[7]

6. Set TESTDIN[4:2] to ROUND_MAX[(AUX_A+AUX_B)/2].

Note Observe TESTDOUT[4:2] to ensure that the optimum value found has effectively been programmed.

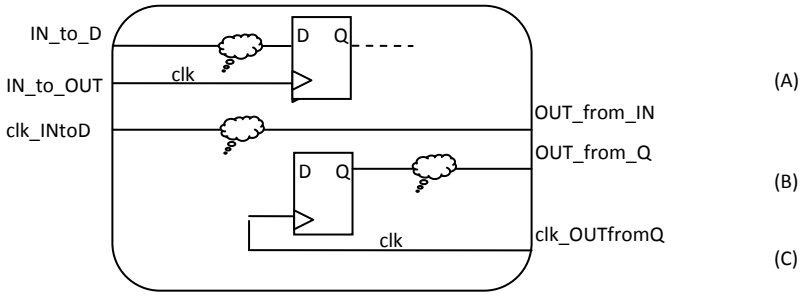
7 Timing Model Usage Guidelines

This section describes the usage of the extracted timing models for MIPI D-PHY Bidir 4L.

7.1 Extracted Timing Model Features

As shown in figure below, the process of extracting a timing model creates a timing arc for each path in the design from an input port to a register (A), from an input port to an output port (B), and from a register to an output port (C).

Figure 7-1 Timing Arcs for Extracted Timing Model



The delay data in the timing arcs is accurate for a range of operating environments, because the extracted delay data does not depend on the specific values of input transition time, output capacitive loads, input arrival times, output required times, and so on. However, the extracted model characteristics depend on the operating conditions and the wire load model in effect at the time of extraction.

The extracted timing model for the MIPI D-PHY Bidir 4L has the following characteristics:

- Timing arcs for three different modes of operation: MASTER, SLAVE, and SCAN
- PVT conditions covered

The asynchronous and synchronous signals present at the MIPI D-PHY Bidir 4L interface and their relation to the respective clock are define in Table 7-1.

7.2 Extracted Models Usage

This section describes usage of the extracted timing models.

7.2.1 Clock Structure

The existing clocks in the extracted timing models are as follows:

Common clock structure for MASTER and SLAVE Modes of Operation

- CFG_CLK: [external] – Input configuration interface clock signal. This is an external clock with a maximum frequency of 27 MHz. This is the clock used for the initialization of the PHY by

sequencing the different blocks power up, performing calibrations, and so on. In addition it is also used for exiting Ultra Low Power state.

- TXCLKESC: [external] – Escape mode transmit clock. This clock is directly used to generate escape sequences. The maximum frequency for this clock is 25 MHz.
- TESTCLK: [external] – Used to clock TESTDIN bus contents into the macro.
- SCANCLK: [external] – Input clock port for scan. The maximum frequency for this clock is 80 MHz.
- lprxdoutlp_clklane: [internal] – Internal LP Receive Clock for clock lane.
- lprxdoutlp_lane0: [internal] – Internal LP Receive Clock for lane 0.
- lprxdoutlp_lane1: [internal] – Internal LP Receive Clock for lane 1.
- lprxdoutlp_lane2: [internal] – Internal LP Receive Clock for lane 2.
- lprxdoutlp_lane3: [internal] – Internal LP Receive Clock for lane 3.
- RXCLKESC_0: [external] – Output Escape Mode Receive Clock for lane 0.
- RXCLKESC_1: [external] – Internal Escape Mode Receive Clock for lane 1.
- RXCLKESC_2: [external] – Internal Escape Mode Receive Clock for lane 2.
- RXCLKESC_3: [external] – Internal Escape Mode Receive Clock for lane 3.

7.2.1.1 MASTER Mode of Operation

- TXBYTECLKHS: [external] – High Speed Transmit byte clock. This is used to synchronize PPI signals in the High-Speed transmit clock domain. The maximum frequency for this clock is 125MHz.
- TXDDRCLKHSI_IN: [external] – In phase high speed clock from the PLL
- TXDDRCLKHSQ_IN: [external] – Inverted high speed clock from the PLL
- byteclkhs_int: [internal] – Possible source for the High Speed transmit byte clock

7.2.1.2 SLAVE Mode of Operation

- hsrxclkdig_clklane: [internal] – Internal DDR clock signal received by the clock lane
- hsrxclkdig_lane0: [internal] – Internal DDR clock signal received by the lane 0
- hsrxclkdig_lane1: [internal] – Internal DDR clock signal received by the lane 1
- hsrxclkdig_lane2: [internal] – Internal DDR clock signal received by the lane 2
- hsrxclkdig_lane3: [internal] – Internal DDR clock signal received by the lane 3
- RXBYTECLKHS: [external] –Output High Speed Receive byte clock. This is used to synchronize PPI signals in the high-speed receive clock domain. The frequency of RXBYTECLKHS is 1/8 of the serial bit rate.

Table 7-1 summarizes the clocks and signal direction in the extracted timing models.

Table 7-1 External and Internal Model Clock Signals

	External Clocks	Direction		Internal Clocks
MASTER	CFG_CLK	INPUT	→	
	TXCLKESC	INPUT	→	
	TXBYTECLKHS	INPUT	→	
	TXDDRCLKHSI_IN	INPUT	→	byteclkhs_int
	TXDDRCLKHSQ_IN	INPUT	→	
	TESTCLK	INPUT	→	
		OUTPUT	←	lprxdoutlp_clklane
	RXCLKESC_0	OUTPUT	←	lprxdoutlp_lane0
	RXCLKESC_1	OUTPUT	←	lprxdoutlp_lane1
	RXCLKESC_2	OUTPUT	←	lprxdoutlp_lane2
	RXCLKESC_3	OUTPUT	←	lprxdoutlp_lane3
SLAVE	CFG_CLK	INPUT	→	
	TXCLKESC	INPUT	→	
	TESTCLK	INPUT	→	
	RXBYTECLKHS	OUTPUT	←	hsrxclkdig_clklane
		OUTPUT	←	hsrxclkdig_lane0
		OUTPUT	←	hsrxclkdig_lane1
		OUTPUT	←	hsrxclkdig_lane2
		OUTPUT	←	hsrxclkdig_lane3
		OUTPUT	←	lprxdoutlp_clklane
	RXCLKESC_0	OUTPUT	←	lprxdoutlp_lane0
	RXCLKESC_1	OUTPUT	←	lprxdoutlp_lane1
	RXCLKESC_2	OUTPUT	←	lprxdoutlp_lane2
	RXCLKESC_3	OUTPUT	←	lprxdoutlp_lane3
	SCANCLK	INPUT	→	

When performing static timing analysis, take care to properly define and observe the existing clocks to ensure that the delay of the clock trees are taken into consideration, providing a correct and accurate timing.

7.2.2 Clock Creation

The clock creation for each mode is as follows:

7.2.2.1 MASTER Mode of Operation

```
create_clock [get_ports CFG_CLK] -name cfg_clk -period 15    -waveform {0 7.5}
create_clock [get_ports TXCLKESC] -name txclkesc -period 40  -waveform {0 20}
create_clock [get_ports TESTCLK] -name testclk -period 10.0 -waveform {0 5.0}
create_clock [get_ports TXBYTECLKHS] -name txbyteclkhs -period 8.0 -waveform [list 0.0
4.0]
```

```
create_clock [get_ports TXDDRCLKHSI_IN] -name txddrclkhsi -period 1.0 -waveform [list
0.0 0.5]
create_clock [get_ports TXDDRCLKHSQ_IN] -name txddrclkhsq -period 1.0 -waveform [list
0.5 1.0]
create_generated_clock -name byteclkhs_int   -source [get_pins <DUTNAME>/txddrclkhsi]
-divide_by 8 [get_pins <DUTNAME>/byteclkhs_int]
create_clock [get_pins <DUTNAME>/lprxdoutlp_clklane] -name lprxdoutlp_clklane -period
10 -waveform {0 5}
create_clock [get_pins <DUTNAME>/lprxdoutlp_lane0] -name lprxdoutlp_lane0   -period 10
-waveform {0 5}
create_clock [get_pins <DUTNAME>/lprxdoutlp_lane1] -name lprxdoutlp_lane1   -period 10
-waveform {0 5}
create_clock [get_pins <DUTNAME>/lprxdoutlp_lane2] -name lprxdoutlp_lane2   -period 10
-waveform {0 5}
create_clock [get_pins <DUTNAME>/lprxdoutlp_lane3] -name lprxdoutlp_lane3   -period 10
-waveform {0 5}
create_generated_clock -name rxclkesc_0 -source [get_pins <DUTNAME>/lprxdoutlp_lane0] -
divide_by 2       [get_pins <DUTNAME>/rxclkesc_out0]
create_generated_clock -name rxclkesc_1 -source [get_pins <DUTNAME>/lprxdoutlp_lane1] -
divide_by 2       [get_pins <DUTNAME>/rxclkesc_out1]
create_generated_clock -name rxclkesc_2 -source [get_pins <DUTNAME>/lprxdoutlp_lane2] -
divide_by 2      [get_pins <DUTNAME>/rxclkesc_out2]
create_generated_clock -name rxclkesc_3 -source [get_pins <DUTNAME>/lprxdoutlp_lane3] -
divide_by 2       [get_pins <DUTNAME>/rxclkesc_out3]
set_propagated_clock [all_clocks]
```

7.2.2.2 SLAVE Mode of Operation

```
create_clock [get_ports CFG_CLK] -name cfg_clk -period 15    -waveform {0 7.5}
create_clock [get_ports TXCLKESC] -name txclkesc -period 40   -waveform {0 20}
create_clock [get_ports TESTCLK] -name testclk -period 10.0  -waveform {0 5.0}
create_clock [get_pins <DUTNAME>/hsrxclkdig_clklane] -name hsrxclkdig_clklane -period
2.0 -waveform [list 0.0 1.0]
create_clock [get_pins <DUTNAME>/hsrxclkdig_lane0] -name hsrxclkdig_lane0   -period 2.0
-waveform [list 0.0 1.0]
create_clock [get_pins <DUTNAME>/hsrxclkdig_lane1] -name hsrxclkdig_lane1   -period 2.0
-waveform [list 0.0 1.0]
create_clock [get_pins <DUTNAME>/hsrxclkdig_lane2] -name hsrxclkdig_lane2   -period 2.0
-waveform [list 0.0 1.0]
create_clock [get_pins <DUTNAME>/hsrxclkdig_lane3] -name hsrxclkdig_lane3   -period 2.0
-waveform [list 0.0 1.0]
create_generated_clock -name rxbyteclkhs   -source [get_pins <DUTNAME>/rxbyteclkhs] -
divide_by 4 [get_pins <DUTNAME>/rxbyteclkhs]
create_clock [get_pins <DUTNAME>/lprxdoutlp_clklane] -name lprxdoutlp_clklane -period
10 -waveform {0 5}
create_clock [get_pins <DUTNAME>/lprxdoutlp_lane0] -name lprxdoutlp_lane0   -period 10
-waveform {0 5}
create_clock [get_pins <DUTNAME>/lprxdoutlp_lane1] -name lprxdoutlp_lane1   -period 10
-waveform {0 5}
create_clock [get_pins <DUTNAME>/lprxdoutlp_lane2] -name lprxdoutlp_lane2   -period 10
-waveform {0 5}
create_clock [get_pins <DUTNAME>/lprxdoutlp_lane3] -name lprxdoutlp_lane3   -period 10
-waveform {0 5}
create_generated_clock -name rxclkesc_0 -source [get_pins <DUTNAME>/lprxdoutlp_lane0] -
divide_by 2       [get_pins <DUTNAME>/rxclkesc_out0]
```

```
create_generated_clock -name rxclkesc_1 -source [get_pins <DUTNAME>/lprxdoutlp_lane1] -
divide_by 2       [get_pins <DUTNAME>/rxclkesc_out1]
create_generated_clock -name rxclkesc_2 -source [get_pins <DUTNAME>/lprxdoutlp_lane2] -
divide_by 2           [get_pins <DUTNAME>/rxclkesc_out2]
create_generated_clock -name rxclkesc_3 -source [get_pins <DUTNAME>/lprxdoutlp_lane3] -
divide_by 2             [get_pins <DUTNAME>/rxclkesc_out3]
set_propagated_clock [all_clocks]
```

7.2.2.3 SCAN Mode of Operation

```
create_clock [get_ports SCANCLK]      -name “scanclk”      period
set_propagated_clock [all_clocks]
```

7.2.2.4 Multi-Mode Operation

Extracted timing models can be created for a single operation mode, the mono-mode model (MASTER, SLAVE or SCAN), or for multiple operation modes, the multi-mode model.

When multi-mode models are read into Prime Time, all models are enabled by default. This means that Prime Time accounts for all timing relations present on the model. It is critical that you select the intended mode to disable all timing constrains for the inactive modes.

This task is performed by using the set_mode command, for example:

```
/*SCANMODE*/
set_mode SCAN <DUTNAME>
/*MASTER*/
set_mode MASTER <DUTNAME>
/*SLAVE*/
set_mode SLAVE <DUTNAME>
```

After setting the mode, a report_mode command can be performed to ensure that the intended mode is enabled while all other modes are disabled

8 Test and Configuration Modes

The DWC D-PHY Bidir 4L macro is designed with a subset of features that can be used during production testing. This chapter describes these features.

8.1 Scan Mode

8.1.1 Definition

The mipi_4_bidir_dphy IP Cell implements a standard scan chain that allows access to all the digital logic section of the Cell.

This design includes a set of 26 scan chains. To enter into this test mode, the signal SCANMODE should be set to high. This ensures that:

- All Registers are clocked by the same clock signal (SCANCLK).
- The internal asynchronous resets are bypassed using the external reset signal (SCANRSTZ).
- All output clocks are bypassed with SCANCLK.

The scan chain lengths are presented in Table 8-1 and the maximum frequency supported is 80 MHz.

Table 8-1 Scan Chain Lengths

Chain Number	Number of Cells	Chain Number	Number of Cells	Chain Number	Number of Cells
0	167	9	149	18	134
1	166	10	134	19	133
2	168	11	133	20	134
3	166	12	134	21	149
4	166	13	149	22	134
5	166	14	134	23	133
6	134	15	133	24	134
7	133	16	134	25	149
8	134	17	149		

In SCAN test, the analog blocks are not operating and stopped. Power consumption should be only leakage of analog blocks.

8.1.2 Pins Used

The scan test interface uses the commonly defined signals:

- SCANIN
- SCANOUT
- SCANEN
- SCANMODE
- SCANCLK
- SCANRSTZ

Refer to the section Scan Mode Interface Signals on page 40 for signal functionality definition.

8.2 Test and Control Modes

8.2.1 Definition

The D-PHY hard macro features a set of control codes that can be used for testability purposes whether under the scope of normal silicon characterization or eventually for production test in ATE environment. These control codes are primarily used for configuration of normal operation of the IP but for the test purposes they will be referred as test codes/modes from here on after.

For proper configuration and testability of the macro the user must ensure that this interface is accessible through the link controller and/or by any other means (multiplex/demultiplex layer to chip IOs, JTAG controller, and so on).

8.2.2 Interface Timing

Shown below are the timing diagrams for configuring a test mode in the macro. The standard procedure is two-folded, first the necessary **Test Code** is programmed and afterwards the related **Test Data** words are fed to the tester's inputs.

It is highly recommended to get the PHY in power down mode (shutdownz=0) and reset it (rstz=0) to avoid transient periods in PHY operation during re-configuration procedures. It is also recommended to apply a tester reset pulse (testclr=1) before any testmode configuration.

As stated above the test mode programming is done in two steps:

1. Set the desired Test Code
    a. Ensure that testclk is set to high.
    b. Place in testdin the 8 bit word corresponding to the testcode.
    c. Set testen to high.
    d. Set testclk to low.

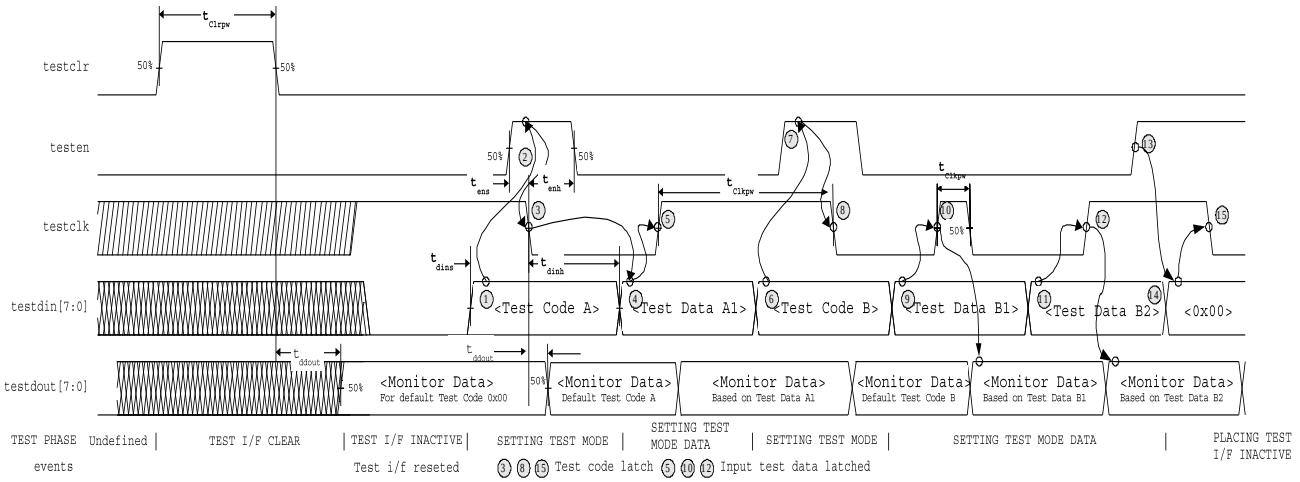
       With the falling edge on testclk, testdin[7:0] content is latched internally as the current testcode.
    e. Set testen to low.
2. Enter the necessary Test Data.
    a. Set testclk to low if not done already.
    b. Place in testdin the 8 bit word corresponding to the required test data.
    c. Set testclk to high.

       testdata is programmed internally.
    d. Repeat same steps if additional test data is intended for the same test mode.

The two steps above should be repeated thereafter to program subsequent test codes. Additionally, a tester reset procedure (testclr=1) is only needed prior to the first programming operation or if one wishes to reset the macro's configuration to its defaults values and override any change made meanwhile.

Figure 8-1 shows a generic timing diagram for tester operation. Note that after a test code is effectively programmed, testdout[7:0] asynchronously outputs relevant data for that specific test code, whether it is pure read-back data or other meaningful signals.

Figure 8-1 Testability Interface Timing Diagram

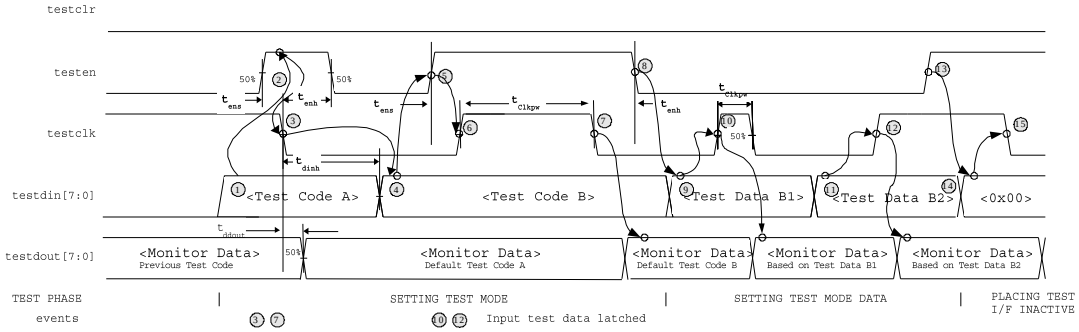


Some notes on Figure 8-1:

- After the required testclr pulse, testdout outputs monitor data for the default testcode (0x00). This is used to get information out right after the macro is powered up, such information may be relevant to determine the operation status of the macro and may not be related to any testcode in particular. For the current implementation, tesdout defaults to 0x00.
- Monitor data for a specific testcode may change in response to three different events
- testcode is programmed and default output data appears in testdout.
- testdin is affected with the testcode already configured.
- testdout outputs asynchronous internal signals whose timing is unpredictable.
- Some testcodes demand for two write data operations, where the first one will see the testclk going from high to low. It is crucial that the falling edge in the clock does not occur with testen asserted or else current testdata will be latched as an erroneous testcode.
- Placing test interface in inactive mode is best achieved by programming testcode 0x00 as shown in final sequence in Figure 8-1. Although not mandatory it is highly recommended to close any reconfiguration with this final sequence.

One additional scenario worth mentioning is that of a case in which two testcodes must be programmed one after the other without any intermediate testdata written to the tester. Caution is in order, as the test code is only latched internally with the falling edge of testclk, the inevitable rising edge must occur only while testen is asserted or else the second testcode will be wrongly interpreted as testdata for the active testcode. Refer to Figure 8-2 for details.

Figure 8-2 Two Consecutive Test Codes Handling



As a guideline, observe the timing constraints shown in Table 8-2:

Table 8-2 Timing Constraints for Test Interface

Timing Arc	Description	Minimum	Typical	Maximum	Unit
tclrpw	testclr min pulse width	10			ns
tclkpw	testclk min pulse width	10			ns
tddout	testdout output delay			10	ns
tens	testen setup time	5			ns
tenh	testen hold time	5			ns
tdins	testdin setup time	5			ns
tdinh	testdin hold time	5			ns

The available test/control codes are presented in the section Control/Test Codes on page 83.

8.3 Silicon Characterization Tests

DWC MIPI D-PHY's correct operation and its conformance with the specification from the MIPI Alliance can be checked through a suite of tests defined by the University of New Hampshire's Interoperability Laboratory (UNH-IOL) as part of the MIPI Alliance Test Program.

If passing, these tests provide a reasonable level of confidence that the tested device will properly operate in many MIPI environments, hopefully all if the interfacing device is also conformant.

Synopsys uses these tests as part of its internal testchip silicon characterization program for D-PHY IPs and ultimately recommends customers to follow similar approach in addition to interoperability tests with multiple hosts or/and devices.

In order to perform all tests described in CTS document, the final system should allow access to all the PPI interface signals of the D-PHY IP. Due to the extensive list of signals in the PPI Synopsys strongly encourages customers to multiplex similar signals from different lanes and provide SW access to the static/quasi-static ones to save chip IOs. Refer to Section 8.5 D-PHY Signal Access Level for further information.

8.4 Production Tests

This section presents an example for a possible set of tests that can be used for test production under ATE environment. The focus goes to both parametric and functional tests.

Test engineers should read this as a possible approach to test and not a strict guideline. Any other set of tests considered relevant can and should be used to complement these.

8.4.1 Power Down

This test intends to verify that when placed in shutdown mode the PHY is characterized by the lowest power consumption of all powered modes, mostly deriving from internal leakage currents. No activity on the PHY is expected.

Setup sequence:

1. Set SHUTDOWNZ and RSTZ signals to logic low, and TESTCLR to logic high.

   This places the macro in shutdown mode.
2. Ensure that no clock is driving the macro (CFG_CLK, TXCLKESC, TESTCLK)

Measure:

3. Check that all digital outputs present their default value, usually logic low state.
4. No clock should be output by the PHY when placed in this mode.
5. Measure the power consumption from both digital and analog supplies to check that they are at minimum values as defined in Table 11-2.

8.4.2 PLL Locking (D-PHY Master Only)

This test checks if the PHY PLL has properly locked, a crucial condition for proper D-PHY initialization in Master mode.

Setup sequence:

1. Apply REFCLK signal with proper frequency.
2. Apply CFG_CLK signal with proper frequency.
3. Set MASTERSLAVEZ = 1 for master mode selection.
4. Set ENABLE* logic high.
5. Set SHUTDOWNZ and RSTZ pin to logic high.

Note	By default, PLL is able to lock with an output frequency of 90 MHz for a 27 MHz input REFCLK signal. If the expected frequencies for the end application are different, and they are expected to be tested during production, additional programming steps are required in between steps 4 and 5. These additional steps rely on control codes to program several parameters on the PLL (hsfreqrange, CP/LPF settings, division ratios, and so on). Refer to the sections Operating Modes and PLL Programming.

Measure:

6. Wait for 1 ms after SHUTDOWNZ and RSTZ are released.
7. Check that the LOCK signal is asserted.

8.4.3 AFE initialization

This test aims at verifying the completeness of the AFE initialization process whether the PHY is configured as master or slave.

Setup sequence:

1. Depending on whether D-PHY is to be tested in Master or Slave mode, consider:
   - If D-PHY is to be tested in Master mode, the current test setup can proceed from step 5 of section 8.4.2 PLL Locking (D-PHY Master Only).
   - If D-PHY is to be tested in Slave mode, perform step 2 to step 5 as in section 8.4.2 PLL Locking (D-PHY Master Only), but now ensuring that MASTERSLAVEZ=0.
2. **[Slave]** Drive LP-11 through clock lane and all enabled data lanes.

Note	All request inputs must be kept at zero to avoid any unexpected behavior from the PHY until STOPSTATEx outputs are set.

Measure:

3. Wait for 500 us.

   The initialization sequence determines that bandgap and biasing blocks are enabled first. After the related voltage and current references get settled, a second step is triggered where the internal

calibrations are performed, this can include internal resistors, receivers offset compensation, and so on. The 500 us time is sufficient to accommodate complete initialization process with different CFG_CLK frequencies.

4. Check that STOPSTATEx PPI signal for data lanes and clock lane is asserted.

   This is valid for Master mode with LP-11 being driven in lines, and in Slave mode by the promptness to decode LP commands.

5. **[Master]** Evaluate DC level in all enabled data and clock lines and ensure it conforms with specification values for V_{OH} of LP-TX.

8.4.4 Low Power Loopback

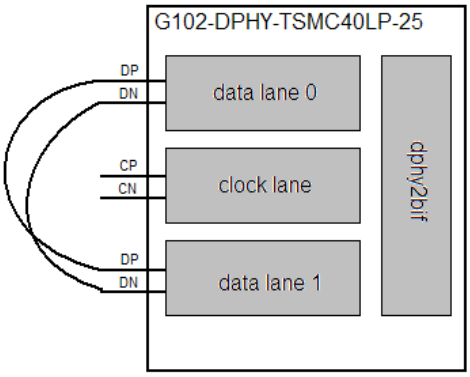
This test enables a functional verification of the LP driver and receiver present in the data lanes through the use of an external loopback connection between any two data lanes.

Note	For the sake of clarity, the test description refers only data lanes 0 and 1 but can and should be considered for the remaining data lanes also.

Setup sequence:

1. Perform external loopback connection:
   a. Shunt connection between DATAP0 and DATAP1.
   b. Shunt connection between DATAN0 and DATAN1.

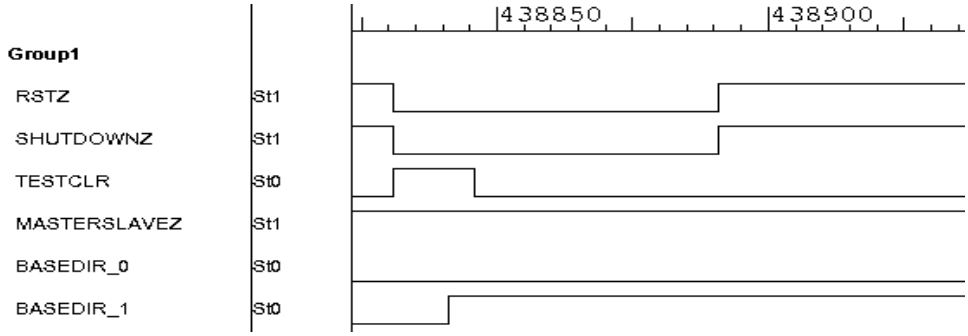
Figure 8-3 External Loopback Connection



2. Initialize the PHY as a MASTER D-PHY with lane 0 in TX mode and lane 1 in RX mode.
   a. Apply REFCLK signal with proper frequency.
   b. Apply CFG_CLK signal with proper frequency.
   c. Apply TXCLKESC signal with proper frequency. The frequency may range from 2 MHz to 20 MHz corresponding to 1 Mbps or 10 Mbps LP operations respectively.
   d. Set MASTERSLAVEZ to high, BASEDIR_0 to low, and BASEDIR_1 to high.
   e. Set ENABLE* to high.
   f. Set RSTZ, SHUTDOWNZ to low and TESTCLR to high (possibly from the start).

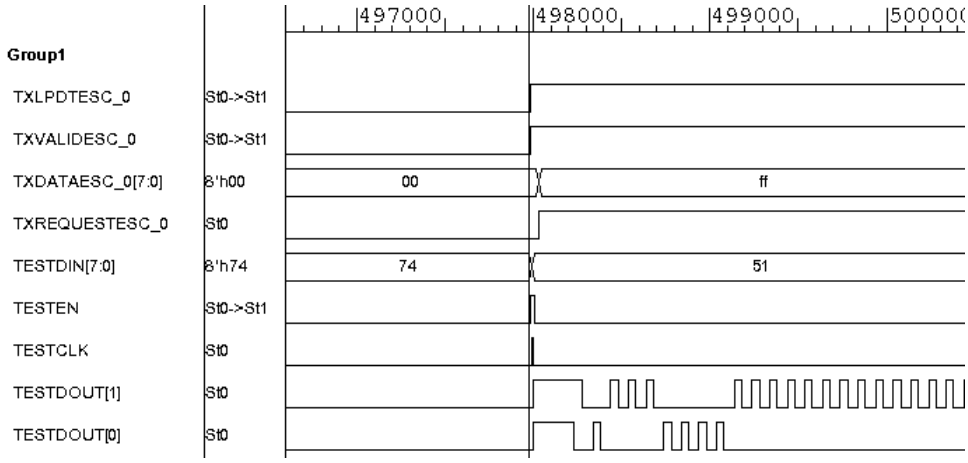
g. Wait for 15 ns.
h. Set TESTCLR to low.
i. Wait for 15 ns.
j. Set RSTZ and SHUTDOWNZ to high.

Figure 8-4 Initialization



3. Wait for 1.5 ms for initialization period
4. **[Measure 1]**
5. Set TXLPDTESC_0 and TXVALIDESC_0 to high.
6. Set TXDATAESC_0[7:0] to 8'b11111111
7. Set TXREQUESTESC_0 to high.
8. Program testcode 0x51 through control interface
9. Wait for 20 us
10. **[Measure 2]**
11. **[Measure 3]**

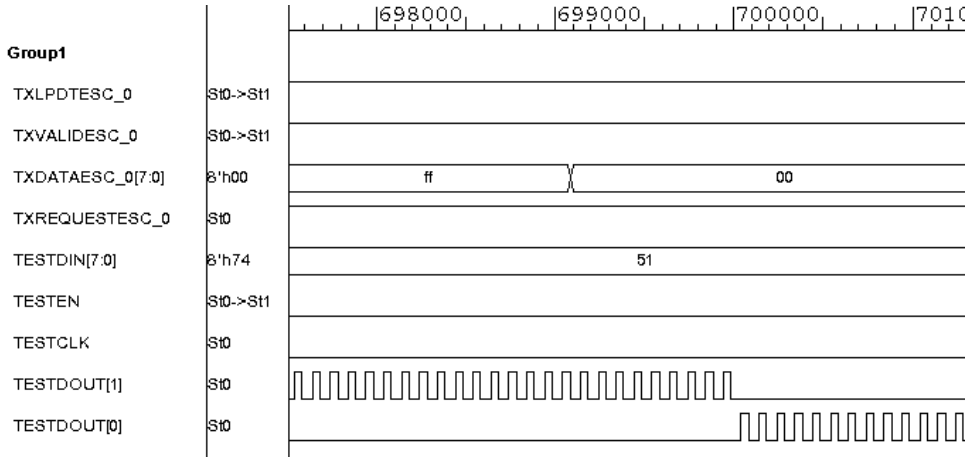
Figure 8-5 Graphical Representation of Steps 5 to 11



12. Set TXDATAESC_0[7:0] to 8'b00000000
13. Wait for 20 us
14. **[Measure 4]**

15. **[Measure 5]**

Figure 8-6 Graphical Representation of Steps 12 to 15



16. Finish the test by setting TXREQUESTESC_0 to low.

Measures:

- **[Measure 1]**

  Check that STOPSTATEDATA1 is asserted, flagging the proper loopback of the LP-11 from LP-TX to LP-RX.

- **[Measure 2]**

  Observe a clock pattern in TESTDOUT[1] whose frequency should be equal to 1/2xFTXCLKESC.

- **[Measure 3]**

  Check that TESTDOUT[0] is flat zero.

- **[Measure 4]**

  Observe similar clock pattern in TESTDOUT[0].

- **[Measure 5]**

  Observe similar clock pattern in TESTDOUT[0].

- Parametric tests can also be performed during the clock toggle in the loopback connection:
  - Capture N repetitions of voltage samples for the loopbacked bits in DATAP*/DATAN* lines.

    If a timing reference is difficult to achieve in order to properly determine the bits boundaries, a sweeping sampling mechanism may be used with different time steps.
  - Determine absolute minimum and maximum values for V_{OH} and $V_{OL.}$
  - Compare the previous values with values from the table below. If value limits are crossed, declare a FAIL otherwise declare a PASS.

Table 8-3 Pass/ Fail Volume

Single Ended Voltage	PASS/FAIL Value (mV)
VOH (max)	1300
VOH (min)	1100
VOL (max)	50
VOL (min)	-50

For maximum coverage, similar procedure may be used to test LP communication on the reverse direction, that is, data lane 1 as TX and data lane 0 as RX.

8.4.5 High Speed Loopback

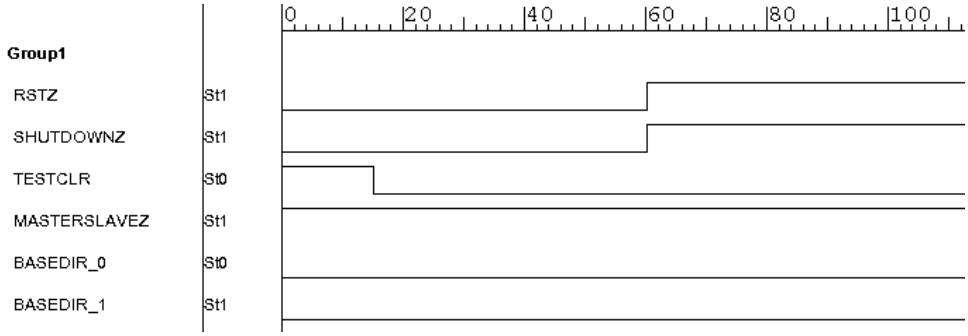
This test enables a functional verification of the HS driver and receiver present in the data lanes through the use of an external loopback connection between the two data lanes.

For the sake of clarity the test description refers only data lanes 0 and 1 but can and should be considered for the remaining data lanes.

Setup sequence:

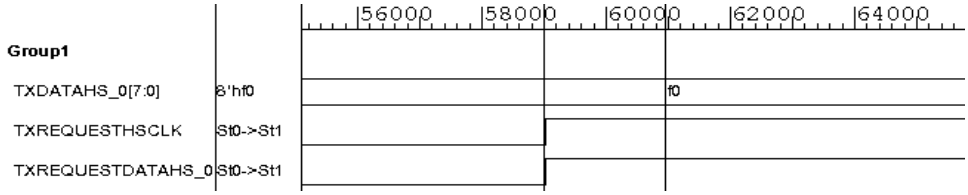
1. Perform external loopback connection as given in the section Low Power Loopback and as shown in Figure 8-3.
2. Initialize the PHY as a MASTER D-PHY with both lanes in TX mode.
   a. Apply REFCLK signal with proper frequency.
   b. Apply CFG_CLK signal with proper frequency.
   c. Apply TXCLKESC signal with proper frequency. The frequency may range from 2 MHz to 20 MHz corresponding to 1 Mbps or 10 Mbps LP operation respectively.
   d. Set MASTERSLAVEZ to high, and BASEDIR_0 and BASEDIR_1 to low.
   e. Set ENABLE* to high.
   f. Set RSTZ and SHUTDOWNZ to low, and TESTCLR to high (possibly from the start).
   g. Wait for 15 ns.
   h. Set TESTCLR to low.
   i. Wait 35 ns.
   j. Set RSTZ, SHUTDOWNZ to high.

Figure 8-7 Initialization



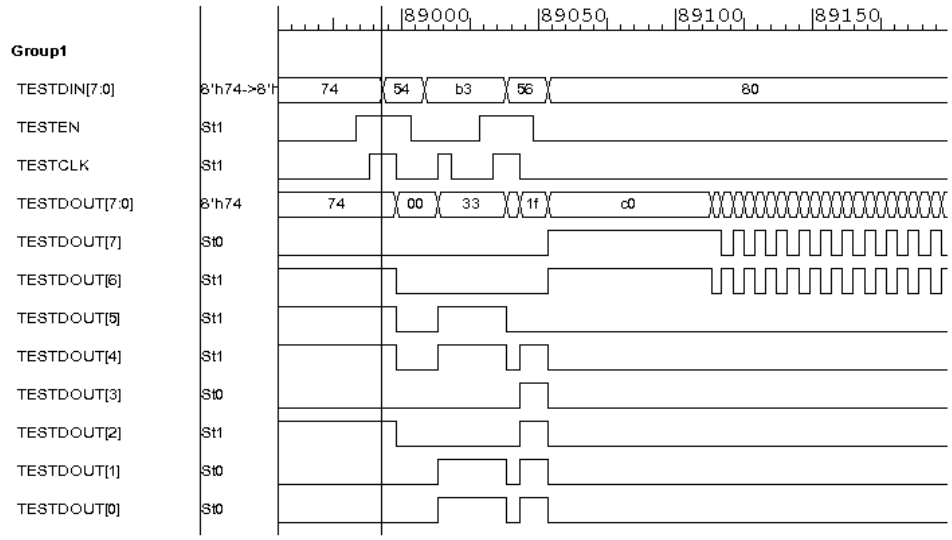
3. Wait for 1.5 ms for the initialization period.
4. **[Measure 1]**
5. Set TXDATAHS_0 to 8’b11110000.
6. Request HS clock transmission.
6. Set TXREQUESTHSCLK to high.
7. Request HS data transmission on lane 0.
7. Set TXREQUESTDATAHS_0 to high.

Figure 8-8 Graphical Representation of Steps 5 to 9



8. Wait for 3 us.
9. Write data 8’b00101000 in testcode 8’h50.
   This disables the HS transmitter LANE 1.
10. Write data 8’b10110011 in testcode 8’h54.
    This enables the HS receiver and termination in LANE 1.
11. Set testcode to 8’h56 and testdin to 8’b10000000.
12. Wait for 500 ns.
13. **[Measure 2]**

Figure 8-9



14. Finish the test by setting TXREQUESTDATAHS_0 and TXREQUESTHSCLK low.

Measures:

- **[Measure 1]**

  Check that STOPSTATEDATA1 is asserted and flagging the proper loopback of the LP-11 from LP-TX to LP-RX.

- **[Measure 2]**

  Observe the HS asynchronous data in TESTDOUT[7:6]. The signals are complementary and should match a clock pattern with a frequency equal to 1/8 of the selected bit rate (for example, for 1 Gbps operation the pattern output in TESTDOUT[7:6] would have 125 MHz frequency).

125 MHz is close to the maximum effective bandwidth of many of the conventional digital IO pads, test engineer must take this into account and reduce maximum bit rate if confronted with problems due to bandwidth limitations of the chip digital IO pads.

- Parametric tests can also be performed for the clock toggling pattern in the loopback connection:
  - Capture N repetitions of voltage samples for the loopbacked bits in DATAP*/DATAN* lines.
  - If a timing reference is difficult to achieve in order to properly determine the bits boundaries, a sweeping sampling mechanism may be used with different time steps.
  - Determine absolute maximum values for voltage V_{OHHS}.
  - Compare the previous value with 360 mV. If the value is higher, then declare a FAIL otherwise it is a PASS**.**
  - Using tester's PMU to get DC value in the loopbacked lines would also yield an interesting and insightful test as DC level of square wave relates directly with the common mode voltage of the HS-TX.
  - Compare DC level of periodic square wave with V_{CMTX} values from spec. If falling within the specified interval, declare a PASS otherwise it is a FAIL**.**

Table 8-4 Pass/Fail Value

Voltage Level	PASS/FAIL Value (mV)
VOHHS	< 360
VCMTX (max)	250
VCMTX (min)	150

For maximum coverage, similar procedure may be used to test HS communication on the reverse direction, that is, data lane 1 as TX and data lane 0 as RX.

8.4.6 ATPG scan test

Use ATPG tools to generate manufacturing test patterns to test the digital logic inside the IP through the scan interface of the different modules.

8.5 D-PHY Signal Access Level

8.5.1 Silicon Characterization

Following are the signal access levels for silicon characterization:

- Internally controllable (Available through software write operation and JTAG)
  - TESTCLK
  - TESTEN
  - TESTCLR
  - TESTDIN[7:0]
  - FORCEPLL
  - SHUTDOWNZ
  - RSTZ
  - MASTERSLAVEZ
  - ENABLE_0/ ENABLE_1/ ENABLE_2/ ENABLE_3/ ENABLECLK
  - Low frequency PPI output signals (static control, escape sequences, …)
- Internally observable (available through software read operation and JTAG)

  Low frequency PPI output signals (escape sequences, error flags, …)
- Externally controllable (available as input chip IOs)

  Medium/High frequency PPI input signals mostly related with data interface for HS and LP (RX/TX data, clocks, fast handshake signals, …)
- Externally observable (available as output chip IOs)
  - LOCK
  - TESTDOUT[7:0]
  - Medium/High frequency PPI output signals mostly related with data interface for HS and LP (RX/TX data, clocks, fast handshake signals, …)

Consider multiplexing similar signals for the different lanes to reduce signal overhead and simplify access.

8.5.2 Production Testing

Following are the signal access levels for production testing:

- Internally controllable (Register bank write operation, JTAG or similar internal control)
  - TESTCLK
  - TESTEN
  - TESTCLR
  - TESTDIN[7:0]
  - FORCEPLL
  - SHUTDOWNZ

- RSTZ
- MASTERSLAVEZ
- ENABLE_0/ ENABLE_1/ ENABLE_2/ ENABLE_3/ ENABLECLK
- BASEDIR_0/BASEDIR_1/ BASEDIR_2/BASEDIR_3
- TXLPDTESC_0/ TXLPDTESC_1/ TXLPDTESC_2/ TXLPDTESC_3
- TXVALIDESC_0/ TXVALIDESC_1/ TXVALIDESC_2/ TXVALIDESC_3
- TXDATAESC_0[7:0]/ TXDATAESC_1[7:0]/ TXDATAESC_2[7:0]/ TXDATAESC_3[7:0]
- TXREQUESTESC_0/ TXREQUESTESC_1/ TXREQUESTESC_2/ TXREQUESTESC_3
- TXDATAHS_0[7:0]/ TXDATAHS_1[7:0]/ TXDATAHS_2[7:0]/ TXDATAHS_3[7:0]
- TXREQUESTDATAHS_0/ TXREQUESTDATAHS_1/ TXREQUESTDATAHS_2/ TXREQUESTDATAHS_3/
- TXREQUESTHSCLK

The list of signals above should be considered merely illustrative and follows the tests presented on previous sections. If customer decides to include additional tests or remove tests, the list of required signals must be updated accordingly. Any of the signals on this list may be routed directly to dedicated IOs if it eases production testing and the system allows it.

- Internally observable: None
- Externally controllable (available as input chip IOs)

  Part or all the signals from “Internally Controllable” list.
- Externally observable (available as output chip IOs)
  - LOCK
  - TESTDOUT[7:0]
  - STOPSTATEx

8.6 Control/Test Codes

Table 8-5 presents a list of all the accessible control/test modes for this IP Cell. An individual control/test mode description is presented hereafter. For all control/test modes without monitoring functionalities defined, TESTDOUT[7:0] is always 0x00.

Table 8-5 Supported Test Codes for Test Mode

Test Code	Test Description	Test Code	Test Description
0x00	No test; normal operation	0x50	bintpon control of lane 1
0x01	LP driver wake up timer counter after exiting ULPS	0x51	LP RX control of lane 1
0x02	Delay between LP driver enable and start to drive LP=11 during initialization state timer control	0x43	LP TX control of lane 0
0x03	Delay between enable calibration and starting calibration timer control	0x44	Operating frequency range selector /HS RX control of lane 0
0x04	Relinquish control timer if PHY configured as TX	0x45	Lane 0 inversion functionality (DATAP/DATAN swap)
0x05	Tta-go timer control	0x46	HS RX Lane 0 outputs and calibration error observability
0x06	Tta-sure timer control	0x52	LP TX control of lane 1
0x07	Turnaround request delay control	0x53	LP TX control of lane 1
0x08	Delay between HS receiver power on and enabling calibration timer control.	0x54	HS RX control of lane 1
0x09	Relinquish control timer for Slave if RX	0x55	Lane 1 inversion functionality (DATAP/DATAN swap)
0x0A	Stop state watchdog timer control	0x56	HS RX lane 1 outputs and calibration error observability
0x0B	Reserved	0x60	HS TX clock lane request state time (TLP) control
0x0C	Stop state watchdog timer enable and contention detection.	0x61	HS TX clock lane prepare state time (T CLK-prepare) control
0x10	PLL bias current selector /Filter capacitance multiplier / VCO control	0x62	HS TX clock lane go state time (TCLK-zero) control
0x11	PLL CP control / PLL lock bypass for initialization and for ULP mode	0x63	HS TX clock lane trail state time (TCLK-trail) control
0x12	PLL LPF and CP control	0x64	HS TX clock lane exit time (THS-exit) control

Test Code	Test Description	Test Code	Test Description
0x13	PLL digital testability	0x65	HS TX clock lane clock post state time (TCLK-post) control
0x14	PLL phase error control	0x70	HS TX data lanes request state time (TLP) control
0x15	PLL locking filter	0x71	HS TX data lanes clock prepare state time (T HS-prepare) control
0x16	PLL unlocking filter	0x72	HS TX data lanes go state time (T HS- zero) control
0x17	PLL input divider ratio	0x73	HS TX data lanes trail state time (THS-trail) control
0x18	PLL loop divider ratio	0x74	HS TX data lanes exit time (THS-exit) control
0x19	PLL post divider ratio and PLL input and divider ratios control	0x80	Benton control of lane 2
0x20	Band gap and bias control	0x81	LP RX control of lane 2
0x21	Termination resistor control	0x82	LP TX control of lane 2
0x30	Benton control of clock lane	0x83	LP TX control of lane 2
0x31	LP RX control of clock lane	0x84	HS RX control of lane 2
0x32	LP TX control of clock lane	0x85	Lane 2 inversion functionality (DATAP/DATAN swap)
0x33	LP TX control of clock lane	0x90	Benton control of lane 3
0x34	HS RX control of clock lane	0x91	LP RX control of lane 3
0x35	CLKP/CLKN swap for clock lane + Ticklers control	0x92	LP TX control of lane 3
0x36	HS RX clock lane outputs and calibration error observability	0x93	LP TX control of lane 3
0x40	bintpon control of lane 0	0x94	HS RX control of lane 3
0x41	LP RX control of lane 0	0x95	Lane 3 inversion functionality (DATAP/DATAN swap)
0x42	LP TX control of lane 0	All others	Reserved for Synopsys usage

8.6.1 Normal Operation

Test Code: 0x00

This is the normal operation mode of the IP Cell and also the wake up state of the test interface. In this mode the test interface is inactive.

Test Data: None

8.6.2 LP Driver Wake Up Timer Counter after Exiting ULPS

Test Code: 0x01

This test mode allows the configuration of the counter threshold that controls the time that goes between exiting ultra low power state and enabling the low power driver. Clocked by CFG_CLK.

Test Data:

Table 8-6 Test Data

w-8'b10111011
Timer counter

Bits 7...0: Timer counter

'XXXXXXXX' – Timer is loaded with value 10'bXXXXXXXX11

Testdout:

Table 8-7 Testdout

r-8'b10111011
Timer counter multiplier bits [9:2] loopback

8.6.3 Delay between LP TX Driver Enable and Start Driving LP = 11 during Initialization Timer Control

Test Code: 0x02

This test mode allows the configuration of the counter threshold that controls the time that goes between LP TX driver enable and start driving LP = 2'b11 during PHY initialization as TX.

Test Data:

Table 8-8 Test Data

w-8'b00001111
Timer counter

Bits 7...0: Timer counter

'XXXXXXXX' – Timer is loaded with value 10'bXXXXXXXX00

Testdout:

Table 8-9 Testdout

r-8'b00001111
Timer counter multiplier bits [9:2] loopback

8.6.4 Delay between Enable Calibration and Starting Calibration Timer Control

Test Code: 0x03

This test mode allows the configuration of the counter threshold that controls the time that goes between calibration enable and effectively starting it. It is clocked by CFG_CLK.

Test Data:

Table 8-10 Test Data

w-8'b00111100
Timer counter

Bits 7...0: Timer counter

Testdout:

Table 8-11 Testdout

r-8'b00111100
Timer counter multiplier bits loopback

8.6.5 Relinquish Control if PHY is Configured as TX

Test Code: 0x04

This test mode allows the control of the time during which all lanes are controlled by a single body. The timer counter starts at top level reset and after reaching the target value, each lane become independent. Default value is 20 assuming a minimum period of 50 ns, only for PHY configuration as TX, clocked by CFG_CLK.

Test Data:

Table 8-12 Test Data

w-8'b10011100
Timer counter

Bits 7...0: Timer counter

'XXXXXXXX' – Timer is loaded with value 10'bXXXXXXXX00

Testdout:

Table 8-13 Testdout

r-8'b10011100
Timer counter multiplier bits [9:2] loopback

8.6.6 $T_{ta\text{-}go}$ Timer Counter

Test Code: 0x05

This test mode allows the control of the number of cycles that the TX drives the bridge state during a turnaround procedure ($T_{ta\text{-}go}$). Refer to the D-PHY specification for more information. It is clocked by TXCLKESC.

Test Data:

Table 8-14 Test Data

w-2'b00	w-6'b000100
Reserved	Number of cycles

Bits 5...0: Number of cycles

Testdout:

Table 8-15 Testdout

r-2'b00	r-6'b000100
2'b00	Number of cycles loopback

8.6.7 $T_{ta\text{-}sure}$ Timer Counter

Test Code: 0x06

This test mode allows the control of the number of cycles that the RX waits after a bridge state has been detected during a turnaround procedure ($T_{ta\text{-}sure}$). Refer to the D-PHY specification for more information. Clocked by TXCLKESC.

Test Data:

Table 8-16 Test Data

w-2'b00	w-6'b000001
Reserved	Number of cycles

Bits 5...0: Number of cycles

Testdout:

Table 8-17 Testdout

r-2'b00	r-6'b000001
2'b00	Number of cycles loopback

8.6.8 Turnaround Request Delay Control

Test Code: 0x07

This test mode allows the control of the number of cycles that the PHY waits until a turnaround request is processed, allowing LP RX to be ready. It is clocked by TXCLKESC.

Test Data:

Table 8-18 Test Data

w-2'b00	w-6'b110010
Reserved	Number of cycles

Bits 5...0: Number of cycles

Testdout:

Table 8-19 Testdout

r-2'b00	r-6'b110010
Reserved	Number of cycles loopback

8.6.9 Delay between HS Receiver Power On and Enabling Calibration Timer Control

Test Code: 0x08

This test mode allows the control of the time between powering on the HS receiver and enabling calibration. It is clocked by CFG_CLK.

Test Data:

Table 8-20 Test Data

w-8'b00000110
Number of cycles

Bits 7...0: Number of cycles

Testdout:

Table 8-21 Testdout

r-8'b00000110
Number of cycles loopback

8.6.10 Relinquish Control when PHY is Configured as RX

Test Code: 0x09

This test mode allows the control of the time during which all lanes are controlled by a single body. The timer counter starts at top level reset and after reaching the target value, each lane becomes independent. It is only for configuration as RX and is clocked by CFG_CLK.

Test Data:

Table 8-22 Test Data

w-8'b00001111
Timer counter

Bits 7...0: Timer counter

XXXXXXXX – Timer is loaded with value 10'bXXXXXXXX00

Testdout:

Table 8-23 Testdout

r-8'b00001111
Timer counter multiplier bits [9:2] loopback

8.6.11 Stop State Watchdog Timer Control

Test Code: 0x0A

This test mode allows to control the time that the PHY is receiving LP=2'b11 without interruption, if this time exceeds timoutstopstate threshold a reset is applied to the corresponding lane. It is disabled by default. It is only for the configuration as RX and is clocked by CFG_CLK.

Test Data:

Table 8-24 Test Data

w-2'b00	**w-6'b110000**
Set 0	timeoutstopstate [5:0]
w-2'b01	**w-6'b011101**
Set 1	timeoutstopstate [11:6]
w-2'b10	**w-3'b001**
Set 2	timeoutstopstate [14:12]

Bits 7...6: Programmability selector

- 00 – Set 0 is programmed (also selects this part of the register for observability) 15'b000000000XXXXXX
- 01 – Set 1 is programmed (also selects this part of the register for observability) 15'b000XXXXXX000000
- 10 – Set 2 is programmed (also selects this part of the register for observability) 15'bXXX000000000000

Bits 5...0: Programmable value

Testdout:

Programmability selector [7:6] – Set 0

Table 8-25 Testdout

r-2'b00	**r-6'b110000**
2'b00	timeoutstopstate [5:0]

Programmability selector [7:6] – Set 1

Table 8-26 Testdout

r-2'b00	**r-6'b011101**
2'b00	timeoutstopstate [11:6]

Programmability selector [7:6] – Set 2

Table 8-27 Testdout

r-5'b00000	r-3'b001
5’b00000	timeoutstopstate [14:12]

8.6.12 Stop State Watchdog Timer Enable and Contention Detection

Test Code: 0x0C

This test mode allows enabling/disabling Stop State watchdog timer. It is only for the configuration as RX. It also provides control for the contention detection mechanism.

Test Data:

Table 8-28 Test Data

w-1'b0	w-4'b0000	w-1'b0	w-2'b00
Error Contention detection	Reserved	Enable/disable watchdog timer	Reserved

- Bit 7: Error Contention detection
  - 0 – Enable Error Contention detection only during TA (default)
  - 1 – Enable Error Contention detection in all LP modes including TA
- Bits 6...3: Reserved
- Bit 2: Enable/disable watchdog timer
  - 0 – Disable watchdog timer
  - 1 – Enable watchdog timer
- Bits 1...0: Reserved

Testdout:

Table 8-29 Testdout

r-1'b0	r-4'b0000	r-1'b0	r-2'b00
Error Contention detection	4'b0000	Enable/disable watchdog timer loopback	2'b00

8.6.13 PLL Bias Current Selector / Filter Capacitance Multiplier / VCO Control

Test Code: 0x10

This test mode allows the control of the biasing of the PLL and of the VCO transfer function.

Test Data:

Table 8-30 Test Data

w-1'b0	w-4'b0001	w-2'b00	w-1'b1
Bypass VCO range	VCO range control	Capacitance multiplier	Reference bias current selector

- Bit 7: Bypass VCO range
  - 0 – VCO range is programmed with default values for correspondent hsfreqrange (testcode 8'h44)
  - 1 – VCO range is programmed with bits 6…3
- Bit 6…3: VCO range control
  - 0001 – When f_{VCO} frequency is between 80 MHz and 160 MHz
  - 0011 – When f_{VCO} frequency is between 160 MHz and 250 MHz
  - 0111 – When f_{VCO} frequency is between 250 MHz and 500 MHz
  - 1111 – When f_{VCO} frequency is between 500 MHz and 1 GHz
- Bits 2...1: Capacitance multiplier
  - 00 – Capacitance multiplication is disabled
  - 01 – Capacitance multiplication is enabled
  - 10 – Capacitance multiplication is enabled x5
  - 11 – Capacitance multiplication is enabled x10
- Bit 0: Reference bias current selector
  - 0 – Internal biasing
  - 1 – Clean external current source of 20 uA

Testdout

Table 8-31 Testdout

r-1'b0	r-4'b0001	r-2'b00	r-1'b1
Bypass VCO range loopback	VCO range loopback	Capacitance multiplier loopback	Reference bias current selector loopback

8.6.14 PLL CP Control / PLL Lock Bypass for Initialization and for ULP

Test Code: 0x11

This test mode allows the control of the charge pump current and the bypass of the PLL lock for initialization and ULP exit.

Test Data:

Table 8-32 Test Data

w-4'b0000	w-4'b0110
PLL lock bypass	CP current

- Bits 7...4: PLL lock bypass
  - xxx0 – Bypass PLL lock during initialization
  - x11x – Bypass PLL lock after exiting ULP
- Bits 3...0: CP current
  - 0000 – 1.5 uA
  - 0001 – 3 uA
  - 0010 – 4.5 uA
  - 0011 – 6.5 uA
  - 0100 – 2.5 uA
  - 0101 – 5 uA
  - 0110 – 7.5 uA
  - 0111 – 10 uA
  - 1000 – 3 uA
  - 1001 – 6 uA
  - 1010 – 9 uA
  - 1011 – 12 uA
  - 1100 – 4 uA
  - 1101 – 8 uA
  - 1110 – 12 uA
  - 1111 – 16 uA

Testdout:

Table 8-33 Testdout

r-4'b0000	r-4'b0110
PLL lock bypass loopback	CP current loopback

8.6.15 PLL LPF and CP control

Test Code: 0x12

This test mode allows the control of the low pass filter resistor.

Test Data:

Table 8-34 Test Data

w-1'b0	w-1'b0	w-6'b010000
Bypass CP default values	Bypass LPF default values	LPF resistor

- Bit 7: Bypass CP default values
  - 0 – CP is programmed with default values for correspondent hsfreqrange (testcode 8'h44)
  - 1 – CP is programmed with bits 3…0 using testcode 8'h11.
- Bit 6: Bypass LPF default values
  - 0 – LPF is programmed with default values for correspondent hsfreqrange (testcode 8'h44)
  - 1 – LPF is programmed with bits 6…0
- Bits 5...0: LPF resistors
  - 100000 – 1 KOhm
  - 010000 – 6 KOhm
  - 001000 – 12 KOhm
  - 000100 – 18 KOhm
  - 000010 – 24 KOhm
  - 000001 – 32 KOhm
  - 000000 – 48 KOhm
  - All others – Reserved

Testdout:

Table 8-35 Testdout

r-1'b0	r-1'b0	r-6'b010000
CP bypass loopback	LPF bypass loopback	LPF resistor loopback

8.6.16 PLL digital testability

Test Code: 0x13

This test mode allows the access to a few internal signals of the PLL.

Test Data:

Table 8-36 Test Data

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-3'b000	w-1'b0
Reserved	Power override enable	Digital reset	Power on/off	Observability control	Bypass post divider

- Bit 7: Reserved
- Bit 6: Power override enable
  - 0 – PLL's power is managed by internal FSM
  - 1 – PLL's power is controlled by the two following bits
- Bit 5: Digital reset (requires power override enable at 1)
  - 0 – Digital block is placed in reset
  - 1 – Digital block is placed in taken out of reset
- Bit 4: Power on/off (requires power override enable at 1)
  - 0 – Analog blocks are turned off
  - 1 – Analog blocks are turned on
- Bits 3..1: Observability control
  - 000 – Internal lock signal
  - 001 – PFDs reference clock
  - 010 – PFD's feedback clock
  - 011 – PLL's input clock (gated with bypass)
  - 100 – Signal after post divider
  - 101 – VCO clock (buffered)
  - 110 – VCO clock (gated with bypass)
  - 111 – Reserved
- Bit 0: Bypass post divider
  - 0 – Post divider output is assigned to TXCLKHSQR
  - 1 – Input reference clock is assigned to TXCLKHSQR

Testdout:

Table 8-37 Testdout

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-3'b000	w-1'b0
Test lock	Power override enable loopback	Digital reset loopback	Power on/off loopback	Observability control loopback	Bypass post divider loopback

8.6.17 PLL Phase Error Control

Test Code: 0x14

This test mode allows the control over the allowed phase error before PLL lock is issued. This phase error is measured in VCO clock cycles.

Test Data:

Table 8-38 Test Data

w-1'b0	**w-2'b00**	**w-5'b00100**
Set 0	Reserved	Phase error [4:0]
w-1'b1	**w-2'b00**	**w-5'b00000**
Set 1	Reserved	Phase error [9:5]

- Bit 7: Programmability selector
  - 0 – Set 0 is programmed (also selects this half of the register for observability) 10'bXXXXX00100
  - 1 – Set 1 is programmed (also selects this half of the register for observability) 10'b00000XXXXX
- Bits 6...5: Reserved
- Bits 4...0: Phase error value

Testdout:

Testdin [7] – Set 0:

Table 8-39 Testdout

r-3'b000	**r-5'b00100**
3'b000	Phase error[4:0] loopback

Testdin [7] – Set 1:

Table 8-40 Testdout

r-3'b000	**r-5'b00000**
3'b000	Phase error[9:5] loopback

8.6.18 PLL Locking Filter

Test Code: 0x15

This test mode allows the control over the length of PLL lock filter. This filter exists to avoid having false lock indications. This filter represents the number of cycles where a phase error smaller than defined (see previous test mode) must be observed before lock is issued.

Test Data:

Table 8-41 Test Data

r-8'b11111111
PLL's lock filter

Testdout:

Table 8-42 Testdout

r-8'b11111111
PLL's lock filter loopback

8.6.19 PLL Unlocking Filter

Test Code: 0x16

This test mode allows the control over the length of PLL unlock filter. This filter exists to avoid that temporary disturbances like peak jitter or supply noise cause loss of lock. This filter represents the number of cycles where a phase error higher than defined (see previous test mode) must be observed before lock is de-asserted.

Test Data:

Table 8-43 Test Data

r-8'b00000010
PLL's unlock filter

Testdout:

Table 8-44 Testdout

r-8'b00000010
PLL's unlock filter loopback

8.6.20 PLL Input Divider Ratio

Test Code: 0x17

This test mode allows the control of the PLL's input divider. It is the divided reference clock which is fed into the phase-frequency-detector. Obtained frequency is <reference clock frequency> / (<input divider> + 1). For the input divider to be effective, bit 4 of register 0x19 must be 1.

Test Data:

Table 8-45 Test Data

w-8'b00001000
Input divider

Testdout:

Table 8-46 Testdout

r-8'b00001000
Input divider loopback

8.6.21 PLL Loop Divider Ratio

Test Code: 0x18

This test mode allows the control of the PLL's feedback divider. It is the divided VCO clock which is fed into the phase-frequency-detector. Obtained frequency is <VCO clock frequency> / (<feedback divider> + 1). For the input divider to be effective, bit 5 of register 0x19 must be 1.

Test Data:

Table 8-47 Test Data

w-1'b0	**w-2'b00**	**w-5'b11101**
Set 0	Reserved	Feedback divider [4:0]
w-1'b1	**w-2'b00**	**w-5'b00000**
Set 1	Reserved	Feedback divider [9:5]

- Bit 7: Programmability selector
  - 0 – Set 0 is programmed (also selects this half of the register for observability) 10'bXXXXX11101
  - 1 – Set 1 is programmed (also selects this half of the register for observability) 10'b00000XXXXX
- Bits 6...5: Reserved
- Bits 4...0: Feedback divider

Testdout:

Testdin [7] - Set 0:

Table 8-48 Testdout

r-3'b000	**r-5'b11101**
3'b000	Feedback divider [4:0] loopback

Testdin [7] – Set 1:

Table 8-49 Testdout

r-3'b000	**r-5'b00000**
3'b000	Feedback divider [9:5] loopback

8.6.22 PLL Post Divider Ratio and PLL Input and Loop Divider Ratios Control

Test Code: 0x19

This test mode allows the control of the PLL's post divider. TXCLKHSQR represents the output of this divider. Obtained frequency is <VCO clock frequency> / (<post divider> + 1).

Test Data:

Table 8-50 Test Data

w-2'b00	w-1'b0	w-1'b0	w-4'b0011
Reserved	Bypass PLL loop divider default values	Bypass PLL input divider default values	Post divider

- Bits 7...6: Reserved
- Bit 5: Bypass PLL loop divider default values
  - 0 – PLL loop divider is programmed with default values for correspondent hsfreqrange (testcode 8'h44)
  - 1 – PLL loop divider is using testcode 8'h18
- Bit 4: Bypass PLL input divider default values
  - 0 – PLL input divider is programmed with default values for correspondent hsfreqrange (testcode 8'h44)
  - 1 – PLL input divider is programmed using testcode 8'h17
- Bits 3...0: Post divider

Testdout:

Table 8-51 Testdout

r-2'b00	r-1'b0	r-1'b0	r-4'b0011
2'b00	Bypass PLL loop divider default loopback	Bypass PLL input divider loopback	Post divider loopback

8.6.23 Bandgap and Bias Control

Test Code: 0x20

This test mode allows the control over bandgap and biasing unit power management.

Test Data:

Table 8-52 Test Data

w-1'b0	w-1'b0	w-2'b00	w-1'b1	w-1'b0	w-1'b0	w-1'b0
Reserved	Power override enable	Reserved	Biasing scheme selector	Bias block power on	Voltage reference generator power on	Bandgap power on

- Bit 7: Reserved
- Bit 6: Power override enable
  - 0 – Power is managed by internal FSM
  - 1 – Power is controlled by tester interface
- Bits 5...4: Reserved
- Bit 3: Biasing scheme selector (requires bandgap)
  - 0 – Reference current is generated through the external resistor
  - 1 – Reference current is generated through an internal resistor
- Bit 2: Bias block power on (requires bandgap)
  - 0 – Bias block is powered off
  - 1 – Bias block is powered on
- Bit 1: Voltage reference generator power on (requires bandgap)
  - 0 – Voltage generator is powered off
  - 1 – Voltage generator is powered on
- Bit 0: Bandgap power on
  - 0 – Bandgap is powered off
  - 1 – Bandgap is powered on

Testdout:

Table 8-53 Testdout

r-1'b0	r-1'b0	r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0
Bandgap OK	Power override enable loopback	2'b00	Biasing scheme selector loopback	Bias block power on loopback	Voltage reference generator power on loopback	Bandgap power on loopback

- Bit 7: Bandgap OK
  - 0 – Bandgap voltage is not at target value yet
  - 1 – Bandgap voltage is stable at target value

8.6.24 Termination Resistor Control

Test Code: 0x21

This test mode allows the control over the termination resistor's value.

Test Data:

Table 8-54 Test Data

w-3'b000	w-3'b011	w-1'b0	w-1'b0
Reserved	Termination resistor value	Termination resistor power override enable	Termination resistor power on

- Bits 7...5: Reserved
- Bits 4...2: Termination resistor value (requires termination resistor power on) BD
- Bit 1: Termination resistor power override enable
  - 0 – Power is managed by internal FSM
  - 1 – Power is managed by test interface
- Bit 0: Termination resistor power on (requires power override enable)
  - 0 – Termination resistors are turned off
  - 1 – Termination resistors are turned on

Testdout:

Table 8-55 Testdout

r-1'b0	r-1'b0	r-1'b0	r-3'b011	r-1'b0	r-1'b0
Resistor comparator	Analog programmability level shifter power on	1'b0	Termination resistor value loopback	Termination resistor power override enable loopback	Termination resistor power on loopback

- Bit 7: Resistor comparator
  - 0 – Term. Resistor lower than external resistor
  - 1 – Term. Resistor higher than external resistor
- Bit 6: Analog programmability level shifter power on
  - 0 – Level shifters are powered off
  - 1 – Level shifters are powered on

8.6.25 AFE /BIAS/ Bandgap Analog Programmability

Test Code: 0x22

This test mode allows the control of various parameters in the analog macro.

Test Data:

Table 8-56 Test Data

w-2'b00	**w-6'b000000**
Set 0	Analog programmability[5:0]
w-2'b01	**w-6'b000000**
Set 1	Analog programmability[11:6]
w-2'b10	**w-6'b000000**
Set 2	Analog programmability[17:12]
w-2'b11	**w-6'b000000**
Set3	Analog programmability[23:18]

- Bits 7...6: Programmability selector
  - 00 – Set 0 is programmed (also selects this half of the register for observability) 24'bXXXXXXXXXXXXXXXXXX000000
  - 01 – Set 1 is programmed (also selects this half of the register for observability) 24' bXXXXXXXXXXXX000000XXXXXX
  - 10 – Set 2 is programmed (also selects this half of the register for observability) 24'bXXXXXX000000XXXXXXXXXXXX
  - 11 – Set3 is programmed (also selects this half of the register for observability) 24'b000000XXXXXXXXXXXXXXXXXX
- Bits 5...0: Analog programmability
  - [23:16] – AFE low voltage programmability
  - [15:8] – AFE high voltage programmability
  - [7:6] – Reserved
  - [5:3] – BIAS high voltage programmability
  - [2:0] – VGEN high voltage programmability

Testdout:

Table 8-57 Testdout

r-2'b00	r-6'b000000
Set 0	Analog programmability[5:0] loopback
Set 1	Analog programmability[11:6] loopback
Set 2	Analog programmability[17:12] loopback
Set 3	Analog programmability[23:18] loopback

8.6.26 Bias power on control of clock lane

Test Code: 0x30

Test Data:

Table 8-58 Test Data

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Bypass HS TX Data in	HS TX Data in	Bypass HS TX enable	HS TX enable	Bypass HS TX power on	HS TX power on	Bypass Bias power on	Bias power on

- Bit 7: Bypass High Speed Driver Data
  - 0 – Internal high speed driver data is controlled by internal FSM
  - 1 – Internal high speed driver data is controlled by test interface
- Bit 6: High Speed Driver Data
  - 0 – Internal high speed driver transmits a low level voltage signal 0
  - 1 – Internal high speed driver transmits a high level voltage signal 1
- Bit 5: Bypass High Speed Driver enable
  - 0 – Internal high speed driver enable is controlled by internal FSM
  - 1 – Internal high speed driver enable is controlled by test interface
- Bit 4: High Speed Driver enable
  - 0 – Internal high speed driver is disabled
  - 1 – Internal high speed driver is enabled
- Bit 3: Bypass High Speed Driver power on
  - 0 – Internal high speed driver power on is controlled by internal FSM
  - 1 – Internal high speed driver power on is controlled by test interface
- Bit 2: High Speed Driver power on
  - 0 – Internal high speed driver is powered off
  - 1 – Internal high speed driver is powered off
- Bit 1: Bypass clock lane bias block power on
  - 0 – Internal biasing block is controlled by internal FSM
  - 1 – Internal biasing block is controlled by test interface
- Bit 0: Clock lane bias block power on
  - 0 – Internal biasing block is powered off
  - 1 – Internal biasing block is powered on

TestDout:

Table 8-59 Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
Bypass HS TX Data in loopback	HS TX Data in loopback	Bypass HS TX enable loopback	HS TX enable loopback	Bypass HS TX power on loopback	HS TX power on loopback	Bypass Bias power on loopback	Bias power on loopback

8.6.27 LP RX Control of Clock Lane

Test Code: 0x31

This test mode allows the control over the low power single-ended receivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 8-60 Test Data

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 1	Reserved	Bypass LP CD power on	LP CD power on	Bypass ULP power on	ULP power on	Bypass LP power on	LP power on

- Bit 7: Programmability selector
  - 0 – Does not program anything
  - 1 – Programs 'Set 1' registers
- Bit 6: Reserved
  - 0 – Signals controlled by internal FSM
  - 1 – LP RX controlled by test interface
- Bit 5: Bypass LP CD power on
  - 0 – LP CD power on is controlled by internal FSM
  - 1 – LP CD power on is controlled by test interface
- Bit 4: LP CD power on
  - 0 – LP CD is powered off
  - 1 – LP CD is powered on
- Bit 3: Bypass ULP RX power on
  - 0 – ULP RX power on is controlled by internal FSM
  - 1 – ULP RX power on is controlled by test interface
- Bit 2: ULP RX power on
  - 0 – ULP RX is powered off
  - 1 – ULP RX is powered on
- Bit 1: Bypass LP RX power on
  - 0 – LP RX power on is controlled by internal FSM
  - 1 – LP RX power on is controlled by test interface

- Bit 0: LP RX power on
  - 0 – LP RX is powered off
  - 1 – LP RX is powered on

Testdout:

Table 8-61 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00	Bypass LP CD power on loopback	LP CD power on loopback	Bypass ULP power on loopback	ULP power on loopback	Bypass LP power on loopback	LP power on loopback
2'b00	LP CD dataout		ULP RX dataout		LP RX dataout	

- First row (if testdin[7] == 1'b1)

  Set 1 loopback
- Second row (if testdin[7] == 1'b0)
- Bits 7...6: Reserved
- Bits 5...4: LP CD dataout

  Data coming out of the two single-ended low power contention detectors
- Bits 3....2: ULP RX dataout

  Data coming out of the two single-ended low power receivers used to detect that TX has left ultra low power state
- Bits 1...0: LP RX dataout

  Data coming out of the two single-ended low power receivers when in low power mode

8.6.28 LP TX Control of Clock Lane

Test Code: 0x32

This test mode allows the control over the low power single-ended drivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 8-62 Test Data

w-2'b00	w-1'b0	w-1'b0	w-1'b00	w-1'b0	w-1'b0	w-1'b0
Reserved	Bypass LP TX enable pull down	LP TX enable pull down	Bypass LP TX enable	LP TX enable	Bypass LP TX power on	LP TX power on

- Bit 7…6: Reserved
- Bit 5: Bypass LP TX enable pull down
  - 0 – LP TX enable pull down is controlled by internal FSM
  - 1 – LP TX enable pull down is controlled by test interface
- Bit 4: LP TX enable pull down
  - 0 – Pull down functionality is turned off
  - 1 – A LP-00 state is forced at the output of the low power drivers
- Bit 3: Bypass LP TX enable
  - 0 – LP TX enable is controlled by internal FSM
  - 1 – LP TX enable is controlled by test interface
- Bit 2: LP TX enable
  - 0 – Driver will not transmit incoming data
  - 1 – Driver will transmit incoming data
- Bit 1: Bypass LP TX power on
  - 0 – LP TX is powered off
  - 1 – LP TX is powered on
- Bit 0: LP TX power on
  - 0 – LP TX is powered off
  - 1 – LP TX is powered on

Testdout:

Table 8-63 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2’b00	Bypass LP TX enable pull down loopback	LP TX enable pull down loopback	Bypass LP TX enable loopback	LP TX enable loopback	Bypass LP TX power on loopback	LP TX power on loopback

8.6.29 LP TX Control of Clock Lane

Test Code: 0x33

This test mode allows the control over the low power single-ended drivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 8-64 Test Data

w-5'b00000	w-1'b0	w-2'b00
Reserved	Bypass LP TX driver datain	LP TX driver datain

- Bit 7…3: Reserved
- Bit 2: Bypass LP TX driver datain
  - 0 – Inputs of LP TX driver are controlled by internal FSM
  - 1 – Inputs of LP TX driver are controlled by test interface
- Bit 1...0: LP TX driver datain

  Inputs of LP TX driver

Testdout:

Table 8-65 Testdout

r-5'b00000	r-1'b0	r-2'b00
5'b00000	Bypass LP TX driver datain loopback	LP TX driver datain loopback

8.6.30 HS RX Control of Clock Lane

Test Code: 0x34

This test mode allows the control over the high speed differential receiver of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 8-66 Test Data

w-2'b00	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 0	Bypass HS RX termination enable	HS RX termination enable	Bypass HS RX offset calibration enable	HS RX offset calibration enable	Bypass HS RX power on	HS RX power on
Set 1	Bypass HS RX offset compensation setting	HS RX offset compensation setting				
Set 2	Reserved					Bypass HS - RX settle filter

- Bits 7...6: Programmability selector
  - 10 – Set 0 is programmed
  - 11 – Set 1 is programmed
  - 0x – Set 2 is programmed

Set 0:

- Bit 5: Bypass HS RX terminations enable
  - 1 – HS RX terminations enable is controlled by test interface
  - 0 – HS RX terminations enable is controlled by internal FSM
- Bit 4 HS RX terminations enable
  - 0 – Termination not enabled
  - 1 – Termination enabled
- Bit 3: Bypass HS RX calibration enable
  - 1 – HS RX calibration enable is controlled by test interface
  - 0 – HS RX calibration enable is controlled by internal FSM
- Bit 2: HS RX calibration enable
  - 1 – HS RX calibration enabled
  - 0 – HS RX calibration not enabled

- Bit 1: Bypass HS RX power on
  - 1 – HS RX powered on is controlled by test interface
  - 0 – HS RX powered on is controlled by internal FSM
- Bit 0: HS RX power on
  - 0 – HS RX powered off
  - 1 – HS RX powered on

Set 1:

- Bit 5: Bypass HS-RX offset compensation setting
- Bits 4...0: HS-RX offset compensation setting

Set 2:

- Bit 5…1: Reserved
- Bit 0: Bypass HS settle filter

Testdout:

Table 8-67 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00	Bypass HS RX termination enable loopback	HS RX termination enable loopback	Bypass HS RX offset calibration enable loopback	HS RX offset calibration enable loopback	Bypass HS RX power on loopback	HS RX power on loopback
2'b00	Bypass HS RX offset compensation setting loopback	HS RX offset compensation setting loopback				
7'b00000000						Bypass HS-RX settle filter loopback

- First row (if testdin[7:6] == 2'b10)
- Second row (if testdin[7:6] == 2'b11)
- Third row (if testdin[7:6] == 2'b0x)

8.6.31 CLKP/CLKN Swap for Clock Lane + Tclk_miss Control

Test Code: 0x35

This test mode allows the correct clock lane operation in case a CLKP/CLKN swap is required.

Test Data:

Table 8-68 Test Data

w-6'b000000	w-1'b0	w-1'b0
Reserved	Clock Miss force	Polarity change

- Bit 7…2: Reserved
- Bit 1: Clock Miss force
  - 0 – Tclk_miss evaluation mechanism enabled
  - 1 –Tclk_miss evaluation mechanism disabled
- Bit 0: Polarity change
  - 0 – Two PHYS with CLKP/CLKN ports connected to CLKP/CLKN respectively
  - 1 – Two PHYS with CLKP/CLKN ports connected to CLKN/CLKP respectively

Testdout:

Table 8-69 Testdout

r-6'b000000	r-1'b0	r-1'b0
6'b000000	Clock Miss force loopback	Polarity change loopback

8.6.32 Calibration Machine Outputs Observability of Clock Lane

Test Code: 0x36

This test mode allows the observability of some outputs of the calibration machine and HS-RX of clock lane.

Testdout:

Table 8-70 Testdout

r-1'b0	**r-1'b0**	**r-1'b0**	**r-1'b0**	**r-4'b0000**
3'b000			HS RX offset compensation setting	
HS RX asynchronous output		HS RX synchronous output		HS RX calibration errors

- First row (if testdin[7] == 1'b0)
- Second row (if testdin[7] == 1'b1)
- Bits 7...6: HS RX asynchronous output

  Asynchronous output of HS RX received in the differential pair.
- Bits 5...4: HS RX synchronous output

  Synchronous output of HS RX (clock from clock lane used to sample).
- Bits 3...0: HS RX calibration errors flags

8.6.33 Bias Power on Control of Lane 0

Test Code: 0x40

Test Data:

Table 8-71 Test Data

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Bypass HS TX Data in	HS TX Data in	Bypass HS TX enable	HS TX enable	Bypass HS TX Power on	HS TX power on	Bypass Bias power on	Bias power on

- Bit 7: Bypass High Speed Driver Data
  - 0 – Internal high speed driver data is controlled by internal FSM
  - 1 – Internal high speed driver data is controlled by test interface
- Bit 6: High Speed Driver Data
  - 0 – Internal high speed driver transmits a low level voltage signal ‘0’
  - 1 – Internal high speed driver transmits a high level voltage signal ‘1’
- Bit 5: Bypass High Speed Driver enable
  - 0 – Internal high speed driver enable is controlled by internal FSM
  - 1 – Internal high speed driver enable is controlled by test interface
- Bit 4: High Speed Driver enable
  - 0 – Internal high speed driver is disabled
  - 1 – Internal high speed driver is enabled
- Bit 3: Bypass High Speed Driver power on
  - 0 – Internal high speed driver power on is controlled by internal FSM
  - 1 – Internal high speed driver power on is controlled by test interface
- Bit 2: High Speed Driver power on
  - 0 – Internal high speed driver is powered off
  - 1 – Internal high speed driver is powered off
- Bit 1: Bypass clock lane bias block power on
  - 0 – Internal biasing block is controlled by internal FSM
  - 1 – Internal biasing block is controlled by test interface
- Bit 0: Clock lane bias block power on
  - 0 – Internal biasing block is powered off
  - 1 – Internal biasing block is powered on

TestDout:

Table 8-72 Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
Bypass HS TX Data in loopback	HS TX Data in loopback	Bypass HS TX enable loopback	HS TX enable loopback	Bypass HS TX Power on loopback	HS TX power on loopback	Bypass Bias power on loopback	Bias power on loopback

8.6.34 LP RX Control of Lane 0

Test Code: 0x41

This test mode allows the control over the low power single-ended receivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 8-73 Test Data

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 1	Reserved	Bypass LP CD power on	LP CD power on	Bypass ULP power on	ULP power on	Bypass LP power on	LP power on

- Bit 7: Programmability selector
  - 0 – Does not program anything
  - 1 – Programs 'Set 1' registers
- Bit 6: Reserved
  - 0 – Signals controlled by internal FSM
  - 1 – LP RX controlled by test interface
- Bit 5: Bypass LP CD power on
  - 0 – LP CD power on is controlled by internal FSM
  - 1 – LP CD power on is controlled by test interface
- Bit 4: LP CD power on
  - 0 – LP CD is powered off
  - 1 – LP CD is powered on
- Bit 3: Bypass ULP RX power on
  - 0 – ULP RX power on is controlled by internal FSM
  - 1 – ULP RX power on is controlled by test interface
- Bit 2: ULP RX power on
  - 0 – ULP RX is powered off
  - 1 – ULP RX is powered on
- Bit 1: Bypass LP RX power on
  - 0 – LP RX power on is controlled by internal FSM
  - 1 – LP RX power on is controlled by test interface
- Bit 0: LP RX power on
  - 0 – LP RX is powered off
  - 1 – LP RX is powered on

Testdout:

Table 8-74 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00	Bypass LP CD power on loopback	LP CD power on loopback	Bypass ULP power on loopback	ULP power on loopback	Bypass LP power on loopback	LP power on loopback
2'b00	LP CD dataout		ULP RX dataout		LP RX dataout	

- First row (if testdin[7] == 1'b1)

  Set 1: loopback
- Second row (if testdin[7] == 1'b0)
- Bits 7...6: Reserved
- Bits 5...4: LP CD dataout

  Data coming out of the two single-ended low power contention detectors
- Bits 3....2: ULP RX dataout

  Data coming out of the two single-ended low power receivers used to detect that TX has left ultra low power state
- Bits 1...0: LP RX dataout

  Data coming out of the two single-ended low power receivers when in low power mode

8.6.35 LP TX Control of Lane 0

Test Code: 0x42

This test mode allows the control over the low power single-ended drivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 8-75 Test Data

w-2'b00	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Reserved	Bypass LP TX enable pull down	LP TX enable pull down	Bypass LP TX enable	LP TX enable	Bypass LP TX power on	LP TX power on

- Bit 7…6: Reserved
- Bit 5: Bypass LP TX enable pull down
  - 0 – LP TX enable pull down is controlled by internal FSM
  - 1 – LP TX enable pull down is controlled by test interface
- Bit 4: LP TX enable pull down
  - 0 – Pull down functionality is turned off
  - 1 – A LP-00 state is forced at the output of the low power drivers
- Bit 3: Bypass LP TX enable
  - 0 – LP TX enable is controlled by internal FSM
  - 1 – LP TX enable is controlled by test interface
- Bit 2: LP TX enable
  - 0 – Driver will not transmit incoming data
  - 1 – Driver will transmit incoming data
- Bit 1: Bypass LP TX power on
  - 0 – LP TX is powered off
  - 1 – LP TX is powered on
- Bit 0: LP TX power on
  - 0 – LP TX is powered off
  - 1 – LP TX is powered on

Testdout:

Table 8-76 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00	Bypass LP TX enable pull down loopback	LP TX enable pull down loopback	Bypass LP TX enable loopback	LP TX enable loopback	Bypass LP TX power on loopback	LP TX power on loopback

8.6.36 LP TX control of lane 0

Test Code: 0x43

This test mode allows the control over the low power single-ended drivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 8-77 Test Data

w-5'b00000	w-1'b0	w-2'b00
Reserved	Bypass LP TX driver datain	LP TX driver datain

- Bit 7…3: Reserved
- Bit 2: Bypass LP TX driver datain
  - 0 – Inputs of LP TX driver are controlled by internal FSM
  - 1 – Inputs of LP TX driver are controlled by test interface
- Bit 0...1: LP TX driver datain

  Inputs of LP TX driver

Testdout:

Table 8-78 Testdout

r-5'b00000	r-1'b0	r-2'b00
5'b00000	Bypass LP TX driver datain loopback	LP TX driver datain loopback

8.6.37 HS RX Control of Lane 0

Test Code: 0x44

This test mode allows the control over the high speed differential receiver of the data lane 0 by overriding the control signals sent by the FSM.

Test Data:

Table 8-79 Test Data

w-2'b00	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 0	Bypass HS RX termination enable	HS RX termination enable	Bypass HS RX offset calibration enable	HS RX offset calibration enable	Bypass HS RX power on	HS RX power on
Set 1	Bypass HS RX offset compensation setting	HS RX offset compensation setting				
Set 2	HS operating frequency range selection					Bypass HS -RX settle filter loopback

- Bits 7...6: Programmability selector
  - 10 – Set 0 is programmed
  - 11 – Set 1 is programmed
  - 0x – Set 2 is programmed

Set 0:

- Bit 5: Bypass HS RX terminations enable.
  - 1 – HS RX terminations enable is controlled by test interface
  - 0 – HS RX terminations enable is controlled by internal FSM
- Bit 4: HS RX terminations enable.
  - 0 – Termination not enabled
  - 1 – Termination enabled
- Bit 3: Bypass HS RX calibration enable
  - 1 – HS RX calibration enable is controlled by test interface
  - 0 – HS RX calibration enable is controlled by internal FSM
- Bit 2: HS RX calibration enable
  - 1 – HS RX calibration enabled.
  - 0 – HS RX calibration not enabled.

- Bit 1: Bypass HS RX power on
  - 1 – HS RX powered on is controlled by test interface
  - 0 – HS RX powered on is controlled by internal FSM
- Bit 0: HS RX power on
  - 0 – HS RX powered off
  - 1 – HS RX powered on

Set 1:

- Bit 5: Bypass HS-RX offset compensation setting
- Bits 4...0: HS-RX offset compensation setting

Set 2:

- Bits 6...1: HS frequency range selection
- Bit 0: Bypass HS settle filter

Testdout:

Table 8-80 Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00		Bypass HS RX termination enable loopback	HS RX termination enable loopback	Bypass HS RX offset calibration enable loopback	HS RX offset calibration enable loopback	Bypass HS RX power on loopback	HS RX power on loopback
2'b00		Bypass HS RX offset compensation setting loopback	HS RX offset compensation setting loopback				
1'b0	HS operating frequency range selection loopback						Bypass HS -RX settle filter loopback

- First row (if testdin[7:6] == 2'b10)
- Second row (if testdin[7:6] == 2'b11)
- Third row (if testdin[7:6] == 2'b0x)

8.6.38 DATAP/DATAN swap for lane 0

Test Code: 0x45

This test mode allows the correct behavior of data lane 0 in case a DATAP/DATAN swap is required.

Test Data:

Table 8-81 Test Data

w-1'b0	w-6'b000100	w-1'b0
Bypass HS RX settle data lane	HS RX settle data lane	Polarity change

- Bits 7: Bypass High Speed Receiver settle data
  - 0 – Internal high speed receiver settle data is controlled by internal FSM
  - 1 - Internal high speed receiver settle data is controlled by test interface
- Bits 6...1: High Speed Receiver settle data
- Bit 0: Polarity change
  - 0 – Two PHYS with DATAP/DATAN ports connected to DATAP/DATAN respectively
  - 1 – Two PHYS with DATAP/DATAN ports connected to DATAN/DATAP respectively

Testdout:

Table 8-82 Testdout

w-1'b0	w-6'b000100	r-1'b0
Bypass HS RX settle data lane loopback	HS RX settle data lane loopback	Polarity change loopback

8.6.39 HS RX Lane 0 Outputs and Calibration Errors Observability

Test Code: 0x46

This test mode allows the observability of some outputs of the calibration machine and HS-RX of lane 0.

Testdout:

Table 8-83 Testdout

r-1'b0	**r-1'b0**	**r-1'b0**	**r-1'b0**	**r-4'b0000**
3'b000			HS RX offset compensation setting	
HS RX asynchronous output		HS RX synchronous output		HS RX calibration errors

- First row (if testdin[7] == 1'b0)
- Second row (if testdin[7] == 1'b1)
- Bits 7...6: HS RX asynchronous output
  Asynchronous output of HS RX received in the differential pair
- Bits 5...4: HS RX synchronous output
  Synchronous output of HS RX (clock from clock lane used to sample)
- Bits 3...0: HS RX calibration errors flags

8.6.40 Bias Power on Control of Lane 1

Test Code: 0x50

Test Data:

Table 8-84 Test Data

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Bypass HS TX Data in	HS TX Data in	Bypass HS TX enable	HS TX enable	Bypass HS TX Power on	HS TX power on	Bypass Bias power on	Bias power on

- Bit 7: Bypass High Speed Driver Data
  - 0 – Internal high speed driver data is controlled by internal FSM
  - 1 – Internal high speed driver data is controlled by test interface
- Bit 6: High Speed Driver Data
  - 0 – Internal high speed driver transmits a low level voltage signal 0
  - 1 – Internal high speed driver transmits a high level voltage signal 1
- Bit 5: Bypass High Speed Driver enable
  - 0 – Internal high speed driver enable is controlled by internal FSM
  - 1 – Internal high speed driver enable is controlled by test interface
- Bit 4: High Speed Driver enable
  - 0 – Internal high speed driver is disabled
  - 1 – Internal high speed driver is enabled
- Bit 3: Bypass High Speed Driver power on
  - 0 – Internal high speed driver power on is controlled by internal FSM
  - 1 – Internal high speed driver power on is controlled by test interface
- Bit 2: High Speed Driver power on
  - 0 – Internal high speed driver is powered off
  - 1 – Internal high speed driver is powered off
- Bit 1: Bypass clock lane bias block power on
  - 0 – Internal biasing block is controlled by internal FSM
  - 1 – Internal biasing block is controlled by test interface
- Bit 0: Clock lane bias block power on
  - 0 – Internal biasing block is powered off
  - 1 – Internal biasing block is powered on

TestDout:

Table 8-85 Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
Bypass HS TX Data in loopback	HS TX Data in loopback	Bypass HS TX enable loopback	HS TX enable loopback	Bypass HS TX Power on loopback	HS TX power on loopback	Bypass Bias power on loopback	Bias power on loopback

8.6.41 LP RX Control of Lane 1

Test Code: 0x51

This test mode allows the control over the low power single-ended receivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 8-86 Test Data

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 1	Reserved	Bypass LP CD power on	LP CD power on	Bypass ULP power on	ULP power on	Bypass LP power on	LP power on

- Bit 7: Programmability selector
  - 0 – Does not program anything
  - 1 – Programs 'Set 1' registers
- Bit 6: Reserved
  - 0 – Signals controlled by internal FSM
  - 1 – LP RX controlled by test interface
- Bit 5: Bypass LP CD power on
  - 0 – LP CD power on is controlled by internal FSM
  - 1 – LP CD power on is controlled by test interface
- Bit 4: LP CD power on
  - 0 – LP CD is powered off
  - 1 – LP CD is powered on
- Bit 3: Bypass ULP RX power on
  - 0 – ULP RX power on is controlled by internal FSM
  - 1 – ULP RX power on is controlled by test interface
- Bit 2: ULP RX power on
  - 0 – ULP RX is powered off
  - 1 – ULP RX is powered on
- Bit 1: Bypass LP RX power on
  - 0 – LP RX power on is controlled by internal FSM
  - 1 – LP RX power on is controlled by test interface
- Bit 0: LP RX power on
  - 0 – LP RX is powered off
  - 1 – LP RX is powered on

Testdout:

Table 8-87 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00	Bypass LP CD power on loopback	LP CD power on loopback	Bypass ULP power on loopback	ULP power on loopback	Bypass LP power on loopback	LP power on loopback
2'b00	LP CD dataout		ULP RX dataout		LP RX dataout	

- First row (if testdin[7] == 1'b1)

  Set 1 loopback
- Second row (if testdin[7] == 1'b0)
- Bits 7...6: Reserved
- Bits 5...4: LP CD dataout

  Data coming out of the two single-ended low power contention detectors
- Bits 3....2: ULP RX dataout

  Data coming out of the two single-ended low power receivers used to detect that TX has left ultra low power state
- Bits 1...0: LP RX dataout

  Data coming out of the two single-ended low power receivers when in low power mode

8.6.42 LP TX Control of Lane 1

Test Code: 0x52

This test mode allows the control over the low power single-ended drivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 8-88 Test Data

w-2'b00	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Reserved	Bypass LP TX enable pull down	LP TX enable pull down	Bypass LP TX enable	LP TX enable	Bypass LP TX power on	LP TX power on

- Bit 7…6: Reserved
- Bit 5: Bypass LP TX enable pull down
  - 0 – LP TX enable pull down is controlled by internal FSM
  - 1 – LP TX enable pull down is controlled by test interface
- Bit 4: LP TX enable pull down
  - 0 – Pull down functionality is turned off
  - 1 – A LP-00 state is forced at the output of the low power drivers
- Bit 3: Bypass LP TX enable
  - 0 – LP TX enable is controlled by internal FSM
  - 1 – LP TX enable is controlled by test interface
- Bit 2: LP TX enable
  - 0 – Driver will not transmit incoming data
  - 1 – Driver will transmit incoming data
- Bit 1: Bypass LP TX power on
  - 0 – LP TX is powered off
  - 1 – LP TX is powered on
- Bit 0: LP TX power on
  - 0 – LP TX is powered off
  - 1 – LP TX is powered on

Testdout:

Table 8-89 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00	Bypass LP TX enable pull down loopback	LP TX enable pull down loopback	Bypass LP TX enable loopback	LP TX enable loopback	Bypass LP TX power on loopback	LP TX power on loopback

8.6.43 LP TX Control of Lane 1

Test Code: 0x53

This test mode allows the control over the low power single-ended drivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 8-90 Test Data

w-5'b00000	w-1'b0	w-2'b00
Reserved	Bypass LP TX driver datain	LP TX driver datain

- Bit 7…3: Reserved
- Bit 2: Bypass LP TX driver datain
  - 0 – Inputs of LP TX driver are controlled by internal FSM
  - 1 – Inputs of LP TX driver are controlled by test interface
- Bits 1...0: LP TX driver datain

  Inputs of LP TX driver

Testdout:

Table 8-91 Testdout

r-5'b00000	r-1'b0	r-2'b00
5'b00000	Bypass LP TX driver datain loopback	LP TX driver datain loopback

8.6.44 HS RX Control of Lane 1

Test Code: 0x54

This test mode allows the control over the high speed differential receiver of the data lane 1 by overriding the control signals sent by the FSM.

Test Data:

Table 8-92 Test Data

w-2'b00	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 0	Bypass HS RX termination enable	HS RX termination enable	Bypass HS RX offset calibration enable	HS RX offset calibration enable	Bypass HS RX power on	HS RX power on
Set 1	Bypass HS RX offset compensation setting	HS RX offset compensation setting				
Set 2	Reserved					Bypass HS -RX settle filter

- Bits 7...6: Programmability selector
  - 01 – Nothing is programmed (combination used for observability only)
  - 10 – Set 0 is programmed
  - 11 – Set 1 is programmed
  - 00 – Set 2 is programmed

Set 0:

- Bit 5: Bypass HS RX terminations enable.
  - 1 – HS RX terminations enable is controlled by test interface
  - 0 – HS RX terminations enable is controlled by internal FSM
- Bit 4: HS RX terminations enable
  - 0 – Termination not enabled
  - 1 – Termination enabled
- Bit 3: Bypass HS RX calibration enable
  - 1 – HS RX calibration enable is controlled by test interface
  - 0 – HS RX calibration enable is controlled by internal FSM
- Bit 2: HS RX calibration enable
  - 1 – HS RX calibration enabled
  - 0 – HS RX calibration not enabled

- Bit 1: Bypass HS RX power on
  - 1 – HS RX powered on is controlled by test interface
  - 0 – HS RX powered on is controlled by internal FSM
- Bit 0: HS RX power on
  - 0 – HS RX powered off
  - 1 – HS RX powered on

Set 1:

- Bit 5: Bypass HS-RX offset compensation setting
- Bits 4...0: HS-RX offset compensation setting

Set 2:

- Bits 5...1: Reserved
- Bit 0: Bypass HS-RX settle filter

Testdout:

Table 8-93 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00	Bypass HS RX termination enable loopback	HS RX termination enable loopback	Bypass HS RX offset calibration enable loopback	HS RX offset calibration enable loopback	Bypass HS RX power on loopback	HS RX power on loopback
2'b00	Bypass HS RX offset compensation setting loopback	HS RX offset compensation setting loopback				
7'b00000000						Bypass HS - RX settle filter loopback

- First row (if testdin[7:6] == 2'b10)
- Second row (if testdin[7:6] == 2'b11)
- Third row (if testdin[7:6] == 2'b00)
- Fourth row (if testdin[7:6] == 2'b0x)

8.6.45 DATAP/DATAN Swap for Lane 1

Test Code: 0x55

This test mode allows the correct operation of data lane 1 in case a DATAP/DATAN swap is required.

Test Data:

Table 8-94 Test Data

w-7'b0000000	w-1'b0
7'b0000000	Polarity change

- Bits 7...1: Reserved
- Bit 0: Polarity change
  - 0 – Two PHYS with DATAP/DATAN ports connected to DATAP/DATAN respectively
  - 1 – Two PHYS with DATAP/DATAN ports connected to DATAN/DATAP respectively

Testdout:

Table 8-95 Testdout

r-7'b0000000	r-1'b0
7'b0000000	Polarity change loopback

8.6.46 HS-RX Lane 1 Outputs and Calibration Errors Observability

Test Code: 0x56

This test mode allows the observability of some outputs of the calibration machine and HS-RX of lane 1.

Testdout:

r-1'b0	**r-1'b0**	**r-1'b0**	**r-1'b0**	**r-4'b00000**
3'b000			HS RX offset compensation setting	
HS RX asynchronous output		HS RX synchronous output		HS RX calibration errors

- First row (if testdin[7] == 1'b0)
- Second row (if testdin[7] == 1'b1)
- Bits 7...6: HS RX asynchronous output

  Asynchronous output of HS RX received in the differential pair
- Bits 5...4: HS RX synchronous output

  Synchronous output of HS RX (clock from clock lane used to sample)
- Bits 3....0: HS RX calibration errors flags

8.6.47 HS-TX Clock Lane Request State Time (T_{LP}) Control

Test Code: 0x60

This test mode allows controlling the time that clock lane CLKP/CLKN lines are at HS request state (LP-01) during a HS clock transmission. Refer to the D-PHY specification for more information.

Test Data:

Table 8-96 Test Data

w-1'b0	w-1'b0	w-6'b001011
Reserved	Bypass T_{LP} clock lane counter threshold	T_{LP} clock lane counter threshold

- Bit 7: Reserved
- Bit 6: Bypass T_{LP} clock lane counter threshold default
  - 0 – HS-TX clock lane request state time (T_{LP}) programmed with default values for correspondent hsfreqrange (testcode 8'h44).
  - 1 – HS-TX clock lane request state time (T_{LP}) programmed with bits 5…0.
- Bits 5...0: T_{LP} clock lane counter threshold

Testdout:

Table 8-97 Testdout

r-1'b0	r-1'b0	r-6'b001011
1'b0	Bypass T_{LP} clock lane counter threshold default loopback	T_{LP} clock lane counter threshold loopback

8.6.48 HS-TX Clock Lane Prepare State Time ($T_{CLK\text{-}prepare}$) Control

Test Code: 0x61

This test mode allows controlling the time that clock lane CLKP/CLKN lines are at state HS prepare state (LP-00) during a HS clock transmission. Refer to the D-PHY specification for more information.

Test Data:

Table 8-98 Test Data

w-1'b0	w-7'b0000110
Bypass $T_{CLK\text{-}prepare}$ counter threshold default	$T_{CLK\text{-}prepare}$ counter threshold

- Bit 7: Bypass $T_{CLK\text{-}prepare}$ counter threshold default
  - 0 – HS-TX clock lane prepare state time ($T_{CLK\text{-}prepare}$) programmed with default values for correspondent hsfreqrange (testcode 8'h44).
  - 1 – HS-TX clock lane prepare state time ($T_{CLK\text{-}prepare}$) programmed with bits 6…0.
- Bits 6...0: $T_{CLK\text{-}prepare}$ counter threshold

Testdout:

Table 8-99 Testdout

r-1'b0	r-7'b0000110
Bypass $T_{CLK\text{-}prepare}$ counter threshold default loopback	$T_{CLK\text{-}prepare}$ counter threshold loopback

8.6.49 HS-TX Clock Lane Go State Time ($T_{CLK\text{-}zero}$) Control

Test Code: 0x62

This test mode allows controlling the time that clock lane CLKP/CLKN lines are at state HS-zero state (HS-0) during a HS clock transmission. Refer to the D-PHY specification for more information.

Test Data:

Table 8-100 Test Data

w-1'b0	w-1'b0	w-6'b001010
Reserved	Bypass $T_{CLK\text{-}Zero}$ counter threshold default	$T_{CLK\text{-}Zero}$ counter threshold

- Bit 7: Reserved
- Bit 6: Bypass $T_{CLK\text{-}Zero}$ counter threshold default
  - 0 – HS-TX clock lane HS-zero state time ($T_{CLK\text{-}Zero}$) programmed with default values for correspondent hsfreqrange (testcode 8'h44).
  - 1 – HS-TX clock lane HS-zero state time ($T_{CLK\text{-}Zero}$) programmed with bits 5…0.
- Bits 5...0: $T_{CLK\text{-}Zero}$ counter threshold

Testdout:

Table 8-101 Testdout

r-1'b0	r-1'b0	r-6'b001010
1'b0	Bypass $T_{CLK\text{-}Zero}$ counter threshold default loopback	$T_{CLK\text{-}Zero}$ counter threshold loopback

8.6.50 HS-TX Clock Lane Trail State Time ($T_{CLK\text{-}trail}$) Control

Test Code: 0x63

This test mode allows controlling the time that clock lane CLKP/CLKN lines are at state HS-trail state (HS-0) during a HS clock transmission. Refer to the D-PHY specification for more information.

Test Data:

Table 8-102 Test Data

w-1'b0	w-7'b0000111
Bypass $T_{CLK\text{-}trail}$ counter threshold default	$T_{CLK\text{-}trail}$ counter threshold

- Bit 7: Bypass $T_{CLK\text{-}prepare}$ counter threshold default
  - 0 – HS-TX clock lane trail state time ($T_{CLK\text{-}trail}$) programmed with default values for correspondent hsfreqrange (testcode 8'h44).
  - 1 – HS-TX clock lane trail state time ($T_{CLK\text{-}trail}$) programmed with bits 6…0.
- Bits 6...0: $T_{CLK\text{-}trail}$ counter threshold

Testdout:

Table 8-103 Testdout

r-1'b0	r-7'b0000111
Bypass $T_{CLK\text{-}trail}$ counter threshold default loopback	$T_{CLK\text{-}trail}$ counter threshold loopback

8.6.51 HS-TX Clock Lane Exit State Time ($T_{HS-exit}$) Control

Test Code: 0x64

This test mode allows controlling the time that clock lane CLKP/CLKN lines are at state HS-exit state (LP-11) after a HS clock transmission. Refer to the D-PHY specification for more information.

Test Data:

Table 8-104 Test Data

w-1'b0	w-1'b0	w-6'b000100
Reserved	Bypass $T_{HS-exit}$ clock lane counter threshold default	$T_{HS-exit}$ clock lane counter threshold

- Bit 7: Reserved
- Bit 6: Bypass $T_{HS-exit}$ counter threshold default
  - 0 – HS-TX clock lane HS-exit state time ($T_{HS-exit}$) programmed with default values for correspondent hsfreqrange (testcode 8'h44).
  - 1 – HS-TX clock lane HS-exit state time ($T_{HS-exit}$) programmed with bits 5…0.
- Bits 5...0: $T_{HS-exit}$ counter threshold

Testdout:

Table 8-105 Testdout

r-1'b0	r-1'b0	r-6'b000100
1'b0	Bypass $T_{HS-exit}$ clock lane counter threshold default loopback	$T_{HS-exit}$ clock lane counter threshold loopback

8.6.52 HS-TX Clock Lane Clock Post Time ($T_{CLK\text{-}post}$) Control

Test Code: 0x65

This test mode allows controlling the time that clock lane keep sending HS-clock after the last associated data lane has transitioned to LP mode. Refer to the D-PHY specification for more information.

Test Data:

Table 8-106 Test Data

w-3'b000	w-1'b0	w-4'b1001
Reserved	Bypass $T_{CLK\text{-}post}$ counter threshold default	$T_{CLK\text{-}post}$ counter threshold

- Bit 7…5: Reserved
- Bit 4: Bypass $T_{CLK\text{-}post}$ counter threshold default
  - 0 – HS-TX clock post state time ($T_{CLK\text{-}post}$) programmed with default values for correspondent hsfreqrange (testcode 8'h44).
  - 1 – HS-TX clock post state time ($T_{CLK\text{-}post}$) programmed with bits 3…0.
- Bits 3...0: $T_{CLK\text{-}post}$ counter threshold

Testdout:

Table 8-107 Testdout

r-3'b000	r-1'b0	r-4'b1001
3'b000	Bypass $T_{CLK\text{-}post}$ clock lane counter threshold default loopback	$T_{CLK\text{-}post}$ clock lane counter threshold loopback

8.6.53 HS-TX Clock Lane Request State Time (T_{LP}) Control

Test Code: 0x70

This test mode allows controlling the time that data lanes DATAP/DATAN lines are at state HS request state (LP-01) during a HS transmission. Refer to the D-PHY specification for more information.

Test Data:

Table 8-108 Test Data

w-1'b0	w-1'b0	w-6'b001011
Reserved	Bypass T_{LP} data lanes counter threshold default	T_{LP} data lanes counter threshold

- Bit 7: Reserved
- Bit 6: Bypass T_{LP} data lanes counter threshold default
  - 0 – HS-TX data lanes request state time (T_{LP}) programmed with default values for correspondent hsfreqrange (testcode 8'h44).
  - 1 – HS-TX data lanes request state time (T_{LP}) programmed with bits 5…0.
- Bits 5...0: T_{LP} data lanes counter threshold

Testdout:

Table 8-109 Testdout

r-1'b0	r-1'b0	r-6'b001011
1'b0	Bypass T_{LP} data lanes counter threshold default loopback	T_{LP} data lanes counter threshold loopback

8.6.54 HS-TX Data Lanes Prepare State Time ($T_{HS\text{-}prepare}$) Control

Test Code: 0x71

This test mode allows controlling the time that data lanes DATAP/DATAN lines are at state HS prepare state (LP-00) during a HS transmission. Refer to the D-PHY specification for more information.

Test Data:

Table 8-110 Test Data

w-1'b0	w-7'b0001010
Bypass $T_{HS\text{-}prepare}$ counter threshold default	$T_{HS\text{-}prepare}$ counter threshold

- Bit 7: Bypass $T_{HS\text{-}prepare}$ counter threshold default
  - 0 – HS-TX data lanes prepare state time ($T_{HS\text{-}prepare}$) programmed with default values for correspondent hsfreqrange (testcode 8'h44).
  - 1 – HS-TX data lanes prepare state time ($T_{HS\text{-}prepare}$) programmed with bits 6…0.
- Bits 6...0: $T_{HS\text{-}prepare}$ counter threshold

Testdout:

Table 8-111 Testdout

r-1'b0	r-7'b0001010
Bypass $T_{HS\text{-}prepare}$ counter threshold default loopback	$T_{HS\text{-}prepare}$ counter threshold loopback

8.6.55 HS-TX Data Lanes Go State Time ($T_{HS-zero}$) Control

Test Code: 0x72

This test mode allows controlling the time that data lanes DATAP/DATAN lines are at state HS-zero state (HS-0) during a HS transmission. Refer to the D-PHY specification for more information.

Test Data:

Table 8-112 Test Data

w-1'b0	w-1'b0	w-6'b000110
Reserved	Bypass $T_{HS-Zero}$ counter threshold default	$T_{HS-Zero}$ counter threshold

- Bit 7: Reserved
- Bit 6: Bypass $T_{CLK-Zero}$ counter threshold default
  - 0 – HS-TX data lanes HS-zero state time ($T_{HS-Zero}$) programmed with default values for correspondent hsfreqrange (testcode 8'h44).
  - 1 – HS-TX data lanes HS-zero state time ($T_{HS-Zero}$) programmed with bits 5…0.
- Bits 5...0: $T_{HS-Zero}$ counter threshold

Testdout:

Table 8-113 Testdout

r-1'b0	r-1'b0	r-6'b000110
1'b0	Bypass $T_{HS-Zero}$ counter threshold default loopback	$T_{HS-Zero}$ counter threshold loopback

8.6.56 HS-TX Data Lanes Go State Time ($T_{HS\text{-}trail}$) Control

Test Code: 0x73

This test mode allows controlling the time that data lanes DATAP/DATAN lines are at state HS-trail state (HS-0) during a HS clock transmission. Refer to the D-PHY specification for more information.

Test Data:

Table 8-114 Test Data

w-1'b0	w-7'b0001110
Bypass $T_{HS\text{-}trail}$ counter threshold default	$T_{HS\text{-}trail}$ counter threshold

- Bit 7: Bypass $T_{HS\text{-}trail}$ counter threshold default
  - 0 – HS-TX data lanes trail state time ($T_{HS\text{-}trail}$) programmed with default values for correspondent hsfreqrange (testcode 8'h44).
  - 1 – HS-TX data lanes trail state time ($T_{HS\text{-}trail}$) programmed with bits 6…0.
- Bits 6...0: $T_{HS\text{-}trail}$ counter threshold

Testdout:

Table 8-115 Testdout

r-1'b0	r-7' b0001110
Bypass $T_{CLK\text{-}trail}$ counter threshold default loopback	$T_{CLK\text{-}trail}$ counter threshold loopback

8.6.57 HS-TX Data Lanes Trail State Time ($T_{HS-exit}$) Control

Test Code: 0x74

This test mode allows controlling the time that data lanes DATAP/DATAN lines are at state HS-exit state (LP-11) after a HS clock transmission. Refer to the D-PHY specification for more information.

Test Data:

Table 8-116 Test Data

w-1'b0	w-1'b0	w-6'b000100
Reserved	Bypass $T_{HS-exit}$ data lanes counter threshold default	$T_{HS-exit}$ data lanes counter threshold

- Bit 7: Reserved
- Bit 6: Bypass $T_{HS-exit}$ counter threshold default
  - 0 – HS-TX data lanes HS-exit state time ($T_{HS-exit}$) programmed with default values for correspondent hsfreqrange (testcode 8'h44).
  - 1 – HS-TX data lanes HS-exit state time ($T_{HS-exit}$) programmed with bits 5…0.
- Bits 5...0: $T_{HS-exit}$ counter threshold

Testdout:

Table 8-117 Testdout

r-1'b0	r-1'b0	r-6'b000100
1'b0	Bypass $T_{HS-exit}$ data lanes counter threshold default loopback	$T_{HS-exit}$ data lanes counter threshold loopback

8.6.58 Bias Power On \Control of Lane 2

Test Code: 0x80

Test Data:

Table 8-118 Test Data

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Bypass HS TX Data in	HS TX Data in	Bypass HS TX enable	HS TX enable	Bypass HS TX power on	HS TX power on	Bypass Bias power on	Bias power on

- Bit 7: Bypass High Speed Driver Data
  - 0 – Internal high speed driver data is controlled by internal FSM
  - 1 – Internal high speed driver data is controlled by test interface
- Bit 6: High Speed Driver Data
  - 0 – Internal high speed driver transmits a low level voltage signal ‘0’
  - 1 – Internal high speed driver transmits a high level voltage signal ‘1’
- Bit 5: Bypass High Speed Driver enable
  - 0 – Internal high speed driver enable is controlled by internal FSM
  - 1 – Internal high speed driver enable is controlled by test interface
- Bit 4: High Speed Driver enable
  - 0 – Internal high speed driver is disabled
  - 1 – Internal high speed driver is enabled
- Bit 3: Bypass High Speed Driver power on
  - 0 – Internal high speed driver power on is controlled by internal FSM
  - 1 – Internal high speed driver power on is controlled by test interface
- Bit 2: High Speed Driver power on
  - 0 – Internal high speed driver is powered off
  - 1 – Internal high speed driver is powered off
- Bit 1: Bypass clock lane bias block power on
  - 0 – Internal biasing block is controlled by internal FSM
  - 1 – Internal biasing block is controlled by test interface
- Bit 0: Clock lane bias block power on
  - 0 – Internal biasing block is powered off
  - 1 – Internal biasing block is powered on

TestDout:

Table 8-119 Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
Bypass HS TX Data in loopback	HS TX Data in loopback	Bypass HS TX enable loopback	HS TX enable loopback	Bypass HS TX power on loopback	HS TX power on loopback	Bypass Bias power on loopback	Bias power on loopback

8.6.59 LP RX Control of Lane 2

Test Code: 0x81

This test mode allows the control over the low power single-ended receivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 8-120 Test Data

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 1	Reserved	Bypass LP CD power on	LP CD power on	Bypass ULP power on	ULP power on	Bypass LP power on	LP power on

- Bit 7: Programmability selector
  - 0 – Does not program anything
  - 1 – Programs 'Set 1' registers
- Bit 6: Reserved
  - 0 – Signals controlled by internal FSM
  - 1 – LP RX controlled by test interface
- Bit 5: Bypass LP CD power on
  - 0 – LP CD power on is controlled by internal FSM
  - 1 – LP CD power on is controlled by test interface
- Bit 4: LP CD power on
  - 0 – LP CD is powered off
  - 1 – LP CD is powered on
- Bit 3: Bypass ULP RX power on
  - 0 – ULP RX power on is controlled by internal FSM
  - 1 – ULP RX power on is controlled by test interface
- Bit 2: ULP RX power on
  - 0 – ULP RX is powered off
  - 1 – ULP RX is powered on
- Bit 1: Bypass LP RX power on
  - 0 – LP RX power on is controlled by internal FSM
  - 1 – LP RX power on is controlled by test interface

- Bit 0: LP RX power on
  - 0 – LP RX is powered off
  - 1 – LP RX is powered on

Testdout:

Table 8-121 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00	Bypass LP CD power on loopback	LP CD power on loopback	Bypass ULP power on loopback	ULP power on loopback	Bypass LP power on loopback	LP power on loopback
2'b00	LP CD dataout		ULP RX dataout		LP RX dataout	

- First row (if testdin[7] == 1'b1)

  Set 1 loopback
- Second row (if testdin[7] == 1'b0)
- Bits 7...6: Reserved
- Bits 5...4: LP CD dataout

  Data coming out of the two single-ended low power contention detectors
- Bits 3...2: ULP RX dataout

  Data coming out of the two single-ended low power receivers used to detect that TX has left ultra low power state
- Bits 1...0: LP RX dataout

  Data coming out of the two single-ended low power receivers when in low power mode

8.6.60 LP TX Control of Lane 2

Test Code: 0x82

This test mode allows the control over the low power single-ended drivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 8-122 Test Data

w-2'b00	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Reserved	Bypass LP TX enable pull down	LP TX enable pull down	Bypass LP TX enable	LP TX enable	Bypass LP TX power on	LP TX power on

- Bit 7…6: Reserved
- Bit 5: Bypass LP TX enable pull down
  - 0 – LP TX enable pull down is controlled by internal FSM
  - 1 – LP TX enable pull down is controlled by test interface
- Bit 4: LP TX enable pull down
  - 0 – Pull down functionality is turned off
  - 1 – A LP-00 state is forced at the output of the low power drivers
- Bit 3: Bypass LP TX enable
  - 0 – LP TX enable is controlled by internal FSM
  - 1 – LP TX enable is controlled by test interface
- Bit 2: LP TX enable
  - 0 – Driver will not transmit incoming data
  - 1 – Driver will transmit incoming data
- Bit 1: Bypass LP TX power on
  - 0 – LP TX is powered off
  - 1 – LP TX is powered on
- Bit 0: LP TX power on
  - 0 – LP TX is powered off
  - 1 – LP TX is powered on

Testdout:

Table 8-123 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2’b00	Bypass LP TX enable pull down loopback	LP TX enable pull down loopback	Bypass LP TX enable loopback	LP TX enable loopback	Bypass LP TX power on loopback	LP TX power on loopback

8.6.61 LP TX Control of Lane 2

Test Code: 0x83

This test mode allows the control over the low power single-ended drivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 8-124 Test Data

w-5'b00000	w-1'b0	w-2'b00
Reserved	Bypass LP TX driver datain	LP TX driver datain

- Bit 7…3: Reserved
- Bit 2: Bypass LP TX driver datain
  - 0 – Inputs of LP TX driver are controlled by internal FSM
  - 1 – Inputs of LP TX driver are controlled by test interface
- Bit 0...1: LP TX driver datain

Inputs of LP TX driver

Testdout:

Table 8-125 Testdout

r-5'b00000	r-1'b0	r-2'b00
5'b00000	Bypass LP TX driver datain loopback	LP TX driver datain loopback

8.6.62 HS RX Control of Lane 2

Test Code: 0x84

This test mode allows the control over the high speed differential receiver of the data lane 2 by overriding the control signals sent by the FSM.

Test Data:

Table 8-126 Test Data

w-2'b00	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 0	Bypass HS RX termination enable	HS RX termination enable	Bypass HS RX offset calibration enable	HS RX offset calibration enable	Bypass HS RX power on	HS RX power on
Set 1	Bypass HS RX offset compensation setting	HS RX offset compensation setting				
Set 2	Reserved					Bypass HS -RX settle filter

- Bits 7...6 Programmability selector
  - 01 – Nothing is programmed (combination used for observability only)
  - 10 – Set 0 is programmed
  - 11 – Set 1 is programmed
  - 00 – Set 2 is programmed

Set 0:

- Bit 5: Bypass HS RX terminations enable
  - 1 – HS RX terminations enable is controlled by test interface
  - 0 – HS RX terminations enable is controlled by internal FSM
- Bit 4: HS RX terminations enable
  - 0 – Termination not enabled
  - 1 – Termination enabled
- Bit 3: Bypass HS RX calibration enable
  - 1 – HS RX calibration enable is controlled by test interface
  - 0 – HS RX calibration enable is controlled by internal FSM
- Bit 2: HS RX calibration enable
  - 1 – HS RX calibration enabled.
  - 0 – HS RX calibration not enabled.

- Bit 1: Bypass HS RX power on
  - 1 – HS RX powered on is controlled by test interface
  - 0 – HS RX powered on is controlled by internal FSM
- Bit 0: HS RX power on
  - 0 – HS RX powered off
  - 1 – HS RX powered on

Set 1:

- Bit 5: Bypass HS-RX offset compensation setting
- Bits 4...0: HS-RX offset compensation setting

Set 2:

- Bits 5...1: Reserved
- Bit 0: Bypass HS-RX settle filter

Testdout:

Table 8-127 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00	Bypass HS RX termination enable loopback	HS RX termination enable loopback	Bypass HS RX offset calibration enable loopback	HS RX offset calibration enable loopback	Bypass HS RX power on loopback	HS RX power on loopback
2'b00	Bypass HS RX offset compensation setting loopback	HS RX offset compensation setting loopback				
7'b00000000						Bypass HS - RX settle filter loopback

- First row (if testdin[7:6] == 2'b10)
- Second row (if testdin[7:6] == 2'b11)
- Third row (if testdin[7:6] == 2'b00)
- Fourth row (if testdin[7:6] == 2'b0x)

8.6.63 DATAP/DATAN Swap for Lane 2

Test Code: 0x85

This test mode allows the correct behavior of data lane 2 in case a DATAP/DATAN swap is required.

Test Data:

Table 8-128 Test Data

w-7'b0000000	w-1'b0
Reserved	Polarity change

- Bits 7...1: Reserved
- Bit 0: Polarity change
  - 0 – Two PHYS with DATAP/DATAN ports connected to DATAP/DATAN respectively
  - 1 – Two PHYS with DATAP/DATAN ports connected to DATAN/DATAP respectively

Testdout:

Table 8-129 Testdout

r-7'b0000000	r-1'b0
Reserved	Polarity change loopback

8.6.64 HS RX Lane 2 Outputs and Calibration Errors Observability

Test Code: 0x86

This test mode allows the observability of some outputs of the calibration machine and HS-RX of lane 2.

Testdout:

Table 8-130 Testdout

r-1'b0	**r-1'b0**	**r-1'b0**	**r-1'b0**	**r-4'b00000**
3'b000			HS RX offset compensation setting	
HS RX asynchronous output		HS RX synchronous output		HS RX calibration errors

- First row (if testdin[7] == 1'b0)
- Second row (if testdin[7] == 1'b1)
- Bits 7...6: HS RX asynchronous output

  Asynchronous output of HS RX received in the differential pair
- Bits 5...4: HS RX synchronous output

  Synchronous output of HS RX (clock from clock lane used to sample)
- Bits 3...0: HS RX calibration errors flags

8.6.65 Bias Power on Control of Lane 3

Test Code: 0x90

Test Data:

Table 8-131 Test Data

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Bypass HS TX Data in	HS TX Data in	Bypass HS TX enable	HS TX enable	Bypass HS TX power on	HS TX power on	Bypass Bias power on	Bias power on

- Bit 7: Bypass High Speed Driver Data
  - 0 – Internal high speed driver data is controlled by internal FSM
  - 1 – Internal high speed driver data is controlled by test interface
- Bit 6: High Speed Driver Data
  - 0 – Internal high speed driver transmits a low level voltage signal 0
  - 1 – Internal high speed driver transmits a high level voltage signal 1
- Bit 5: Bypass High Speed Driver enable
  - 0 – Internal high speed driver enable is controlled by internal FSM
  - 1 – Internal high speed driver enable is controlled by test interface
- Bit 4: High Speed Driver enable
  - 0 – Internal high speed driver is disabled
  - 1 – Internal high speed driver is enabled
- Bit 3: Bypass High Speed Driver power on
  - 0 – Internal high speed driver power on is controlled by internal FSM
  - 1 – Internal high speed driver power on is controlled by test interface
- Bit 2: High Speed Driver power on
  - 0 – Internal high speed driver is powered off
  - 1 – Internal high speed driver is powered off
- Bit 1: Bypass clock lane bias block power on
  - 0 – Internal biasing block is controlled by internal FSM
  - 1 – Internal biasing block is controlled by test interface
- Bit 0: Clock lane bias block power on
  - 0 – Internal biasing block is powered off
  - 1 – Internal biasing block is powered on

TestDout:

Table 8-132 Testdout

r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
Bypass HS TX Data in loopback	HS TX Data in loopback	Bypass HS TX enable loopback	HS TX enable loopback	Bypass HS TX power on loopback	HS TX power on loopback	Bypass Bias power on loopback	Bias power on loopback

8.6.66 LP RX Control of Lane 3

Test Code: 0x91

This test mode allows the control over the low power single-ended receivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 8-133 Test Data

w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 1	Reserved	Bypass LP CD power on	LP CD power on	Bypass ULP power on	ULP power on	Bypass LP power on	LP power on

- Bit 7: Programmability selector
  - 0 – Does not program anything
  - 1 – Programs 'Set 1' registers
- Bit 6: Reserved
  - 0 – Signals controlled by internal FSM
  - 1 – LP RX controlled by test interface
- Bit 5: Bypass LP CD power on
  - 0 – LP CD power on is controlled by internal FSM
  - 1 – LP CD power on is controlled by test interface
- Bit 4: LP CD power on
  - 0 – LP CD is powered off
  - 1 – LP CD is powered on
- Bit 3: Bypass ULP RX power on
  - 0 – ULP RX power on is controlled by internal FSM
  - 1 – ULP RX power on is controlled by test interface
- Bit 2: ULP RX power on
  - 0 – ULP RX is powered off
  - 1 – ULP RX is powered on
- Bit 1: Bypass LP RX power on
  - 0 – LP RX power on is controlled by internal FSM
  - 1 – LP RX power on is controlled by test interface

- Bit 0: LP RX power on
  - 0 – LP RX is powered off
  - 1 – LP RX is powered on

Testdout:

Table 8-134 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00	Bypass LP CD power on loopback	LP CD power on loopback	Bypass ULP power on loopback	ULP power on loopback	Bypass LP power on loopback	LP power on loopback
2'b00	LP CD dataout		ULP RX dataout		LP RX dataout	

- First row (if testdin[7] == 1'b1)

  Set 1 loopback
- Second row (if testdin[7] == 1'b0)
- Bits 7...6: Reserved
- Bits 5...4: LP CD dataout

  Data coming out of the two single-ended low power contention detectors
- Bits 3...2: ULP RX dataout

  Data coming out of the two single-ended low power receivers used to detect that TX has left ultra low power state
- Bits 1...0: LP RX dataout

  Data coming out of the two single-ended low power receivers when in low power mode

8.6.67 LP TX Control of Lane 3

Test Code: 0x92

This test mode allows the control over the low power single-ended drivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 8-135 Test Data

w-2'b00	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Reserved	Bypass LP TX enable pull down	LP TX enable pull down	Bypass LP TX enable	LP TX enable	Bypass LP TX power on	LP TX power on

- Bit 7…6: Reserved
- Bit 5: Bypass LP TX enable pull down
  - 0 – LP TX enable pull down is controlled by internal FSM
  - 1 – LP TX enable pull down is controlled by test interface
- Bit 4: LP TX enable pull down
  - 0 – Pull down functionality is turned off
  - 1 – A LP-00 state is forced at the output of the low power drivers
- Bit 3: Bypass LP TX enable
  - 0 – LP TX enable is controlled by internal FSM
  - 1 – LP TX enable is controlled by test interface
- Bit 2: LP TX enable
  - 0 – Driver does not transmit incoming data
  - 1 – Driver does transmit incoming data
- Bit 1: Bypass LP TX power on
  - 0 – LP TX is powered off
  - 1 – LP TX is powered on
- Bit 0: LP TX power on
  - 0 – LP TX is powered off
  - 1 – LP TX is powered on

Testdout:

Table 8-136 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00	Bypass LP TX enable pull down loopback	LP TX enable pull down loopback	Bypass LP TX enable loopback	LP TX enable loopback	Bypass LP TX power on loopback	LP TX power on loopback

8.6.68 LP TX Control of Lane 3

Test Code: 0x93

This test mode allows the control over the low power single-ended drivers of the clock lane by overriding the control signals sent by the FSM.

Test Data:

Table 8-137 Test Data

w-5'b00000	w-1'b0	w-2'b00
Reserved	Bypass LP TX driver datain	LP TX driver datain

- Bit 7…3: Reserved
- Bit 2: Bypass LP TX driver datain
  - 0 – Inputs of LP TX driver are controlled by internal FSM
  - 1 – Inputs of LP TX driver are controlled by test interface
- Bit 0...1: LP TX driver datain

  Inputs of LP TX driver

Testdout:

Table 8-138 Testdout

r-5'b00000	r-1'b0	r-2'b00
5'b00000	Bypass LP TX driver datain loopback	LP TX driver datain loopback

8.6.69 HS RX Control of Lane 3

Test Code: 0x94

This test mode allows the control over the high speed differential receiver of the data lane 3 by overriding the control signals sent by the FSM.

Test Data:

Table 8-139 Test Data

w-2'b00	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0	w-1'b0
Set 0	Bypass HS RX termination enable	HS RX termination enable	Bypass HS RX offset calibration enable	HS RX offset calibration enable	Bypass HS RX power on	HS RX power on
Set 1	Bypass HS RX offset compensation setting	HS RX offset compensation setting				
Set 2	Reserved					Bypass HS - RX settle filter

- Bits 7...6: Programmability selector
  - 01 – Nothing is programmed (combination used for observability only)
  - 10 – Set 0 is programmed
  - 11 – Set 1 is programmed
  - 00 – Set 2 is programmed

Set 0:

- Bit 5: Bypass HS RX terminations enable.
  - 1 – HS RX terminations enable is controlled by test interface
  - 0 – HS RX terminations enable is controlled by internal FSM
- Bit 4: HS RX terminations enable.
  - 0 – Termination not enabled
  - 1 – Termination enabled
- Bit 3: Bypass HS RX calibration enable
  - 1 – HS RX calibration enable is controlled by test interface
  - 0 – HS RX calibration enable is controlled by internal FSM

- Bit 2: HS RX calibration enable
  - 1 – HS RX calibration enabled.
  - 0 – HS RX calibration not enabled.
- Bit 1: Bypass HS RX power on
  - 1 – HS RX powered on is controlled by test interface
  - 0 – HS RX powered on is controlled by internal FSM
- Bit 0: HS RX power on
  - 0 – HS RX powered off
  - 1 – HS RX powered on

Set 1:

- Bit 5: Bypass HS-RX offset compensation setting
- Bits 4...0: HS-RX offset compensation setting

Set 2:

- Bits 5...1: Reserved
- Bit: Bypass HS-RX settle filter

Testdout:

Table 8-140 Testdout

r-2'b00	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0	r-1'b0
2'b00	Bypass HS RX termination enable loopback	HS RX termination enable loopback	Bypass HS RX offset calibration enable loopback	HS RX offset calibration enable loopback	Bypass HS RX power on loopback	HS RX power on loopback
2'b00	Bypass HS RX offset compensation setting loopback	HS RX offset compensation setting loopback				
7'b00000000						Bypass HS - RX settle filter loopback

- First row (if testdin[7:6] == 2'b10)
- Second row (if testdin[7:6] == 2'b11)
- Third row (if testdin[7:6] == 2'b00)
- Fourth row (if testdin[7:6] == 2'b0x)

8.6.70 DATAP/DATAN Swap for Lane 3

Test Code: 0x95

This test mode allows the correct behavior of data lane 3 in case a DATAP/DATAN swap is required.

Test Data:

Table 8-141 Test Data

w-7'b0000000	w-1'b0
Reserved	Polarity change

- Bits 7...1: Reserved
- Bit 0: Polarity change
  - 0 – Two PHYS with DATAP/DATAN ports connected to DATAP/DATAN respectively
  - 1 – Two PHYS with DATAP/DATAN ports connected to DATAN/DATAP respectively

Testdout:

Table 8-142 Testdout

r-7'b0000000	r-1'b0
Reserved	Polarity change loopback

8.6.71 HS RX Lane 3 Outputs and Calibration Errors Observability

Test Code: 0x96

This test mode allows the observability of some outputs of the calibration machine and HS-RX of lane 3.

Testdout:

Table 8-143 Testdout

r-1'b0	**r-1'b0**	**r-1'b0**	**r-1'b0**	**r-4'b00000**
3'b000			HS RX offset compensation setting	
HS RX asynchronous output		HS RX synchronous output		HS RX calibration errors

- First row (if testdin[7] == 1'b0)
- Second row (if testdin[7] == 1'b1)
- Bits 7...6: HS RX asynchronous output

  Asynchronous output of HS RX received in the differential pair.
- Bits 5...4: HS RX synchronous output

  Synchronous output of HS RX (clock from clock lane used to sample).
- Bits 3...0: HS RX calibration errors flags

9 Assembly Guidelines

This chapter includes general guidelines regarding the IP integration.

9.1 Cell Placement

It is recommended to place this PHY core away from any other block that may generate noise, which could lead to the degradation of the cell performance. The best location will be on a corner of the ASIC, close to its dedicated input and power supply pads.

The PHY has already N-well "moats" but if the PHY core is close to a noise source an extra 10 um N-well moat tied to AVDD should be added.

No additional routing can be done within the PHY core area.

9.2 Cell Routing

9.2.1 Data/Clock Signals (DATAP*/DATAN* and CLKP/CLKN)

The connection of the SLVS data and clock signals is very critical and must be done carefully. To obtain the maximum performance it is highly recommended:

- The analog I/O pads must be placed near the DATAP/DATAN & CLKP/CLKN pins.
- The connections must be as short as possible (< 0.5 Ω) and at least with the pin width.
- Capacitance of these connections should be as lower as possible.
- Complementary **P* and **N* routing must be matched, up to and including the bonding wire connections and PCB traces.

The analog I/O pads used for DATAP/DATAN & CLKP/CLKN signals must have the following characteristics:

- Serial resistance as low as possible (< 0.5 Ω).
- Must include Primary ESD structures (secondary ESD protections are inside the PHY).

Total capacitance of analog I/O pad + connection must be lower than 5 pF.

These requirements apply to all lanes, both clock and data, independently of the system application.

9.2.2 Power Supplies

The PHY core is designed with separate power supplies to reduce noise coupling between clean and noisiest supplies.

The recommendations to obtain the maximum performance are provided in the following sections.

9.2.2.1 Analog 2.5 V Supply (AVDD/AVDDREF)

The recommendations to obtain the maximum performance are:

- Like REXT/REXTV, the two analog power supply pins (AVDD and AVDDREF) should be connected separately from the IP and tied together only at the pad connection.
- Additionally, the connection between each AVDD/AVDDREF pin pair and each I/O power pad should be as short as possible and the resistance must be lower than 0.5 Ω to reduce IR drop.
- The power supplies should be connected with the same nominal pad through wide interconnections (at least pin width). The width of the route should be calculated for a current of 35 mA.
- All supply pins must be routed separately from the IP to the I/O power pads, they should be only connected together as close as possible to the respective I/O pad.
- To reduce supply noise and promote the better current distribution, four I/O power pads should be used for AVDD/AVDDREF in mipi_4_bidir_dphy.
- The maximum ripple noise (peak-peak) amplitude is:
  - 100 mV for the frequencies > 1.2 MHz
  - 20 mV for the frequencies < 1.2 MHz

9.2.2.2 Analog Ground (AGND/AGNDREF)

Analog ground connections follow identical requirements as analog voltage supply connections, including the requirement of three I/O pads for AGND/AGNDREF connections for standalone mipi_4_bidir_dphy or four if mipi_pll_dphy is integrated as well. This will force the use of three/four bonding wires and thus reduce the overall bonding inductance.

9.2.2.3 Digital Supply (VDD/VSS)

- Digital supply (VDD and VSS) can and should be connected to digital core power supplies in order to reduce the overall power supply pin count.
- DWC IP is prepared to work with the digital voltage defined in the Databook. These values are valid at IP level (not package level). Customer must take in account the voltage drop from the voltage source until the IP connections.
- Adequate decoupling should be included to accommodate current up to 40 mA. This overhead is designed to accommodate loopback (simultaneous TX-RX) test modes.
- The maximum ripple noise amplitude is 50 mV (peak-peak).

9.2.3 External Reference (REXT and REXTV)

The connection of the external reference should be:

- Made through short and shielded lines
- The resistance of the line should be as lower as possible (< 20 Ω)
- Each pin must be connected in all metal layers with the respective track
- Each track must have the pin width (at least)

REXT and REXTV pins should be routed separately from the IP to the I/O pad, they should be only connected together as close as possible to the I/O pad.

This pad should be placed away from any other noisy place namely the data pins. It is highly recommended to be placed in between two grounded pads.

The analog I/O pad does not have any special requirement. Sometimes, the analog I/O pad includes a serial resistor; this value must be taken into account for the external resistor calculation.

9.3 Package Requirements

The following parameters should be taken in account when selecting the Package Type:

- R < 300 mΩ
- L < 5.5 nH
- C < 0.8 pF

Keeping these RLC parasitic values small, ensures optimum operation of the IP based on improved receiving end timing margins.

9.4 ESD/Latch-Up

All input/output elements connecting directly to pads, are designed according to the rules for ESD and Latch-Up protection.

The IP is delivered with internal secondary ESD protections that go from simple ESD clamps to cross power domain protections.

Primary ESD protections should be present on the IOs and/or externally to the chip to ensure maximum ESD robustness.

9.5 Additional External Components

The REXT/REXTV pins should be connected to an external resistor that is used to generate internal reference currents critical to the normal operation of the IP. This connection should be made as short as possible on the PCB board to minimize additional series resistance.

A 6.04 K E96 resistor should be used to connect this pin to AGND or the board ground plane.

9.6 Macro Integration

9.6.1 Attachable PLL

This bidirectional D-PHY IP may be used for Master or Slave applications where the last does not require a PLL. In order to allow for maximum flexibility and higher area savings, the PHY is delivered with an attachable PLL that may be integrated or not with the core PHY depending on the target applications.

Table 9-1 Signal Interface Between mipi_pll_dphy and mipi_4_bidir_dphy

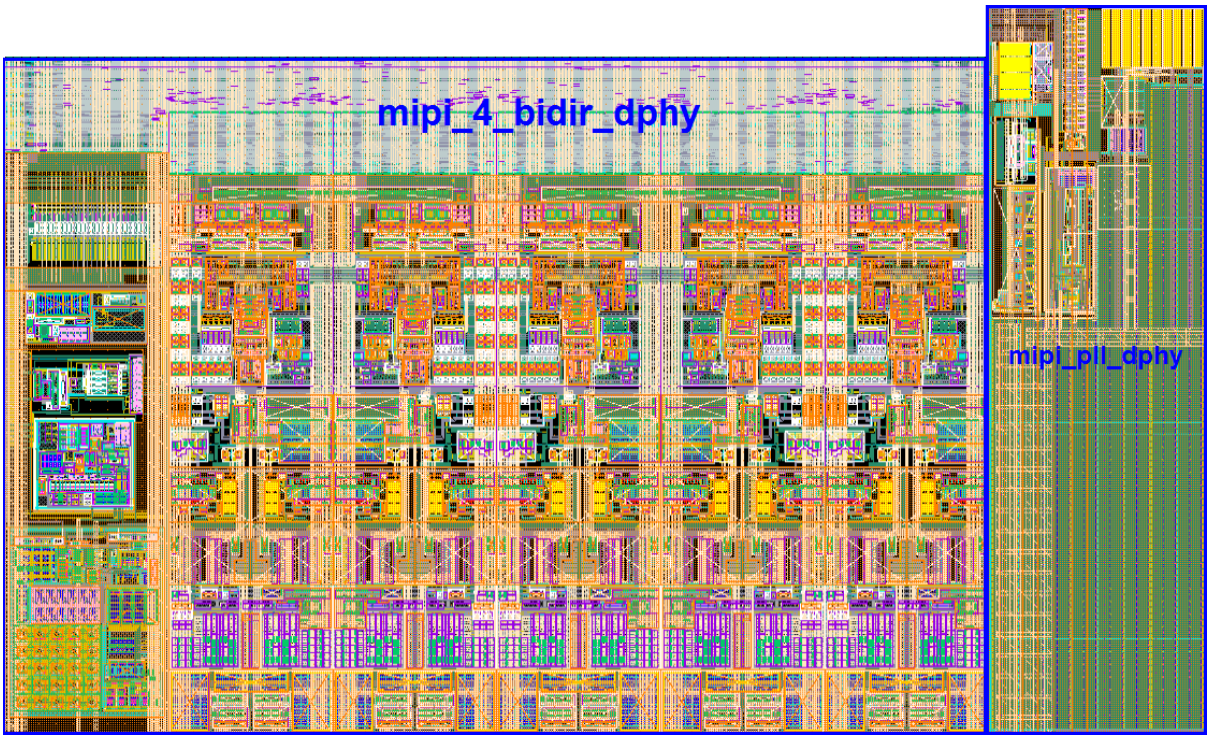
Core PHY			D-PHY Master (With PLL)	D-PHY Slave (Without PLL)
mipi_4_bidir_dphy Signal	**I/O**		**mipi_pll_dphy Signal**	**Signal**
PLL_LOCK	I	Input	lock	Tie Low (VSS)
TESTLOCK	I	Input	testlock	Tie Low (VSS)
TXDDRCLKHSI_IN	I	Input	clkout1	Tie Low (VSS)
TXDDRCLKHSQ_IN	I	Input	clkout1n	Tie Low (VSS)
CLKOUT2	I	Input	clkout2	Tie Low (VSS)
PLLIBIAS	O	Output	ipll	Floating
REFCLK_FT	O	Output	clkin	Floating
ONPLL	O	Output	onpll	Floating
RSTZPLL	O	Output	rstz	Floating
N[7:0]	O	Output	n[7:0]	Floating
M[9:0]	O	Output	m[9:0]	Floating
P[3:0]	O	Output	p[3:0]	Floating
TH1[9:0]	O	Output	th1[9:0]	Floating
TH2[7:0]	O	Output	th2[7:0]	Floating
TH3[7:0]	O	Output	th3[7:0]	Floating
BYPASS	O	Output	bypass	Floating
TSTPLLDIG[2:0]	O	Output	tstplldig[2:0]	Floating
IBEXT	O	Output	ibext	Floating
ICPCTRL[3:0]	O	Output	icpctrl[3:0]	Floating
LPFCTRL[5:0]	O	Output	lpfctrl[5:0]	Floating
CMX	O	Output	Floating	Floating

Core PHY			D-PHY Master (With PLL)	D-PHY Slave (Without PLL)
VCORANGE [3:0]	O	Output	vcorange[3:0]	Floating

Table 9-1 lists the signal connections to be performed upon integration depending on whether the D-PHY IP is expected to work as Master or Slave.

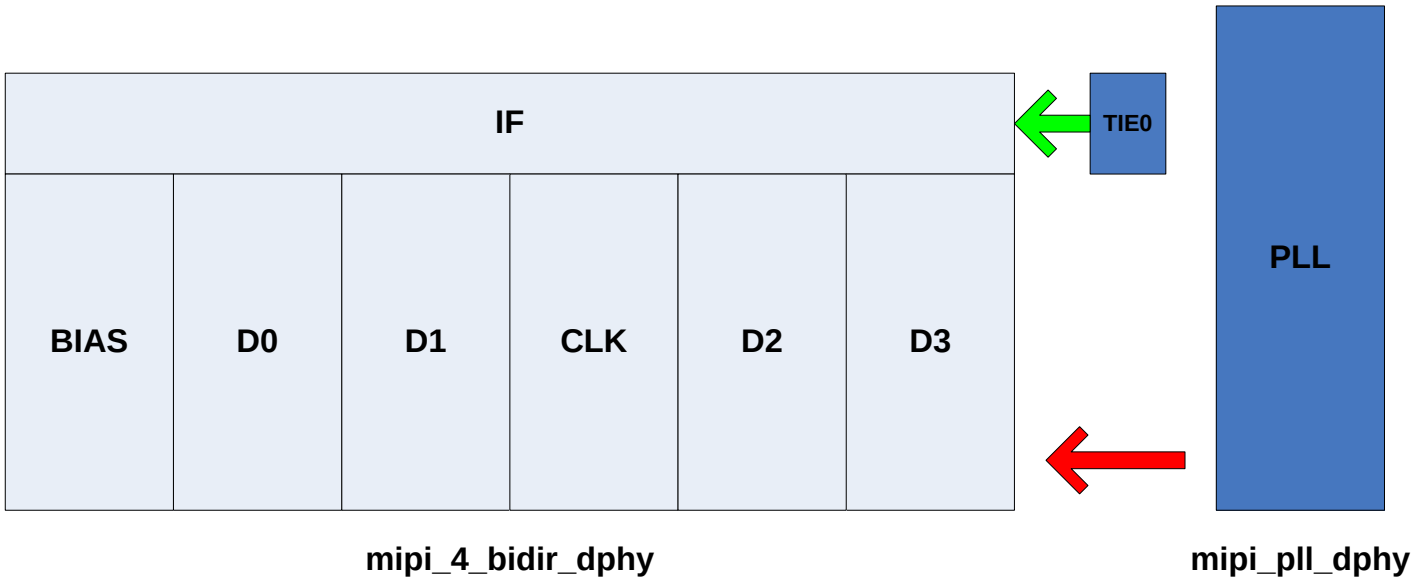
For Master applications, the PLL can be connected directly by abutment to the right of the PHY. No additional routing is needed as shown in Figure 9-1.

Figure 9-1 mipi_4_bidir_dphy and mipi_pll_dphy Connection by Abutment



For Slave applications, interface input signals of mipi_4_bidir_dphy should be tied to ground (VSS) while the outputs can be left floating. Refer to Table 9-1.

Figure 9-2 Attachable PLL and TIE0 connections for Slave Operation



9.6.2 Analog IO ring

All analog IOs should fulfill the requirements listed in section 9.2 Cell Routing. As a possible solution, Synopsys recommends the use of TSMC analog library tpan40lpgv2 to assemble the analog IO ring. The IO cells shown in Table 9-2 should be used:

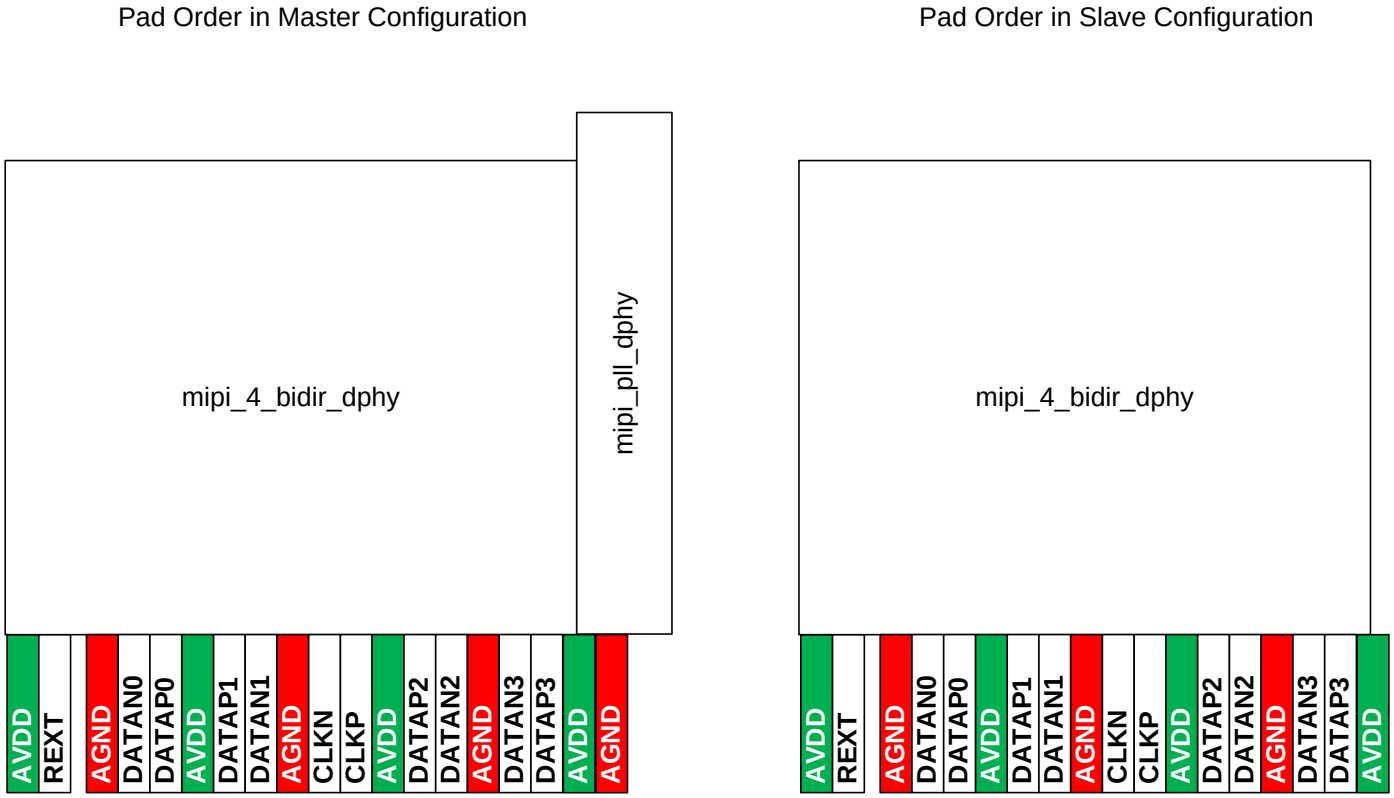
Table 9-2 Example of TPAN40LP TSMC Analog IO Library Usage

I/O Cells	Description	mipi_4_bidir_dphy (xNr.Pads)
PDB1A	Analog I/O Cell with I/O Voltage (Approximately 100 fF at steady state)	DATAP0 (x1), DATAN0 (x1), DATAP1 (x1), DATAN1 (x1), DATAP2 (x1), DATAN2 (x1), DATAP3 (x1), DATAN3 (x1), CLKP (x1), CLKN (x1), REXT (x1)
PVDD3A	Power Provider for Both Analog Macro and Analog I/O Power Rail (I/O Voltage)	AVDD (x4)
PVSS3A	Analog Ground Provider Used with PVDD3A Analog Power Cell	AGND (x3 without PLL; x4 with PLL)

Both mipi_4_bidir_dphy and mipi_pll_dphy IP blocks are designed to easily accommodate the IO pad pitch of 60 um meaning that an analog IO ring may be constructed in such a way that no/minimum routing is needed between it and the PHY.

9.6.3 IO Pad Order Recommendations

Figure 9-3 Pad Order in Master and Slave Configurations



10 PCB Guidelines

This chapter provides general recommendations for PCB layout common to most high speed digital communication environments.

For DWC D-PHY Bidir 4L to operate reliably at high data rates (1 Gbps), excellent signal integrity is required. Good PCB layout is a key factor to achieve good signal integrity.

10.1 Schematic Diagram

Figure 10-1 shows a high level schematic diagram of the external circuitry required by the D-PHY and Table 10-1 provides power supply requirements.

Figure 10-1 Schematic Diagram of the External Circuitry

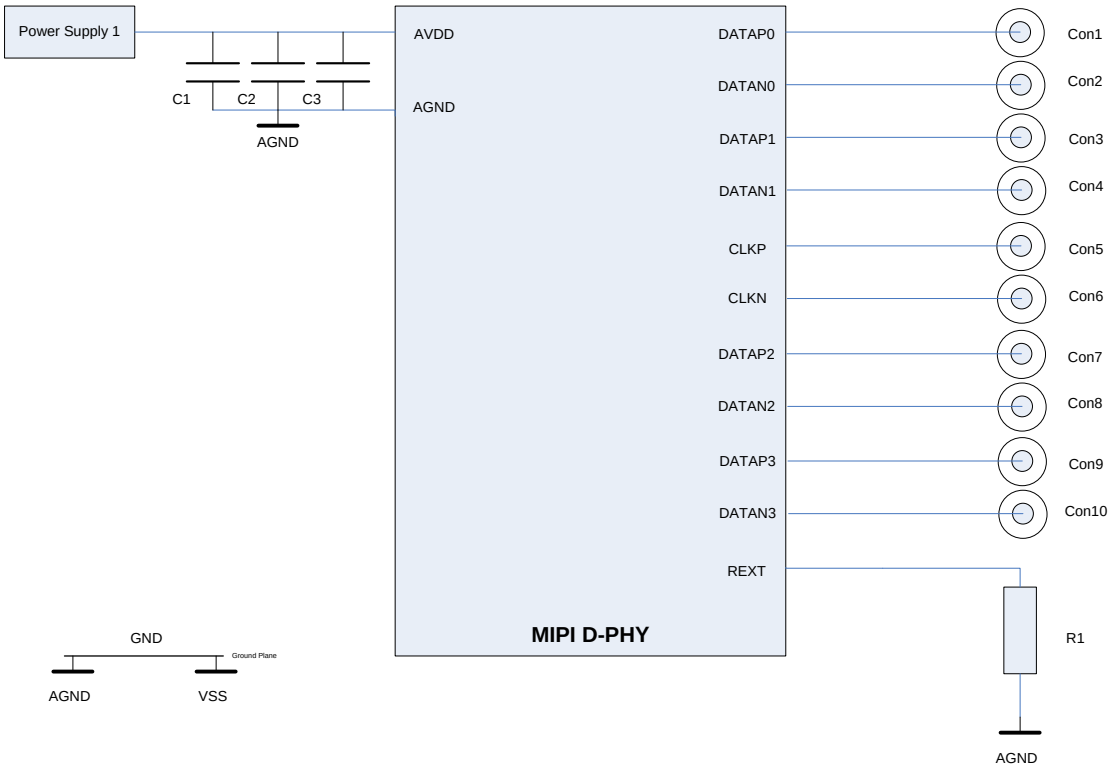


Table 10-1 Power Supply Requirements

Power Supply 1
2.5 V

10.2 Bill of Materials

The bill of materials is shown in Table 10-2.

Table 10-2 Bill of Materials

Connectors	Con1, Con2, Con3, ... Con10 – SMA connectors or other surface mount coaxial connectors with 50 Ω impedance and bandwidth > 3 GHz
Power Supplies	2.5 V DC power supply
Decoupling	C1 – Capacitor 10 nF (ceramic X7R)
	C2 – Capacitor 100 nF (ceramic X7R)
	C3 – Capacitor 1 uF (Tantalum)
Others	R1 - 6.04 KΩ E96

10.3 Components Placement

To achieve a good level of decoupling, follow these rules during the PCB layout:

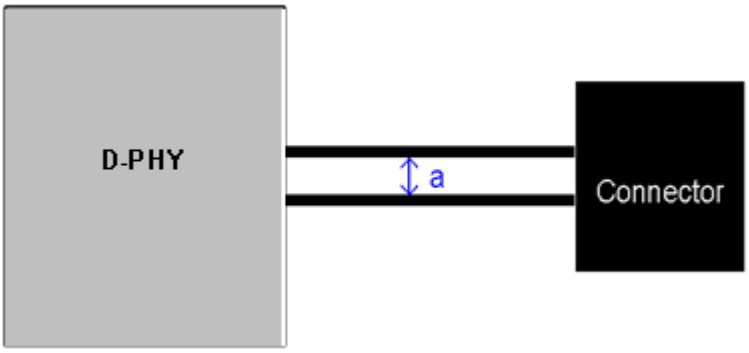
- The ceramic type capacitors used for transient load decoupling should be placed as close as possible to the chip power supply pins.
- Any additional supply decoupling should also be placed close to chip supply pins.
- External resistor R1 should be placed as close as possible to the chip REXT pin/ball. This ensures minimum resistance added because of the connection, which in turn ensures accurate internal references and optimum performance.

10.4 Trace Characteristics

Synopsys recommends that you maintain the TX/RX differential pairs with 100 Ω differential impedance at the frequency of 500 MHz and routed on the top layer without any vias. This ensures minimum reflections and signal integrity degradation at the higher rates.

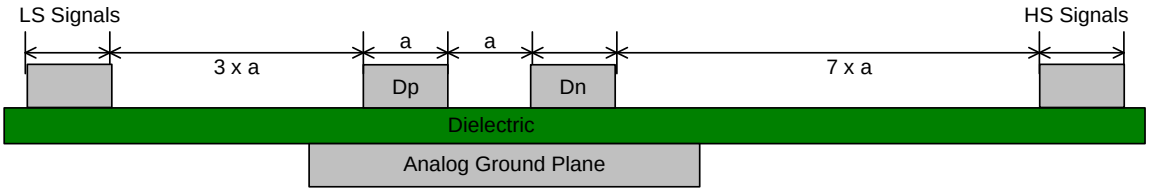
Calculate the trace width and spacing for specific PCB characteristics such as copper weight, dielectric thickness, and so on. Symmetry in both shape and length is recommended.

Figure 10-2 PCB Differential Traces



To minimize the crosstalk, take care of signal traces which are routed close to the TX/RX data differential pairs. The minimum recommended spacing is 3x for low-speed non-periodic signals and 7x for high-speed periodic signals. A continuous ground plane below Dp/Dn lines is required.

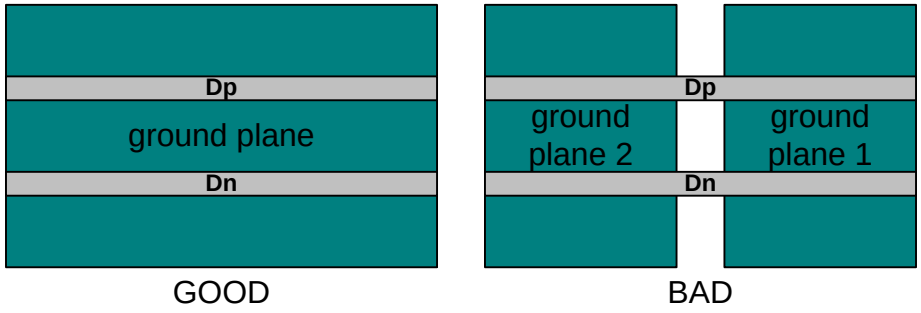
Figure 10-3 Crosstalk Protection for Dp/Dn Lines



10.5 PCB Layers

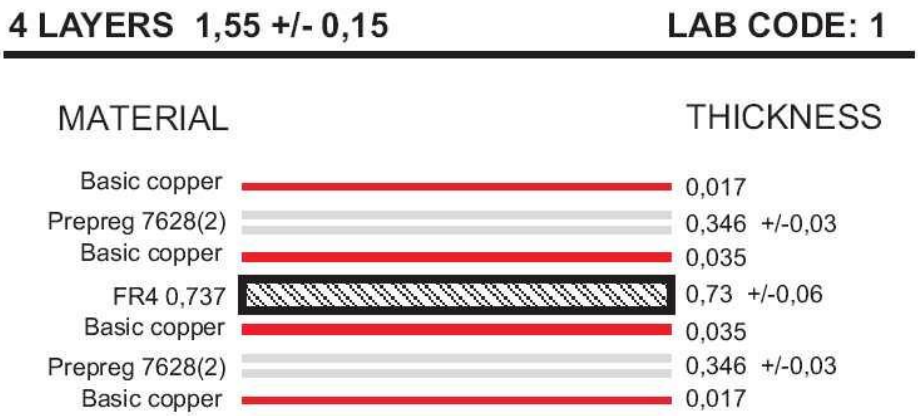
If high-speed signals are routed on the Top layer, best results are obtained, if the Layer 2 is a ground plane. Also, there must be only one ground plane under high-speed signals in order to avoid the high-speed signals to cross another ground plane.

Figure 10-4 Ground Planes



Four layers stack example is shown in section PCB Stack Layers (4 Layers).

Figure 10-5 PCB Stack Layers (4 Layers)



11 Process-Specific Specifications

11.1 Design Implementation Values, Voltage, and Temperature Specifications

Table 11-1 Design Implementation Values

Design Implementation	Value
PHY macro size (required for Slave configuration)	0.81 mm^2 (1080 x 750)
PHY + PLL macro size (required for Master configuration)	1.005 mm^2 (1320 x 810)
External reference resistor (R_{REF}) 1% (or better) resistor connected to ground	6.04 KΩ

Table 11-2 Overall Voltage and Temperature Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Operating Junction Temperature		-40	+25	+125	°C
Analog Supply Voltage[10]		2.25	2.5	2.75	V
Digital Supply Voltage		0.99	1.1	1.21	V

[10] Specifications for IP only (not at Test Chip level). The supply range includes supply variation, noise and IR drops.

11.2 Power Consumption

Table 11-3 provides power consumption values for Current Consumption for basic configuration with additional data lanes.

Table 11-3 Project Specific Values for Power Consumption

Para-meter	Conditions			Minimum Single Data + Clock Lane Configuration		Each Additional Data Lane		PLL		Quad data Lane D-PHY Bidir as Slave (No PLL)		Quad Data Lane D-PHY Bidir as Master (with PLL)		Unit
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
Supply Current	HS Mode	TX @1 Gbps	AVDD	6.5		3		6		N/A		21.5		mA
			VDD	7		3.5		3.5		N/A		21		mA
		RX @1 Gbps	AVDD	2		1		0.005		5		N/A		mA
			VDD	6		3		0.02		15		N/A		mA
	LP Mode	TX @10 Mbps	AVDD	1.8		1.2		0.005		5.4		5.4		mA
			VDD	0.6		0.5		0.02		2.1		2.1		mA
		RX @10 Mbps	AVDD	0.5		0.5		0.005		2		2		mA
			VDD	0.5		0.4		0. 02		1.7		1.7		mA
	IDLE Mode	TX[11]	AVDD	0.6		0.3		6		N/A	N/A	7.5		mA
			VDD	1		0.3		3.5		N/A	N/A	5.4		mA
		RX	AVDD	0.6		0.2		0.005		1.2		N/A	N/A	mA
			VDD	0.6		0.2		0.02		1.2		N/A	N/A	mA

[11] PLL enabled for fast turn on

Table 11-3 Project Specific Values for Power Consumption

Para-meter	Conditions			Minimum Single Data + Clock Lane Configuration		Each Additional Data Lane		PLL		Quad data Lane D-PHY Bidir as Slave (No PLL)		Quad Data Lane D-PHY Bidir as Master (with PLL)		Unit
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
Supply Current	ULPS	TX	AVDD	0.6		0.05		0.005		N/A	N/A	0.75		mA
			VDD	0.4		0.1		0.02		N/A	N/A	0.7		mA
		RX	AVDD	0.6		0.05		0.005		0.75		N/A	N/A	mA
			VDD	0.4		0.1		0.02		0.7		N/A	N/A	mA
	Power Down		AVDD	10		5		1.5		25		26.5		uA
			VDD	50		15		1		95		96		uA

11.3 Electrical and Timing Information

Table 11-4 provides the electrical and timing characteristics for the DWC D-PHY Bidir 4L.

The following hold unless otherwise noted:

- Vdd (core) = V
- Vdd (IO) = V
- $T_A{}^o$ = Tmin to Tmax

Table 11-4 Electrical and Timing Specification

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
Input DC Specifications - Apply to CLKP/N and DATAP/N inputs						
V_I	Input signal voltage range	Transient voltage range is limited from -300 mV to 1600 mV	-50		1350	mV
I_{LEAK}	Input leakage current	$V_{GNDSH(min)} \le V_I \le V_{GNDSH(max)} + V_{OH(absmax)}$ Lane module in LP Receive Mode	-10		10	mA
V_{GNDSH}	Ground shift		-50		50	mV
$V_{OH(absmax)}$	Maximum transient output voltage level				1.45	V
$t_{VOH(absmax)}$	Maximum transient time above $\mathbf{V_{OH(absmax)}}$				20	ns
HS Line Drivers DC Specifications						
$\lvert V_{OD} \rvert$	HS Transmit Differential output voltage magnitude	80 Ω ≤ R_L ≤ 125 Ω	140	200	270	mV
$\Delta \lvert V_{OD} \rvert$	Change in Differential output voltage magnitude between logic states	80 Ω ≤ R_L ≤ 125 Ω			10	mV
V_{CMTX}	Steady-state common-mode output voltage.	80 Ω ≤ R_L ≤ 125 Ω	150	200	250	mV
$\Delta V_{CMTX(1,0)}$	Changes in steady-state common-mode output voltage between logic states	80 Ω ≤ R_L ≤ 125 Ω			5	mV
V_{OHHS}	HS output high voltage	80 Ω ≤ R_L ≤ 125 Ω			360	mV
Z_{OS}	Single-ended output impedance.		40	50	62.5	Ω

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
ΔZ_{OS}	Single-ended output impedance mismatch.				10	%
LP Line Drivers DC Specifications						
V_{OL}	Output low-level SE voltage		-50		50	mV
V_{OH}	Output high-level SE voltage		1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance.		110			Ω
$\Delta Z_{OLP(01,10)}$	Single-ended output impedance mismatch driving opposite level				20	%
$\Delta Z_{OLP(00,11)}$	Single-ended output impedance mismatch driving same level				5	%
HS Line Receiver DC Specifications						
V_{IDTH}	Differential input high voltage threshold				70	mV
V_{IDTL}	Differential input low voltage threshold		-70			mV
V_{IHHS}	Single ended input high voltage				460	mV
V_{ILHS}	Single ended input low voltage		-40			mV
V_{CMRXDC}	Input common mode voltage		70		330	mV
Z_{ID}	Differential input impedance		80		125	Ω
LP Line Receiver DC Specifications						
V_{IL}	Input low voltage				550	mV
V_{IH}	Input high voltage		880			mV
V_{HYST}	Input hysteresis		25			mV
Contention Line Receiver DC Specifications						
V_{ILF}	Input low fault threshold		200		450	mV

11.4 Switching Characteristics

This section provides the various specifications for the switching characteristics of D-PHY.

Table 11-5 Switching Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
Configuration clock						
F_{CFG_CLK}	CFG_CLK frequency		17		27	MHz
DC_{CFG_CLK}	CFG_CLK duty cycle		40	50	60	%
HS Line Drivers AC Specifications						
-	Maximum Serial Data rate (forward direction)	On DATAP/N outputs. 80 Ω ≤ R_L ≤ 125 Ω	80		1000	Mbps
F_{DDRCLK}	DDR CLK frequency	On CLKP/N outputs	40		500	MHz
P_{DDRCLK}	DDR CLK period	80 Ω ≤ R_L ≤ 125 Ω	2		25	ns
t_{CDC}	DDR CLK duty cycle	t_{CDC} = t_{CPH} / P_{DDRCLK}		50		%
t_{CPH}	DDR CLK high time			1		UI
t_{CPL}	DDR CLK low time			1		UI
-	DDR CLK / DATA Jitter[12]			75		ps pk-pk
$t_{SKEW[PN]}$	Intra-Pair (Pulse) skew			0.075		UI
$t_{SKEW[TX]}$	Data to Clock Skew		0.350		0.650	UI
$t_{SETUP[RX]}$	Data to Clock Receiver Setup time		0.15			UI
$t_{HOLD[RX]}$	Clock to Data Receiver Hold time		0.15			UI
t_r	Differential output signal rise time	20% to 80%, R_L = 50 Ω	150		0.3 UI	ps
t_f	Differential output signal fall time	20% to 80%, R_L = 50 Ω	150		0.3 UI	ps
$\Delta V_{CMTX(HF)}$	Common level variation above 450 MHz	80 Ω ≤ R_L ≤ 125 Ω			15	mVrms
$\Delta V_{CMTX(LF)}$	Common level variation between 50 MHz and 450 MHz.	80 Ω ≤ R_L ≤ 125 Ω			25	mVp

[12] Jitter specification with clean clock at REFCLK input.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
LP Line Drivers AC Specifications						
t_{rlp} , t_{flp}	Single ended output rise/fall time	15% to 85%, C_L < 70 pF			25	ns
t_{reot}		30% to 85%, C_L < 70 pF			35	ns
$\partial V/\partial t_{SR}$	Signal slew rate[13]	15% to 85%, C_L < 70 pF			120	mV/ns
C_L	Load capacitance		0		70	pF
HS Line Receiver AC Specifications						
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz				200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz.		-50		50	mVpp
C_{CM}	Common mode termination				60	pF
LP Line Receiver AC Specifications						
e_{SPIKE}	Input pulse rejection				300	V.ps
T_{MIN}	Minimum pulse response		50			ns
V_{INT}	Pk-to-Pk interference voltage				400	mV
f_{INT}	Interference frequency		450			MHz
Model Parameters used for Driver Load switching performance evaluation						
C_{PAD}	Equivalent Single ended I/O PAD capacitance.				1	pF
C_{PIN}	Equivalent Single ended Package + PCB capacitance.				2	pF
L_S	Equivalent wire bond series inductance				1.5	nH

[13] Measured as average across any 50 mV of the output signal transition.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
R_S	Equivalent wire bond series resistance				0.15	Ω
R_L	Load Resistance		80	100	125	Ω

11.4.1 Clock Multiplier Switching Characteristics

Table 11-6 Clock Multiplier Switching Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
F_{REFCLK}	REFCLK frequency		17		27	MHz
t_{CDC}	REFCLK duty cycle		40		60	%
J_{REFCLK}	REFCLK input phase noise	>1MHz offset			-120	dBc/Hz
Data and Control Interface Specifications						
t_{LPLL}	Lock Time				1	ms

11.4.2 PPI Interface Signal Switching Characteristics

Table 11-7 PPI Interface Signal Switching Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
Data and Control Interface Specifications						
t_{PWrstz}	Reset pulse duration		$2xP_{REFLK}$			ns
t_S	Data/Control input setup time					ns
t_H	Data/Control input hold time					ns
t_D	Data/Control delay time					ns
SCAN Interface Specifications						
F_{SCAN}	SCAN clock frequency				80	MHz
Test/Config Interface Specification						
t_{clrpw}	TESTCLR min pulse width		10			ns
t_{clkpw}	TESTCLK min pulse width		10			ns
t_{ddout}	TESTDOUT output delay				10	ns
t_{ens}	TESTEN setup time		5			ns
t_{enh}	TESTEN hold time		5			ns
t_{dins}	TESTDIN setup time		5			ns
t_{dinh}	TESTDIN hold time		5			ns
t_{min}	TESTDIN minimum time between events		5			ns

A Timing Diagrams

This appendix illustrates some important timing diagrams.

A.1 Operating Modes Control

Table 11-8 Operating Modes Control

	Operating Modes					
Input Signals	**Reset**	**High Speed Data Transmission**	**Low-Power Data Transmission**	**Trigger Request**	**Ultra Low-Power State**	**Turnaround**
RESETZ	1'b0	1'b1	1'b1	1'b1	1'b1	1'b1
SHUTDOWNZ	1'b0	1'b1	1'b1	1'b1	1'b1	1'b1
TESTCLEAR	1'b1	1'b0	1'b0	1'b0	1'b0	1'b0
TXRQSTHSCLK	1'b0	1'b1	1'b0	1'b0	1'b0	1'b0
TXRQSTHSDATA	1'b0	1'b1	1'b0	1'b0	1'b0	1'b0
TXRQSTESC	1'b0	1'b0	1'b1	1'b1	1'b1	1'b0
TXLPDTESC	1'b0	1'b0	1'b1	1'b0	1'b0	1'b0
TXVALIDESC	1'b0	1'b0	1'b1 (when valid data is in TXDATAESC)	1'b0	1'b0	1'b0
TXTRIGGERESC	4'b0000	4'b0000	4'b0000	4'b1000 4'b0100 4'b0010 4'b0001	4'b0000	4'b0000
TXULPSESC	1'b0	1'b0	1'b0	1'b0	1'b1	1'b0

	Operating Modes					
TXULPSEXIT	1'b0	1'b0	1'b0	1'b0	1'b1 (to start exit procedure from ULP mode)	1'b0
TURNREQUEST	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1

A.1.1 Reset Sequence for Master

Input sequence:

1. Set RSTZ = 1'b0.
2. Set SHUTDOWNZ = 1'b0.
3. Set TESTCLEAR = 1'b1.
4. Set MASTERSLAVEZ = 1'b1 (for MASTER) / 1'b0 (for SLAVE).
5. Set BASEDIRX to the desired values.
6. Set all REQUEST inputs to zero.
7. Wait for t > $T_{min.}$
8. Set RSTZ = 1'b1.
9. Set SHUTDOWNZ = 1'b1.
10. Set TESTCLEAR = 1'b0.
11. Wait until STOPSTATEX outputs are asserted. At this point the PLL has already locked (for MASTER) and the initialization of the analog drivers has finished. From this point the REQUEST inputs can be set accordingly with the desired transmission.

Figure 11-1 Initialization Sequence for Master

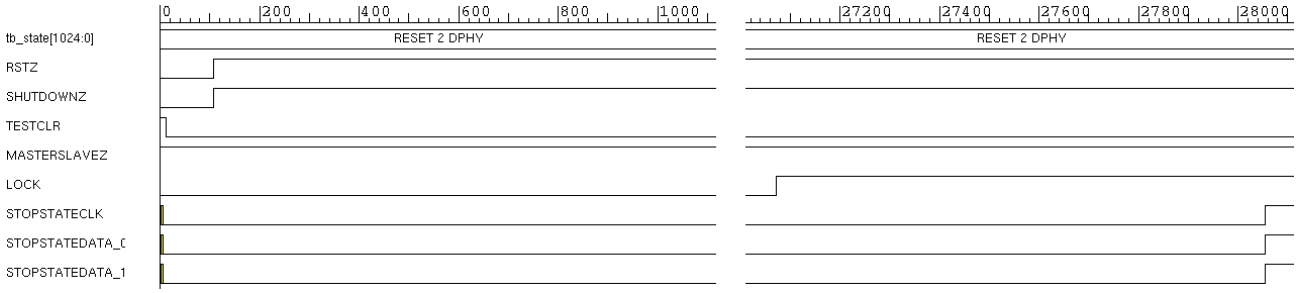
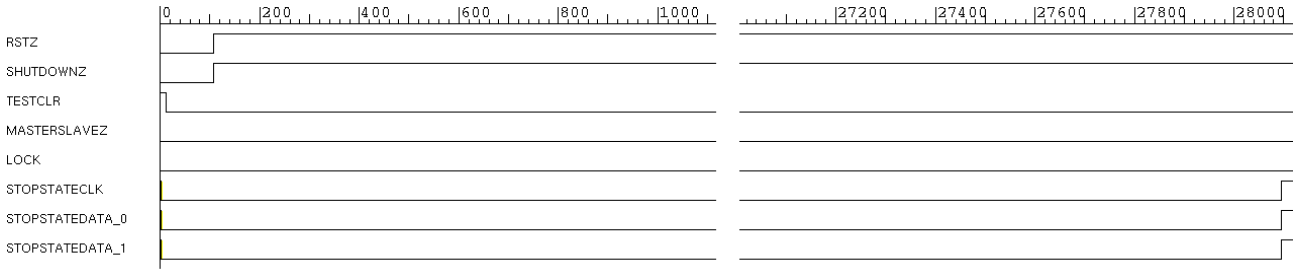


Figure 11-2 Initialization Sequence for Slave



Note All request inputs must be kept at zero to avoid any unexpected behavior from the PHY until STOPSTATEX outputs are set.

A.1.2 High Speed Data

Input Sequence (TXBYTECLKHS synchronous):

1. Set TXREQUESTHSCLK = 1'b1.
2. Set TXREQUESTDATAHSX = 1'b1.
3. Wait for TXREADYHS assertion.
4. Change TXDATAHS_X @ posedge TXBYTECLKHS until the completion of the desired burst.
5. Set TXREQUESTDATAHSX = 1'b0.
7. Wait for STOPSTATEDATAX assertion.
7. Wait for more than 100 ns.
8. Repeat sequence to send new burst.
9. After complete HS transmission, set TXREQUESTHSCLK = 1'b0.

Figure 11-3 HS Transmission

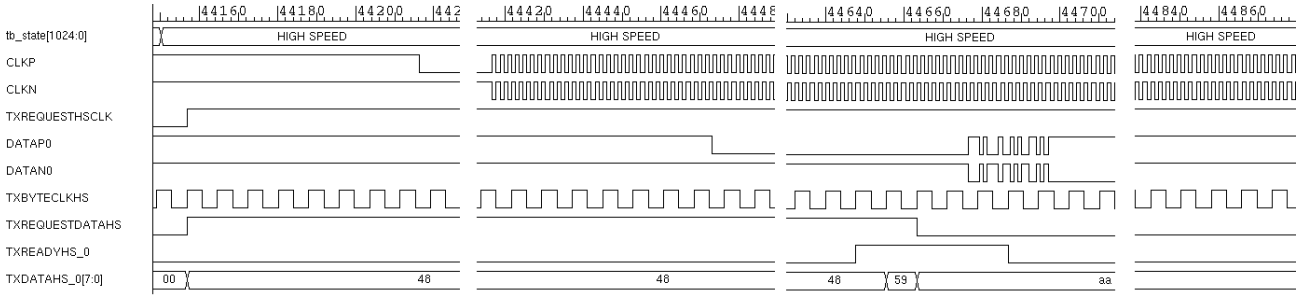
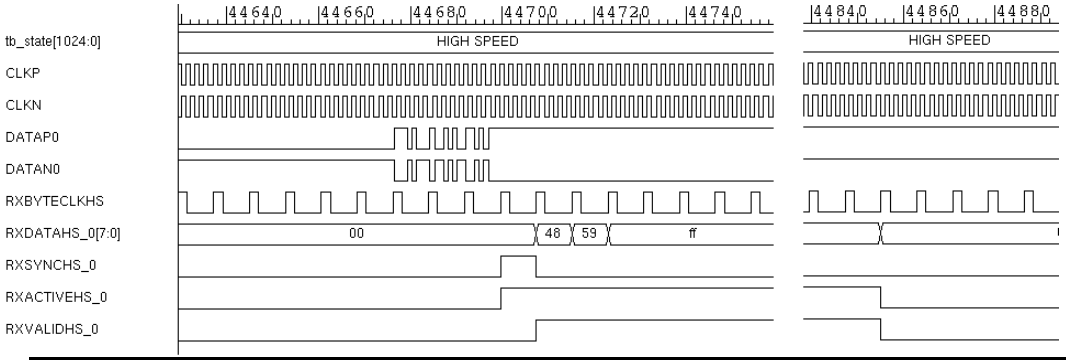


Figure 11-4 HS Reception



Note If a new HS request is done before the completion of the ongoing HS transmission process, the PHY starts the new transmission as soon as the current one ends. As the lanes are independent, each lane starts a new transmission regardless of the state of the remaining lanes. To avoid such behavior, the new HS request should not be done before t > 100 ns after the assertion of all STOPSTATEDATAX outputs.

A.1.3 Low-Power Data

Input sequence (TXCLKESC synchronous):

1. Set TXREQUESTESC = 1'b1
2. Set TXLPDTESC = 1'b1
3. Set the data to transmit in TXDATAESC
4. Set TXVALIDESC = 1'b1
5. Wait for TXREADYESC assertion
8. Insert new value in TXDATAESC
7. Repeat the TXDATAESC/TXVALIDESC/TXREADYESC sequence for the several bytes to be transmitted
8. Set TXREQUESTESC = 1'b0
9. Set TXVALIDESC = 1'b0
10. Set TXLPDTESC = 1'b0

Note Data is sampled when TXREADYESC is asserted simultaneously with TXVALIDESC. If pauses between each byte are to be inserted, TXVALIDESC input should not be set to one during the complete transmission, but rather set to one only when the correct data is set in the TXDATAESC input.

Figure 11-5 LP Transmission

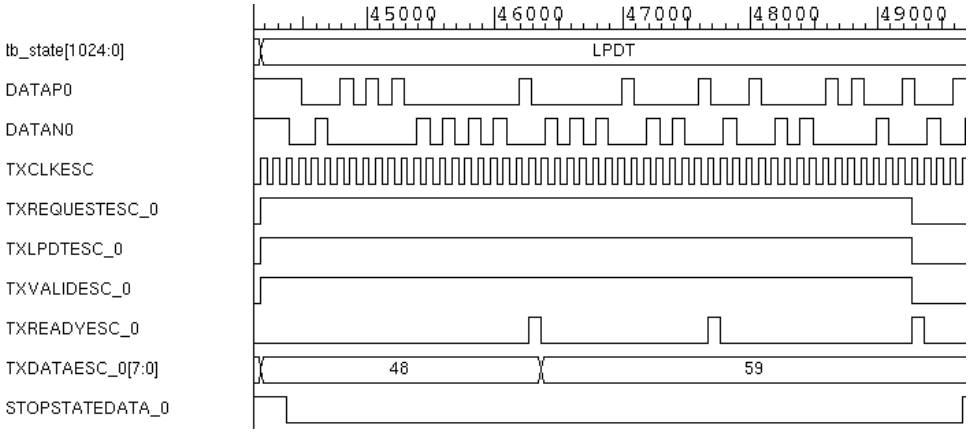
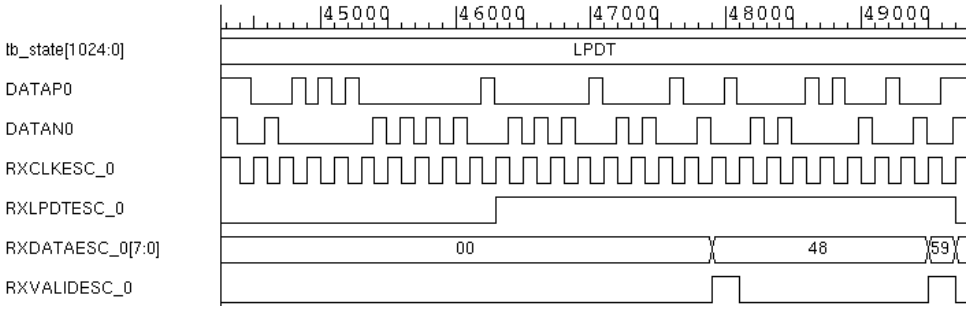


Figure 11-6 LP Reception



A.1.4 Escape Mode Trigger Request

Input Sequence (TXCLKESC synchronous):

1. Set TXTRIGGERESC = 4'bXXXX (only one X is equal to 1, the remaining must be left set to 0)

Table 11-9 Escape Mode Trigger

TXTRIGGERESC Value	Escape Mode Trigger
4'b1000	Reset Trigger
4'b0100	Unknown-3
4'b0010	Unknown-4
4'b0001	Unknown-5

2. Wait until STOPSTATE is de-asserted
3. Set TXREQUESTESC = 1'b0
4. Set TXTRIGGERESC = 4'b0000

Note

- TXREQUESTESC and TXTRIGGERESC should be kept high until STOPSTATE is low.
- TXREQUESTESC and TXTRIGGERESC should be set to zero at max when STOPSTATE is reasserted.
- If a second request is done before the first is finished (and is not kept until after STOPSTATE assertion/de-assertion), it is ignored.
- TXTRIGGERESC input must be one-hot encoded (the simultaneous assertion of two bits causes erroneous behavior).

Figure 11-7 Trigger Transmission

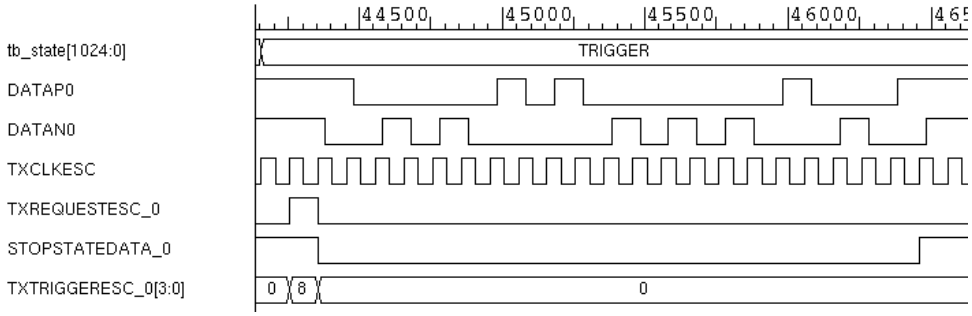
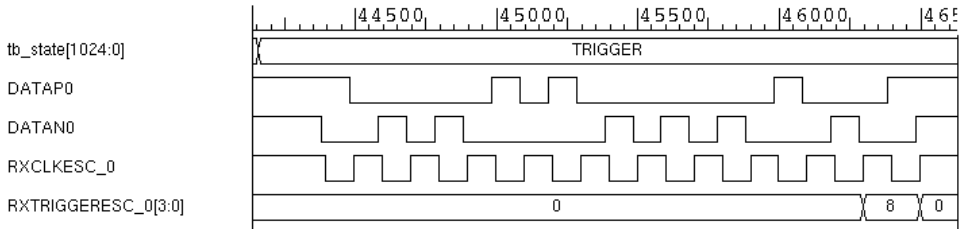


Figure 11-8 Trigger Reception



A.1.5 Ultra Low-Power Request (TXCLKESC Synchronous)

Input sequence:

1. Set TXREQUESTESC = 1'b1
2. Set TXULPSESC = 1'b1
3. Wait for t > $t_{request}$ (ULPSCATIVENOT = 1'b0)
4. Set TXULPSEXIT = 1'b1
5. Wait for t>1 ms (at least after rising edge of ULPSACTIVENOT)
9. Set TXREQUESTESC = 1'b0
7. Set TXULPSESC = 1'b0
8. Set TXULPSEXIT = 1'b0

Note

- TXULPSESC must be maintained set at least until STOPSTATE is de-asserted.
- TXULPSEXIT must be asserted only after the request is completed (when ULPSCATIVENOT is set to 0).
- Mark-1 state begins sometime after TXULPSEXIT assertion.
- Exit from ULPS state only occurs when TXREQUESTESC is set low.

Figure 11-9 Ultra Low-Power Entry Command Transmission

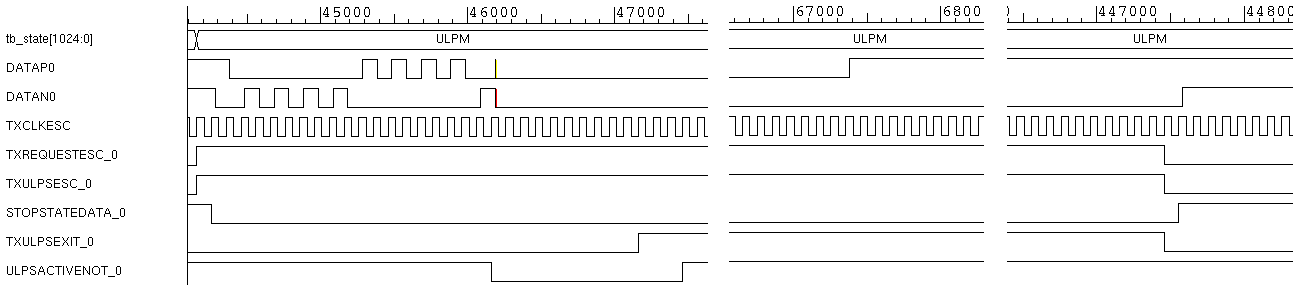
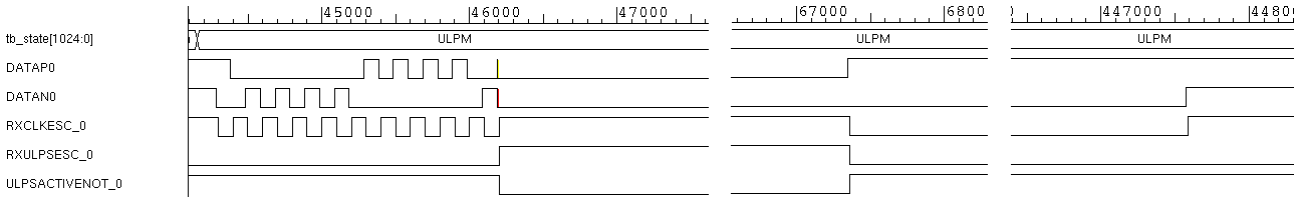


Figure 11-10 Ultra Low-Power Entry Command Reception



A.1.6 Turnaround Request

Input sequence (TXCLKESC synchronous):

1. Set TURNREQUESTX = 1'b1
2. Wait until DIRECTIONX output is set to 1'b1
3. Set TURNREQUESTX = 1'b0
4. Wait until STOPSTATEDATAX is asserted (turnaround procedure is completed)

Figure 11-11 Turnaround Procedure (TX -> RX)

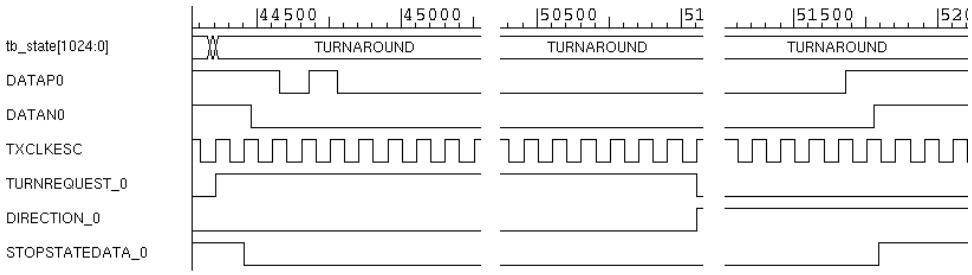


Figure 11-12 Turnaround Procedure (RX -> TX)