MIPI Alliance Specification for

D-PHY

Version 1.00.00 – 14 May 2009

MIPI Board Approved 22 September 2009

* Caution to Implementers *

This document is a MIPI® Specification formally approved by the MIPI Alliance Board of Directors per the process defined in the MIPI Alliance Bylaws. However, implementers should be aware of the following:

It is the good faith expectation of the MIPI PHY Working Group that D-PHY v1.00.00 is stable and robust. The MIPI Alliance currently recommends that any member companies considering implementation of D-PHY base their work on this version of the specification (v1.00.00).

MIPI Alliance strongly recommends that member companies NOT implement previously adopted D-PHY specification v0.65 or D-PHY specification v0.90 which are superseded by this version (v1.00.00).

It is the good faith expectation of the MIPI PHY WG that there will be no significant functional changes to the fundamental technology described in this specification.

The D-PHY specification requires that powered-up Lanes be initialized simultaneously. However, some corresponding protocol specifications may not mention this fact. The D-PHY specification will continue to describe this requirement until all corresponding protocol specifications are updated.

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Further technical changes to this document are expected as work continues in the PHY Working Group

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285 # MIPI Alliance Specification for D-PHY

286 ## 1   Overview

287 This specification provides a flexible, low-cost, High-Speed serial interface solution for communication
288 interconnection between components inside a mobile device. Traditionally, these interfaces are CMOS
289 parallel busses at low bit rates with slow edges for EMI reasons. The D-PHY solution enables significant
290 extension of the interface bandwidth for more advanced applications. The D-PHY solution can be realized
291 with very low power consumption.

292 ### 1.1   Scope

293 The scope of this document is to specify the lowest layers of High-Speed source-synchronous interfaces to
294 be applied by MIPI Alliance application or protocol level specifications. This includes the physical
295 interface, electrical interface, low-level timing and the PHY-level protocol. These functional areas taken
296 together are known as D-PHY.

297 The D-PHY specification shall always be used in combination with a higher layer MIPI specification that
298 references this specification. Initially, this specification will be used for the connection of a host processor
299 to display and camera modules as used in mobile devices. However, this specification can also be
300 referenced by other upcoming MIPI Alliance specifications.

301 The following topics are outside the scope of this document:

302 - **Explicit specification of signals of the clock generator unit.** Of course, the D-PHY
303   specification does implicitly require some minimum performance from the clock signals.
304   Intentionally, only the behavior on the interface pins is constrained. Therefore, the clock
305   generation unit is excluded from this specification, and will be a separate functional unit that
306   provides the required clock signals to the D-PHY in order to meet the specification. This allows
307   all kinds of implementation trade-offs as long as these do not violate this specification. More
308   information can be found in section 4.

309 - **Test modes, patterns, and configurations.** Obviously testability is very important, but because
310   the items to test are mostly application specific or implementation related, the specification of
311   tests is deferred to either the higher layer specifications or the product specification. Furthermore
312   MIPI D-PHY compliance testing is not included in this specification.

313 - **Procedure to resolve contention situations.** The D-PHY contains several mechanisms to detect
314   Link contention. However, certain contention situations can only be detected at higher levels and
315   are therefore not included in this specification.

316 - **Ensure proper operation of a connection between different Lane Module types.** There are
317   several different Lane Module types to optimally support the different functional requirements of
318   several applications. This means that next to some base-functionality there are optional features
319   which can be included or excluded. This specification only ensures correct operation for a
320   connection between matched Lane Modules types, which means: Modules that support the same
321   features and have complementary functionality. In case the two sides of the Lane are not the same
322   type, and these are supposed to work correctly, it shall be ensured by the manufacturer(s) of the
323   Lane Module(s) that the provided additional functionality does not corrupt operation. This can be
324   easiest accomplished if the additional functionality can be disabled by other means independent of
325   the MIPI D-PHY interface, such that the Lane Modules behave as if they were the same type.

326 - **ESD protection level of the IO.** The required level will depend on a particular application
327   environment and product type.

328   •   **Exact Bit-Error-Rate (BER) value.** The actual value of the achieved BER depends on the total
329   system integration and the hostility of the environment. Therefore, it is impossible to specify a
330   BER for individual parts of the Link. This specification allows for implementations with a
331          $BER < 10^{-12}$.

332   •   **Specification of the PHY-Protocol Interface.** The D-PHY specification includes a PHY-
333   Protocol Interface (PPI) annex that provides one possible solution for this interface. This annex is
334   limited to the essential signals for normal operation in order to clarify the kind of signals needed
335   at this interface. For power reasons this interface will be internal for most applications. Practical
336   implementations may be different without being inconsistent with the D-PHY specification.

337   •   **Implementations.** This specification is intended to restrict the implementation as little as
338   possible. Various sections of this specification use block diagrams or example circuits to illustrate
339   the concept and are not in any way claimed to be the preferred or required implementation. Only
340   the behavior on the D-PHY interface pins is normative.

341 Regulatory compliance methods are not within the scope of this document. It is the responsibility of
342 product manufacturers to ensure that their designs comply with all applicable regulatory requirements.

343 **1.2   Purpose**

344 The D-PHY specification is used by manufacturers to design products that adhere to MIPI Alliance
345 interface specifications for mobile device such as, but not limited to, camera, display and unified protocol
346 interfaces.

347 Implementing this specification reduces the time-to-market and design cost of mobile devices by
348 standardizing the interface between products from different manufacturers. In addition, richer feature sets
349 requiring high bit rates can be realized by implementing this specification. Finally, adding new features to
350 mobile devices is simplified due to the extensible nature of the MIPI Alliance Specifications.
351

2   Terminology

353 The MIPI Alliance has adopted Section 13.1 of the *IEEE Standards Style Manual*, which dictates use of the
354 words "shall", "should", "may", and "can" in the development of documentation, as follows:

355   The word *shall* is used to indicate mandatory requirements strictly to be followed in
356   order to conform to the standard and from which no deviation is permitted (*shall* equals
357   *is required to*).

358   The use of the word *must* is deprecated and shall not be used when stating mandatory
359   requirements; must is used only to describe unavoidable situations.

360   The use of the word *will* is deprecated and shall not be used when stating mandatory
361   requirements; *will* is only used in statements of fact.

362   The word *should* is used to indicate that among several possibilities one is recommended
363   as particularly suitable, without mentioning or excluding others; or that a certain course
364   of action is preferred but not necessarily required; or that (in the negative form) a certain
365   course of action is deprecated but not prohibited (*should* equals *is recommended that*).

366   The word *may* is used to indicate a course of action permissible within the limits of the
367   standard (*may* equals *is permitted*).

368   The word *can* is used for statements of possibility and capability, whether material,
369   physical, or causal (*can* equals *is able to*).

370 Throughout this document, the chronology for binary sequences and timing diagrams is from left (first in
371 time) to right (later in time), unless otherwise specified.

372 This document uses the C/Verilog representation for operators where bitwise AND is represented by '&',
373 bitwise OR is represented by '|', bitwise exclusive-OR is represented by '^' and 1's complement (negation)
374 is represented by '~'.

375 All sections are normative, unless they are explicitly indicated to be informative.

2.1   Definitions

377 **Bi-directional:** A single Data Lane that supports communication in both the Forward and Reverse
378 directions.

379 **DDR Clock:** Half rate clock used for dual-edged data transmission.

380 **D-PHY:** The source synchronous PHY defined in this document. D-PHYs communicate on the order of
381 500 Mbit/s hence the Roman numeral for 500 or "D."

382 **Escape Mode:** An optional mode of operation for Data Lanes that allows low bit-rate commands and data
383 to be transferred at very low power.

384 **Forward Direction:** The signal direction is defined relative to the direction of the High-Speed DDR clock.
385 Transmission from the side sending the clock to the side receiving the clock is the Forward direction.

386   **Lane:** Consists of two complementary Lane Modules communicating via two-line, point-to-point Lane
387   Interconnects. Sometimes Lane is also used to denote interconnect only. A Lane can be used for either Data
388   or Clock signal transmission.

389   **Lane Interconnect:** Two-line, point-to-point interconnect used for both differential High-Speed signaling
390   and Low-Power, single-ended signaling.

391   **Lane Module:** Module at each side of the Lane for driving and/or receiving signals on the Lane.

392   **Line:** An interconnect wire used to connect a driver to a receiver. Two Lines are required to create a Lane
393   Interconnect.

394   **Link:** A connection between two devices containing one Clock Lane and at least one Data Lane. A Link
395   consists of at least two PHYs and two Lane Interconnects.

396   **Master:** The Master side of a Link is defined as the side that transmits the High-Speed Clock. The Master
397   side transmits data in the Forward direction.

398   **PHY:** A functional block that implements the features necessary to communicate over the Lane
399   Interconnect. A PHY consists of one Lane Module configured as a Clock Lane, one or more Lane Modules
400   configured as Data Lanes and a PHY Adapter Layer.

401   **PHY Adapter:** A protocol layer that converts symbols from an APPI to the signals used by a specific PHY
402   PPI.

403   **PHY Configuration:** A set of Lanes that represent a possible Link. A PHY configuration consists of a
404   minimum of two Lanes, one Clock Lane and one or more Data Lanes.

405   **Reverse Direction:** Reverse direction is the opposite of the forward direction. See the description for
406   Forward Direction.

407   **Slave:** The Slave side of a Link is defined as the side that does not transmit the High-Speed Clock. The
408   Slave side may transmit data in the Reverse direction.

409   **Turnaround:** Reversing the direction of communication on a Data Lane.

410   **Unidirectional:** A single Lane that supports communication in the Forward direction only.

411   ## 2.2   Abbreviations

412   e.g.   For example (Latin: exempli gratia)

413   i.e.   That is (Latin: id est)

414   ## 2.3   Acronyms

415   APPI   Abstracted PHY-Protocol Interface

416   BER   Bit Error Rate

417   CIL   Control and Interface Logic

418   DDR   Double Data Rate

419	EMI	Electro Magnetic Interference
420	EoT	End of Transmission
421	HS	High-Speed; identifier for operation mode
422	HS-RX	High-Speed Receiver (Low-Swing Differential)
423	HS-TX	High-Speed Transmitter (Low-Swing Differential)
424	IO	Input-Output
425	ISTO	Industry Standards and Technology Organization
426	LP	Low-Power: identifier for operation mode
427	LP-CD	Low-Power Contention Detector
428	LPDT	Low-Power Data Transmission
429	LP-RX	Low-Power Receiver (Large-Swing Single-Ended)
430	LP-TX	Low-Power Transmitter (Large-Swing Single-Ended)
431	LPS	Low-Power State(s)
432	LSB	Least Significant Bit
433	Mbps	Megabits per second
434	MIPI	Mobile Industry Processor Interface
435	MSB	Most Significant Bit
436	PHY	Physical Layer
437	PLL	Phase-Locked Loop
438	PPI	PHY-Protocol Interface
439	RF	Radio Frequency
440	RX	Receiver
441	SE	Single-Ended
442	SoT	Start of Transmission
443 444	TLIS and Slave	Transmission-Line Interconnect Structure: physical interconnect realization between Master
445	TX	Transmitter
446	UI	Unit Interval, equal to the duration of any HS state on the Clock Lane

447 ULPS   Ultra-Low Power State
448

3   D-PHY Introduction

D-PHY describes a source synchronous, high speed, low power, low cost PHY, especially suited for mobile applications. This D-PHY specification has been written primarily for the connection of camera and display applications to a host processor. Nevertheless, it can be applied to many other applications. It is envisioned that the same type of PHY will also be used in a dual-simplex configuration for interconnections in a more generic communication network. Operation and available data-rates for a Link are asymmetrical due to a master-slave relationship between the two sides of the Link. The asymmetrical design significantly reduces the complexity of the Link. Some features like bi-directional, half-duplex operation are optional. Exploiting this feature is attractive for applications that have asymmetrical data traffic requirements and when the cost of separate interconnects for a return channel is too high. While this feature is optional, it avoids mandatory overhead costs for applications that do not have return traffic requirements or want to apply physically distinct return communication channels.

3.1   Summary of PHY Functionality

The D-PHY provides a synchronous connection between Master and Slave. A practical PHY Configuration consists of a clock signal and one or more data signals. The clock signal is unidirectional, originating at the Master and terminating at the Slave. The data signals can either be unidirectional or bi-directional depending on the selected options. For half-duplex operation, the reverse direction bandwidth is one-fourth of the forward direction bandwidth. Token passing is used to control the communication direction of the Link.

The Link includes a High-Speed signaling mode for fast-data traffic and a Low-Power signaling mode for control purposes. Optionally, a Low-Power Escape mode can be used for low speed asynchronous data communication. High speed data communication appears in bursts with an arbitrary number of payload data bytes.

The PHY uses two wires per Data Lane plus two wires for the Clock Lane. This gives four wires for the minimum PHY configuration. In High-Speed mode each Lane is terminated on both sides and driven by a low-swing, differential signal. In Low-Power mode all wires are operated single-ended and non-terminated. For EMI reasons, the drivers for this mode shall be slew-rate controlled and current limited.

The actual maximum achievable bit rate in High-Speed mode is determined by the performance of transmitter, receiver and interconnect implementations. Therefore, the maximum bit rate is not specified in this document. However, this specification is primarily intended to define a solution for a bit rate range of 80 to 1000 Mbps per Lane. Although PHY Configurations are not limited to this range, practical constraints make it the most suitable range for the intended applications. It is anticipated a typical implementation will have a bit rate of approximately 500 Mbps per Lane. For a fixed clock frequency, the available data capacity of a PHY Configuration can be increased by using more Data Lanes. Effective data throughput can be reduced by employing burst mode communication. The maximum data rate in Low-Power mode is 10Mbps.

3.2   Mandatory Functionality

All functionality that is specified in this document and which is not explicitly stated in section 4.5 shall be implemented for all D-PHY configurations.

489 ## 4   Architecture

490 This section describes the internal structure of the PHY including its functions at the behavioral level.
491 Furthermore, several possible PHY configurations are given. Each configuration can be considered as a
492 suitable combination from a set of basic modules.

493 ### 4.1   Lane Modules

494 A PHY configuration contains a Clock Lane Module and one or more Data Lane Modules. Each of these
495 PHY Lane Modules communicates via two Lines to a complementary part at the other side of the Lane
496 Interconnect.

497
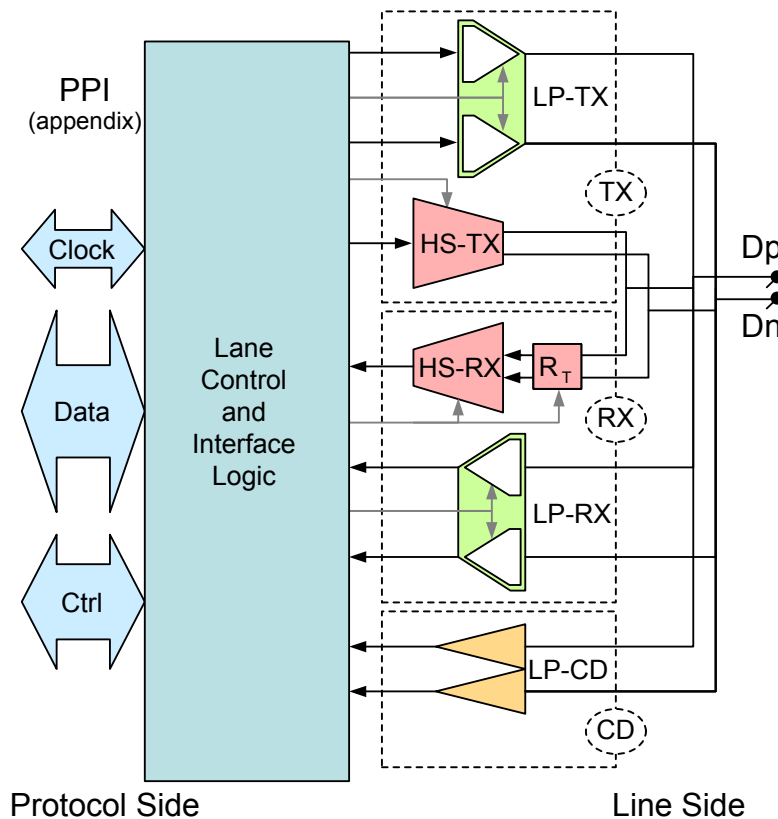
498 **Figure 1 Universal Lane Module Functions**

499 Each Lane Module consists of one or more differential High-Speed functions utilizing both interconnect
500 wires simultaneously, one or more single-ended Low-Power functions operating on each of the
501 interconnect wires individually, and control & interface logic. An overview of all functions is shown in
502 Figure 1. High-Speed signals have a low voltage swing, e.g. 200 mV, while Low-Power signals have a
503 large swing, e.g. 1.2V. High-Speed functions are used for High-Speed Data transmission. The Low-Power
504 functions are mainly used for Control, but have other, optional, use cases. The I/O functions are controlled
505 by a Lane Control and Interface Logic block. This block interfaces with the Protocol and determines the
506 global operation of the Lane Module.

507 High-Speed functions include a differential transmitter (HS-TX) and a differential receiver (HS-RX).

508   A Lane Module may contain a HS-TX, a HS-RX, or both. A HS-TX and a HS-RX within a single Lane
509   Module are never enabled simultaneously during normal operation. An enabled High-Speed function shall
510   terminate the Lane on its side of the Lane Interconnect as defined in sections 8.1.1 and 8.2.1. If a High-
511   Speed function in the Lane Module is not enabled then the function shall be put into a high impedance
512   state.

513   Low-Power functions include single-ended transmitters (LP-TX), receivers (LP-RX) and Low-Power
514   Contention-Detectors (LP-CD). Low-Power functions are always present in pairs as these are single-ended
515   functions operating on each of the two interconnect wires individually.

516   Presence of High-Speed and Low-Power functions is correlated. That is, if a Lane Module contains a HS-
517   TX it shall also contain a LP-TX. A similar constraint holds for HS-RX and LP-RX.

518   If a Lane Module containing a LP-RX is powered, that LP-RX shall always be active and continuously
519   monitor line levels. A LP-TX shall only be enabled when driving Low-Power states. The LP-CD function
520   is only required for bi-directional operation. If present, the LP-CD function is enabled to detect contention
521   situations while the LP-TX is driving Low-Power states. The LP-CD shall check for contention at least
522   once before driving a new state on the line.

523   The activities of LP-TX, HS-TX, and HS-RX in a single Lane Module are mutually exclusive, except for
524   some short crossover periods. For detailed specification of the Line side Clock and Data signals, and the
525   HS-TX, HS-RX, LP-TX, LP-RX and LP-CD functions, see sections 8 and 9.

526   For proper operation, the set of functions in the Lane Modules on both sides of the Lane Interconnect has
527   to be matched. This means for each HS and LP transmit or receive function on one side of the Lane
528   Interconnect, a complementary HS or LP receive or transmit function must be present on the other side. In
529   addition, a Contention Detector is needed in any Lane Module that combines TX and RX functions.

4.2   Master and Slave

531   Each Link has a Master and a Slave side. The Master provides the High-Speed DDR Clock signal to the
532   Clock Lane and is the main data source. The Slave receives the clock signal at the Clock Lane and is the
533   main data sink. The main direction of data communication, from source to sink, is denoted as the Forward
534   direction. Data communication in the opposite direction is called Reverse transmission. Only bi-directional
535   Data Lanes can transmit in the Reverse direction. In all cases, the Clock Lane remains in the Forward
536   direction, but bi-directional Data Lane(s) can be turned around, sourcing data from the Slave side.

4.3   High Frequency Clock Generation

538   In many cases a PLL Clock Multiplier is needed for the high frequency clock generation at the Master
539   Side. The D-PHY specification uses an architectural model where a separate Clock Multiplier Unit outside
540   the PHY generates the required high frequency clock signals for the PHY. Whether this Clock Multiplier
541   Unit in practice is integrated inside the PHY is left to the implementer.

4.4   Clock Lane, Data Lanes and the PHY-Protocol Interface

543   A complete Link contains, beside Lane Modules, a PHY Adapter Layer that ties all Lanes, the Clock
544   Multiplier Unit, and the PHY Protocol Interface together. Figure 2 shows a PHY configuration example for
545   a Link with two Data Lanes plus a separate Clock Multiplier Unit. The PHY Adapter Layer, though a
546   component of a PHY, is not within the scope of this specification.

547   The logical PHY-Protocol interface (PPI) for each individual Lane includes a set of signals to cover the
548   functionality of that Lane. As shown in Figure 2, Clock signals may be shared for all Lanes. The reference
549   clock and control signals for the Clock Multiplier Unit are not within the scope of this specification.
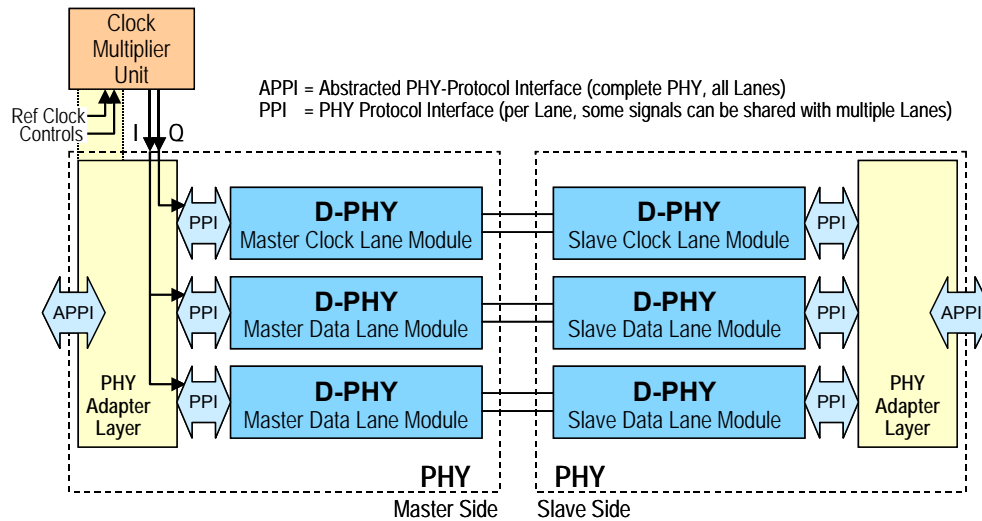
Figure 2 Two Data Lane PHY Configuration

4.5   Selectable Lane Options

A PHY configuration consists of one Clock Lane and one or more Data Lanes. All Data Lanes shall support High-Speed transmission and Escape mode in the Forward direction.

There are two main types of Data Lanes:

- Bi-directional (featuring Turnaround and some Reverse communication functionality)
- Unidirectional (without Turnaround or any kind of Reverse communication functionality)

Bi-directional Data Lanes shall include one or both of the following Reverse communication options:

- High-Speed Reverse data communication
- Low-Power Reverse Escape mode (including or excluding LPDT)

All Lanes shall include Escape mode support for ULPS and Triggers in the Forward direction. Other Escape mode functionality is optional; all possible Escape mode features are described in section 5.6. Applications shall define what additional Escape mode functionality is required and, for bi-directional Lanes, shall select Escape mode functionality for each direction individually.

This results in many options for complete PHY Configurations. The degrees of freedom are:

- Single or Multiple Data Lanes
- Bi-directional and/or Unidirectional Data Lane (per Lane)
- Supported types of Reverse communication (per Lane)
- Functionality supported by Escape mode (for each direction per Lane)
- Data transmission can be with 8-bit raw data (default) or using 8b9b encoded symbol (see Annex C)

Figure 3 is a flow graph of the option selection process. Practical configuration examples can be found in section 4.7.
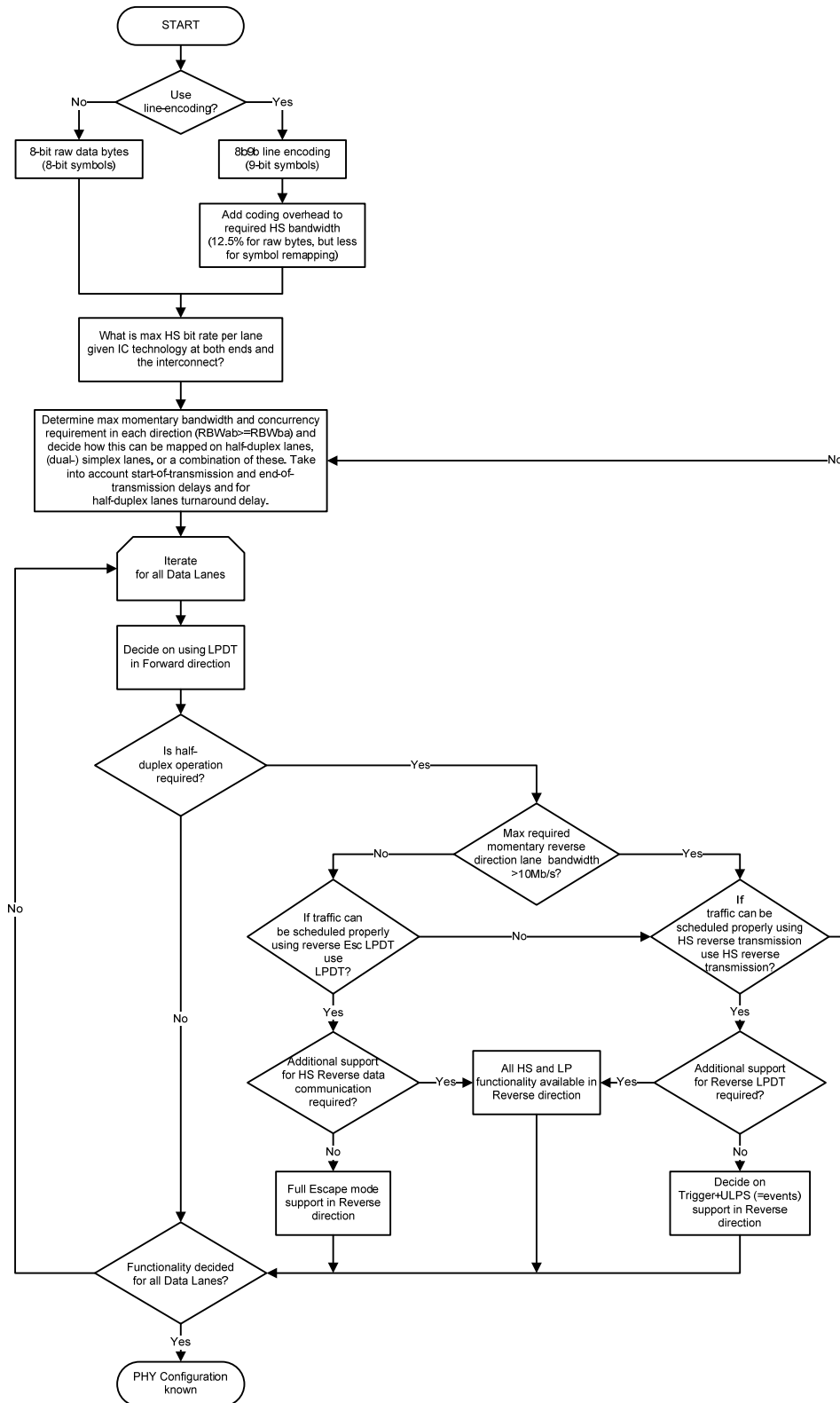
574
575   **Figure 3 Option Selection Flow Graph**

576 ## 4.6   Lane Module Types

577 The required functions in a Lane Module depend on the Lane type and which side of the Lane Interconnect
578 the Lane Module is located. There are three main Lane types: Clock Lane, Unidirectional Data Lane and
579 Bi-directional Data Lane. Several PHY configurations can be constructed with these Lane types. See
580 Figure 3 for more information on selecting Lane options.

581 Figure 4 shows a Universal Lane Module Diagram with a global overview of internal functionality of the
582 CIL function. This Universal Module can be used for all Lane Types. The requirements for the 'Control
583 and Interface Logic' (CIL) function depend on the Lane type and Lane side. Section 5 and Annex A
584 implicitly specify the contents of the CIL function. The actual realization is left to the implementer.

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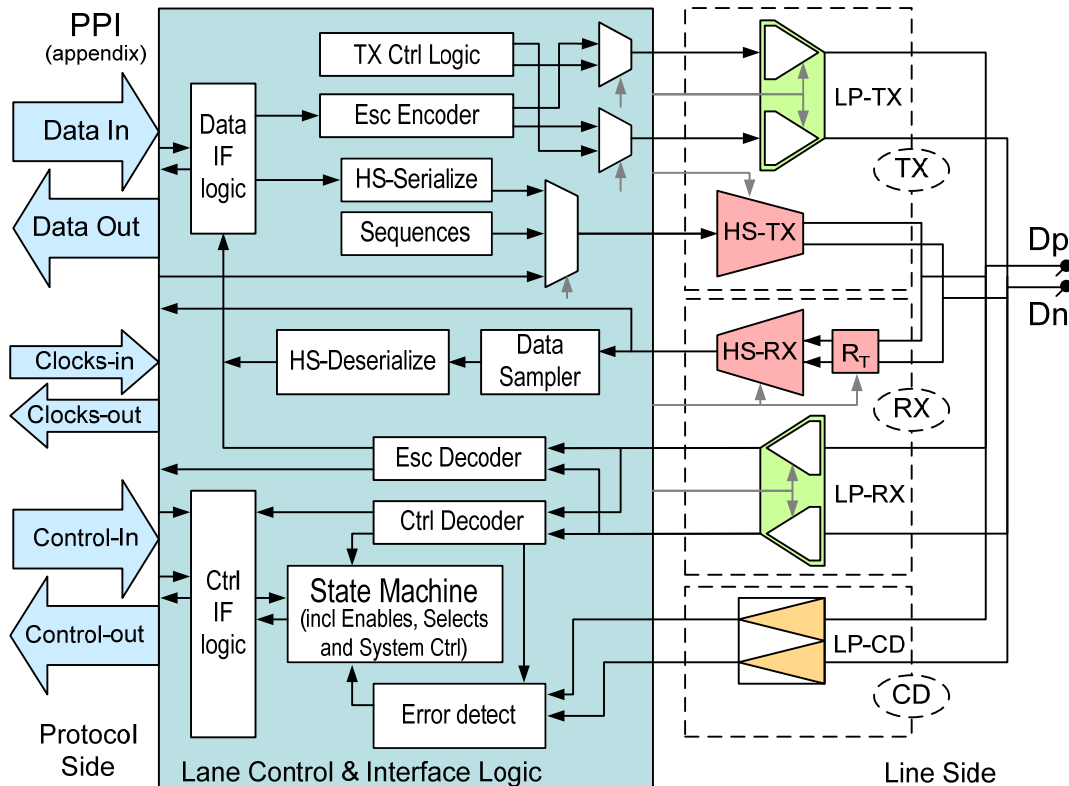
586 **Figure 4 Universal Lane Module Architecture**

587 Of course, stripped-down versions of the Universal Lane Module that just support the required
588 functionality for a particular Lane type are possible. These stripped-down versions are identified by the
589 acronyms in Table 1. For simplification reasons, any of the four identification characters can be replaced
590 by an X, which means that this can be any of the available options. For example, a CIL-MFEN is therefore
591 a stripped-down CIL function for the Master Side of a Unidirectional Lane with Escape mode functionality
592 only in the Forward direction. A CIL-SRXX is a CIL function for the Slave Side of a Lane with support for
593 Bi-directional High-Speed communication and any allowed subset of Escape mode.

594 Note that a CIL-XFXN implies a unidirectional Link, while either a CIL-XRXX or CIL-XXXY block
595 implies a bidirectional Link. Note that Forward 'Escape' (ULPS) entry for Clock Lanes is different than
596 Escape mode entry for Data Lanes.

597   **Table 1 Lane Type Descriptors**

Prefix	Lane Interconnect Side	High-Speed Capabilities	Forward Direction Escape Mode Features Supported	Reverse Direction Escape Mode Features Supported[1]
CIL-	M – Master S – Slave X – Don't Care	F – Forward Only R – Reverse and Forward X – Don't Care[2]	A – All (including LPDT) E – events – Triggers and ULPS Only X – Don't Care	A – All (including LPDT) E – events – Triggers and ULPS Only N – None Y – Any (A, E or A and E) X – Don't Care
		C – Clock	N – Not Applicable	N – Not Applicable

598   Notes:

599   1.   "Any" is any combination of one or more functions.

600   2.   Only valid for Data Lanes, means "F" or "R".

601   The recommend PHY Protocol Interface contains Data-in and Data-out in byte format, Input and/or output
602   Clock signals and Control signals. Control signals include requests, handshakes, test settings, and
603   initialization. A proposal for a logical internal interface is described in Annex A. Although not a
604   requirement it may be very useful to use the proposed PPI. For external use on IC's an implementation may
605   multiplex many signals on the same pins. However, for power efficiency reasons, the PPI is normally
606   within an IC.

607   4.6.1   Unidirectional Data Lane

608   For a Unidirectional Data Lane the Master Module shall contain at least a HS-TX, a LP-TX, and a CIL-
609   MFXN function. The Slave side shall contain at least a HS-RX, a LP-RX and a CIL-SFXN.

610   4.6.2   Bi-directional Data Lanes

611   A bi-directional Data Lane Module includes some form of reverse communication; either High-Speed
612   Reverse Communication, Reverse Escape mode, or both. The functions required depend on what methods
613   of Reverse communication are included in the Lane Module.

614   4.6.2.1   Bi-directional Data Lane without High-Speed Reverse Communication

615   A bi-directional Data Lane Module without High-Speed Reverse Communication shall include a Reverse
616   Escape mode. The Master-side Lane Module includes a HS-TX, LP-TX, LP-RX, LP-CD, and CIL-MFXY.
617   The Slave-side consists of a HS-RX, LP-RX, LP-TX, LP-CD and a CIL-SFXY.

618 **4.6.2.2   Bi-directional Data Lane with High-Speed Reverse Communication**

619   A bi-directional Data Lane Module with High-Speed Reverse Communication shall include a Reverse
620   Escape mode. The Master-side Lane Module includes a HS-TX, HS-RX, LP-TX, LP-RX, LP-CD, and
621   CIL-MRXX. The Slave-side consists of a HS-RX, HS-TX, LP-RX, LP-TX, LP-CD and a CIL-SRXX.

622   This type of Lane Module may seem suitable for both Master and Slave side but because of the asymmetry
623   of the Link one side shall be configured as Master and the other side as Slave.

624   ## 4.6.3   Clock Lane

625   For the Clock Lane, only a limited set of line states is used. However, for Clock Transmission and Low-
626   Power mode the same TX and RX functions are required as for Unidirectional Data Lanes. A Clock Lane
627   Module for the Master Side therefore contains a HS-TX, LP-TX, and a CIL-MCNN function, while the
628   Slave Side Module includes a HS-RX, a LP-RX and a CIL-SCNN function.

629   Note that the required functionality for a Clock Lane is similar, but not identical, to a Unidirectional Data
630   Lane. The High-Speed DDR clock is transmitted in quadrature phase with Data signals instead of in-phase.
631   In addition, the Clock Lane Escape mode entry is different than that used for Data Lanes. Furthermore,
632   since a Clock Lane only supports ULPS, an Escape mode entry code is not required.

633   The internal clock signals with the appropriate phases are generated outside the PHY and delivered to the
634   individual Lanes. The realization of the Clock generation unit is outside the scope of this specification. The
635   quality of the internal clock signals shall be sufficient to meet the timing requirement for the signals as
636   specified in section 9.

637   ## 4.7   Configurations

638   This section outlines several common PHY configurations but should not be considered an exhaustive list
639   of all possible arrangements. Any other configuration that does not violate the requirements of this
640   document is also allowed.

641   In order to create an abstraction level, the Lane Modules are represented in this section by Lane Module
642   Symbols. Figure 5 shows the syntax and meaning of symbols.

Universal Master/Slave
Module

Universal Module   Universal Module
Configured as Master   Configured as Slave
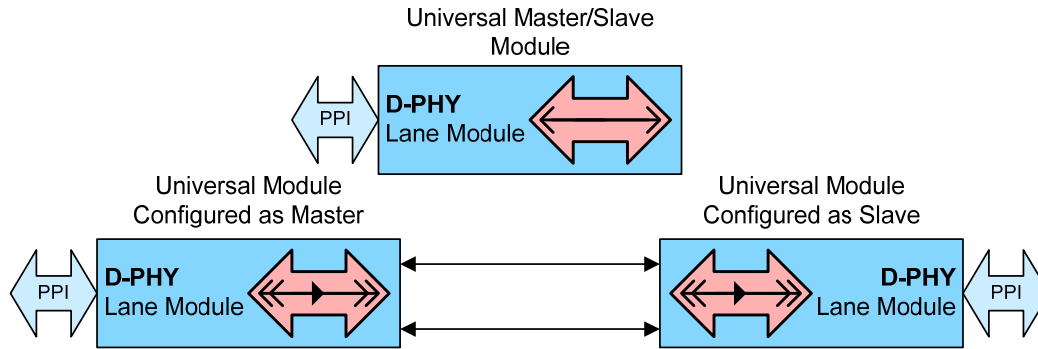
Legend:

This	Other Options	Meaning
		Supported Directions for High-Speed Data Transmission (Bi-directional or Unidirectional)
		Clock Lane
⟷	→ ←	Supported Directions for Escape mode excluding LPDT (Bi-directional or Forward Only)
⟪⟶⟫	⟶⟫ ⟪⟵	Supported Directions for Escape mode including LPDT (Bi-directional, Forward Only or Reverse Only)
→	←	Clock Direction (by definition from Master to Slave, must point in the same direction as the "Clock Only Lane" arrow)
		PPI: PHY-Protocol Interface

643

644   **Figure 5 Lane Symbol Macros and Symbols Legend**

645   For multiple Data Lanes a large variety of configurations is possible. Figure 6 shows an overview of
646   symbolic representations for different Lane types. The acronyms mentioned for each Lane type represent
647   the functionality of each module in a short way. This also sets the requirements for the CIL function inside
648   each Module.

D-PHY Lane Module		D-PHY Lane Module	• Bi-directional High-speed • Bi-directional Escape Mode • Bi-directional LDPT	MRAA & SRAA
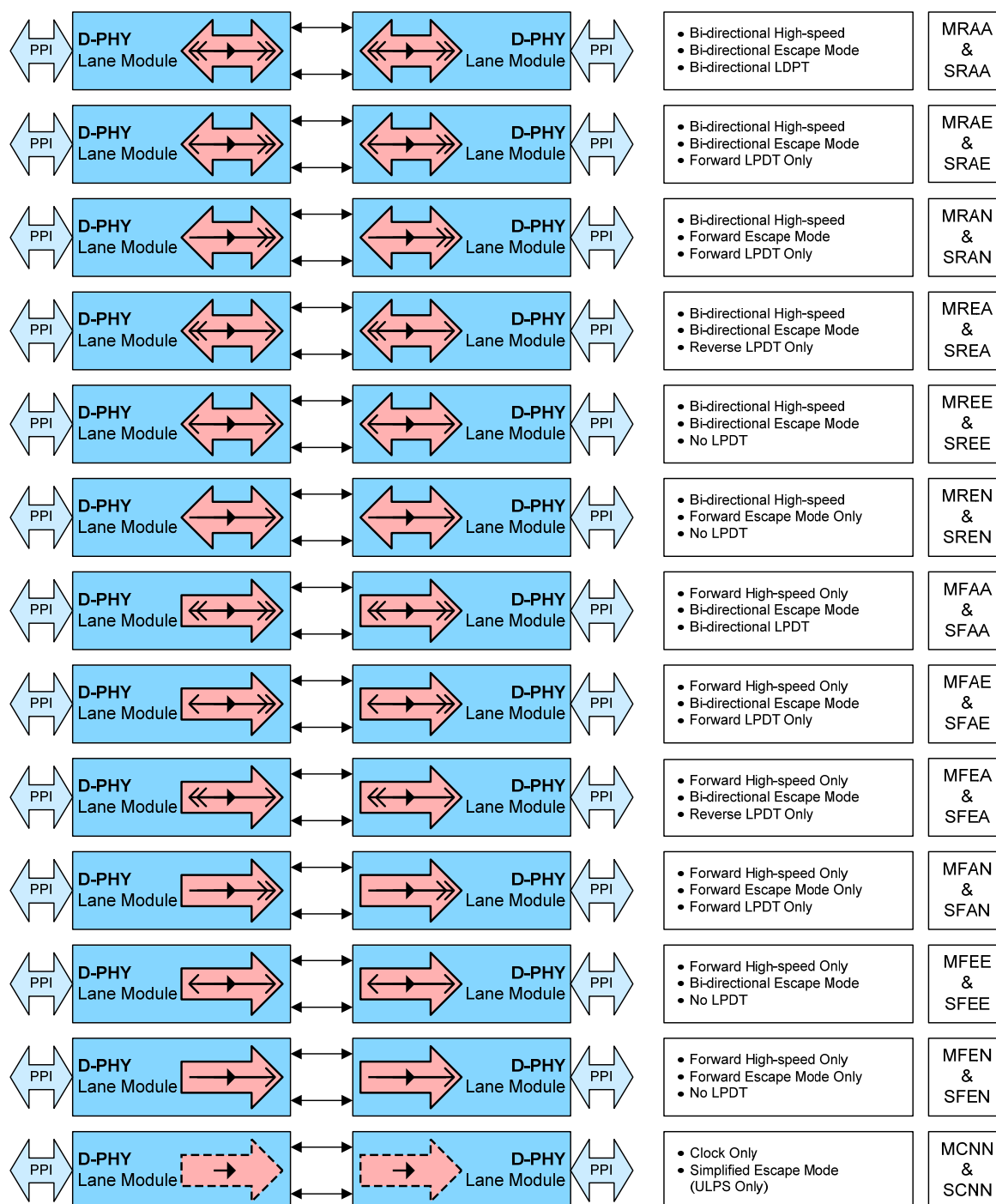
Figure 6 All Possible Data Lane Types and a Basic Unidirectional Clock Lane

4.7.1   Unidirectional Configurations

All unidirectional configurations are constructed with a Clock Lane and one or more Unidirectional Data Lanes. Two basic configurations can be distinguished: Single Data Lane and Multiple Data Lanes. For completeness a Dual-Simplex configuration is also shown. At the PHY level there is no difference between a Dual-Simplex configuration and two independent unidirectional configurations.

657   4.7.1.1   PHY Configuration with a Single Data Lane

658   This configuration includes one Clock Lane and one Unidirectional Data Lane from Master to Slave.
659   Communication is therefore only possible in the Forward direction. Figure 7 shows an example
660   configuration without LPDT. This configuration requires four interconnect signal wires.

661
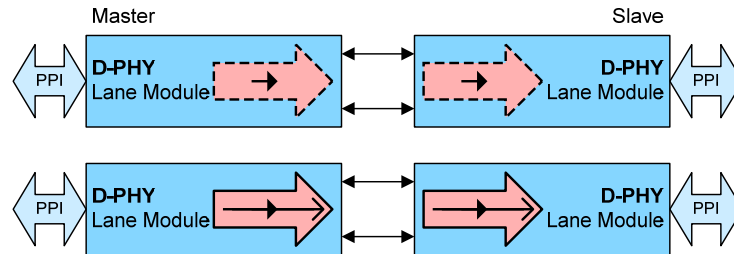
662   **Figure 7 Unidirectional Single Data Lane Configuration**

663   4.7.1.2   PHY Configuration with Multiple Data Lanes

664   This configuration includes one Clock Lane and multiple Unidirectional Data Lanes from Master to Slave.
665   Bandwidth is extended, but communication is only possible in the Forward direction. The PHY
666   specification does not require all Data Lanes to be active simultaneously. In fact, the Protocol layer
667   controls all Data Lanes individually. Figure 8 shows an example of this configuration for three Data Lanes.
668   If N is the number of Data Lanes, this configuration requires 2*(N+1) interconnect wires.

669
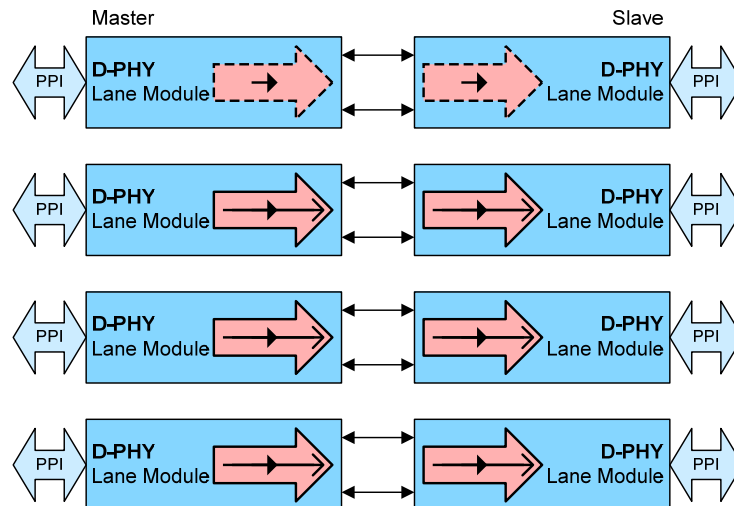
670   **Figure 8 Unidirectional Multiple Data Lane Configuration without LPDT**

671   4.7.1.3   Dual-Simplex (Two Directions with Unidirectional Lanes)

672   This case is the same as two independent (dual), unidirectional (simplex) Links: one for each direction.
673   Each direction has its own Clock Lane and may contain either a single, or multiple, Data Lanes. Please
674   note that the Master and Slave side for the two different directions are opposite. The PHY configuration for
675   each direction shall comply with the D-PHY specifications. As both directions are conceptually
676   independent, the bit rates for each direction do not have to match. However, for practical implementations,
677   it is attractive to match rates and share some internal signals as long as both Links fulfill all specifications
678   externally. Figure 9 shows an example of this dual PHY configuration.

679
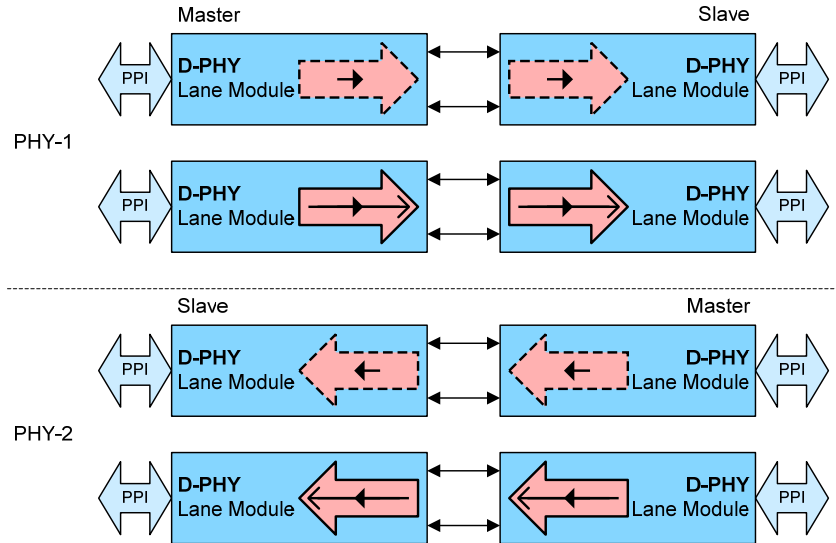
Figure 9 Two Directions Using Two Independent Unidirectional PHYs without LPDT

680

681   ### 4.7.2   Bi-Directional Half-Duplex Configurations

682   Bi-directional configurations consist of a Clock Lane and one or more bi-directional Data Lanes. Half-
683   duplex operation enables bi-directional traffic across shared interconnect wires. This configuration saves
684   wires compared to the Dual-Simplex configuration. However, time on the Link is shared between Forward
685   and Reverse traffic and Link Turnaround. The High-Speed bit rate in the Reverse direction is, by
686   definition, one-fourth of the bit rate in the Forward direction. LPDT can have similar rates in the Forward
687   and Reverse directions. This configuration is especially useful for cases with asymmetrical data traffic.

688   #### 4.7.2.1   PHY Configurations with a Single Data Lane

689   This configuration includes one Clock Lane and one of any kind of bi-directional Data Lane. This allows
690   time-multiplexed data traffic in both Forward and Reverse directions. Figure 10 shows this configuration
691   with a Data Lane that supports both High-Speed and Escape (without LPDT) communication in both
692   directions. Other possibilities are that only one type of reverse communication is supported or LPDT is also
693   included in one or both directions. All these configurations require four interconnect wires.

694
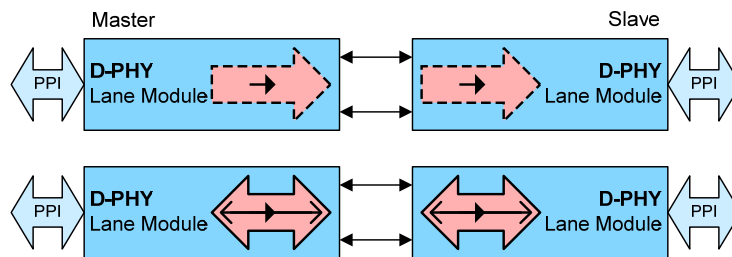
Figure 10 Bidirectional Single Data Lane Configuration

695

696   #### 4.7.2.2   PHY Configurations with Multiple Data Lanes

697   This configuration includes one Clock Lane and multiple bi-directional Data Lanes. Communication is
698   possible in both the Forward and Reverse direction for each individual Lane. The maximum available
699   bandwidth scales with the number of Lanes for each direction. The PHY specification does not require all
700   Data Lanes to be active simultaneously or even to be operating in the same direction. In fact, the Protocol

701   layer controls all Data Lanes individually. Figure 11 shows an example configuration with two Data Lanes.
702   If N is the number of Data Lanes, this configuration requires 2*(N+1) interconnect wires.

703
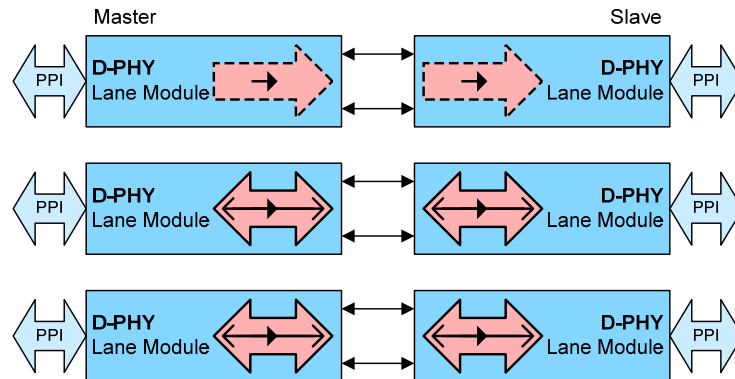
704   **Figure 11 Bi-directional Multiple Data Lane Configuration**

705   ### 4.7.3   Mixed Data Lane Configurations

706   Instead of using only one Data Lane type, PHY configurations may combine different unidirectional and
707   bi-directional Data Lane types. Figure 12 shows an example configuration with one bi-directional and one
708   unidirectional Data Lane, both without LPDT.

709
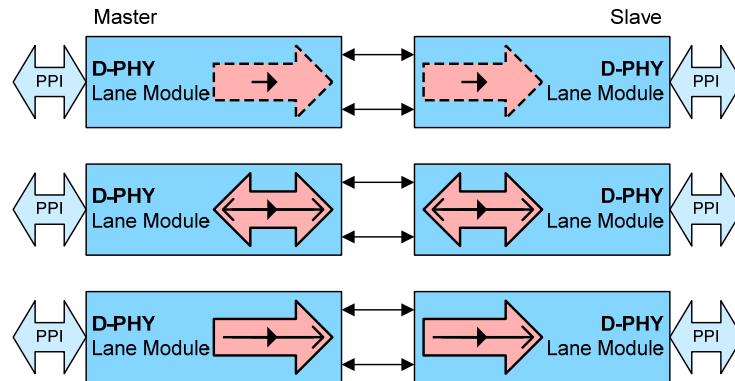
710   **Figure 12 Mixed Type Multiple Data Lane Configuration**

711

712 ## 5   Global Operation

713 This section specifies operation of the D-PHY including signaling types, communication mechanisms,
714 operating modes and coding schemes. Detailed specifications of the required electrical functions can be
715 found in section 8.

716 ### 5.1   Transmission Data Structure

717 During High-Speed, or Low-Power, transmission, the Link transports payload data provided by the
718 protocol layer to the other side of the Link. This section specifies the restrictions for the transmitted and
719 received payload data.

720 ### 5.1.1   Data Units

721 The minimum payload data unit shall be one byte. Data provided to a TX and taken from a RX on any
722 Lane shall be an integer number of bytes. This restriction holds for both High-Speed and Low-Power data
723 transmission in any direction.

724 ### 5.1.2   Bit order, Serialization, and De-Serialization

725 For serial transmission, the data shall be serialized in the transmitting PHY and de-serialized in the
726 receiving PHY. The PHY assumes no particular meaning, value or order of incoming and outgoing data.

727 ### 5.1.3   Encoding and Decoding

728 Line coding is not required by this specification. However, if line coding is used, it shall be implemented
729 according to Annex C.

730 ### 5.1.4   Data Buffering

731 Data transmission takes place on protocol request. As soon as communication starts, the protocol layer at
732 the transmit side shall provide valid data as long as it does not stop its transmission request. For Lanes that
733 use line coding, control symbols can also be inserted into the transmission. The protocol on the receive side
734 shall take the data as soon as delivered by the receiving PHY. The signaling concept, and therefore the
735 PHY protocol handshake, does not allow data throttling. Any data buffering for this purpose shall be inside
736 the protocol layer.

737 ### 5.2   Lane States and Line Levels

738 Transmitter functions determine the Lane state by driving certain Line levels. During normal operation
739 either a HS-TX or a LP-TX is driving a Lane. A HS-TX always drives the Lane differentially. The two LP-
740 TX's drive the two Lines of a Lane independently and single-ended. This results in two possible High-
741 Speed Lane states and four possible Low-Power Lane states. The High-Speed Lane states are Differential-0
742 and Differential-1. The interpretation of Low-Power Lane states depends on the mode of operation. The
743 LP-Receivers shall always interpret both High-Speed differential states as LP-00.

744
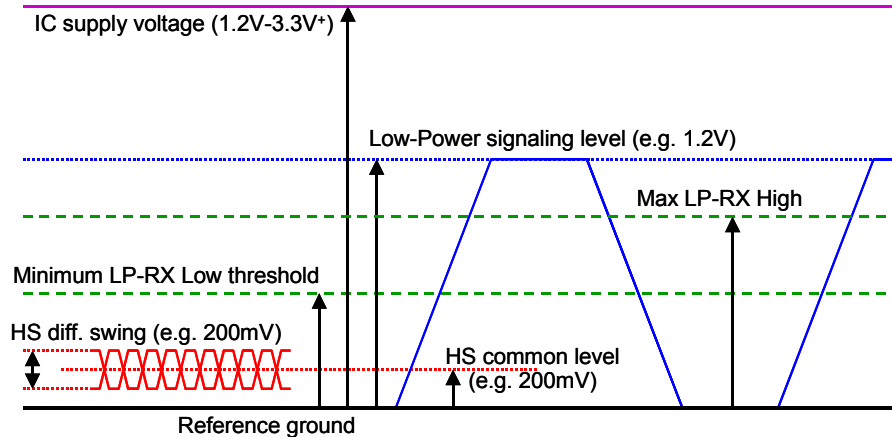
745   **Figure 13 Line Levels**

746   The Stop state has a very exclusive and central function. If the Line levels show a Stop state for the
747   minimum required time, the PHY state machine shall return to the Stop state regardless of the previous
748   state. This can be in RX or TX mode depending on the most recent operating direction. Table 2 lists all the
749   states that can appear on a Lane during normal operation. Detailed specifications of electrical levels can be
750   found in section 8.

751   All LP state periods shall be at least T_{LPX} in duration. State transitions shall be smooth and exclude glitch
752   effects. A clock signal can be reconstructed by exclusive-ORing the Dp and Dn Lines. Ideally, the
753   reconstructed clock has a duration of at least $2*T_{LPX}$, but may have a duty cycle other than 50% due to
754   signal slope and trip levels effects.

755   **Table 2 Lane State Descriptions**

State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	**Dn-Line**	**Burst Mode**	**Control Mode**	**Escape Mode**
HS-0	HS Low	HS High	Differential-0	N/A, Note 1	N/A, Note 1
HS-1	HS High	HS Low	Differential-1	N/A, Note 1	N/A, Note 1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A, Note 2

756   Notes:

757   1. During High-Speed transmission the Low-Power Receivers observe LP-00 on the Lines.

758   2. If LP-11 occurs during Escape mode the Lane returns to Stop state (Control Mode LP-11)

759   **5.3   Operating Modes: Control, High-Speed, and Escape**

760   During normal operation a Data Lane will be either in Control or High-Speed mode. High-Speed Data
761   transmission happens in bursts and starts from and ends at a Stop state (LP-11), which is by definition in
762   Control mode. The Lane is only in High-Speed mode during Data bursts. The sequence to enter High-
763   Speed mode is: LP-11, LP-01, LP-00 at which point the Data Lane remains in High-Speed mode until a
764   LP-11 is received. The Escape mode can only be entered via a request within Control mode. The Data Lane

765 shall always exit Escape mode and return to Control mode after detection of a Stop state. If not in High-
766 Speed or Escape mode the Data Lane shall stay in Control mode. For Data Lanes and for Clock Lanes the
767 Stop state serves as general standby state and may last for any period of time $> T_{LPX}$. Possible events
768 starting from the Stop state are High-Speed Data Transmission request (LP-11, LP-01, LP-00), Escape
769 mode request (LP-11, LP-10, LP-00, LP-01, LP-00) or Turnaround request (LP-11, LP-10, LP-00, LP-10,
770 LP-00).

771 ## 5.4   High-Speed Data Transmission

772 High-Speed Data Transmission occurs in bursts. To aid receiver synchronization, data bursts shall be
773 extended on the transmitter side with a leader and trailer sequence and shall be eliminated on the receiver
774 side. These leader and trailer sequences can therefore only be observed on the transmission lines.

775 Transmission starts from, and ends with, a Stop state. During the intermediate time between bursts a Data
776 Lane shall remain in the Stop state, unless a Turnaround or Escape request is presented on the Lane.
777 During a HS Data Burst the Clock Lane shall be in High-Speed mode, providing a DDR Clock to the Slave
778 side.

779 ### 5.4.1   Burst Payload Data

780 The payload data of a burst shall always represent an integer number of payload data bytes with a
781 minimum length of one byte. Note that for short bursts the Start and End overhead consumes much more
782 time than the actual transfer of the payload data. There is no maximum number of bytes implied by the
783 PHY. However, in the PHY there is no autonomous way of error recovery during a HS data burst and the
784 practical BER will not be zero. Therefore, it is important to consider for every individual protocol what the
785 best choice is for maximum burst length.

786 ### 5.4.2   Start-of-Transmission

787 After a Transmit request, a Data Lane leaves the Stop state and prepares for High-Speed mode by means of
788 a Start-of-Transmission (SoT) procedure. Table 3 describes the sequence of events on TX and RX side.

789   **Table 3 Start-of-Transmission Sequence**

TX Side	RX Side
Drives Stop state (LP-11)	Observes Stop state
Drives HS-Rqst state (LP-01) for time T_{LPX}	Observes transition from LP-11 to LP-01 on the Lines
Drives Bridge state (LP-00) for time $T_{HS\text{-}PREPARE}$	Observes transition form LP-01 to LP-00 on the Lines, enables Line Termination after time $T_{D\text{-}TERM\text{-}EN}$
Enables High-Speed driver and disables Low-Power drivers simultaneously.	
Drives HS-0 for a time $T_{HS\text{-}ZERO}$	Enables HS-RX and waits for timer $T_{HS\text{-}SETTLE}$ to expire in order to neglect transition effects
	Starts looking for Leader-Sequence
Inserts the HS Sync-Sequence '00011101' beginning on a rising Clock edge	
	Synchronizes upon recognition of Leader Sequence '011101'
Continues to Transmit High-Speed payload data	

TX Side	RX Side
	Receives payload data

5.4.3 End-of-Transmission

At the end of a Data Burst, a Data Lane leaves High-Speed Transmission mode and enters the Stop state by means of an End-of-Transmission (EoT) procedure. Table 4 shows a possible sequence of events during the EoT procedure. Note, EoT processing may be handled by the protocol or by the D-PHY.

Table 4 End-of-Transmission Sequence

TX Side	RX Side
Completes Transmission of payload data	Receives payload data
Toggles differential state immediately after last payload data bit and keeps that state for a time $T_{HS\text{-}TRAIL}$	
Disables the HS-TX, enables the LP-TX, and drives Stop state (LP-11) for a time $T_{HS\text{-}EXIT}$	Detects the Lines leaving LP-00 state and entering Stop state (LP-11) and disables Termination
	Neglect bits of last period $T_{HS\text{-}SKIP}$ to hide transition effects
	Detect last transition in valid Data, determine last valid Data byte and skip trailer sequence

5.4.4 HS Data Transmission Burst

Figure 14 shows the sequence of events during the transmission of a Data Burst. Transmission can be started and ended independently for any Lane by the protocol. However, for most applications the Lanes will start synchronously but may end at different times due to an unequal amount of transmitted bytes per Lane. The handshake with the protocol-layer is described in Annex A.
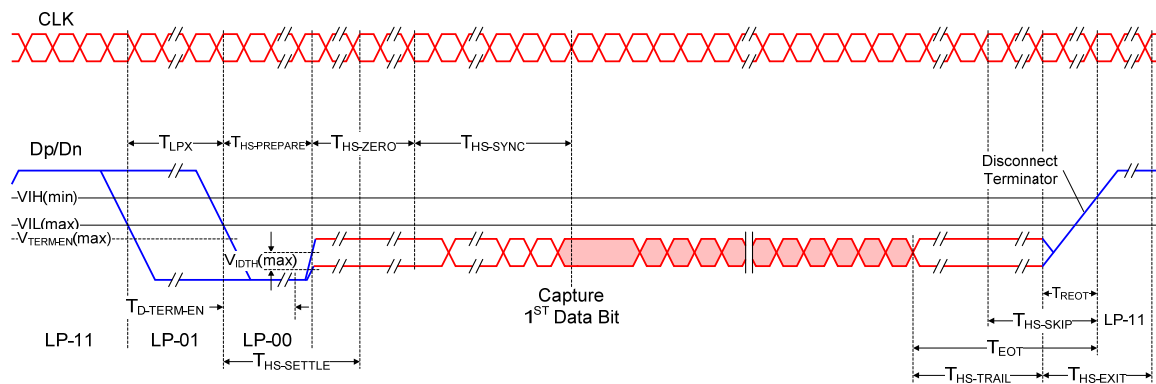
Figure 14 High-Speed Data Transmission in Bursts

Figure 15 shows the state machine for High-Speed data transmission that is described in Table 5.

Note: Horizontally aligned states occur simultaneously.

804
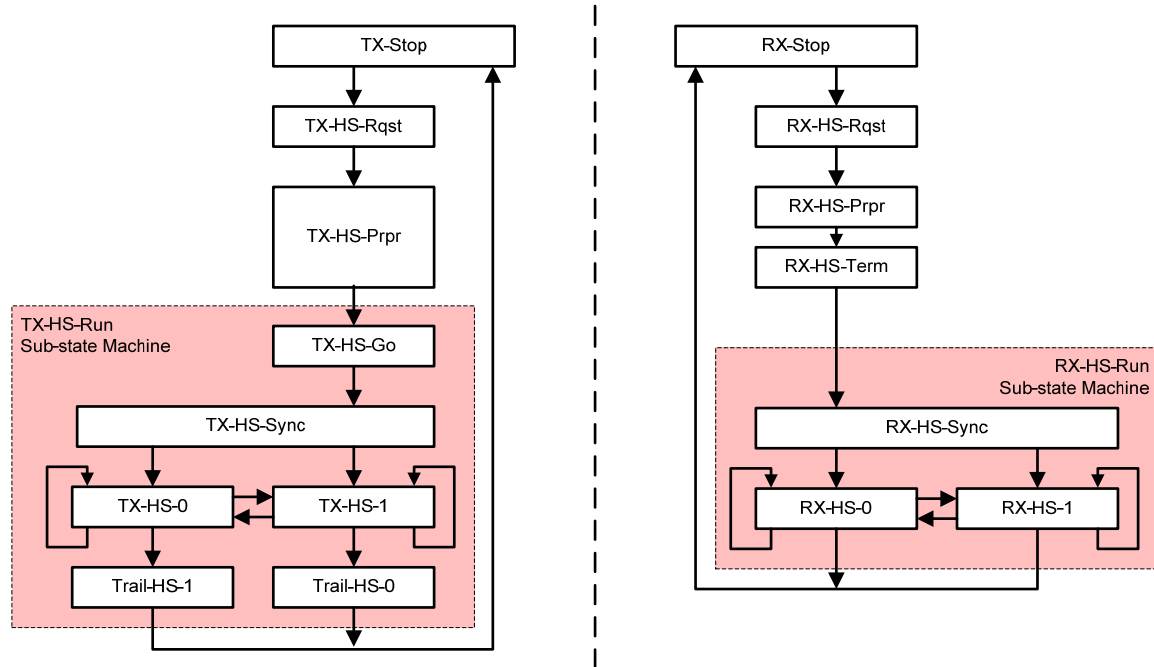
Figure 15 TX and RX State Machines for High-Speed Data Transmission

805

806   **Table 5 High-Speed Data Transmission State Machine Description**

State	Line Condition/State	Exit State	Exit Conditions
TX-Stop	Transmit LP-11	TX-HS-Rqst	On request of Protocol for High-Speed Transmission
TX-HS-Rqst	Transmit LP-01	TX-Bridge	End of timed interval T_{LPX}
TX-HS-Prpr	Transmit LP-00	TX-HS-Go	End of timed interval $T_{HS-PREPARE}$
TX-HS-Go	Transmit HS-0	TX-HS-Sync	End of timed interval $T_{HS-ZERO}$
TX-HS-Sync	Transmit sequence HS-00011101	TX-HS-0	After Sync sequence if first payload data bit is 0
		TX-HS-1	After Sync sequence if first payload data bit is 1
TX-HS-0	Transmit HS-0	TX-HS-0	Send another HS-0 bit after a HS-0 bit
		TX-HS-1	Send a HS-1 bit after a HS-0 bit
		Trail-HS-1	Last payload bit is HS-0, trailer sequence is HS-1
TX-HS-1	Transmit HS-1	TX-HS-0	Send a HS-1 bit after a HS-0 bit
		TX-HS-1	Send another HS-1 bit after a HS-1
		Trail-HS-0	Last payload bit is HS-1, trailer sequence is HS-0
Trail-HS-0	Transmit HS-0	TX-Stop	End of timed interval $T_{HS-TRAIL}$

State	Line Condition/State	Exit State	Exit Conditions
Trail-HS-1	Transmit HS-1	TX-Stop	End of timed interval $T_{HS-TRAIL}$
RX-Stop	Receive LP-11	RX-HS-Rqst	Line transition to LP-01
RX- HS-Rqst	Receive LP-01	RX-HS-Prpr	Line transition to LP-00
RX-HS- Prpr	Receive LP-00	RX-HS-Term	End of timed interval $T_{D-TERM-EN}$
RX-HS-Term	Receive LP-00	RX-HS-Sync	End of timed interval $T_{HS-SETTLE}$
RX-HS-Sync	Receive HS sequence …00000011101	RX-HS-0	Proper match found (any single bit error allowed) for Sync sequence in HS stream, the following bits are payload data.
		RX-HS-1	
RX-HS-0	Receive HS-0	RX-HS-0	Receive payload data bit or trailer bit
		RX-HS-1	
		RX-Stop	Line transition to LP-11
RX-HS-1	Receive HS-1	RX-HS-0	Receive payload data bit or trailer bit
		RX-HS-1	
		RX-Stop	Line transition to LP-11

807   Notes:

808   Stop states (TX-Stop, RX-Stop) have multiple valid exit states.

809   ## 5.5   Bi-directional Data Lane Turnaround

810   The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround
811   procedure. This procedure enables information transfer in the opposite direction of the current direction.
812   The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward
813   direction. Notice that Master and Slave side shall not be changed by Turnaround. Link Turnaround shall be
814   handled completely in Control mode. Table 6 lists the sequence of events during Turnaround.

815   **Table 6 Link Turnaround Sequence**

Initial TX Side = Final RX Side	Initial RX Side = Final TX Side
Drives Stop state (LP-11)	Observes Stop state
Drives LP-Rqst state (LP-10) for a time T_{LPX}	Observes transition from LP-11 to LP-10 states
Drives Bridge state (LP-00) for a time T_{LPX}	Observes transition from LP-10 to LP-00 states
Drives LP-10 for a time T_{LPX}	Observes transition from LP-00 to LP-10 states
Drives Bridge state (LP-00) for a time T_{TA-GO}	Observes the transition from LP-10 to Bridge state and waits for a time $T_{TA-SURE}$. After correct completion of this time-out this side knows it is in control.
	Drives Bridge state (LP-00) for a period T_{TA-GET}

Initial TX Side = Final RX Side	Initial RX Side = Final TX Side
Stops driving the Lines and observes the Line states with its LP-RX in order to see an acknowledgement.	
	Drives LP-10 for a period T_{LPX}
Observes LP-10 on the Lines, interprets this as acknowledge that the other side has indeed taken control. Waits for Stop state to complete Turnaround procedure.	
	Drives Stop state (LP-11) for a period T_{LPX}
Observes transition to Stop state (LP-11) on the Lines, interprets this as Turnaround completion acknowledgement, switches to normal LP receive mode and waits for further actions from the other side	

816   Figure 16 shows the Turnaround procedure graphically.

817
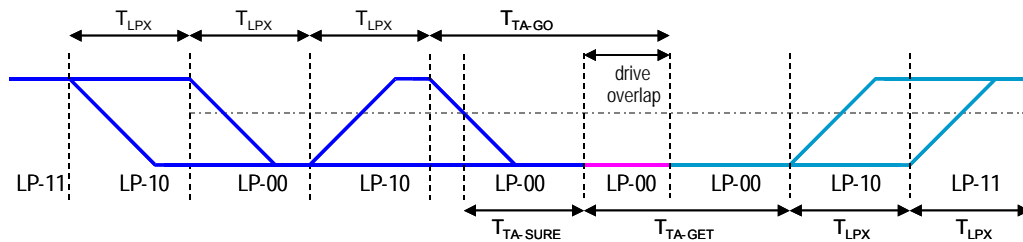
818   **Figure 16 Turnaround Procedure**

819   The Low-Power clock timing for both sides of the Link does not have to be the same, but may differ.
820   However, the ratio between the Low-Power State Periods, T_{LPX}, is constrained to ensure proper
821   Turnaround behavior. See Table 14 for the ratio of $T_{LPX(MASTER)}$ to $T_{LPX(SLAVE)}$.

822   The Turnaround procedure can be interrupted if the Lane is not yet driven into TX-LP-Yield by means of
823   driving a Stop state. Driving the Stop state shall abort the Turnaround procedure and return the Lane to the
824   Stop state. The PHY shall ensure against interruption of the procedure after the end of TX-TA-Rqst, RX-
825   TA-Rqst, or TX-TA-GO. Once the PHY drives TX-LP-Yield, it shall not abort the Turnaround procedure.
826   The Protocol may take appropriate action if it determines an error has occurred because the Turnaround
827   procedure did not complete within a certain time. See section 6.3.5 for more details. Figure 17 shows the
828   Turnaround state machine that is described in Table 7.

Note: Horizontally aligned states occur simultaneously.

829
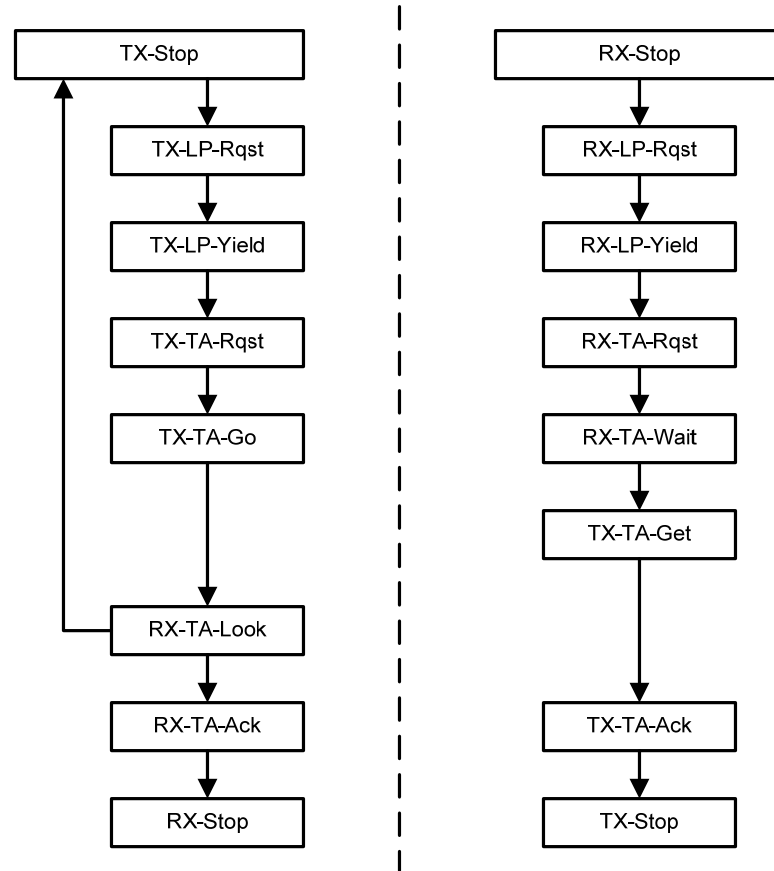
Figure 17 Turnaround State Machine

831

Table 7 Turnaround State Machine Description

State	Line Condition/State	Exit State	Exit Conditions
Any RX state	Any Received	RX-Stop	Observe LP-11 at Lines
TX-Stop	Transmit LP-11	TX-LP-Rqst	On request of Protocol for Turnaround
TX-LP-Rqst	Transmit LP-10	TX-LP-Yield	End of timed interval T_{LPX}
TX-LP-Yield	Transmit LP-00	TX-TA-Rqst	End of timed interval T_{LPX}
TX-TA-Rqst	Transmit LP-10	TX-TA-Go	End of timed interval T_{LPX}
TX-TA-Go	Transmit LP-00	RX-TA-Look	End of timed interval T_{TA-GO}
RX-TA-Look	Receive LP-00	RX-TA-Ack	Line transition to LP-10
RX-TA-Ack	Receive LP-10	RX-Stop	Line transition to LP-11
RX-Stop	Receive LP-11	RX-LP-Rqst	Line transition to LP-10
RX-LP-Rqst	Receive LP-10	RX-LP-Yield	Line transition to LP-00
RX-LP-Yield	Receive LP-00	RX-TA-Rqst	Line transition to LP-10

State	Line Condition/State	Exit State	Exit Conditions
RX-TA-Rqst	Receive LP-10	RX-TA-Wait	Line transition to LP-00
RX-TA-Wait	Receive LP-00	TX-TA-Get	End of timed interval $T_{TA-SURE}$
TX-TA-Get	Transmit LP-00	TX-TA-Ack	End of timed interval T_{TA-GET}
TX-TA-Ack	Transit LP-10	TX-Stop	End of timed interval T_{LPX}

832   Notes:

833   During RX-TA-Look, the protocol may cause the PHY to transition to TX-Stop.

834   During High-Speed data transmission, Stop states (TX-Stop, RX-Stop) have multiple valid exit states.

835   5.6   Escape Mode

836   Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some
837   additional functionality becomes available. Escape mode operation shall be supported in the Forward
838   direction and is optional in the Reverse direction. If supported, Escape mode does not have to include all
839   available features.

840   A Data Lane shall enter Escape mode via an Escape mode Entry procedure (LP-11, LP-10, LP-00, LP-01,
841   LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape
842   mode in Space state (LP-00). If an LP-11 is detected at any time before the final Bridge state (LP-00), the
843   Escape mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop
844   state.

845   For Data Lanes, once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate
846   the requested action. Table 8 lists all currently available Escape mode commands and actions. All
847   unassigned commands are reserved for future expansion.

848   The Stop state shall be used to exit Escape mode and cannot occur during Escape mode operation because
849   of the Spaced-One-Hot encoding. Stop state immediately returns the Lane to Control mode. If the entry
850   command doesn't match a supported command, that particular Escape mode action shall be ignored and the
851   receive side waits until the transmit side returns to the Stop state.

852   The PHY in Escape mode shall apply Spaced-One-Hot bit encoding for asynchronous communication.
853   Therefore, operation of a Data Lane in this mode does not depend on the Clock Lane. The complete Escape
854   mode action for a Trigger-Reset command is shown in Figure 18.

LP-11>10>00>01>00>01>00>10>00>...

LP CLK = EXOR(Dp, Dn)

855
856
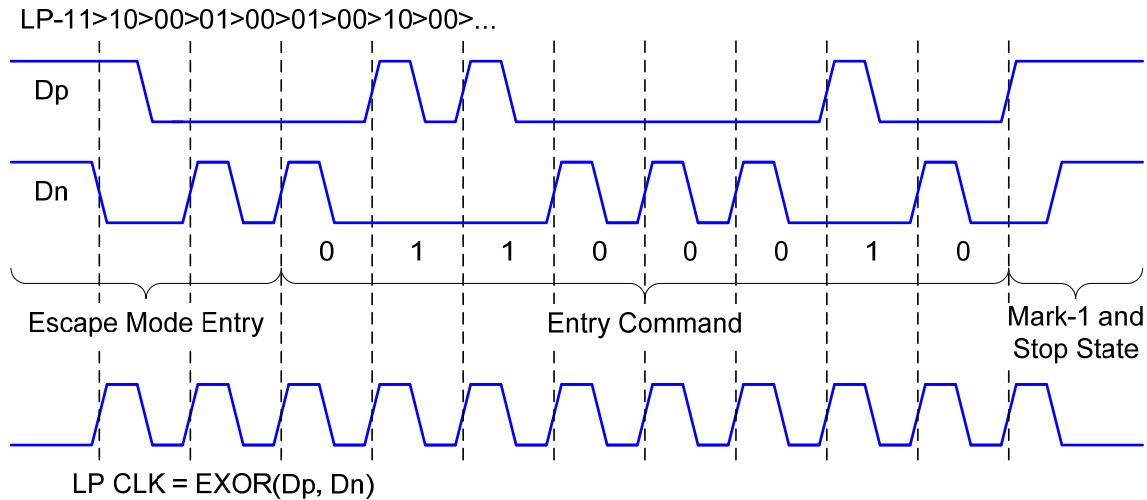
857   **Figure 18 Trigger-Reset Command in Escape Mode**

858   Spaced-One-Hot coding means that each Mark state is interleaved with a Space state. Each symbol consists
859   therefore of two parts: a One-Hot phase (Mark-0 or Mark-1) and a Space phase. The TX shall send Mark-0
860   followed by a Space to transmit a 'zero-bit' and it shall send a Mark-1 followed by a Space to transmit a
861   'one-bit'. A Mark that is not followed by a Space does not represent a bit. The last phase before exiting
862   Escape mode with a Stop state shall be a Mark-1 state that is not part of the communicated bits, as it is not
863   followed by a Space state. The Clock can be derived from the two Line signals, Dp and Dn, by means of an
864   exclusive-OR function. The length of each individual LP state period shall be at least $T_{LPX,MIN}$.

865   **Table 8 Escape Entry Codes**

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low Power State	mode	00011110
Undefined-1	mode	10011111
Undefined-2	mode	11011110
Reset-Trigger [Remote Application]	Trigger	01100010
Unknown-3	Trigger	01011101
Unknown-4	Trigger	00100001
Unknown-5	Trigger	10100000

866   ## 5.6.1   Remote Triggers

867   Trigger signaling is the mechanism to send a flag to the protocol at the receiving side, on request of the
868   protocol on the transmitting side. This can be either in the Forward or Reverse direction depending on the
869   direction of operation and available Escape mode functionality. Trigger signaling requires Escape mode
870   capability and at least one matching Trigger Escape Entry Command on both sides of the interface.

871   Figure 18 shows an example of an Escape mode Reset-Trigger action. The Lane enters Escape mode via
872   the Escape mode Entry procedure. If the Entry Command Pattern matches the Reset-Trigger Command a

873   Trigger is flagged to the protocol at the receive side via the logical PPI. Any bit received after a Trigger
874   Command but before the Lines go to Stop state shall be ignored. Therefore, dummy bytes can be
875   concatenated in order to provide Clock information to the receive side.

876   Note that Trigger signaling including Reset-Trigger is a generic messaging system. The Trigger commands
877   do not impact the behavior of the PHY itself. Therefore, Triggers can be used for any purpose by the
878   Protocol layer.

879   ## 5.6.2   Low-Power Data Transmission

880   If the Escape mode Entry procedure is followed-up by the Entry Command for Low-Power Data
881   Transmission (LPDT), Data can be communicated by the protocol at low speed, while the Lane remains in
882   Low-Power mode.

883   Data shall be encoded on the lines with the same Spaced-One-Hot code as used for the Entry Commands.
884   The data is self-clocked by the applied bit encoding and does not rely on the Clock Lane. The Lane can
885   pause while using LPDT by maintaining a Space state on the Lines. A Stop state on the Lines stops LPDT,
886   exits Escape mode, and switches the Lane to Control mode. The last phase before Stop state shall be a
887   Mark-1 state, which does not represent a data-bit. Figure 19 shows a two-byte transmission with a pause
888   period between the two bytes.

889
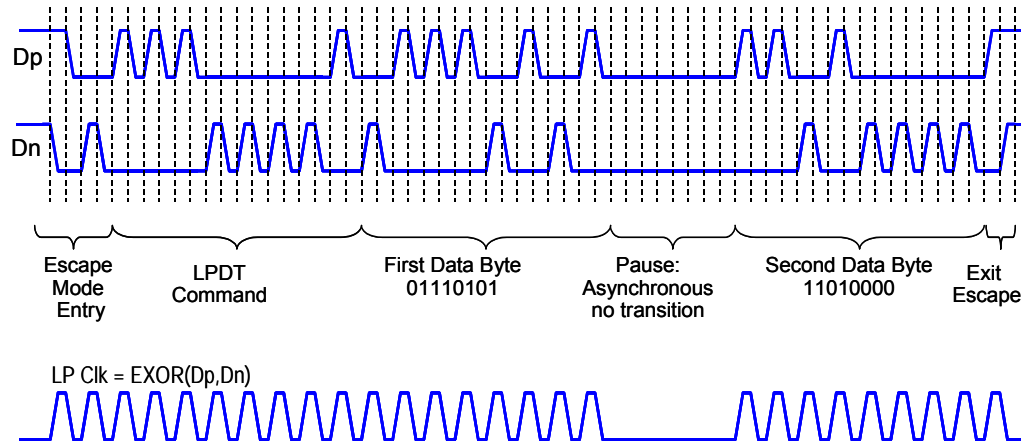
890   **Figure 19 Two Data Byte Low-Power Data Transmission Example**

891   Using LPDT, a Low-Power (Bit) Clock signal ($f_{MOMENTARY}$<20MHz) provided to the transmit side is used
892   to transmit data. Data reception is self-timed by the bit encoding. Therefore, a variable clock rate can be
893   allowed. At the end of LPDT the Lane shall return to the Stop state.

894   ## 5.6.3   Ultra-Low Power State

895   If the Ultra-Low Power State Entry Command is sent after an Escape mode Entry command, the Lane shall
896   enter the Ultra-Low Power State (ULPS). This command shall be flagged to the receive side Protocol.
897   During this state, the Lines are in the Space state (LP-00). Ultra-Low Power State is exited by means of a
898   Mark-1 state with a length T_{WAKEUP} followed by a Stop state. Annex A describes an example of an exit
899   procedure and a procedure to control the length of time spent in the Mark-1 state.

900   ## 5.6.4   Escape Mode State Machine

901   The state machine for Escape mode operation is shown in Figure 20 and described in Table 9.

Note: Horizontally aligned states occur simultaneously.

902
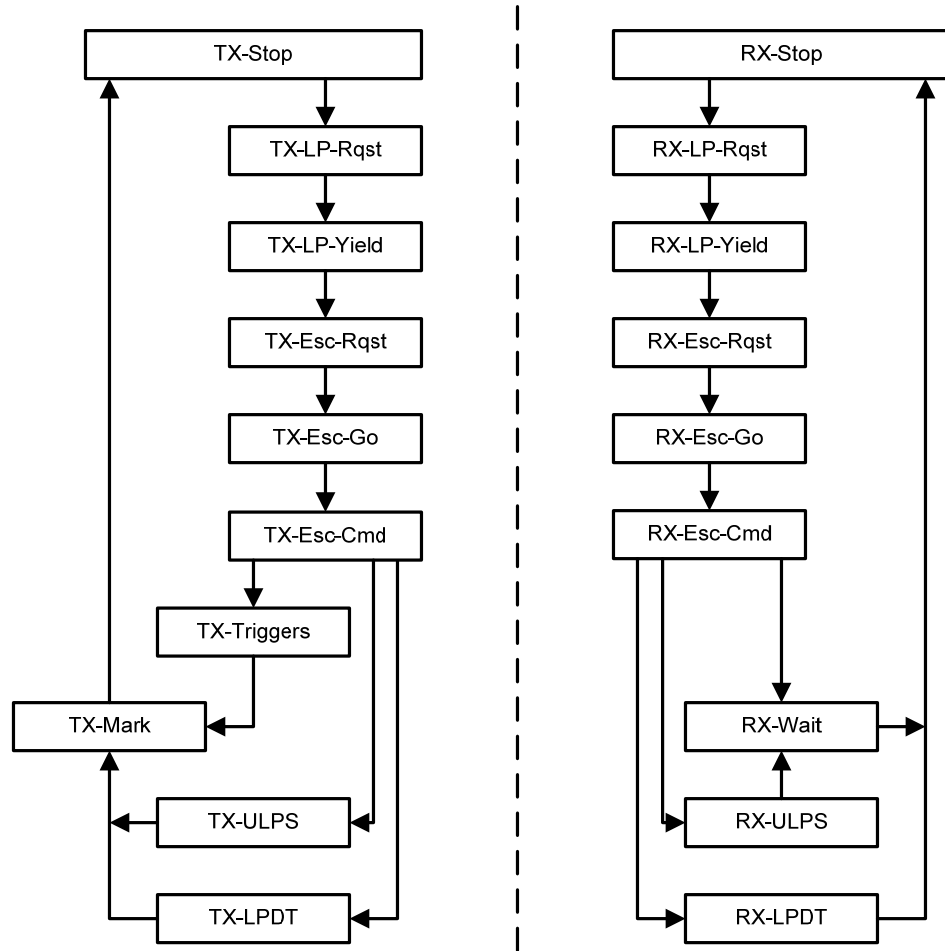
903   **Figure 20 Escape Mode State Machine**

904   **Table 9 Escape Mode State Machine Description**

State	Line Condition/State	Exit State	Exit Conditions
Any RX state	Any Received	RX-Stop	Observe LP-11 at Lines
TX-Stop	Transmit LP-11	TX-LP-Rqst	On request of Protocol for Esc mode (PPI)
TX-LP-Rqst	Transmit LP-10	TX-LP-Yield	After time T_{LPX}
TX-LP-Yield	Transmit LP-00	TX-Esc-Rqst	After time T_{LPX}
TX-Esc-Rqst	Transmit LP-01	TX-Esc-Go	After time T_{LPX}
TX-Esc-Go	Transmit LP-00	TX-Esc-Cmd	After time T_{LPX}
TX-Esc-Cmd	Transmit sequence of 8-bit (16-line-states) One-Spaced-Hot encoded Entry Command	TX-Triggers	After a Trigger Command
		TX-ULPS	After Ultra-Low Power Command

State	Line Condition/State	Exit State	Exit Conditions
		TX-LPDT	After Low-Power Data Transmission Command
TX-Triggers	Space state or optional dummy bytes for the purpose of generating clocks	TX-Mark	Exit of the Trigger State on request of Protocol (PPI)
TX-ULPS	Transmit LP-00	TX-Mark	End of ULP State on request of Protocol (PPI)
TX-LPDT	Transmit serialized, Spaced-One-Hot encoded payload data		After last transmitted data bit
TX-Mark	Mark-1	TX-Stop	Next driven state after time T_{LPX}, or T_{WAKEUP} if leaving ULP State
RX-Stop	Receive LP-11	RX-LP-Rqst	Line transition to LP-10
RX-LP-Rqst	Receive LP-10	RX-LP-Yield	Line transition to LP-00
RX-LP-Yield	Receive LP-00	RX-Esc-Rqst	Line transition to LP-01
RX-Esc-Rqst	Receive LP-01	RX-Esc-Go	Line transition to LP-00
RX-Esc-Go	Receive LP-00	RX-Esc-Cmd	Line transition out of LP-00
RX-Esc-Cmd	Receive sequence of 8-bit (16-line-states) One-Spaced-Hot encoded Entry Command	RX-Wait	After Trigger and Unrecognized Commands
		RX-ULPS	After Ultra-Low Power Command
		RX-LPDT	After Low-Power Data Transmission Command
RX-ULPS	Receive LP-00	RX-Wait	Line transition to LP-10
RX-LPDT	Receive serial, Spaced-One-Hot encoded payload data	RX-Stop	Line transition to LP-11 (Last state should be a Mark-1)
RX-Wait	Any, except LP-11	RX-Stop	Line transition to LP-11

905   Notes:

906   During High-Speed data transmission, Stop states (TX-Stop, RX-Stop) have multiple valid exit states.

907   **5.7   High-Speed Clock Transmission**

908   In High-Speed mode the Clock Lane provides a low-swing, differential DDR (half-rate) clock signal from
909   Master to Slave for High-Speed Data Transmission. The Clock signal shall have quadrature-phase with
910   respect to a toggling bit sequence on a Data Lane in the Forward direction and a rising edge in the center of
911   the first transmitted bit of a burst. Details of the Data-Clock relationship and timing specifications can be
912   found in section 9.

913 A Clock Lane is similar to a Unidirectional Data Lane. However, there are some timing differences and a
914 Clock Lane transmits a High-Speed DDR clock signal instead of data bits. Furthermore, the Low-Power
915 mode functionality is defined differently for a Clock Lane than a Data Lane. A Clock Lane shall be
916 unidirectional and shall not include regular Escape mode functionality. Only ULPS shall be supported via a
917 special entry sequence using the LP-Rqst state. High-Speed Clock Transmission shall start from, and exit
918 to, a Stop state.

919 The Clock Lane module is controlled by the Protocol via the Clock Lane PPI. The Protocol shall only stop
920 the Clock Lane when there are no High-Speed transmissions active in any Data Lane.

921 The High-Speed Data Transmission start-up time of a Data Lane is extended if the Clock Lane is in Low-
922 Power mode. In that case the Clock Lane shall first return to High-Speed operation before the Transmit
923 Request can be handled.

924 The High-Speed Clock signal shall continue running for a period $T_{CLK-POST}$ after the last Data Lane
925 switches to Low-Power mode and ends with a HS-0 state. The procedure for switching the Clock Lane to
926 Low-Power mode is given in Table 10. Note the Clock Burst always contains an even number of
927 transitions as it starts and ends with a HS-0 state. This implies that the clock provides transitions to sample
928 an even number of bits on any associated Data Lanes. Clock periods shall be reliable and according to the
929 HS timing specifications. The procedure to return the Clock Lane to High-Speed Clock Transmission is
930 given in Table 11. Both Clock Start and Stop procedures are shown in Figure 21.
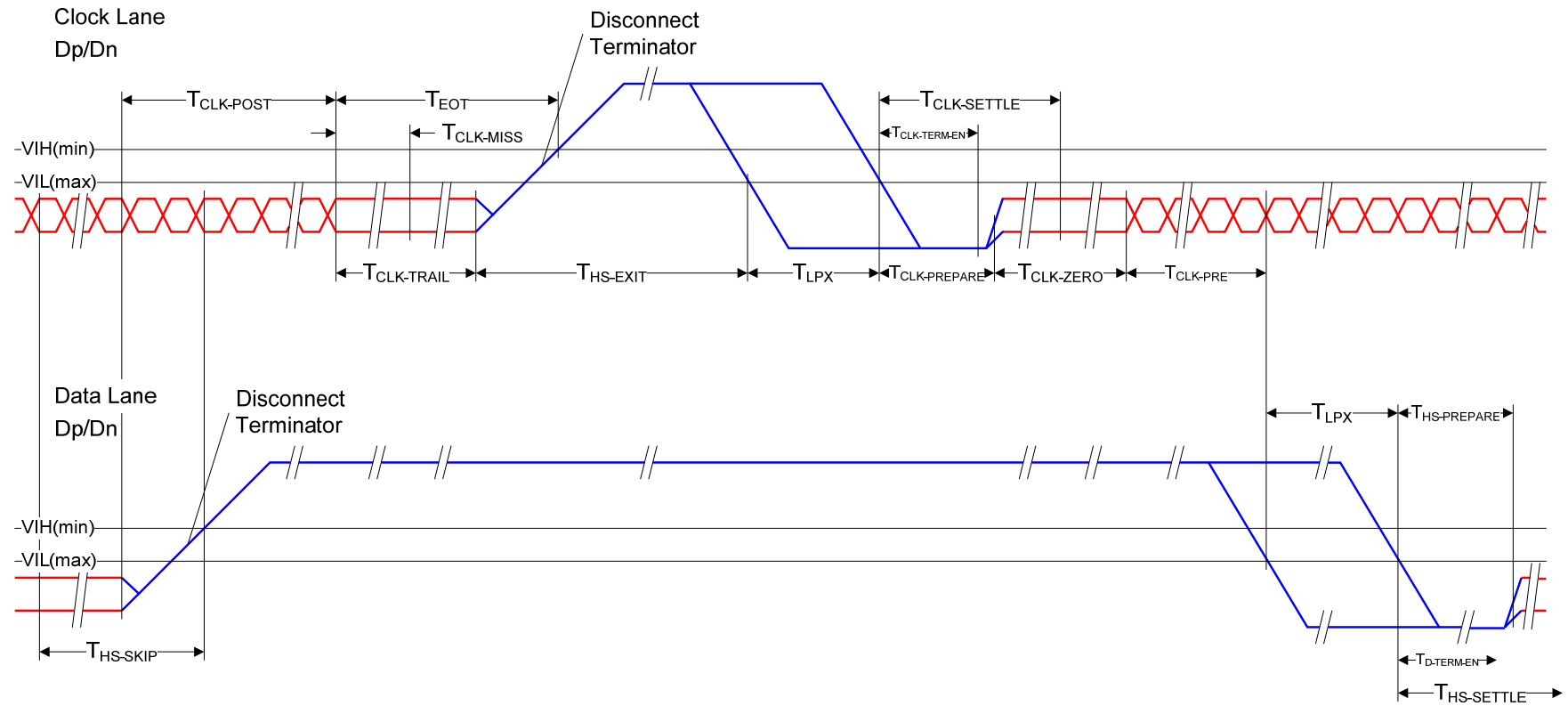
Figure 21 Switching the Clock Lane between Clock Transmission and Low-Power Mode

934 **Table 10 Procedure to Switch Clock Lane to Low-Power Mode**

Master Side	Slave Side
Drives High-Speed Clock signal (Toggling HS-0/HS-1)	Receives High-Speed Clock signal (Toggling HS-0/HS-1)
Last Data Lane goes into Low-Power mode	
Continues to drives High-Speed Clock signal for a period $T_{CLK-POST}$ and ends with HS-0 state	
Drives HS-0 for a time $T_{CLK-TRAIL}$	Detects absence of Clock transitions within a time $T_{CLK-MISS}$, disables HS-RX then waits for a transition to the Stop state
Disables the HS-TX, enables LP-TX, and drives Stop state (LP-11) for a time $T_{HS-EXIT}$	
	Detects the Lines transitions to LP-11, disables HS termination, and enters Stop state

935 **Table 11 Procedure to Initiate High-Speed Clock Transmission**

TX Side	RX Side
Drives Stop state (LP-11)	Observes Stop state
Drives HS-Req state (LP-01) for time T_{LPX}	Observes transition from LP-11 to LP-01 on the Lines
Drives Bridge state (LP-00) for time $T_{CLK-PREPARE}$	Observes transition from LP-01 to LP-00 on the Lines. Enables Line Termination after time $T_{CLK-TERM-EN}$
Enables High-Speed driver and disables Low-Power drivers simultaneously. Drives HS-0 for a time $T_{CLK-ZERO}$.	Enables HS-RX and waits for timer $T_{CLK-SETTLE}$ to expire in order to neglect transition effects
	Receives HS-signal
Drives the High-Speed Clock signal for time period $T_{CLK-PRE}$ before any Data Lane starts up	Receives High-Speed Clock signal

936   The Clock Lane state machine is shown in Figure 22 and is described in Table 12.
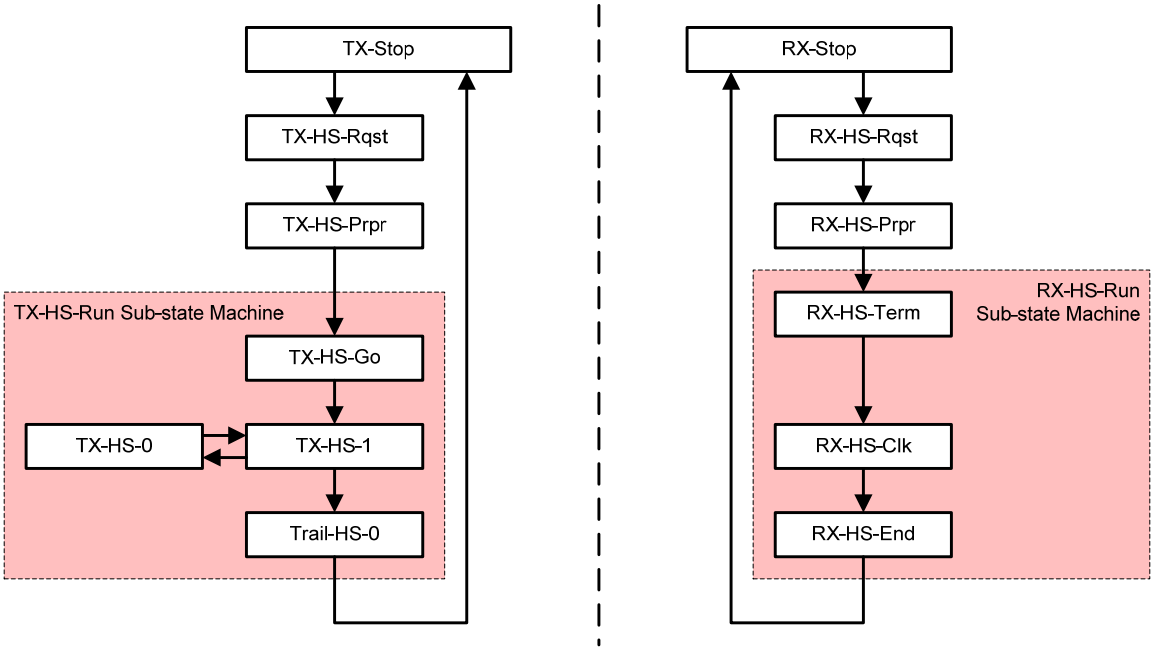
Note: Horizontally aligned states
937   occur simultaneously.

938   **Figure 22 High-Speed Clock Transmission State Machine**

939   **Table 12 Description of High-Speed Clock Transmission State Machine**

State	Line Condition/State	Exit State	Exit Conditions
TX-Stop	Transmit LP-11	TX-HS-Rqst	On request of Protocol for High-Speed Transmission
TX-HS-Rqst	Transmit LP-01	TX-HS-Prpr	End of timed interval T_{LPX}
TX-HS-Prpr	Transmit LP-00	TX-HS-Go	End of timed interval $T_{CLK\text{-}PREPARE}$
TX-HS-Go	Transmit HS-0	TX-HS-1	End of timed interval $T_{CLK\text{-}ZERO}$
TX-HS-0	Transmit HS-0	TX-HS-1	Send a HS-1 phase after a HS-0 phase: DDR Clock
TX-HS-1	Transmit HS-1	TX-HS-0	Send a HS-0 phase after a HS-1 phase: DDR Clock
		Trail-HS-0	On request to put Clock Lane in Low-Power
Trail-HS-0	Transmit HS-0	TX-Stop	End of timed interval $T_{CLK\text{-}TRAIL}$

State	Line Condition/State	Exit State	Exit Conditions
RX-Stop	Receive LP-11	RX-HS-Rqst	Line transition to LP-01
RX-HS-Rqst	Receive LP-01	RX-HS-Prpr	Line transition to LP-00
RX-HS-Prpr	Receive LP-00	RX-HS-Term	End of timed interval $T_{CLK-TERM-EN}$
RX-HS-Term	Receive LP-00	RX-HS-Clk	End of timed interval $T_{CLK-SETTLE}$
RX-HS-Clk	Receive DDR-Q Clock signal	RX-Clk-End	Time-out $T_{CLK-MISS}$ on the period on the Clock Lane without Clock signal transitions
RX-HS-End	Receive HS-0	RX-HS-Stop	Line transition to LP-11

940 Notes:

941 During High-Speed data transmission, Stop states (TX-Stop, RX-Stop) have multiple valid exit states.

5.8 Clock Lane Ultra-Low Power State

943 Although a Clock Lane does not include regular Escape mode, the Clock Lane shall support the Ultra-Low
944 Power State.

945 A Clock Lane shall enter Ultra-Low Power State via a Clock Lane Ultra-Low Power State Entry
946 procedure. In this procedure, starting from Stop state, the transmit side shall drive TX-ULPS-Rqst State
947 (LP-10) and then drive TX-ULPS State (LP-00). After this, the Clock Lane shall enter Ultra-Low Power
948 State. If an error occurs, and an LP-01 or LP-11 is detected immediately after the TX-ULPS-Rqst state, the
949 Ultra-Low Power State Entry procedure shall be aborted, and the receive side shall wait for, or return to,
950 the Stop state, respectively.

951 The receiving PHY shall flag the appearance of ULP State to the receive side Protocol. During this state
952 the Lines are in the ULP State (LP-00). Ultra-Low Power State is exited by means of a Mark-1 TX-ULPS-
953 Exit State with a length T_{WAKEUP} followed by a Stop State. Annex A describes an example of an exit
954 procedure that allows control of the length of time spent in the Mark-1 TX-ULPS-Exit State.

Note: Horizontally aligned states occur simultaneously.

955
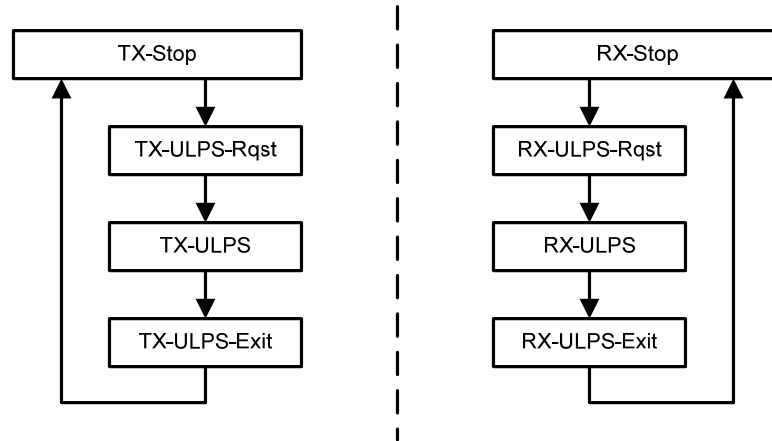
Figure 23 Clock Lane Ultra-Low Power State State Machine

957

Table 13 Clock Lane Ultra-Low Power State State Machine Description

State	Line Condition/State	Exit State	Exit Conditions
TX-Stop	Transmit LP-11	TX-ULPS-Rqst	On request of Protocol for Ultra-Low Power State
TX-ULPS-Rqst	Transmit LP-10	TX-ULPS	End of timed interval T_{LPX}
TX-ULPS	Transmit LP-00	TX-ULPS-Exit	On request of Protocol to leave Ultra-Low Power State
TX-ULPS-Exit	Transmit LP-10	TX-Stop	End of timed interval T_{WAKEUP}
RX-Stop	Receive LP-11	RX-ULPS-Rqst	Line transition to LP-10
RX-ULPS-Rqst	Receive LP-10	RX-ULPS	Line transition to LP-00
RX-ULPS	Receive LP-00	RX-ULPS-Exit	Line transition to LP-10
RX-ULPS-Exit	Receive LP-10	RX-Stop	Line transition to LP-11

958   Notes:

959   During High-Speed data transmission, Stop states (TX-Stop, RX-Stop) have multiple valid exit states.
960

961   ## 5.9   Global Operation Timing Parameters

962   Table 14 lists the ranges for all timing parameters used in this section. The values in the table assume a
963   clock tolerance no worse than ±10% for implementation.

964   Transmitters shall support all transmitter-specific timing parameters defined in Table 14.

965   Receivers shall support all Receiver-specific timing parameters in defined in Table 14.

966   Also note that while corresponding receiver tolerances are not defined for every transmitter-specific
967   parameter, receivers shall also support reception of all allowed conformant values for all transmitter-
968   specific timing parameters in Table 14 for all HS UI values up to, and including, the maximum supported
969   HS clock rate specified in the receiver's datasheet.

Table 14 Global Operation Timing Parameters

970

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns	1, 6
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI			ns	5
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI	5
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns	5
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPARE}$.	95		300	ns	6
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns	6
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns	5
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns	5
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns + 4*UI		6
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to the start of the LP-11 state following a HS burst.			105 ns + n*12*UI		3, 5
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100			ns	5

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + 4*UI		85 ns + 6*UI	ns	5
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI			ns	5
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$.	85 ns + 6*UI		145 ns + 10*UI	ns	6
$T_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55 ns + 4*UI	ns	6
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 ns + n*4*UI)			ns	2, 3, 5
T_{INIT}	See section 5.11.	100			μs	5
T_{LPX}	Transmitted length of any Low-Power state period	50			ns	4, 5
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	2/3		3/2		
T_{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	5*T_{LPX}			ns	5
T_{TA-GO}	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	4*T_{LPX}			ns	5
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T_{LPX}		2*T_{LPX}	ns	5
T_{WAKEUP}	Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1			ms	5

971 Notes

972 1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.

973 2. If a > b then max(a, b) = a otherwise max(a, b) = b

974 3. Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode

975 4. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

976 5. Transmitter-specific parameter

977 6. Receiver-specific parameter

978

979   ## 5.10   System Power States

980   Each Lane within a PHY configuration, that is powered and enabled, has potentially three different power
981   consumption levels: High-Speed Transmission mode, Low-Power mode and Ultra-Low Power State. For
982   details on Ultra-Low Power State see sections 5.6.3 and 5.8. The transition between these modes shall be
983   handled by the PHY.

984   ## 5.11   Initialization

985   After power-up, the Slave side PHY shall be initialized when the Master PHY drives a Stop State (LP-11)
986   for a period longer then T_{INIT}. The first Stop state longer than the specified T_{INIT} is called the Initialization
987   period. The Master PHY itself shall be initialized by a system or Protocol input signal (PPI). The Master
988   side shall ensure that a Stop State longer than T_{INIT} does not occur on the Lines before the Master is
989   initialized. The Slave side shall ignore all Line states during an interval of unspecified length prior to the
990   Initialization period. In multi-Lane configurations, all Lanes shall be initialized simultaneously.

991   Note that T_{INIT} is considered a protocol-dependent parameter, and thus the exact requirements for
992    $T_{INIT,MASTER}$ and $T_{INIT,SLAVE}$ (transmitter and receiver initialization Stop state lengths, respectively,) are
993   defined by the protocol layer specification and are outside the scope of this document. However, the D-
994   PHY specification does place a minimum bound on the lengths of $T_{INIT,MASTER}$ and $T_{INIT,SLAVE}$, which each
995   shall be no less than 100 µs. A protocol layer specification using the D-PHY specification may specify any
996   values greater than this limit, for example, $T_{INIT,MASTER} \geq 1$ ms and $T_{INIT,SLAVE} = 500$ to 800 µs.

997   **Table 15 Initialization States**

State	Entry Conditions	Exit State	Exit Conditions	Line Levels
Master Off	Power-down	Master Initialization	Power-up	Any LP level except Stop States for periods >100us
Master Init	Power-up or Protocol request	TX-Stop	A First Stop state for a period longer than $T_{INIT,MASTER}$ as specified by the Protocol	Any LP signaling sequence that ends with a long Initialization Stop state
Slave Off	Power-down	Any LP state	Power-up	Any
Slave Init	Power-up or Protocol request	RX-Stop	Observe Stop state at the inputs for a period $T_{INIT,SLAVE}$ as specified by the Protocol	Any LP signaling sequence which ends with the first long Initialization Stop period

998   ## 5.12   Calibration

999   There is no explicit calibration required by the D-PHY specification. If an implementation requires
1000   calibration, the calibration can take place off-line during the initialization period T_{INIT} while the lines are in
1001   Stop state. The calibration process should not be visible on the Lines. Any further detail on calibration is
1002   outside the scope of this specification.

1003   **5.13   Global Operation Flow Diagram**

1004   All previously described aspects of operation, either including or excluding optional parts, are contained in
1005   Lane Modules. Figure 24 shows the operational flow diagram for a Data Lane Module. Within both TX
1006   and RX four main processes can be distinguished: High-Speed Transmission, Escape mode, Turnaround,
1007   and Initialization.

1008
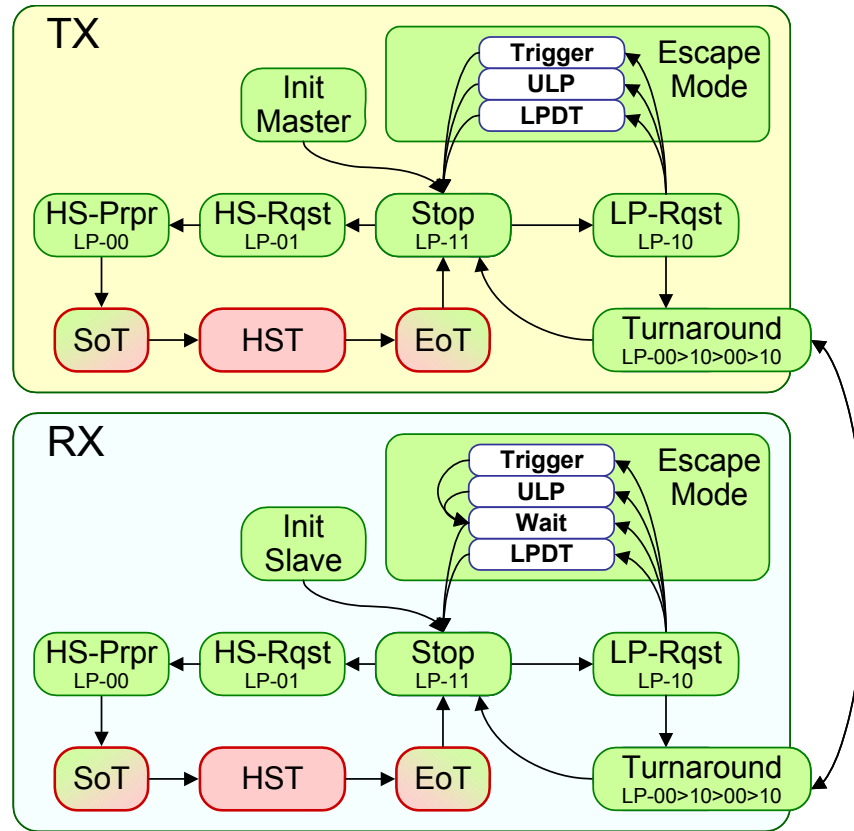
1009   **Figure 24 Data Lane Module State Diagram**

1010 Figure 25 shows the state diagram for a Clock Lane Module. The Clock Lane Module has four major
1011 operational states: Init (of unspecified duration), Low-Power Stop state, Ultra-Low Power state, and High-
1012 Speed clock transmission. The figure also shows the transition states as described previously.
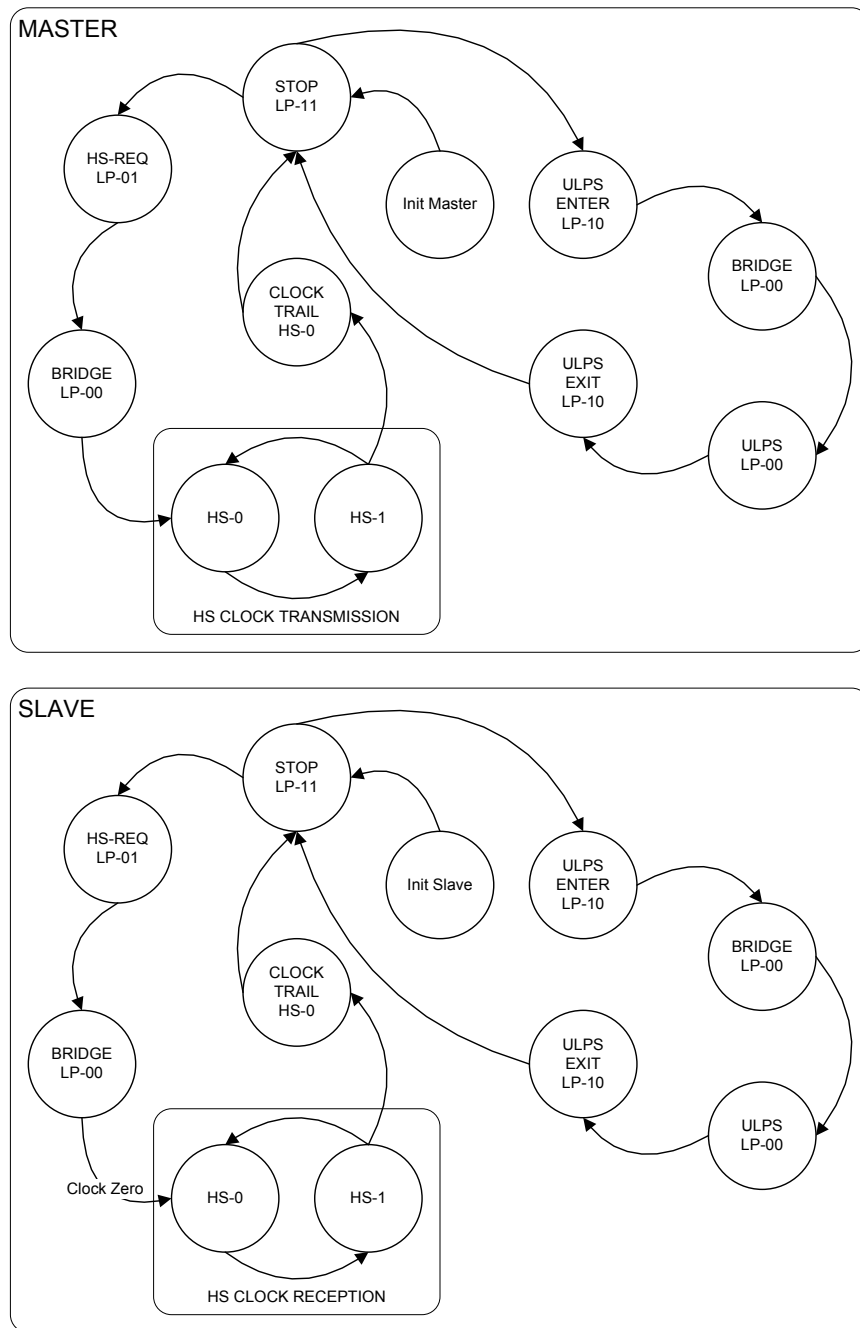
1013
1014 **Figure 25 Clock Lane Module State Diagram**

1015 **5.14 Data Rate Dependent Parameters (informative)**

1016 The high speed data transfer rate of the D-PHY may be programmable to values determined by a particular
1017 implementation. Any individual data transfer between SoT and EoT sequences must take place at a given,
1018 fixed rate. However, reprogramming the data rate of the D-PHY high speed transfer is allowed at

1019   initialization, before starting the exit from ULP state or in Stop state whenever the HS clock is not running.
1020   The method of data rate reprogramming is out of the scope of this document.

1021   Many time parameter values in this document are specified as the sum of a fixed time and a particular
1022   number of High-Speed UIs. The parameters may need to be recomputed if the data rate, and therefore the
1023   UI value, is changed. These parameters, with their allowed values, are listed in Table 14. For clarity, the
1024   parameter names and purposes are repeated here.

5.14.1   Parameters Containing Only UI Values

1026 $T_{CLK-PRE}$ is the minimum number of High-Speed clock cycles the Master must send over the Clock Lane
1027   after it is restarted in HS mode and before any data transmission may begin. If a particular protocol at the
1028   Slave side requires more clock cycles then $T_{CLK-PRE}$, the Master side protocol should ensure that these are
1029   transmitted.

5.14.2   Parameters Containing Time and UI values

1031   Several parameters are specified as the sum of an explicit time and a number of UI. The explicit time
1032   values, in general, are derived from the time needed to charge and discharge the interconnect to its
1033   specified values given the specified drive voltages and line termination values. As such, the explicit time
1034   values are not data rate dependent. It is conceivable to use the sum of an analog timer and a HS clock
1035   counter to ensure the implementation satisfies these parameters. If these explicit time values are
1036   implemented by counting HS clock cycles only, the count value is a function of the data rate and, therefore,
1037   must be changed when the data rate is changed.

1038 $T_{D-TERM-EN}$ is the time to enable Data Lane receiver line termination measured from when Dn crosses
1039 $V_{IL,MAX}$.

1040 $T_{HS-PREPARE}$, is the time to drive LP-00 before starting the HS transmission on a Data Lane.

1041 $T_{HS-PREPARE} + T_{HS-ZERO,MIN}$ is the sum of the time to drive LP-00 in preparation for the start of HS
1042   transmission plus the time to send HS-0, i.e. turn on the line termination and drive the interconnect with the
1043   HS driver, prior to sending the SoT Sync sequence.

1044 $T_{HS-TRAIL}$ is the time the transmitter must drive the flipped last data bit after sending the last payload data
1045   bit of a HS transmission burst. This time is required by the receiver to determine EoT.

1046 $T_{HS-SKIP}$ is the time the receiver must "back up" and skip data to ignore the transition period of the EoT
1047   sequence.

1048 $T_{CLK-POST,MIN}$ is the minimum time that the transmitter continues sending HS clocks after the last Data Lane
1049   has transitioned to LP mode following a HS transmission burst. If a particular receiver implementation
1050   requires more clock cycles than $T_{CLK-POST,MIN}$ to finish reception, the transmitter must supply sufficient
1051   clocks to accomplish the reception.

5.14.3   Parameters Containing Only Time Values

1053   Several parameters are specified only as explicit time values. As in section 5.14.2, these explicit time
1054   values are typically derived from the time needed to charge and discharge the interconnect and are,
1055   therefore, not data rate dependent. It is conceivable to use an analog timer or a HS clock counter to ensure
1056   the implementation satisfies these parameters. However, if these time values are implemented by counting
1057   HS clock cycles only, the count value is a function of the data rate and, therefore, must be changed when
1058   the data rate is changed.

1059   The following parameters are based on time values alone:

1060   • $T_{HS-SKIP,MIN}$

1061   • $T_{CLK-MISS,MAX}$

1062   • $T_{CLK-TRAIL,MIN}$

1063   • $T_{CLK-TERM-EN}$

1064   • $T_{CLK-PREPARE}$

5.14.4   Parameters Containing Only Time Values That Are Not Data Rate Dependent

1067   The remaining parameters in Table 14 shall be complied with even when the High-Speed clock is off.
1068   These parameters include Low-Power and initialization state durations and LP signaling intervals. Though
1069   these parameters are not HS data rate dependent, some implementations of D-PHY may need to adjust
1070   these values when the data rate is changed.
1071

1072　## 6　Fault Detection

1073　There are three different mechanisms to detect malfunctioning of the Link. Bus contention and error
1074　detection functions are contained within the D-PHY. These functions should detect many typical faults.
1075　However, some faults cannot be detected within the D-PHY and require a protocol-level solution.
1076　Therefore, the third detection mechanism is a set of application specific watchdog timers.

1077　### 6.1　Contention Detection

1078　If a bi-directional Lane Module and a Unidirectional Module are combined in one Lane, only
1079　unidirectional functionality is available. Because in this case the additional functionality of one bi-
1080　directional PHY Module cannot be reliably controlled from the limited functionality PHY side, the bi-
1081　directional features of the bi-directional Module shall be safely disabled. Otherwise in some cases deadlock
1082　may occur which can only be resolved with a system power-down and re-initialization procedure.

1083　During normal operation one and only one side of a Link shall drive a Lane at any given time except for
1084　certain transition periods. Due to errors or system malfunction a Lane may end up in an undesirable state,
1085　where the Lane is driven from two sides or not driven at all. This condition eventually results in a state
1086　conflict and is called Contention.

1087　All Lane Modules with LP bi-directionality shall include contention detection functions to detect the
1088　following contention conditions:

1089　• Modules on both sides of the same line drive opposite LP levels against each other. In this case,
1090　the line voltage will settle to some value between $V_{OL,MIN}$ and $V_{OH,MAX}$. Because V_{IL} is greater
1091　than V_{IHCD}, the settled value will always be either higher than V_{IHCD}, lower than V_{IL}, or both.
1092　Refer to section 8. This ensures that at least one side of the link, possibly both, will detect the fault
1093　condition.

1094　• The Module at one side drives LP-high while the other side drives HS-low on the same Line. In
1095　this case, the line voltage will settle to a value lower than V_{IL}. The contention shall be detected at
1096　the side that is transmitting the LP-high.

1097　The first condition can be detected by the combination of LP-CD and LP-RX functions. The LP-RX
1098　function should be able to detect the second contention condition. Details on the LP-CD and LP-RX
1099　electrical specifications can be found in section 8. Contention shall be checked at the end of every Low-
1100　Power bit period when the signals are settled, except in ULPS. Contention detection in ULPS is not
1101　required because there is no pre-defined bit period and a clock might not be available.

1102　After contention has been detected, the Protocol shall take proper measures to resolve the situation.

1103　### 6.2　Sequence Error Detection

1104　If for any reason the Lane signal is corrupted the receiving PHY may detect signal sequence errors. Errors
1105　detected inside the PHY may be communicated to the Protocol via the PPI. This kind of error detection is
1106　optional, but strongly recommended as it enhances reliability. The following sequence errors can be
1107　distinguished:

1108　• SoT Error

1109　• SoT Sync Error

1110　• EoT Sync Error

1111　• Escape Entry Command Error

1112   •   LP Transmission Sync Error

1113   •   False Control Error

6.2.1   SoT Error

1115   The Leader sequence for Start of High-Speed Transmission is fault tolerant for any single-bit error and
1116   some multi-bit errors. Therefore, the synchronization may be usable, but confidence in the payload data is
1117   lower. If this situation occurs an SoT Error is indicated.

6.2.2   SoT Sync Error

1119   If the SoT Leader sequence is corrupted in a way that proper synchronization cannot be expected, a SoT
1120   Sync Error is indicated.

6.2.3   EoT Sync Error

1122   The EoT Sync Error is indicated when the last bit of a transmission does not match a byte boundary. This
1123   error can only be indicated in case of EoT processing on detection of LP-11.

6.2.4   Escape Mode Entry Command Error

1125   If the receiving Lane Module does not recognize the received Entry Command for Escape mode an Escape
1126   mode Entry Command Error is indicated.

6.2.5   LP Transmission Sync Error

1128   At the end of a Low-Power Data transmission procedure, if data is not synchronized to a Byte boundary an
1129   Escape Sync Error signal is indicated.

6.2.6   False Control Error

1131   If a LP-Rqst (LP-10) is not followed by the remainder of a valid Escape or Turnaround sequence, a False
1132   Control Error is indicated. This error is also indicated if a HS-Rqst (LP-01) is not correctly followed by a
1133   Bridge State (LP-00).

6.3   Protocol Watchdog Timers (informative)

1135   It is not possible for the PHY to detect all fault cases. Therefore, additional protocol-level time-out
1136   mechanisms are necessary in order to limit the maximum duration of certain modes and states.

6.3.1   HS RX Timeout

1138   In HS RX mode if no EoT is received within a certain period the protocol should time-out. The timeout
1139   period can be protocol specific.

6.3.2   HS TX Timeout

1141   The maximum transmission length in HS TX is bounded. The timeout period is protocol specific.

6.3.3   Escape Mode Timeout

1143   A device may timeout during Escape mode. The timeout should be greater than the Escape mode Silence
1144   Limit of the other device. The timeout period is protocol specific.

6.3.4   Escape Mode Silence Timeout

A device may have a bounded length for LP TX-00 during Escape mode, after which the other device may timeout. The timeout period is protocol specific. For example, a display module should have an Escape mode Silence Limit, after which the host processor can timeout.

6.3.5   Turnaround Errors

A Turnaround procedure always starts from a Stop State. The procedure begins with a sequence of Low-Power States ending with a Bridge State (LP-00) during which drive sides are swapped. The procedure is finalized by the response including a Turn State followed by a Stop State driven from the other side. If the actual sequence of events violates the normal Turnaround procedure a "False Control Error" may be flagged to the Protocol. See section 6.2.6. The Turn State response serves as an acknowledgement for the correctly completed Turnaround procedure. If no acknowledgement is observed within a certain time period the Protocol should time-out and take appropriate action. This period should be larger than the maximum possible Turnaround time for a particular system. There is no time-out for this condition in the PHY.

1160 ## 7 Interconnect and Lane Configuration

1161 The interconnect between transmitter and receiver carries all signals used in D-PHY communication. This
1162 includes both high speed, low voltage signaling I/O technology and low speed, low power signaling for
1163 control functions. For this reason, the physical connection shall be implemented by means of balanced,
1164 differential, point-to-point transmission lines referenced to ground. The total interconnect may consist of
1165 several cascaded transmission line segments, such as, printed circuit boards, flex-foils, and cable
1166 connections.

1167

1168 **Figure 26 Point-to-point Interconnect**

1169 ### 7.1 Lane Configuration

1170 The complete physical connection of a Lane consists of a transmitter (TX), and/or receiver (RX) at each
1171 side, with some Transmission-Line-Interconnect-Structure (TLIS) in between. The overall Lane
1172 performance is therefore determined by the combination of these three elements. The split between these
1173 elements is defined to be on the module (IC) pins. This section defines both the required performance of
1174 the Transmission-Line-Interconnect-Structure for the signal routing as well as the I/O-cell Reflection
1175 properties of TX and RX. This way the correct overall operation of the Lane can be ensured.

1176 With respect to physical dimensions, the Transmission-Line-Interconnect-Structure will typically be the
1177 largest part. Besides printed circuit board and flex-foil traces, this may also includes elements such as vias
1178 and connectors.

1179 ### 7.2 Boundary Conditions

1180 The reference characteristic impedance level is 100 Ohm differential, 50 Ohm single-ended per Line, and
1181 25 Ohm common-mode for both Lines together. The 50 Ohm impedance level for single-ended operation is
1182 also convenient for test and characterization purposes.

1183 This typical impedance level is required for all three parts of the Lane: TX, TLIS, and RX. The tolerances
1184 for characteristic impedances of the interconnect and the tolerance on line termination impedances for TX
1185 and RX are specified by means of S-parameter templates over the whole operating frequency range.

1186 The differential channel is also used for LP single-ended signaling. Therefore, it is strongly recommended
1187 to apply only very loosely coupled differential transmission lines.

1188 The flight time for signals across the interconnect shall not exceed two nanoseconds.

1189 ### 7.3 Definitions

1190 The frequency 'fh' is the highest fundamental frequency for data transmission and is equal to
1191 $1/(2*UI_{INST,MIN})$. Implementers shall specify a value $UI_{INST,MIN}$ that represents the minimum instantaneous
1192 UI possible within a high speed data transfer for a given implementation.

1193 The frequency 'fh_{MAX}' is a device specification and indicates the maximum supported fh for a particular
1194 device.

1195   The frequency '$f_{LP,MAX}$' is the maximum toggle frequency for Low-Power mode.

1196   RF interference frequencies are denoted by 'f_{INT}', where $f_{INT,MIN}$ defines the lower bound for the band of
1197   relevant RF interferers.

1198   The frequency f_{MAX} is defined by the maximum of ($1/5t_{F,MIN}$, $1/5t_{R,MIN}$), where t_R and t_F are the rise and fall
1199   times of the High-Speed signaling. These parameters are specified in section 8. For the fastest allowed D-
1200   PHY signals f_{MAX} is 1.33GHz.

1201   7.4   S-parameter Specifications

1202   The required performance of the physical connection is specified by means of S-parameter requirements
1203   for TX, TLIS, and RX, for TLIS by mixed-mode, 4-port parameters, and for RX and TX by mixed-mode,
1204   reflection (return loss) parameters. The S-parameter limits are defined over the whole operating frequency
1205   range by means of templates.

1206   The differential transmission properties are most relevant and therefore this specification uses mixed-mode
1207   parameters. As the performance needs depend on the targeted bit rates, most S-parameter requirements are
1208   specified on a normalized frequency axis with respect to bit rate. Only the parameters that are important for
1209   the suppression of external (RF) interference are specified on an absolute frequency scale. This scale
1210   extends up to f_{MAX}. Beyond this frequency the circuitry itself shall suppress the high-frequency interference
1211   signals sufficiently.

1212   Only the overall performance of the TLIS and the maximum reflection of RX and TX are specified. This
1213   fully specifies the signal behavior at the RX/TX-module pins. The subdivision of losses, reflections and
1214   mode-conversion budget to individual physical fractions of the TLIS is left to the system designer. Annex
1215   B includes some rules of thumb for system design and signal routing guidelines.

1216   7.5   Characterization Conditions

1217   All S-parameter definitions are based on a 50 Ω impedance reference level. The characterization can be
1218   done with a measurement system, as shown in Figure 27.
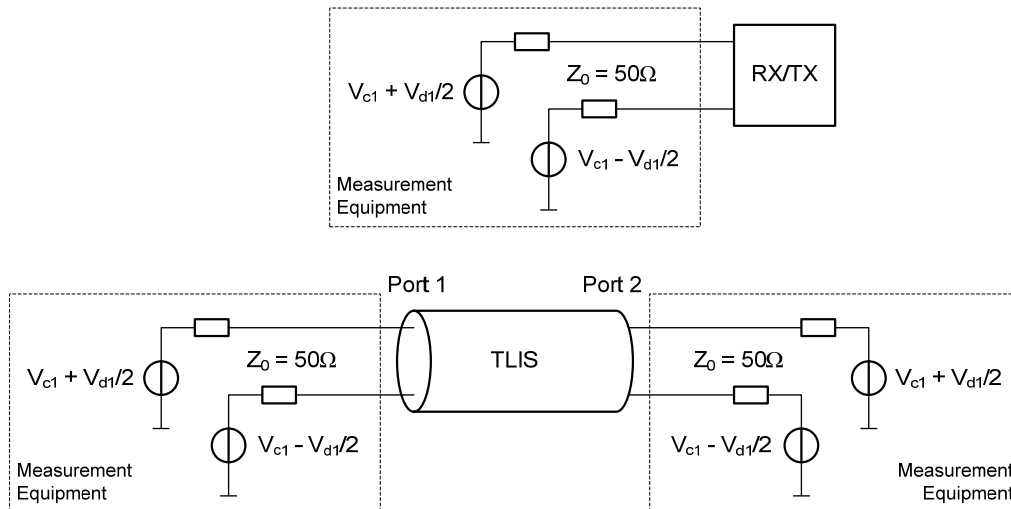
1219
1220   **Figure 27 Set-up for S-parameter Characterization of RX, TX and TLIS**

1221   The syntax of S-parameters is S[measured-mode][driven-mode][measured-port][driven-port]. Examples:
1222   Sdd21of TLIS is the differential signal at port 2 due to a differential signal driven at port 1; Sdc22 is the
1223   measured differential reflected signal at port 2 due to a common signal driven at port 2.

7.6   Interconnect Specifications

1225   The Transmission-Line Signal-Routing (TLSR) is specified by means of mixed-mode 4-port S-parameter
1226   behavior templates over the frequency range. This includes the differential and common-mode, insertion
1227   and return losses, and mode-conversion limitations.

7.6.1   Differential Characteristics

1229   The differential transfer behavior (insertion loss) of the TLIS shall meet the Sdd21 and Sdd12 template
1230   shown in Figure 28, where i ≠ j.

f/fh	0	1	3
Sddij, dB	-0.5	-2	-5
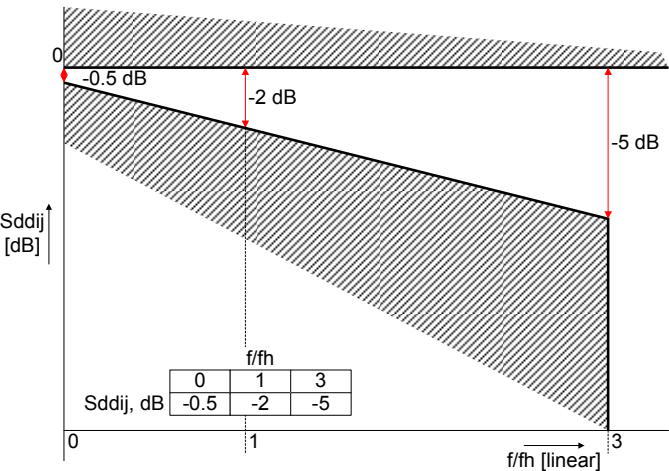
1232   **Figure 28 Template for Differential Insertion Losses**

1233   The differential reflection for both ports of the TLIS is specified by Sdd11 and Sdd22, and should match
1234   the template shown in Figure 29. Not meeting the differential reflection coefficients might impact
1235   interoperability and operation.

Frequency	0	f_LP,MAX	fh	f_MAX
Sddii, dB	-20	-20	-15	-9

1237   **Figure 29 Template for Differential Reflection at Both Ports**

1238 ## 7.6.2   Common-mode Characteristics

1239 The common-mode insertion loss is implicitly specified by means of the differential insertion loss and the
1240 Intra-Lane cross coupling. The requirements for common-mode insertion loss are therefore equal to the
1241 differential requirements.

1242 The common-mode reflection coefficients Scc11 and Scc22 should both be below –20 dB at frequencies up
1243 to $f_{LP,MAX}$, below -15dB at fh and –9 dB at f_{MAX}, similar to the differential requirements shown in Figure
1244 29. Not meeting the common-mode reflection coefficients might impact interoperability and operation.

1245 ## 7.6.3   Intra-Lane Cross-Coupling

1246 The two lines applied as a differential pair during HS transmission are also used individually for single-
1247 ended signaling during Low-Power mode. Therefore, the coupling between the two wires shall be
1248 restricted in order to limit single-ended cross coupling. The coupling between the two wires is defined as
1249 the difference of the S-parameters Scc21 and Sdd21 or Scc12 and Sdd12. In either case, the difference
1250 shall not exceed –20 dB for frequencies up to $10*f_{LP,MAX}$.

1251 ## 7.6.4   Mode-Conversion Limits

1252 All mixed-mode, 4-port S-parameters for differential to common-mode conversion, and vice-versa, shall
1253 not exceed –26 dB for frequencies below f_{MAX}. This includes Sdc12, Scd21, Scd12, Sdc21, Scd11, Sdc11,
1254 Scd22, and Sdc22.

1255 ## 7.6.5   Inter-Lane Cross-Coupling

1256 The common-mode and differential inter-Lane cross coupling between Lanes (clock and data) shall meet
1257 the requirements as shown in Figure 30 and Figure 31, respectively.

Frequency	0	$f_{LP,MAX}$	fh	f_{MAX}
Sccii, dB	–40	–40	–20	-12

1258
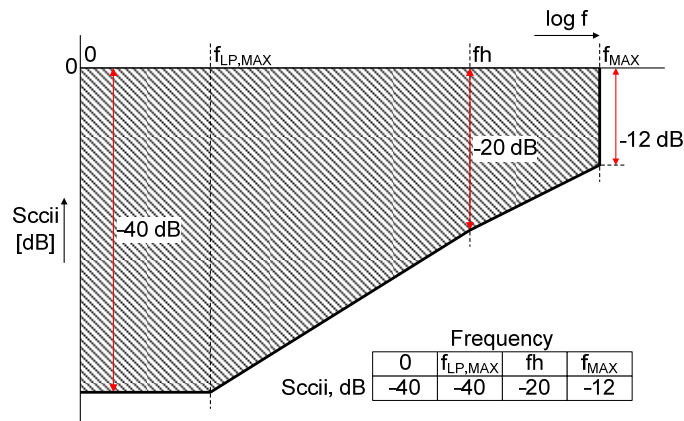
1259 **Figure 30 Inter-Lane Common-mode Cross-Coupling Template**

1260
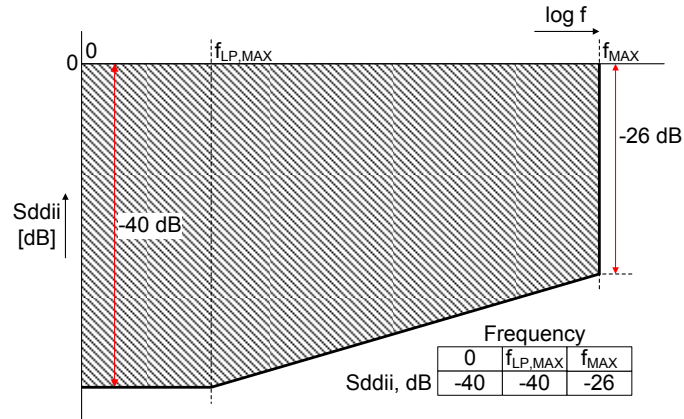
1261 **Figure 31 Inter-Lane Differential Cross-Coupling Template**

1262 ### 7.6.6 Inter-Lane Static Skew

1263 The difference in signal delay between any Data Lane and the Clock Lane shall be less than UI/50 for all
1264 frequencies up to, and including, fh.

1265
$$\frac{\left|Sdd12_{DATA}(\varphi) - Sdd12_{CLOCK}(\varphi)\right|}{\omega} < \frac{UI}{50}$$

1266 ## 7.7 Driver and Receiver Characteristics

1267 Besides the TLIS the Lane consists of two RX-TX modules, one at each side. This paragraph specifies the
1268 reflection behavior (return loss) of these RX-TX modules in HS-mode. The signaling characteristics of all
1269 possible functional blocks inside the RX-TX modules can be found in section 8. The low-frequency
1270 impedance range for line terminations at Transmitter and Receiver is 80-125Ohm.

1271 ### 7.7.1 Differential Characteristics

1272 The differential reflection of a Lane Module in High-Speed RX mode is specified by the template shown in
1273 Figure 32.

1274
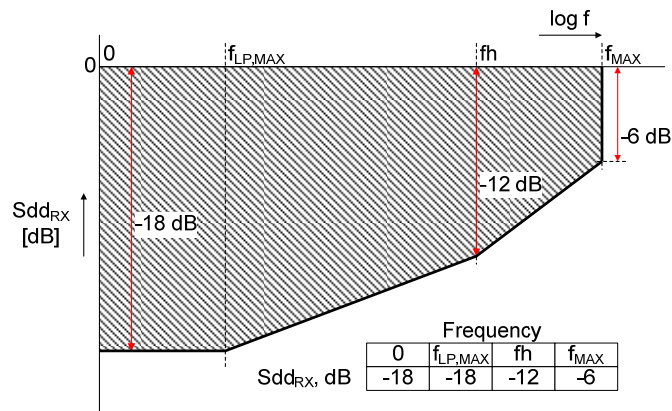
1275 **Figure 32 Differential Reflection Template for Lane Module Receivers**

1276   The differential reflection of a Lane Module in High-Speed TX mode is specified by the template shown in
1277   Figure 33.
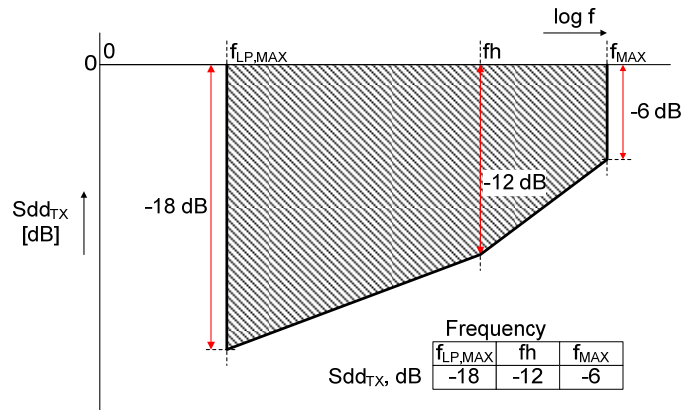
1278
1279   **Figure 33 Differential Reflection Template for Lane Module Transmitters**

1280   ## 7.7.2   Common-Mode Characteristics

1281   The common-mode return loss specification is different for a High-Speed TX and RX mode, because the
1282   RX is not DC terminated to ground. For an active TX the common-mode reflection shall be less than –6dB
1283   from $f_{LP,MAX}$ up to f_{MAX}. For an RX reflection shall be less than –6 dB for the frequency range $f_{INT,MIN}$ −
1284 f_{MAX}. Assuming a high DC common-mode impedance this implies a sufficiently large capacitor at the
1285   termination center tap. The minimum value allows integration. While the common-mode termination is
1286   especially important for reduced influence of RF interferers the RX requirement limits reflection for the
1287   most relevant frequency band.
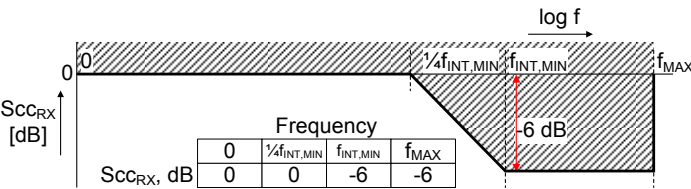
1288
1289   **Figure 34 Template for RX Common-Mode Return Loss**

1290   ## 7.7.3   Mode-Conversion Limits

1291   The differential to common-mode conversion limits of TX and RX shall be -26dB up to f_{MAX}.

1292   ## 7.7.4   Inter-Lane Matching

1293   The return loss difference between multiple Lanes shall be less than -26dB for all frequencies up to f_{MAX}.
1294

8   Electrical Characteristics

A PHY may contain the following electrical functions: a High-Speed Transmitter (HS-TX), a High-Speed
Receiver (HS-RX), a Low-Power Transmitter (LP-TX), a Low-Power Receiver (LP-RX), and a Low-
Power Contention Detector (LP-CD). A PHY does not need to contain all electrical functions, only the
functions that are required for a particular PHY configuration. The required functions for each
configuration are specified in section 4. All electrical functions included in any PHY shall meet the
specifications in this section. Figure 35 shows the complete set of electrical functions required for a fully
featured PHY transceiver.
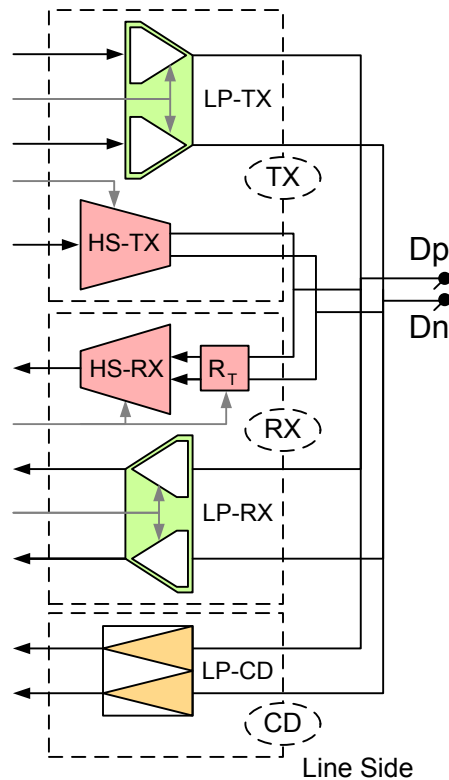
Figure 35 Electrical Functions of a Fully Featured D-PHY Transceiver

The HS transmitter and HS receiver are used for the transmission of the HS data and clock signals. The HS
transmitter and receiver utilize low-voltage differential signaling for signal transmission. The HS receiver
contains a switchable parallel termination.

The LP transmitter and LP receiver serve as a low power signaling mechanism. The LP transmitter is a
push-pull driver and the LP receiver is an un-terminated, single-ended receiver.

The signal levels are different for differential HS mode and single-ended LP mode. Figure 36 shows both
the HS and LP signal levels on the left and right sides, respectively. The HS signaling levels are below the
LP low-level input threshold such that LP receiver always detects low on HS signals.

All absolute voltage levels are relative to the ground voltage at the transmit side.

1314
1315
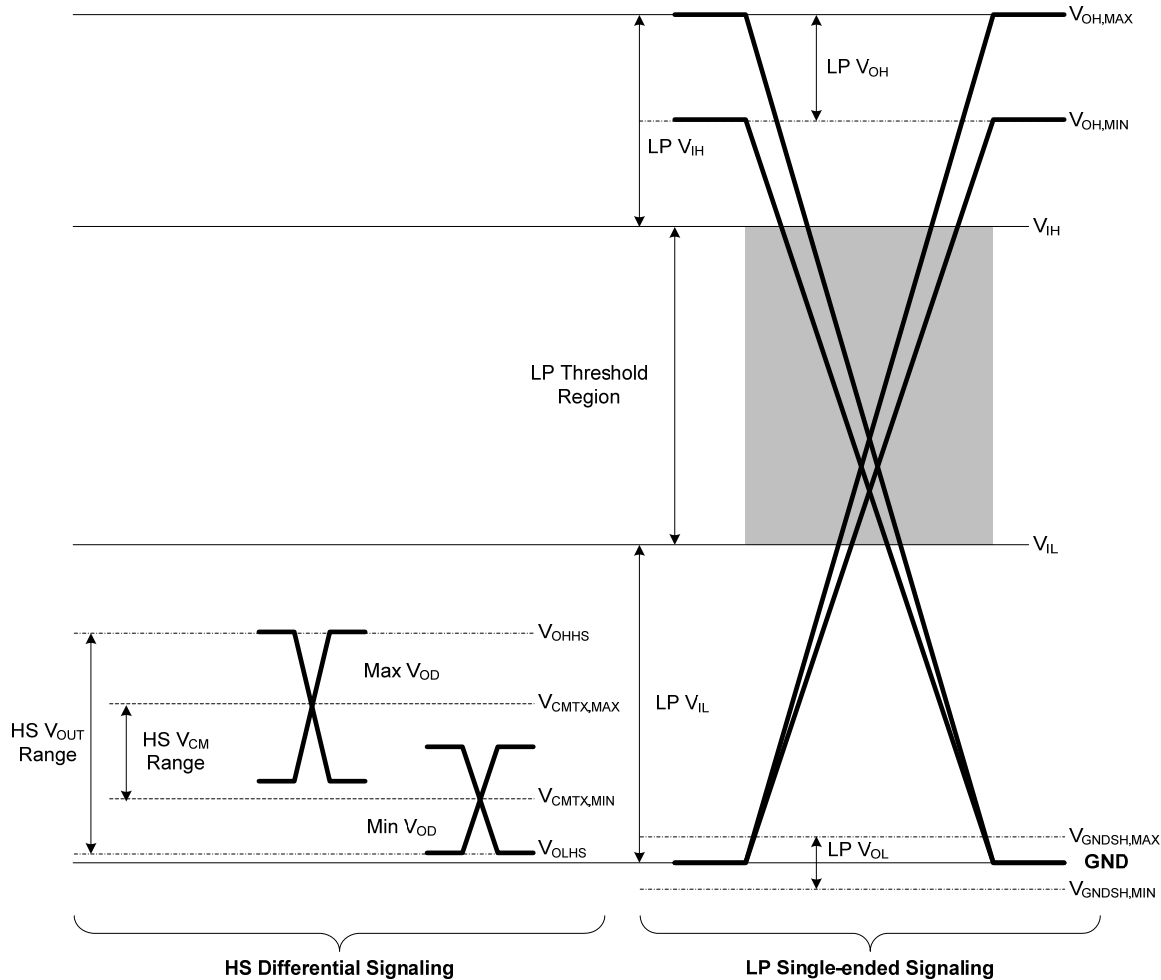
Figure 36 D-PHY Signaling Levels

1317   A Lane switches between Low-Power and High-Speed mode during normal operation. Bidirectional Lanes
1318   can also switch communication direction. The change of operating mode or direction requires enabling and
1319   disabling of certain electrical functions. These enable and disable events shall not cause glitches on the
1320   Lines that would result in a detection of an incorrect signal level. Therefore, all mode and direction
1321   changes shall be smooth to always ensure a proper detection of the Line signals.

1322   ## 8.1   Driver Characteristics

1323   ## 8.1.1   High-Speed Transmitter

1324   A HS differential signal driven on the Dp and Dn pins is generated by a differential output driver. For
1325   reference, Dp is considered as the positive side and Dn as the negative side. The Lane state is called
1326   Differential-1 (HS-1) when the potential on Dp is higher than the potential of Dn. The Lane state is called
1327   Differential-0 (HS-0), when the potential on Dp is lower than the potential of Dn. Figure 37 shows an
1328   example implementation of a HS transmitter.

1329   Note, this section uses Dp and Dn to reference the pins of a Lane Module regardless of whether the pins
1330   belong to a Clock Lane Module or a Data Lane Module.

1331
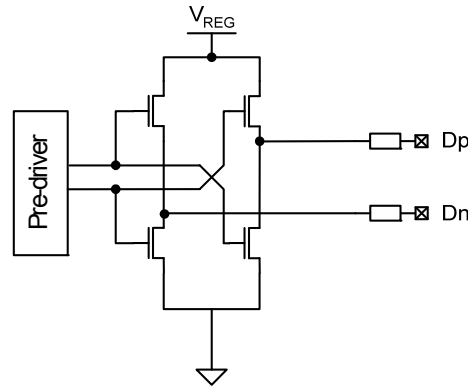
1332   **Figure 37 Example HS Transmitter**

1333   The differential output voltage V_{OD} is defined as the difference of the voltages V_{DP} and V_{DN} at the Dp and
1334   Dn pins, respectively.

1335
$$V_{OD} = V_{DP} - V_{DN}$$

1336   The output voltages V_{DP} and V_{DN} at the Dp and Dn pins shall not exceed the High-Speed output high
1337   voltage V_{OHHS}. V_{OLHS} is the High-Speed output, low voltage on Dp and Dn and is determined by V_{OD} and
1338 V_{CMTX}. The High-Speed V_{OUT} is bounded by the minimum value of V_{OLHS} and the maximum value of
1339 V_{OHHS}.

1340   The common-mode voltage V_{CMTX} is defined as the arithmetic mean value of the voltages at the Dp and Dn
1341   pins:

1342
$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

1343 V_{OD} and V_{CMTX} are graphically shown in Figure 38 for ideal HS signals. Figure 38 shows single-ended HS
1344   signals with the possible kinds of distortion of the differential output and common-mode voltages. V_{OD} and
1345 V_{CMTX} may be slightly different for driving a Differential-1 or a Differential-0 on the pins. The output
1346   differential voltage mismatch ΔV_{OD} is defined as the difference of the absolute values of the differential
1347   output voltage in the Differential-1 state $V_{OD(1)}$ and the differential output voltage in the Differential-0 state
1348 $V_{OD(0)}$. This is expressed by:

1349
$$\Delta V_{OD} = \left| V_{OD(1)} \right| - \left| V_{OD(0)} \right|$$

1350   If $V_{CMTX(1)}$ and $V_{CMTX(0)}$ are the common-mode voltages for static Differential-1 and Differential-0 states
1351   respectively, then the common-mode reference voltage is defined by:

1352
$$V_{CMTX,REF} = \frac{V_{CMTX(1)} + V_{CMTX(0)}}{2}$$

1353   The transient common-mode voltage variation is defined by:

1354
$$\Delta V_{CMTX}(t) = V_{CMTX}(t) - V_{CMTX,REF}$$

1355   The static common-mode voltage mismatch between the Differential-1 and Differential-0 state is given by:

1356
$$\Delta V_{CMTX(1,0)} = \frac{V_{CMTX(1)} - V_{CMTX(0)}}{2}$$

1357   The transmitter shall send data such that the high frequency and low frequency common-mode voltage
1358   variations do not exceed $\Delta V_{CMTX(HF)}$ and $\Delta V_{CMTX(LF)}$, respectively. An example test circuit for the
1359   measurement of V_{OD} and V_{CMTX} is shown in Figure 40.

1360

1361   **Figure 38 Ideal Single-ended and Resulting Differential HS Signals**

ΔV_OD (SE HS Signals)

Static ΔV_CMTX (SE HS Signals)

Dynamic ΔV_CMTX (SE HS Signals)

1362
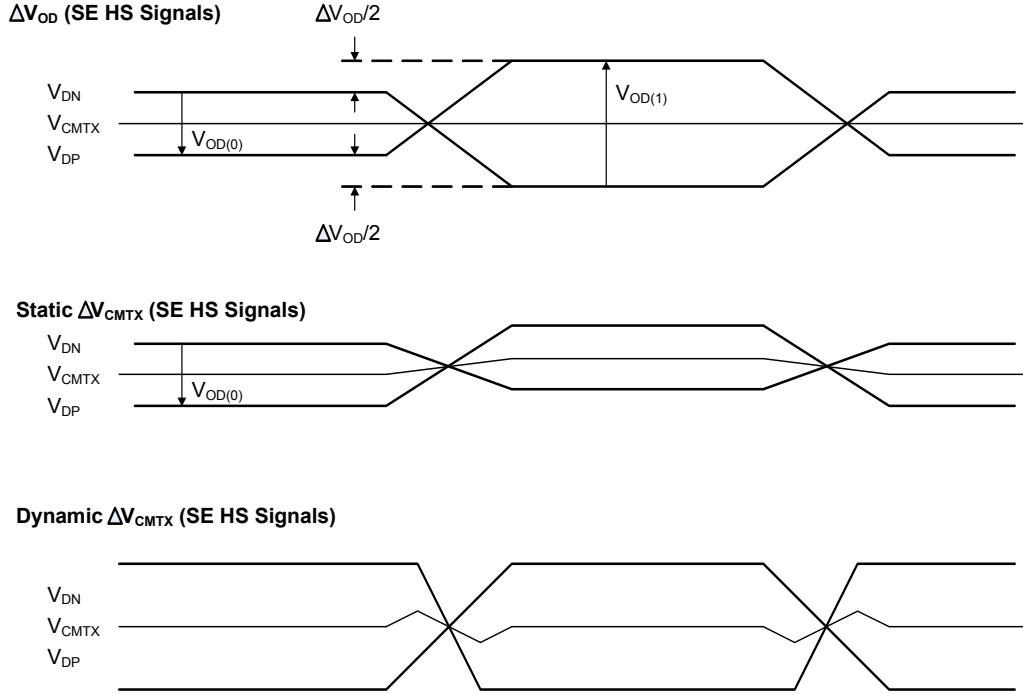
1363   **Figure 39 Possible ΔV_CMTX and ΔV_OD Distortions of the Single-ended HS Signals**

1364
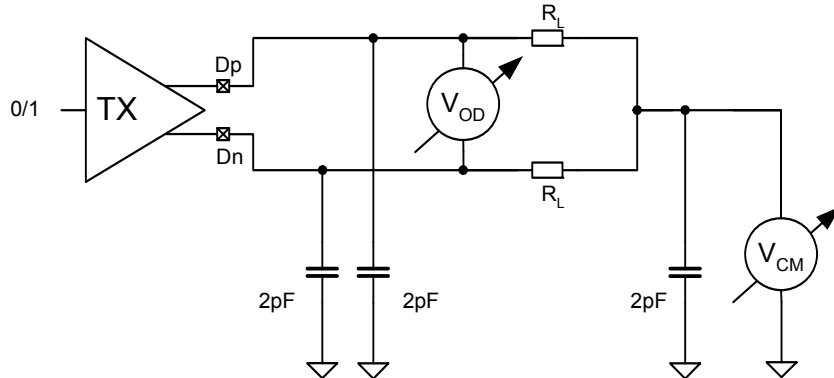
1365   **Figure 40 Example Circuit for V_CMTX and V_OD Measurements**

1366 The single-ended output impedance of the transmitter at both the Dp and Dn pins is denoted by Z_{OS}. ΔZ_{OS}
1367 is the mismatch of the single ended output impedances at the Dp and Dn pins, denoted by Z_{OSDP} and Z_{OSDN}
1368 respectively. This mismatch is defined as the ratio of the absolute value of the difference of Z_{OSDP} and
1369 Z_{OSDN} and the average of those impedances:

$$1370 \qquad \Delta Z_{OS} = 2\frac{\left| Z_{OSDP} - Z_{OSDN} \right|}{Z_{OSDP} + Z_{OSDN}}$$

1371 The output impedance Z_{OS} and the output impedance mismatch ΔZ_{OS} shall be compliant with Table 16 for
1372 both the Differential-0 and Differential-1 states for all allowed loading conditions. It is recommended that
1373 implementations keep the output impedance during state transitions as close as possible to the steady state
1374 value. The output impedance Z_{OS} can be determined by injecting an AC current into the Dp and Dn pins
1375 and measuring the peak-to-peak voltage amplitude.

1376   The rise and fall times, t_R and t_F, are defined as the transition time between 20% and 80% of the full HS
1377   signal swing. The driver shall meet the t_R and t_F specifications for all allowable Z_{ID}. The specifications for
1378   TX common-mode return loss and the TX differential mode return loss can be found in section 7.

1379   It is recommended that a High-Speed transmitter that is directly terminated at its pins should not generate
1380   any overshoot in order to minimize EMI.

1381   **Table 16 HS Transmitter DC Specifications**

Parameter	Description	Min	Nom	Max	Units	Notes
V_{CMTX}	HS transmit static common-mode voltage	150	200	250	mV	1
$|\Delta V_{CMTX(1,0)}|$	V_{CMTX} mismatch when output is Differential-1 or Differential-0			5	mV	2
$|V_{OD}|$	HS transmit differential voltage	140	200	270	mV	1
$|\Delta V_{OD}|$	V_{OD} mismatch when output is Differential-1 or Differential-0			10	mV	2
V_{OHHS}	HS output high voltage			360	mV	1
Z_{OS}	Single ended output impedance	40	50	62.5	Ω	
ΔZ_{OS}	Single ended output impedance mismatch			10	%	

1382   Notes:

1383   1. Value when driving into load impedance anywhere in the Z_{ID} range.

1384   2. It is recommended the implementer minimize ΔV_{OD} and $\Delta V_{CMTX(1,0)}$ in order to minimize radiation and
1385   optimize signal integrity.

1386   **Table 17 HS Transmitter AC Specifications**

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMTX(HF)}$	Common-level variations above 450MHz			15	mV$_{RMS}$	
$\Delta V_{CMTX(LF)}$	Common-level variation between 50-450MHz			25	mV$_{PEAK}$	
t_R and t_F	20%-80% rise time and fall time			0.3	UI	1
		150			ps	

1387   Notes:

1388   1. UI is equal to 1/(2*fh). See section 7.3 for the definition of fh.

1389   ### 8.1.2   Low-Power Transmitter

1390   The Low-Power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the Lines
1391   in all Low-Power operating modes It is therefore important that the static power consumption of a LP
1392   transmitter be as low as possible. The slew-rate of signal transitions is bounded in order to keep EMI low.
1393   An example of a LP transmitter is shown in Figure 41.

1.2V

1394
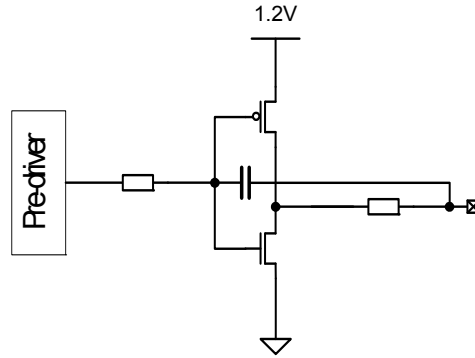
Figure 41 Example LP Transmitter

1396 V_{OL} is the Thevenin output, low-level voltage in the LP transmit mode. This is the voltage at an unloaded
1397   pad pin in the low-level state. V_{OH} is the Thevenin output, high-level voltage in the high-level state, when
1398   the pad pin is not loaded. The LP transmitter shall not drive the pad pin potential statically beyond the
1399   maximum value of V_{OH}. The pull-up and pull-down output impedances of LP transmitters shall be as
1400   described in Figure 42 and Figure 43, respectively. The circuit for measuring V_{OL} and V_{OH} is shown in
1401   Figure 44.

1402
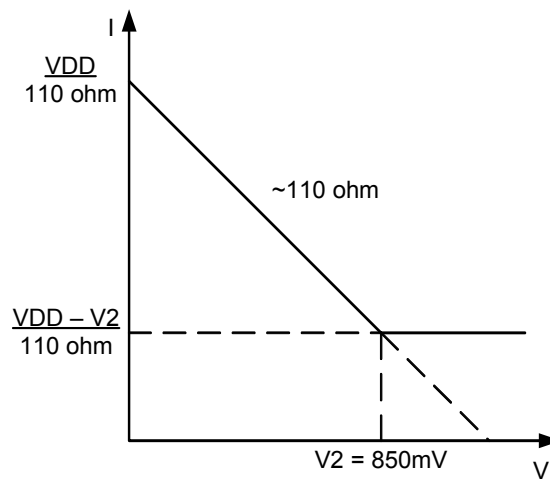
Figure 42 V-I Characteristic for LP Transmitter Driving Logic High

1404
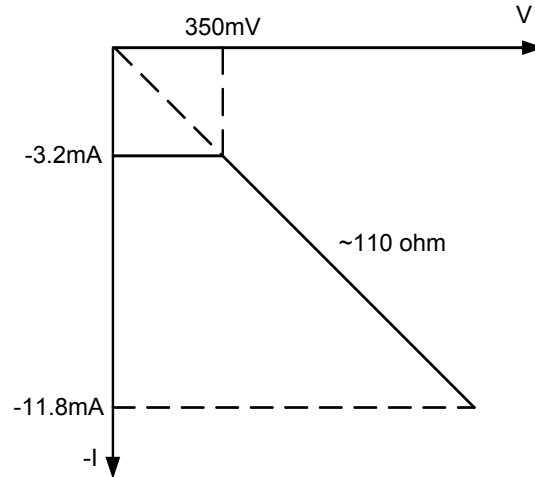
1405   **Figure 43 V-I Characteristic for LP Transmitter Driving Logic Low**

1406
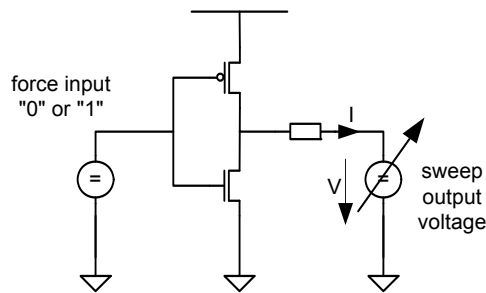
1407   **Figure 44 LP Transmitter V-I Characteristic Measurement Setup**

1408   The impedance Z_{OLP} is defined by:

1409
$$Z_{OLP} = \left| \frac{V_{THEVENIN} - V_{PIN}}{I_{OUT}} \right|$$

1410   The times T_{RLP} and T_{FLP} are the 15%-85% rise and fall times, respectively, of the output signal voltage,
1411   when the LP transmitter is driving a capacitive load C_{LOAD}. The 15%-85% levels are relative to the fully
1412   settled V_{OH} and V_{OL} voltages. The slew rate $\delta V/\delta t_{SR}$ is the derivative of the LP transmitter output signal
1413   voltage over time. The LP transmitter output signal transitions shall meet the maximum and minimum slew
1414   rate specifications as shown in Table 19, Figure 45 and Figure 46. The intention of specifying a maximum
1415   slew rate value is to limit EMI.

1416   **Table 18 LP Transmitter DC Specifications**

Parameter	Description	Min	Nom	Max	Units	Notes
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	
V_{OL}	Thevenin output low level	-50		50	mV	
Z_{OLP}	Output impedance of LP transmitter	110			Ω	1, 2

1417   Notes:

1418   1. See Figure 42 and Figure 43.

1419   2. Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the
1420 T_{RLP}/T_{FLP} specification is met.

1421   **Table 19 LP Transmitter AC Specifications**

Parameter	Description		Min	Nom	Max	Units	Notes
T_{RLP}/T_{FLP}	15%-85% rise time and fall time				25	ns	1
T_{REOT}	30%-85% rise time and fall time				35	ns	1, 5, 6
$T_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40			ns	4
		All other pulses	20			ns	4
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock		90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ C_{LOAD} = 0pF				500	mV/ns	1, 3, 7, 8
	Slew rate @ C_{LOAD} = 5pF				300	mV/ns	1, 3, 7, 8
	Slew rate @ C_{LOAD} = 20pF				250	mV/ns	1, 3, 7, 8
	Slew rate @ C_{LOAD} = 70pF				150	mV/ns	1, 3, 7, 8
	Slew rate @ C_{LOAD} = 0 to 70pF (Falling Edge Only)		30			mV/ns	1, 2, 3
	Slew rate @ C_{LOAD} = 0 to 70pF (Rising Edge Only)		30			mV/ns	1, 3, 9
	Slew rate @ C_{LOAD} = 0 to 70pF (Rising Edge Only)		30 – 0.075 * ($V_{O,INST}$ – 700)			mV/ns	1, 10, 11
C_{LOAD}	Load capacitance		0		70	pF	1

1422   Notes:

1423   1. C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX
1424   are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line
1425   with 2ns delay.

1426   2. When the output voltage is between 400 mV and 930 mV.

1427   3. Measured as average across any 50 mV segment of the output signal transition.

1428
1429
1430

4. This parameter value can be lower than T_{LPX} due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior as described in section 8.2.2.

1431
1432

5. The rise-time of T_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.

1433
1434

6. With an additional load capacitance C_{CM} between 0 and 60pF on the termination center tap at RX side of the Lane

1435

7. This value represents a corner point in a piecewise linear curve. See Figure 45 and Figure 46.

1436

8. When the output voltage is in the range specified by $V_{PIN(absmax)}$.

1437

9. When the output voltage is between 400 mV and 700 mV.

1438

10. Where $V_{O,INST}$ is the instantaneous output voltage, V_{DP} or V_{DN}, in millivolts.

1439

11. When the output voltage is between 700 mV and 930 mV.

1440
1441
1442
1443

There are minimum requirements on the duration of each LP state. To determine the duration of the LP state, the Dp and Dn signal lines are each compared to a common trip-level. The result of these comparisons is then exclusive-ORed to produce a single pulse train. The output of this "exclusive-OR clock" can then be used to find the minimum pulse width output of an LP transmitter.

1444
1445

Using a common trip-level in the range $[V_{IL,MAX} + V_{OL,MIN}, V_{IH,MIN} + V_{OL,MAX}]$, the exclusive-OR clock shall not contain pulses shorter than T_{MIN-TX}.

1446

C_{LOAD}, pF			
0	5	20	70
$\delta V/\delta t_{SR,MIN}$, mV/ns	30	30	30	30
$\delta V/\delta t_{SR,MAX}$, mV/ns	500	300	250	150

1447
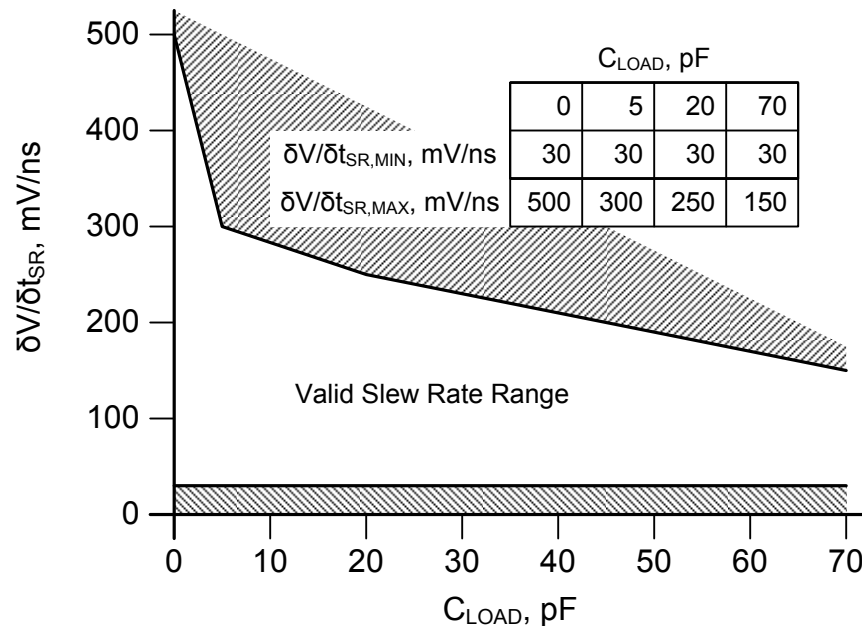
Figure 45 Slew Rate vs. C_{LOAD} (Falling Edge)

C_{LOAD}, pF			
0	5	20	70

	0	5	20	70
$\delta V/\delta t_{SR,MIN}$, mV/ns (400 mV to 700 mV)	30	30	30	30
$\delta V/\delta t_{SR,MIN}$, mV/ns (700 mV to 930 mV)	See Table 19			
$\delta V/\delta t_{SR,MAX}$, mV/ns	500	300	250	150

1448
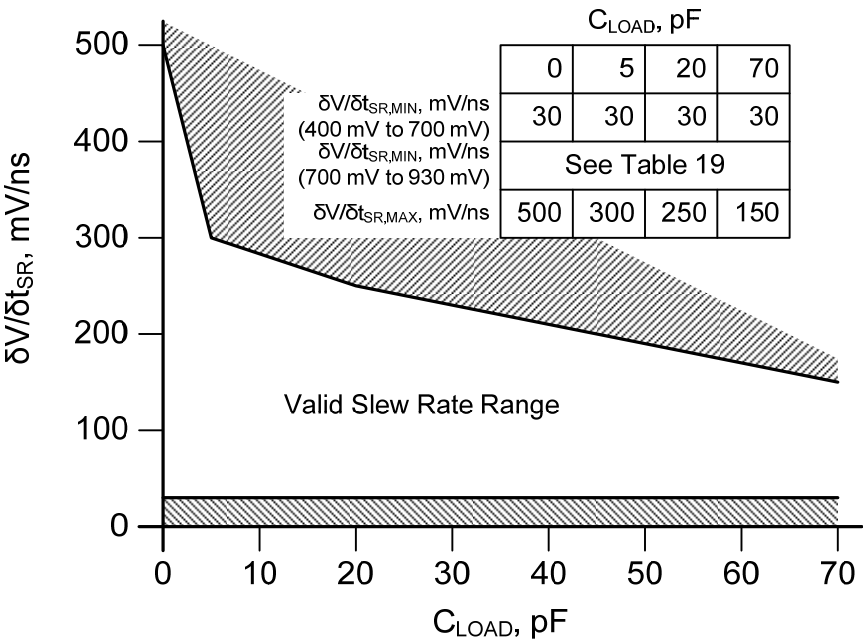
1449　　　　　　　　　**Figure 46 Slew Rate vs. C_{LOAD} (Rising Edge)**

1450　**8.2　　Receiver Characteristics**

1451　**8.2.1　　High-Speed Receiver**

1452　The HS receiver is a differential line receiver. It contains a switchable parallel input termination, Z_{ID},
1453　between the positive input pin Dp and the negative input pin Dn. A simplified diagram of an example
1454　implementation using a PMOS input stage is shown in Figure 47.

1455
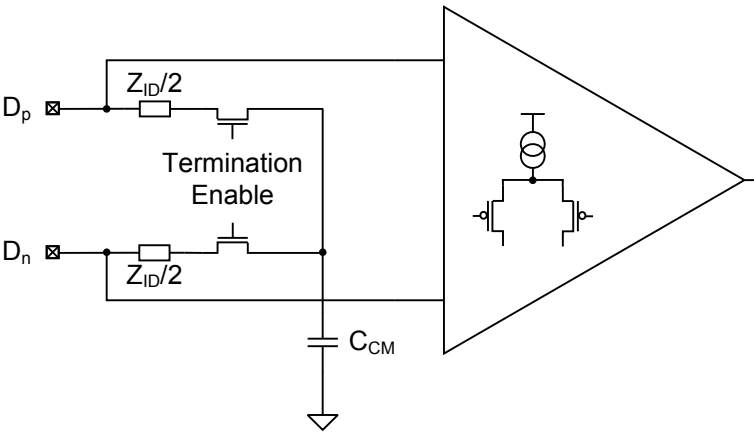
1456　　　　　　　　　**Figure 47 HS Receiver Implementation Example**

1457　The differential input high and low threshold voltages of the HS receiver are denoted by V_{IDTH} and V_{IDTL},
1458　respectively. V_{ILHS} and V_{IHHS} are the single-ended, input low and input high voltages, respectively.
1459　$V_{CMRX(DC)}$ is the differential input common-mode voltage. The HS receiver shall be able to detect
1460　differential signals at its Dp and Dn input signal pins when both signal voltages, V_{DP} and V_{DN}, are within
1461　the common-mode voltage range and if the voltage difference of V_{DP} and V_{DN} exceeds either V_{IDTH} or

1462 V_{IDTL}. The High-Speed receiver shall receive High-Speed data correctly while rejecting common-mode
1463   interference $\Delta V_{CMRX(HF)}$ and $\Delta V_{CMRX(LF)}$.

1464   During operation of the HS receiver, termination impedance Z_{ID} is required between the Dp and Dn pins of
1465   the HS receiver. Z_{ID} shall be disabled when the module is not in the HS receive mode. When transitioning
1466   from Low-Power Mode to HS receive mode the termination impedance shall not be enabled until the
1467   single-ended input voltages on both Dp and Dn fall below $V_{TERM-EN}$. To meet this requirement, a receiver
1468   does not need to sense the Dp and Dn lines to determine when to enable the line termination, rather the LP
1469   to HS transition timing can allow the line voltages to fall to the appropriate level before the line
1470   termination is enabled.

1471   The RX common-mode return loss and the RX differential mode return loss are specified in section 7. C_{CM}
1472   is the common-mode AC termination, which ensures a proper termination of the receiver at higher
1473   frequencies. For higher data rates, C_{CM} is needed at the termination centre tap in order to meet the
1474   common-mode reflection requirements.

1475   **Table 20 HS Receiver DC Specifications**

Parameter	Description	Min	Nom	Max	Units	Note
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70		330	mV	1,2
V_{IDTH}	Differential input high threshold			70	mV	
V_{IDTL}	Differential input low threshold	-70			mV	
V_{IHHS}	Single-ended input high voltage			460	mV	1
V_{ILHS}	Single-ended input low voltage	-40			mV	1
$V_{TERM-EN}$	Single-ended threshold for HS termination enable			450	mV	
Z_{ID}	Differential input impedance	80	100	125	Ω	

1476   Notes:

1477   1.   Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

1478   2.   This table value includes a ground difference of 50mV between the transmitter and the receiver, the static
1479   common-mode level tolerance and variations below 450MHz

1480   **Table 21 HS Receiver AC Specifications**

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450 MHz			100	mV	2
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz – 450MHz	-50		50	mV	1, 4
C_{CM}	Common-mode termination			60	pF	3

1481   Notes:

1482   1.   Excluding 'static' ground shift of 50mV

1483   2. $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.

1484   3.   For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

1485   4.   Voltage difference compared to the DC average common-mode potential.

8.2.2   Low-Power Receiver

1487   The Low-Power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to
1488   detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses
1489   and RF interference. It is recommended the implementer optimize the LP receiver design for low power.

1490   The input low-level voltage, V_{IL}, is the voltage at which the receiver is required to detect a low state in the
1491   input signal. A lower input voltage, $V_{IL-ULPS}$, may be used when the receiver is in the Ultra-Low Power
1492   State. V_{IL} is larger than the maximum single-ended Line voltage during HS transmission. Therefore, a LP
1493   receiver shall detect low during HS signaling.

1494   The input high-level voltage, V_{IH}, is the voltage at which the receiver is required to detect a high state in
1495   the input signal. In order to reduce noise sensitivity on the received signal, an LP receiver shall incorporate
1496   a hysteresis, The hysteresis voltage is defined as V_{HYST}.

1497   The LP receiver shall reject any input signal smaller than e_{SPIKE}. Signal pulses wider than T_{MIN-RX} shall
1498   propagate through the LP receiver.

1499   Furthermore, the LP receivers shall be tolerant of super-positioned RF interference on top of the wanted
1500   Line signals. This implies an input signal filter. The LP receiver shall meet all specifications for
1501   interference with peak amplitude V_{INT} and frequency f_{INT}. The interference shall not cause glitches or
1502   incorrect operation during signal transitions.
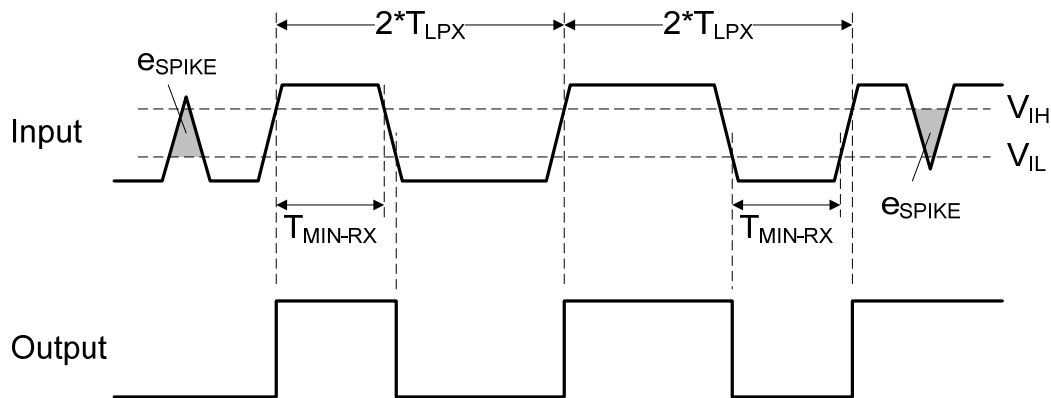
1503
1504   **Figure 48 Input Glitch Rejection of Low-Power Receivers**

1505   **Table 22 LP Receiver DC specifications**

Parameter	Description	Min	Nom	Max	Units	Notes
V_{IH}	Logic 1 input voltage	880			mV	
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV	
$V_{IL-ULPS}$	Logic 0 input voltage, ULP State			300	mV	
V_{HYST}	Input hysteresis	25			mV	

1506   **Table 23 LP Receiver AC Specifications**

Parameter	Description	Min	Nom	Max	Units	Notes
e_{SPIKE}	Input pulse rejection			300	V·ps	1, 2, 3
T_{MIN-RX}	Minimum pulse width response	20			ns	4
V_{INT}	Peak interference amplitude			200	mV	
f_{INT}	Interference frequency	450			MHz	

1507   Notes:

1508   1. Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1
1509   state

1510   2. An impulse less than this will not change the receiver state.

1511   3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

1512   4. An input pulse greater than this shall toggle the output.

1513   ## 8.3   Line Contention Detection

1514   The Low-Power receiver and a separate Contention Detector (LP-CD) shall be used in a bi-directional Data
1515   Lane to monitor the line voltage on each Low-Power signal. This is required to detect line contention as
1516   described in section 6.1. The Low-Power receiver shall be used to detect an LP high fault when the LP
1517   transmitter is driving high and the pin voltage is less than V_{IL}. Refer to Table 22. The LP-CD shall be used
1518   to detect an LP low fault when the LP transmitter is driving low and the pin voltage is greater than V_{IHCD}.
1519   Refer to Table 24. An LP low fault shall not be detected when the pin voltage is less than V_{ILCD}.

1520   The general operation of a contention detector shall be similar to that of an LP receiver with lower
1521   threshold voltages. Although the DC specifications differ, the AC specifications of the LP-CD are defined
1522   to match those of the LP receiver and the LP-CD shall meet the specifications listed in Table 23 except for
1523 T_{MIN-RX}. The LP-CD shall sufficiently filter the input signal to avoid false triggering on short events.

1524   The LP-CD threshold voltages ($V_{ILCD,}$ V_{IHCD}) are shown along with the normal signaling voltages in Figure
1525   49.
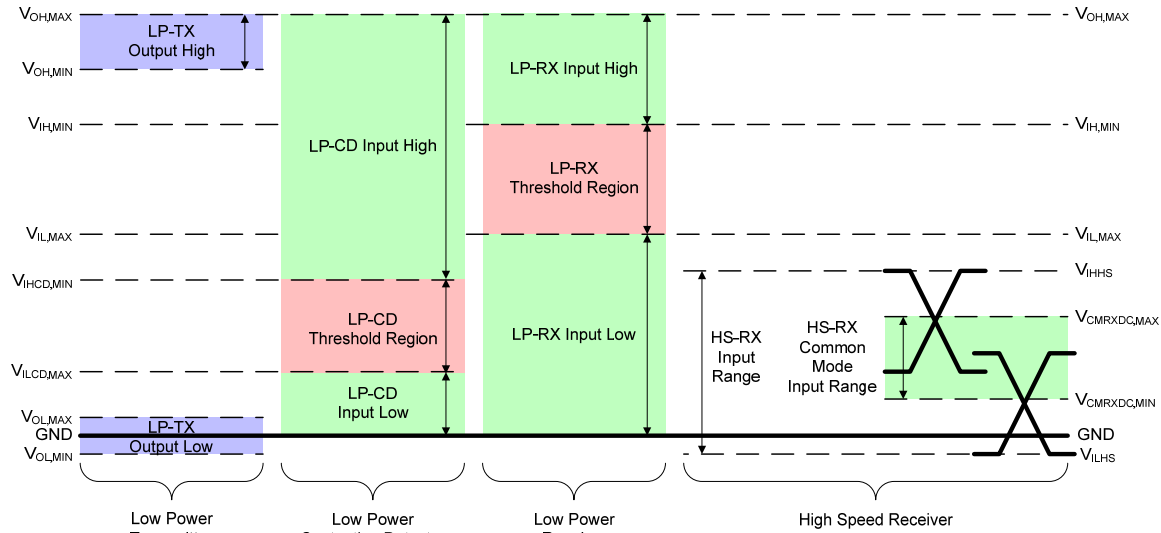
Figure 49 Signaling and Contention Voltage Levels

Table 24 Contention Detector (LP-CD) DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{IHCD}	Logic 1 contention threshold	450			mV	
V_{ILCD}	Logic 0 contention threshold			200	mV	

8.4   Input Characteristics

No structure within the PHY may be damaged when a DC signal that is within the signal voltage range V_{PIN} is applied to a pad pin for an indefinite period of time. $V_{PIN(absmax)}$ is the maximum transient output voltage at the transmitter pin. The voltage on the transmitter's output pin shall not exceed $V_{PIN,MAX}$ for a period greater than $T_{VPIN(absmax)}$. When the PHY is in the Low-Power receive mode the pad pin leakage current shall be I_{LEAK} when the pad signal voltage is within the signal voltage range of V_{PIN}. The specification of I_{LEAK} assures interoperability of any PHY in the LP mode by restricting the maximum load current of an LP transmitter. An example test circuit for leakage current measurement is shown in Figure 50.

The ground supply voltages shifts between a Master and a Slave shall be less than V_{GNDSH}.

1540
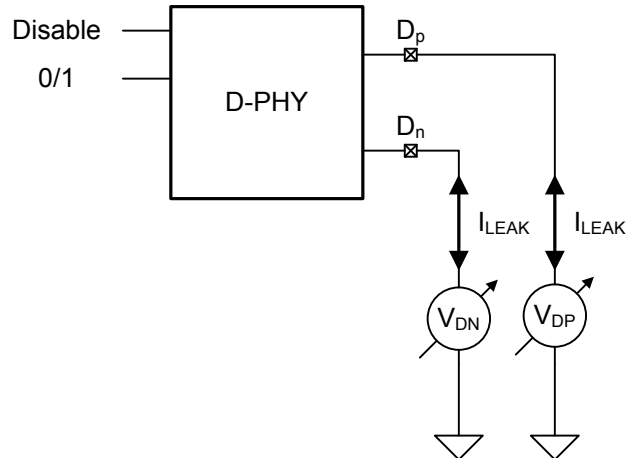
1541   **Figure 50 Pin Leakage Measurement Example Circuit**

1542   **Table 25 Pin Characteristic Specifications**

Parameter	Description	Min	Nom	Max	Units	Note
V_{PIN}	Pin signal voltage range	-50		1350	mV	
I_{LEAK}	Pin leakage current	-10		10	μA	1
V_{GNDSH}	Ground shift	-50		50	mV	
$V_{PIN(absmax)}$	Transient pin voltage level	-0.15		1.45	V	3
$T_{VPIN(absmax)}$	Maximum transient time above $V_{PIN(max)}$ or below $V_{PIN(min)}$			20	ns	2

1543   Notes:

1544   1.   When the pad voltage is in the signal voltage range from $V_{GNDSH,MIN}$ to $V_{OH} + V_{GNDSH,MAX}$ and the Lane
1545   Module is in LP receive mode.

1546   2.   The voltage overshoot and undershoot beyond the V_{PIN} is only allowed during a single 20ns window after
1547   any LP-0 to LP-1 transition or vice versa. For all other situations it must stay within the V_{PIN} range.

1548   3.   This value includes ground shift.
1549

1550 **9   High-Speed Data-Clock Timing**

1551 This section specifies the required timings on the High-Speed signaling interface independent of the
1552 electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction.
1553 In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse
1554 direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

1555 Data transmission may occur at any rate greater than the minimum specified data bit rate.

1556 Figure 51 shows an example PHY configuration including the compliance measurement planes for the
1557 specified timings. Note that the effect of signal degradation inside each package due to parasitic effects is
1558 included in the timing budget for the transmitter and receiver and is not included in the interconnect
1559 degradation budget. See section 7 for details.

1560
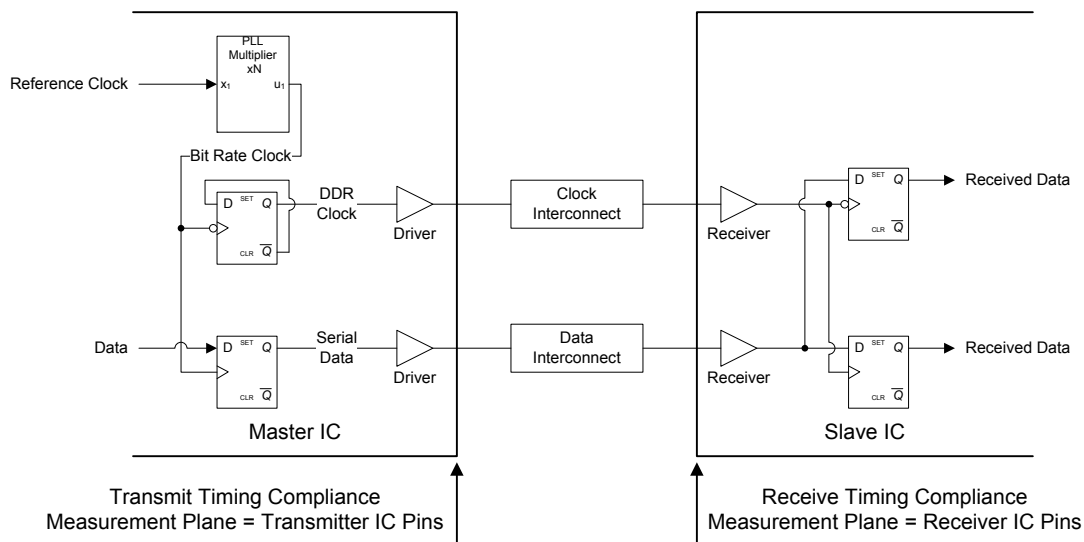
1561   **Figure 51 Conceptual D-PHY Data and Clock Timing Compliance Measurement Planes**

1562 **9.1   High-Speed Clock Timing**

1563 The Master side of the Link shall send a differential clock signal to the Slave side to be used for data
1564 sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All
1565 timing relationships required for correct data sampling are defined relative to the clock transitions.
1566 Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

1567 The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be
1568 sampled on both the rising and falling edges of the Clock signal. The term "rising edge" means "rising
1569 edge of the differential signal, i.e. CLKp – CLKn, and similarly for "falling edge". Therefore, the period of
1570 the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown
1571 in Figure 52.

1572 Note that the UI indicated in Figure 52 is the instantaneous UI and shall have a value less than 12.5 ns. A
1573 minimum value is not specified. However, implementers shall specify a maximum data rate and
1574 corresponding maximum clock frequency, fh_{MAX}, for a given implementation. For a description of fh_{MAX},
1575 see section 7.3.

1576
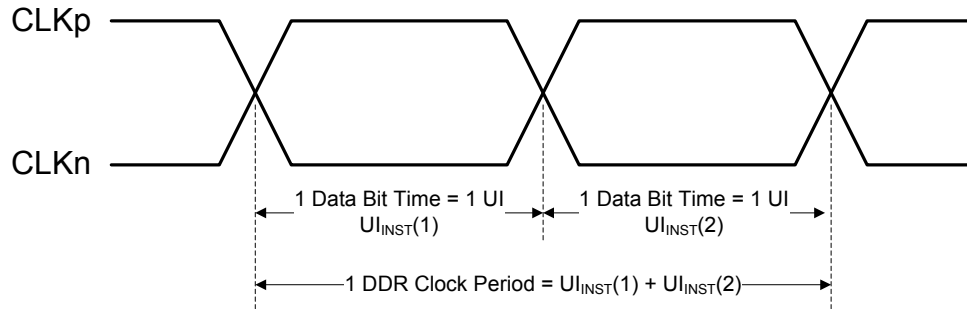
1577   **Figure 52 DDR Clock Definition**

1578   As can be seen in Figure 51, the same clock source is used to generate the DDR Clock and launch the serial
1579   data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may
1580   be used directly to sample the Data lines in the receiver. Such a system can accommodate large
1581   instantaneous variations in UI.

1582   The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore,
1583   devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the
1584   PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

1585   The UI_{INST} specifications for the Clock signal are summarized in Table 26.

1586   **Table 26 Clock Signal Specification**

Clock Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}			12.5	ns	1,2

1587   Notes:

1588   1.   This value corresponds to a minimum 80 Mbps data rate.

1589   2.   The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

1590   ## 9.2   Forward High-Speed Data Transmission Timing

1591   The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in
1592   Figure 53. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be
1593   used directly by the receiver to sample the received data.

1594   The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a
1595   transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge,
1596   the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating
1597   rising and falling edges.

1598   All timing values are measured with respect to the actual observed crossing of the Clock differential signal.
1599   The effects due to variations in this level are included in the clock to data timing budget.

1600   Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold
1601   parameters.

Reference Time

1602
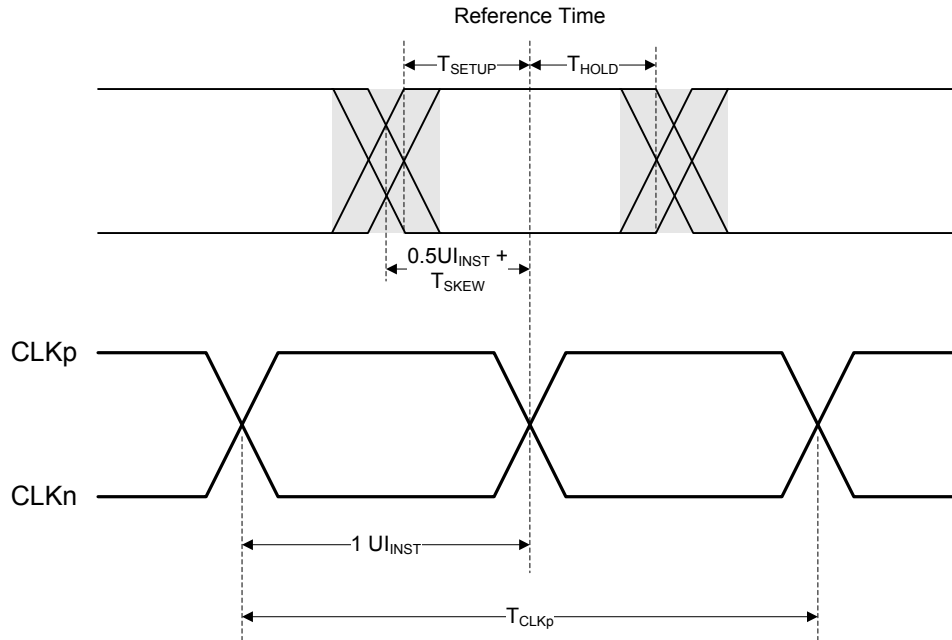
1603   **Figure 53 Data to Clock Timing Definitions**

1604   **9.2.1   Data-Clock Timing Specifications**

1605   The Data-Clock timing specifications are shown in Table 27. Implementers shall specify a value $UI_{INST,MIN}$
1606   that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given
1607   implementation. Parameters in Table 27 are specified as a part of this value. The skew specification,
1608 $T_{SKEW[TX]}$, is the allowed deviation of the data launch time to the ideal ½UI_{INST} displaced quadrature clock
1609   edge. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships
1610   between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising
1611   or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a
1612   rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum
1613   variations observable at the receiver for which the receiver will operate at the maximum specified
1614   acceptable bit error rate.

1615   The intent in the timing budget is to leave $0.4*UI_{INST}$, i.e. $\pm 0.2*UI_{INST}$ for degradation contributed by the
1616   interconnect.

1617   **Table 27 Data-Clock Timing Specifications**

Parameter	Symbol	Min	Typ	Max	Units	Notes
Data to Clock Skew (measured at transmitter)	$T_{SKEW[TX]}$	-0.15		0.15	UI_{INST}	1
Data to Clock Setup Time (receiver)	$T_{SETUP[RX]}$	0.15			UI_{INST}	2
Clock to Data Hold Time (receiver)	$T_{HOLD[RX]}$	0.15			UI_{INST}	2

1618   Notes:

1619   1.   Total silicon and package delay budget of $0.3*UI_{INST}$

1620   2.   Total setup and hold window for receiver of $0.3*UI_{INST}$

1621 ## 9.3   Reverse High-Speed Data Transmission Timing

1622 This section only applies to Half-Duplex Lane Modules that include Reverse High-Speed Data
1623 Transmission functionality.

1624 A Lane enters the Reverse High-Speed Data Transmission mode by means of a Link Turnaround procedure
1625 as specified in section 5.5. Reverse Data Transmission is not source-synchronous; the Clock signal is
1626 driven by the Master side while the Data Lane is driven by the Slave side. The Slave Side transmitter shall
1627 send one data bit every two periods of the received Clock signal. Therefore, for a given Clock frequency,
1628 the Reverse direction data rate is one-fourth the Forward direction data rate. The bit period in this case is
1629 defined to be $4*UI_{INST}$. UI_{INST} is the value specified for the full-rate forward transmission.

1630 Note that the clock source frequency may change between transmission bursts. However, all Data Lanes
1631 shall be in a Low-Power state before changing the clock source frequency.

1632 The conceptual overview of Reverse HS Data Transmission is shown in Figure 54.
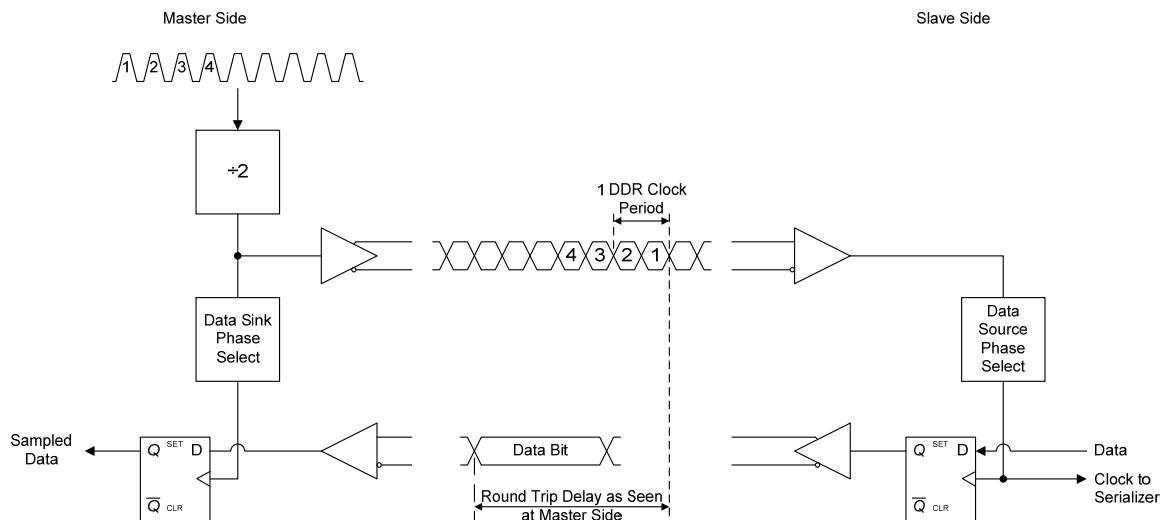
1633
1634 **Figure 54 Conceptual View of HS Data Transmission in Reverse Direction**

1635 There are four possible phase relationships between clock and data signals in the Reverse direction. The
1636 Clock phase used to send data is at the discretion of the Slave side, but once chosen it shall remain fixed
1637 throughout that data transmission burst. Signal delays in the interconnect, together with internal signal
1638 delays in the Master and Slave Modules, cause a fixed, but unknown, phase relationship in the Master
1639 Module between received (Reverse) Data and its own (Forward) Clock. Therefore, the Reverse traffic
1640 arriving at the Master side may not be phase aligned with the Forward direction clock.

1641 Synchronization between Clock and Data signals is achieved with the Sync sequence sent by the Slave
1642 during the Start of Transmission (SoT). The Master shall include sufficient functionality to correctly
1643 sample the received data given the instantaneous UI variations of the Clock sent to the Slave.

1644 Reverse transmission by the Slave side is one-fourth of the Forward direction speed, based on the Forward
1645 direction Clock as transmitted via the Clock Lane. This ratio makes it easy to find a suitable phase at the
1646 Master Side for Data recovery of Reverse direction traffic.

1647 The known transitions of the received Sync sequence shall be used to select an appropriate phase of the
1648 clock signal for data sampling. Thus, there is no need to specify the round trip delay between the source of
1649 the clock and the receiver of the data.

1650   The timing of the Reverse transmission as seen at the Slave side is shown in Figure 55.
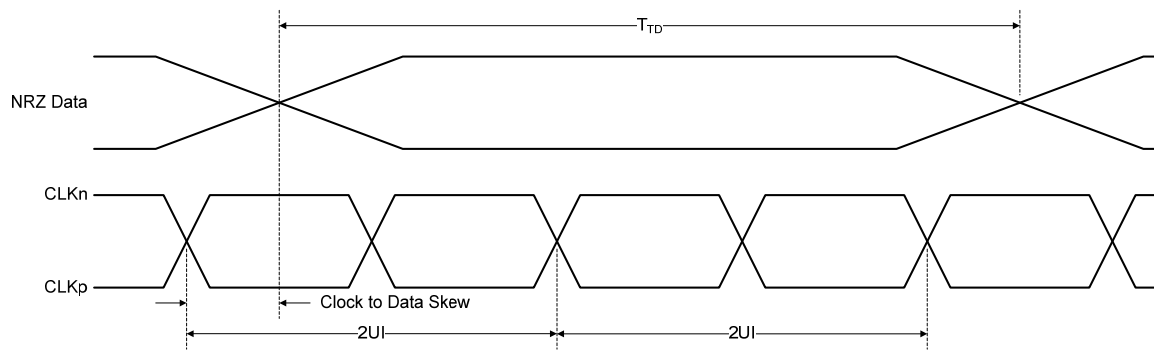
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1653   **Figure 55 Reverse High-Speed Data Transmission Timing at Slave Side**

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1655 **10 Regulatory Requirements**

1656 All MIPI D-PHY based devices should be designed to meet the applicable regulatory requirements.

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Annex A Logical PHY-Protocol Interface Description (informative)

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The PHY Protocol Interface (PPI) is used to make a connection between the PHY Lane Modules and the higher protocol layers of a communication stack. The interface described here is intended to be generic and application independent.

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This appendix is informative only. Conformance to the D-PHY specification does not depend on any portion of the PPI defined herein. Because of that, this section avoids normative language and does not use words like "shall" and "should." Instead, present tense language has been used to describe the PPI, utilizing words like "is" and "does." The reader may find it helpful to consider this appendix to be a description of an example implementation, rather than a specification.

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This PPI is optimized for controlling a D-PHY and transmitting and receiving parallel data. The interface described here is defined as an on-chip connection, and does not attempt to minimize signal count or define timing parameters or voltage levels for the PPI signals.

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A.1   Signal Description

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Table 28 defines the signals used in the PPI. For a PHY with multiple Data Lanes, a set of PPI signals is used for each Lane. Each signal has been assigned into one of six categories: High-Speed transmit signals, High-Speed receive signals, Escape mode transmit signals, Escape mode receive signals, control signals, and error signals. Bi-directional High-Speed Data Lanes with support for bi-directional Escape mode include nearly all of the signals listed in the table. Unidirectional Lanes or Clock Lanes include only a subset of the signals. The direction of each signal is listed as "I" or "O". Signals with the direction "I" are PHY inputs, driven from the Protocol. Signals with the direction "O" are PHY outputs, driven to the Protocol. For this logical interface, most clocks are described as being generated outside the PHY, although any specific PHY may implement the clock circuit differently.

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The "Categories" column in Table 28 indicates for which Lane Module types each signal applies. The category names are described in Table 1 and are summarized here for convenience. Each category is described using a four-letter acronym, defined as <Side, HS-capabilities, Escape-Forward, Escape-Reverse>. The first letter, Side, can be M (Master) or S (Slave). The second letter, High-Speed capabilities, can be F (Forward data), R (Reverse and Forward data), or C (Clock). The third and fourth letters indicate Escape mode capability in the Forward and Reverse directions, respectively. For Data Lanes, the third letter can be A (All) or E (Events – Triggers and ULPS only), while the fourth letter can be A (All, including LPDT), E (Events, triggers and ULPS only), Y (Any but not None: so A or E) or N (None). For a Data Lane, any of the four identification letters can be replaced by an X, to indicate that each of the available options is appropriate. For a Clock Lane, only the first letter can be X, while the other three letters are always CNN.

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Table 28 PPI Signals

Symbol	Dir	Categories	Description
High-Speed Transmit Signals			
TxDDRClkHS-I	I	MXXX	Data Lane High-Speed Transmit DDR Clock.
		MCNN	This signal is used to transmit High-Speed data bits over the Lane Interconnect. All Data Lanes use the same TxDDRClkHS-I (in-phase) clock signal.

Symbol	Dir	Categories	Description
TxDDRClkHS-Q	I	MCNN	Clock Lane High-Speed Transmit DDR Clock. This signal is used to generate the High-Speed clock signal for the Lane Interconnect. The TxDDRClkHS-Q (quadrature) clock signal is phase shifted from the TxDDRClkHS-I clock signal.
TxByteClkHS	O	MXXX SRXX	High-Speed Transmit Byte Clock. This is used to synchronize PPI signals in the High-Speed transmit clock domain. It is recommended that all transmitting Data Lane Modules share one TxByteClkHS signal. The frequency of TxByteClkHS is exactly 1/8 the High-Speed bit rate.
TxDataHS[7:0]	I	MXXX SRXX	High-Speed Transmit Data. Eight bit High-Speed data to be transmitted. The signal connected to TxDataHS[0] is transmitted first. Data is captured on rising edges of TxByteClkHS.
TxRequestHS	I	MXXX SRXX MCNN	High-Speed Transmit Request and Data Valid. A low-to-high transition on TxRequestHS causes the Lane Module to initiate a Start-of-Transmission sequence. A high-to-low transition on TxRequest causes the Lane Module to initiate an End-of-Transmission sequence. For Clock Lanes, this active high signal causes the Lane Module to begin transmitting a High-Speed clock. For Data Lanes, this active high signal also indicates that the protocol is driving valid data on TxDataHS to be transmitted. The Lane Module accepts the data when both TxRequestHS and TxReadyHS are active on the same rising TxByteClkHS clock edge. The protocol always provides valid transmit data when TxRequestHS is active. Once asserted, TxRequestHS remains high until the data has been accepted, as indicated by TxReadyHS. TxRequestHS is only asserted while TxRequestEsc is low.
TxReadyHS	O	MXXX SRXX	High-Speed Transmit Ready. This active high signal indicates that TxDataHS is accepted by the Lane Module to be serially transmitted. TxReadyHS is valid on rising edges of TxByteClkHS.
High-Speed Receive Signals			
RxByteClkHS	O	MRXX SXXX	High-Speed Receive Byte Clock. This is used to synchronize signals in the High-Speed receive clock domain. The RxByteClkHS is generated by dividing the received High-Speed DDR clock.

Symbol	Dir	Categories	Description
RxDataHS[7:0]	O	MRXX	High-Speed Receive Data.
		SXXX	Eight bit High-Speed data received by the Lane Module. The signal connected to RxDataHS[0] was received first. Data is transferred on rising edges of RxByteClkHS.
RxValidHS	O	MRXX	High-Speed Receive Data Valid.
		SXXX	This active high signal indicates that the Lane Module is driving data to the protocol on the RxDataHS output. There is no "RxReadyHS" signal, and the protocol is expected to capture RxDataHS on every rising edge of RxByteClkHS where RxValidHS is asserted. There is no provision for the protocol to slow down ("throttle") the receive data.
RxActiveHS	O	MRXX	High-Speed Reception Active.
		SXXX	This active high signal indicates that the Lane Module is actively receiving a High-Speed transmission from the Lane interconnect.
RxSyncHS	O	MRXX	Receiver Synchronization Observed.
		SXXX	This active high signal indicates that the Lane Module has seen an appropriate synchronization event. In a typical High-Speed transmission, RxSyncHS is high for one cycle of RxByteClkHS at the beginning of a High-Speed transmission when RxActiveHS is first asserted.
RxClkActiveHS	O	SCNN	Receiver Clock Active.
			This asynchronous, active high signal indicates that a Clock Lane is receiving a DDR clock signal.
RxDDRClkHS	O	SCNN	Receiver DDR Clock.
			This is the received DDR clock – it may be used by the protocol if required. This signal is low whenever RxClkActiveHS is low.
Escape Mode Transmit Signals			
TxClkEsc	I	MXXX	Escape mode Transmit Clock.
		SXXY	This clock is directly used to generate escape sequences. The period of this clock determines the phase times for Low-Power signals as defined in section 5.6.2. It is therefore constrained by the normative part of the D-PHY specification. See section 8. Note that this clock is used to synchronize TurnRequest and is included for any module that supports bi-directional High-Speed operation, even if that module does not support transmit or bi-directional escape mode.

Symbol	Dir	Categories	Description
TxRequestEsc	I	MXXX SXXY	Escape mode Transmit Request. This active high signal, asserted together with exactly one of TxLpdtEsc, TxUlpsEsc, or one bit of TxTriggerEsc, is used to request entry into escape mode. Once in escape mode, the Lane stays in escape mode until TxRequestEsc is de-asserted. TxRequestEsc is only asserted by the protocol while TxRequestHS is low.
TxLpdtEsc	I	MXAX SXXA	Escape mode Transmit Low-Power Data. This active high signal is asserted with TxRequestEsc to cause the Lane Module to enter Low-Power data transmission mode. The Lane Module remains in this mode until TxRequestEsc is de-asserted. TxUlpsEsc and all bits of TxTriggerEsc are low when TxLpdtEsc is asserted.
TxUlpsExit	I	MXXX SXXY MCNN	Transmit ULP Exit Sequence. This active high signal is asserted when ULP state is active and the protocol is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark-1 after TxUlpsExit is asserted. The PHY later drives the Stop state (LP-11) when TxRequestEsc is deasserted. TxUlpsExit is synchronous to TxClkEsc. This signal is ignored when the Lane is not in the ULP State.
TxUlpsEsc	I	MXXX SXXY	Escape mode Transmit Ultra-Low Power State. This active high signal is asserted with TxRequestEsc to cause the Lane Module to enter the Ultra-Low Power State. The Lane Module remains in this mode until TxRequestEsc is de-asserted. TxLpdtEsc and all bits of TxTriggerEsc are low when TxUlpsEsc is asserted.
TxTriggerEsc[3:0]	I	MXXX SXXY	Escape mode Transmit Trigger 0-3. One of these active high signals is asserted with TxRequestEsc to cause the associated Trigger to be sent across the Lane interconnect. In the receiving Lane Module, the same bit of RxTriggerEsc is then asserted and remains asserted until the Lane interconnect returns to Stop state, which happens when TxRequestEsc is de-asserted at the transmitter. Only one bit of TxTriggerEsc is asserted at any given time, and only when TxLpdtEsc and TxUlpsEsc are both low.

Symbol	Dir	Categories	Description
TxDataEsc[7:0]	I	MXAX	Escape mode Transmit Data.
		SXXA	This is the eight bit escape mode data to be transmitted in Low-Power data transmission mode. The signal connected to TxDataEsc[0] is transmitted first. Data is captured on rising edges of TxClkEsc.
TxValidEsc	I	MXAX	Escape mode Transmit Data Valid.
		SXXA	This active high signal indicates that the protocol is driving valid data on TxDataEsc to be transmitted. The Lane Module accepts the data when TxRequestEsc, TxValidEsc and TxReadyEsc are all active on the same rising TxClkEsc clock edge.
TxReadyEsc	O	MXAX	Escape mode Transmit Ready.
		SXXA	This active high signal indicates that TxDataEsc is accepted by the Lane Module to be serially transmitted. TxReadyEsc is valid on rising edges of TxClkEsc.
Escape Mode Receive Signals			
RxClkEsc	O	MXXY	Escape mode Receive Clock.
		SXXX	This signal is used to transfer received data to the protocol during escape mode. This "clock" is generated from the two Low-Power signals in the Lane interconnect. Because of the asynchronous nature of Escape mode data transmission, this "clock" may not be periodic.
RxLpdtEsc	O	MXXA	Escape Low-Power Data Receive mode.
		SXAX	This active high signal is asserted to indicate that the Lane Module is in Low-Power data receive mode. While in this mode, received data bytes are driven onto the RxDataEsc output when RxValidEsc is active. The Lane Module remains in this mode with RxLpdtEsc asserted until a Stop state is detected on the Lane interconnect.
RxUlpsEsc	O	MXXY	Escape Ultra-Low Power (Receive) mode.
		SXXX	This active high signal is asserted to indicate that the Lane Module has entered the Ultra-Low Power State. The Lane Module remains in this mode with RxUlpsEsc asserted until a Stop state is detected on the Lane interconnect.
RxTriggerEsc[3:0]	O	MXXY	Escape mode Receive Trigger 0-3.
		SXXX	These active high signals indicate that a trigger event has been received. The asserted RxTriggerEsc signal remains active until a Stop state is detected on the Lane interconnect.

Symbol	Dir	Categories	Description
RxDataEsc[7:0]	O	MXXA	Escape mode Receive Data.
		SXAX	This is the eight-bit escape mode Low-Power data received by the Lane Module. The signal connected to RxDataEsc[0] was received first. Data is transferred on rising edges of RxClkEsc.
RxValidEsc	O	MXXA	Escape mode Receive Data Valid.
		SXAX	This active high signal indicates that the Lane Module is driving valid data to the protocol on the RxDataEsc output. There is no "RxReadyEsc" signal, and the protocol is expected to capture RxDataEsc on every rising edge of RxClkEsc where RxValidEsc is asserted. There is no provision for the protocol to slow down ("throttle") the receive data.
Control Signals			
TurnRequest	I	XRXX	Turn Around Request.
		XFXY	This active high signal is used to indicate that the protocol desires to turn the Lane around, allowing the other side to begin transmission. TurnRequest is valid on rising edges of TxClkEsc. TurnRequest is only meaningful for a Lane Module that is currently the transmitter (Direction=0). If the Lane Module is in receive mode (Direction=1), this signal is ignored.
Direction	O	XRXX	Transmit/Receive Direction.
		XFXY	This signal is used to indicate the current direction of the Lane interconnect. When Direction=0, the Lane is in transmit mode (0=Output). When Direction=1, the Lane is in receive mode (1=Input).
TurnDisable	I	XRXX	Disable Turn-around.
		XFXY	This signal is used to prevent a (bi-directional) Lane from going into transmit mode – even if it observes a turn-around request on the Lane interconnect. This is useful to prevent a potential "lock-up" situation when a unidirectional Lane Module is connected to a bi-directional Lane Module.
ForceRxmode	I	MRXX	Force Lane Module Into Receive mode / Wait for Stop state.
		MXXY	
		SXXX	This signal allows the protocol to initialize a Lane Module, or force a bi-directional Lane Module, into receive mode. This signal is used during initialization or to resolve a contention situation. When this signal is high, the Lane Module immediately transitions into receive control mode and waits for a Stop state to appear on the Lane interconnect. When used for initialization, this signal should be released, i.e. driven low, only when the Dp & Dn inputs are in Stop state for a time T_{INIT}, or longer.

Symbol	Dir	Categories	Description
ForceTxStopmode	I	MXXX SRXX SXXY	Force Lane Module Into Transmit mode / Generate Stop state. This signal allows the protocol to force a Lane Module into transmit mode and Stop state during initialization or following an error situation, e.g. expired time out. When this signal is high, the Lane Module immediately transitions into transmit mode and the module state machine is forced into the Stop state.
Stopstate	O	XXXX XCNN	Lane is in Stop state. This active high signal indicates that the Lane Module, regardless of whether the Lane Module is a transmitter or a receiver, is currently in Stop state. Note that this signal is asynchronous to any clock in the PPI interface. Also, the protocol may use this signal to indirectly determine if the PHY line levels are in the LP-11 state.
Enable	I	XXXX XCNN	Enable Lane Module. This active high signal forces the Lane Module out of "shutdown". All line drivers, receivers, terminators, and contention detectors are turned off when Enable is low. Furthermore, while Enable is low, all other PPI inputs are ignored and all PPI outputs are driven to the default inactive state. Enable is a level sensitive signal and does not depend on any clock.
TxUlpsClk	I	MCNN	Transmit Ultra-Low Power State on Clock Lane. This active high signal is asserted to cause a Clock Lane Module to enter the Ultra-Low Power State. The Lane Module remains in this mode until TxUlpsClk is de-asserted.
RxUlpsClkNot	O	SCNN	Receive Ultra-Low Power State on Clock Lane. This active low signal is asserted to indicate that the Clock Lane Module has entered the Ultra-Low Power State. The Lane Module remains in this mode with RxUlpsClkNot asserted until a Stop state is detected on the Lane Interconnect.

Symbol	Dir	Categories	Description
UlpsActiveNot	O	XXXX	ULP State (not) Active.
		XCNN	This active low signal is asserted to indicate that the Lane is in ULP state.
			For a transmitter, this signal is asserted some time after TxUlpsEsc and TxRequestEsc (TxUlpsClk for a Clock Lane) are asserted. The transmitting PHY continues to supply TxClkEsc until UlpsActiveNot is asserted. In order to leave ULP state, the transmitter first drives TxUlpsExit high, then waits for UlpsActiveNot to become high (inactive). At that point, the transmitting PHY is active and has started transmitting a Mark-1 on the Lines. The protocol waits for a time Twakeup and then drives TxRequestEsc (TxUlpsClk) inactive to return the Lane to Stop state.
			For a receiver, this signal indicates that the Lane is in ULP state. At the beginning of ULP state, UlpsActiveNot is asserted together with RxUlpsEsc, or RxClkUlpsNot for a Clock Lane. At the end of the ULP state, this signal becomes inactive to indicate that the Mark-1 state has been observed. Later, after a period of time Twakeup, the RxUlpsEsc (or RxClkUlpsNot) signal is deasserted.
Error Signals			
ErrSotHS	O	MRXX	Start-of-Transmission (SoT) Error.
		SXXX	If the High-Speed SoT leader sequence is corrupted, but in such a way that proper synchronization can still be achieved, this active high signal is asserted for one cycle of RxByteClkHS. This is considered to be a "soft error" in the leader sequence and confidence in the payload data is reduced.
ErrSotSyncHS	O	MRXX	Start-of-Transmission Synchronization Error.
		SXXX	If the High-Speed SoT leader sequence is corrupted in a way that proper synchronization cannot be expected, this active high signal is asserted for one cycle of RxByteClkHS.
ErrEsc	O	MXXY	Escape Entry Error.
		SXXX	If an unrecognized escape entry command is received, this active high signal is asserted and remains asserted until the next change in line state.
ErrSyncEsc	O	MXXA	Low-Power Data Transmission Synchronization Error.
		SXAX	If the number of bits received during a Low-Power data transmission is not a multiple of eight when the transmission ends, this active high signal is asserted and remains asserted until the next change in line state.

Symbol	Dir	Categories	Description
ErrControl	O	MXXY	Control Error.
		SXXX	This active high signal is asserted when an incorrect line state sequence is detected. For example, if a turn-around request or escape mode request is immediately followed by a Stop state instead of the required Bridge state, this signal is asserted and remains asserted until the next change in line state.
ErrContentionLP0	O	MXXX	LP0 Contention Error.
		SXXY	This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low.
ErrContentionLP1	O	MXXX	LP1 Contention Error.
		SXXY	This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line high.

A.2   High-Speed Transmit from the Master Side

Figure 56 shows an example of a High-Speed transmission on the Master side. While TxRequestHS is low, the Lane Module ignores the value of TxDataHS. To begin transmission, the protocol drives TxDataHS with the first byte of data and asserts TxRequestHS. This data byte is accepted by the PHY on the first rising edge of TxByteClkHS with TxReadyHS also asserted. At this point, the protocol logic drives the next data byte onto TxDataHS. After every rising clock cycle with TxReadyHS active, the protocol supplies a new valid data byte or ends the transmission. After the last data byte has been transferred to the Lane Module, TxRequestHS is driven low to cause the Lane Module to stop the transmission and enter Stop state. The minimum number of bytes transmitted could be as small as one.
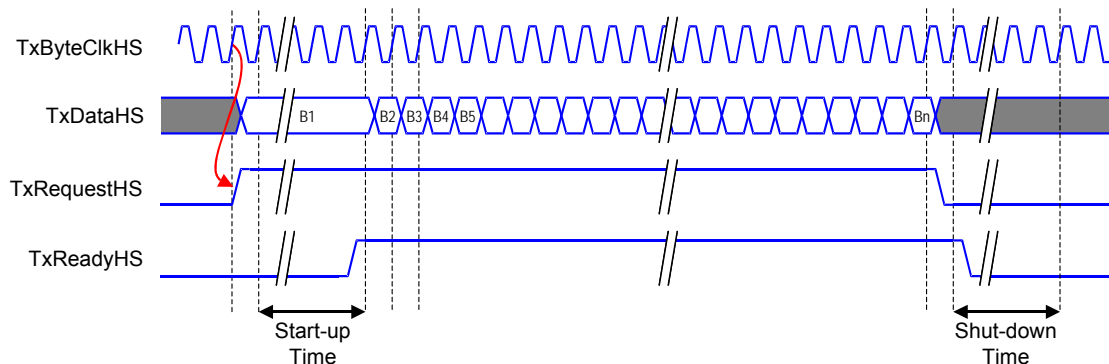
Figure 56 Example High-Speed Transmission from the Master Side

A.3   High-Speed Receive at the Slave Side

Figure 57 shows an example of a High-Speed reception at the Slave side. The RxActiveHS signal indicates that a receive operation is occurring. A normal reception starts with a pulse on RxSyncHS followed by valid receive data on subsequent cycles of RxByteClkHS. Note that the protocol is prepared to receive all of the data. There is no method for the receiving protocol to pause or slow data reception.

1709   If EoT Processing is performed inside the PHY, the RxActiveHS and RxValidHS signals transition low
1710   following the last valid data byte, Bn. See Figure 57.

1711   If EoT processing is not performed in the PHY, one or more additional bytes are presented after the last
1712   valid data byte. The first of these additional bytes, shown as byte "C" in Figure 57, is all ones or all zeros.
1713   Subsequent bytes may or may not be present, and can have any value. For a PHY that does not perform
1714   EoT processing, the RxActiveHS and RxValidHS signals transition low simultaneously some time after
1715   byte "C" is received. Once these signals have transitioned low, they remain low until the next High-Speed
1716   data reception begins.
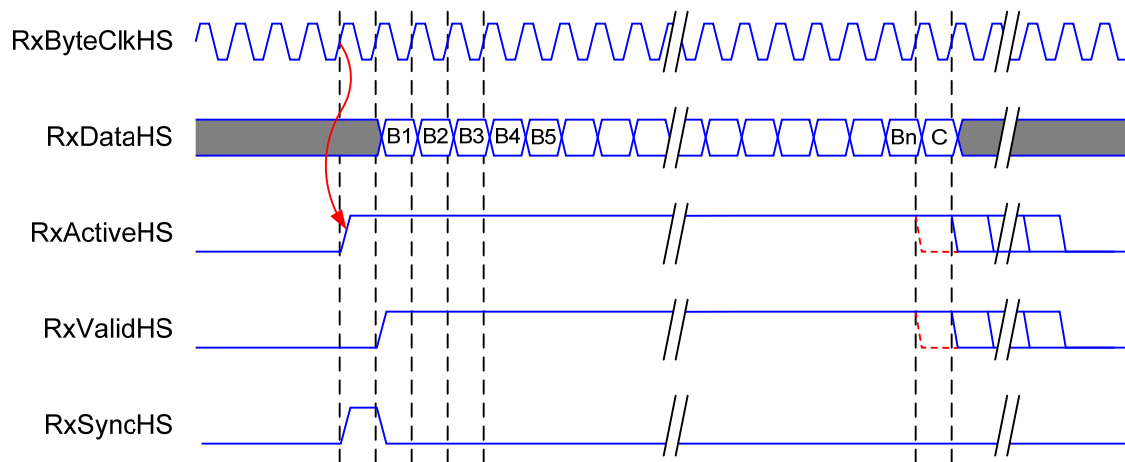
1717
1718   **Figure 57 Example High-Speed Receive at the Slave Side**

1719   ## A.4   High-Speed Transmit from the Slave Side

1720   A Slave can only transmit at one-fourth the bandwidth of a Master. Because of this, the TxReadyHS signal
1721   is not constant high for a transmitting slave. Otherwise, the transmission is very much like that seen at the
1722   PPI interface of a transmitting Master-side Lane Module. Figure 58 shows an example of transmitting from
1723   the Slave side.
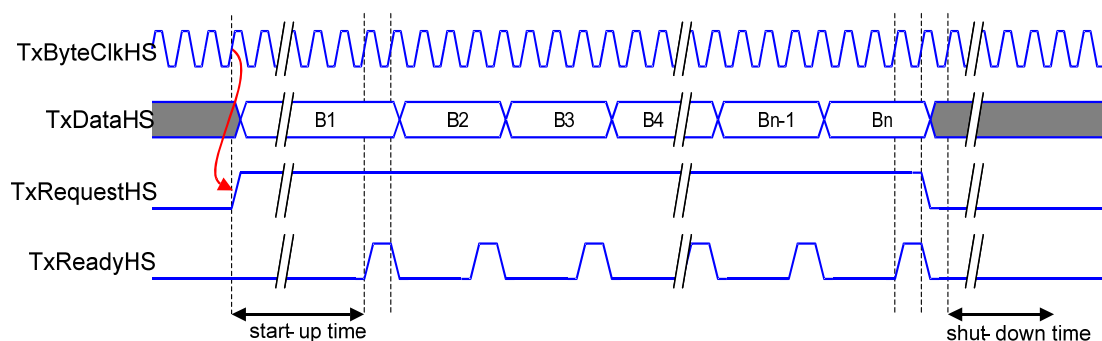
1724
1725   **Figure 58 Example High-Speed Transmit from the Slave Side**

1726   ## A.5   High-Speed Receive at the Master Side

1727   Because a Slave is restricted to transmitting at one-fourth the bandwidth of a Master, the RxValidHS signal
1728   is only asserted one out of every four cycles of RxByteClkHS during a High-Speed receive operation at the

1729   Master side. An example of this is shown in Figure 59. Note that, depending on the bit rate, there may be
1730   one or more extra pulses on RxValidHS after the last valid byte, Bn, is received.

1731
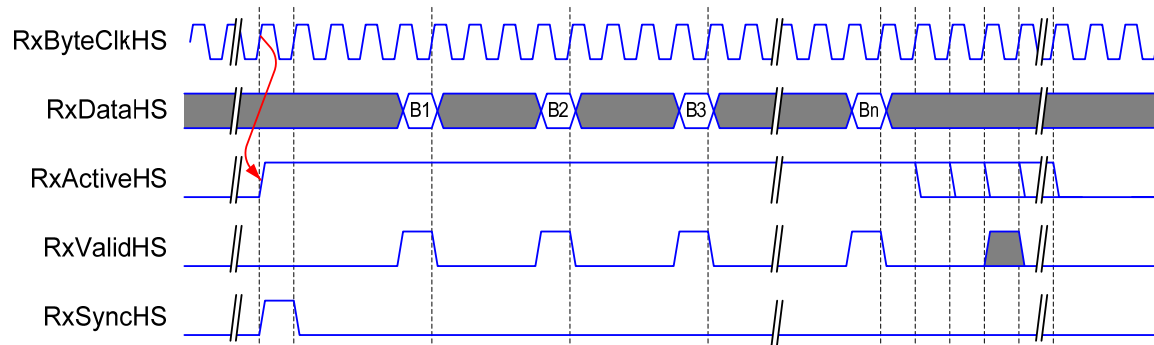
1732   **Figure 59 Example High-Speed Receive at the Master Side**

1733   ## A.6   Low-Power Data Transmission

1734   For Low-Power data transmission the TxClkEsc is used instead of TxDDRClkHS-I/Q and TxByteClkHS.
1735   Furthermore, while the High-Speed interface signal TxRequestHS serves as both a transmit request and a
1736   data valid signal, on the Low-Power interface two separate signals are used. The Protocol directs the Data
1737   Lane to enter Low-Power data transmission Escape mode by asserting TxRequestEsc with TxLpdtEsc
1738   high. The Low-Power transmit data is transferred on the TxDataEsc lines when TxValidEsc and
1739   TxReadyEsc are both active at a rising edge of TxClkEsc. The byte is transmitted in the time after the
1740   TxDataEsc is accepted by the Lane Module (TxValidEsc = TxReadyEsc = high) and therefore the
1741   TxClkEsc continues running for some minimum time after the last byte is transmitted. The Protocol knows
1742   the byte transmission is finished when TxReadyEsc is asserted. After the last byte has been transmitted, the
1743   protocol de-asserts TxRequestEsc to end the Low-Power data transmission. This causes TxReadyEsc to
1744   return low, after which the TxClkEsc clock is no longer needed. Whenever TxRequestEsc transitions from
1745   high-to-low, it always remains in the low state for a minimum of two TxClkEsc clock cycles. Figure 60
1746   shows an example Low-Power data transmission operation.

1747
1748
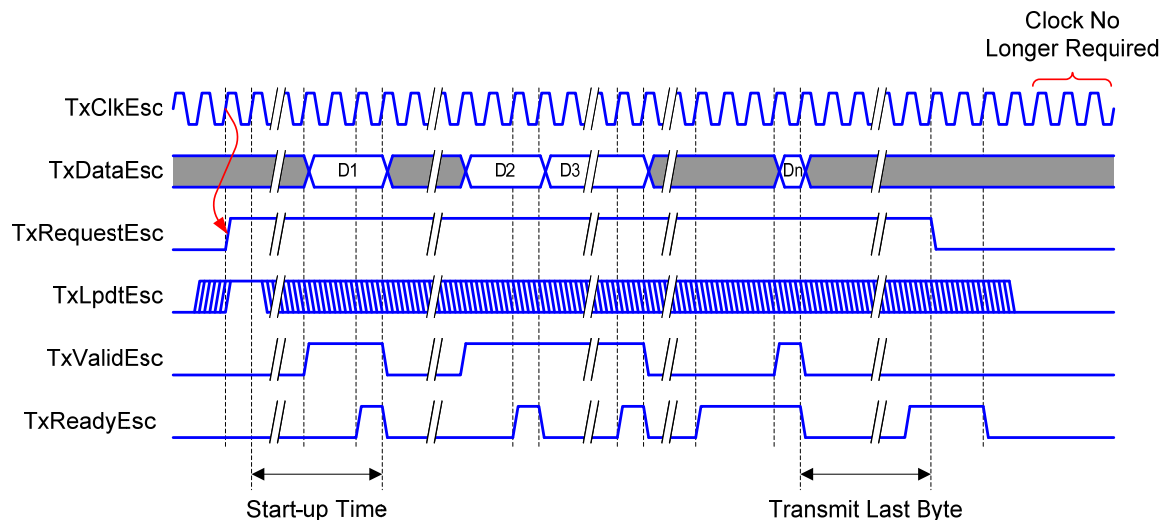
1749   **Figure 60 Low-Power Data Transmission**

1750 ## A.7   Low-Power Data Reception

1751 Figure 61 shows an example Low-Power data reception. In this example, a Low-Power escape "clock" is
1752 generated from the Lane Interconnect by the logical exclusive-OR of the Dp and Dn lines. This "clock" is
1753 used within the Lane Module to capture the transmitted data. In this example, the "clock" is also used to
1754 generate RxClkEsc.

1755 The signal RxLpdtEsc is asserted when the escape entry command is detected and stays high until the Lane
1756 returns to Stop state, indicating that the transmission has finished. It is important to note that because of the
1757 asynchronous nature of Escape mode transmission, the RxClkEsc signal can stop at anytime in either the
1758 high or low state. This is most likely to happen just after a byte has been received, but it could happen at
1759 other times as well.

1760
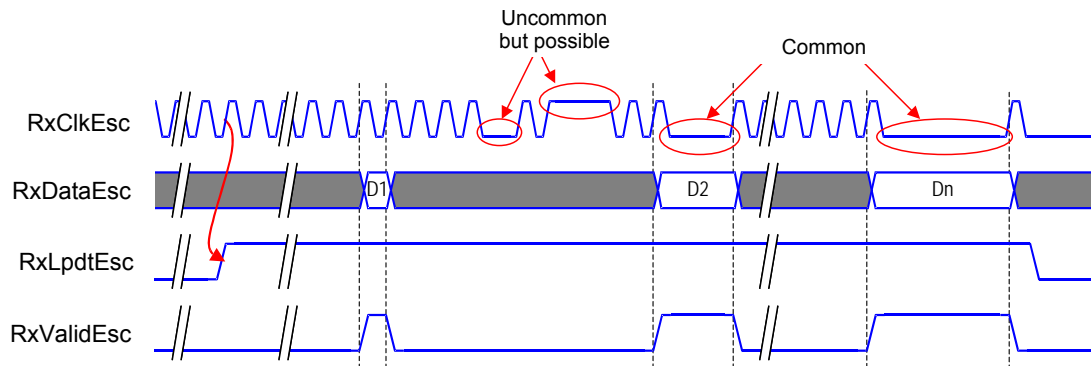
1761 **Figure 61 Example Low-Power Data Reception**

1762 ## A.8   Turn-around

1763 If the Master side and Slave side Lane Modules are both bi-directional, it is possible to turn around the
1764 Link for High-Speed and/or Escape mode signaling. As explained in section 5.5, which side is allowed to
1765 transmit is determined by passing a "token" back and forth. That is, the side currently transmitting passes
1766 the token to the receiving side. If the receiving side acknowledges the turn-around request, as indicated by
1767 driving the appropriate line state, the direction is switched.

1768 Figure 62 shows an example of two turn-around events. At the beginning, the local side is the transmitter,
1769 as shown by Direction=0. When the protocol on this side wishes to turn the Lane around (i.e. give the
1770 token to the other side), it asserts TurnRequest for at least one cycle of TxClkEsc. This initiates the turn-
1771 around procedure. The remote side acknowledges the turn-around request by driving the appropriate states
1772 on the Lines. When this happens, the local Direction signal changes from transmit (0) to receive (1).

1773 Later in the example of Figure 62, the remote side initiates a turn-around request, passing the token back to
1774 the local side. When this happens, the local Direction signal changes back to transmit (0). Note that there is
1775 no prescribed way for a receiver to request access to the Link. The current transmitter is in control of the
1776 Link direction and decides when to turn the Link around, passing control to the receiver.

1777 If the remote side does not acknowledge the turn-around request, the Direction signal does not change.
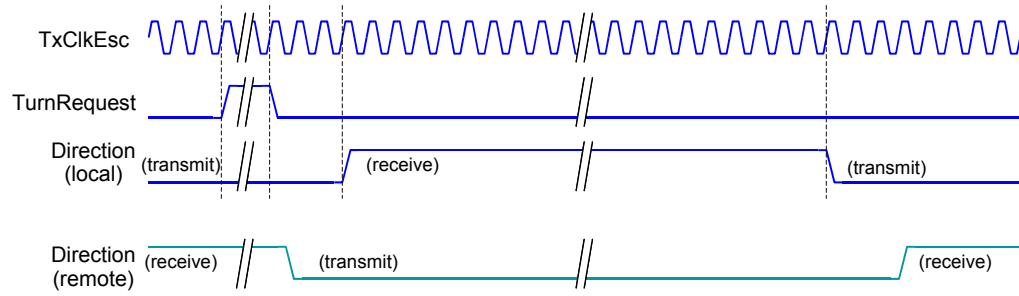
Figure 62 Example Turn-around Actions Transmit-to-Receive and Back to Transmit

Annex B Interconnect Design Guidelines (informative)

This appendix contains design guidelines in order to meet the interconnect requirements as specified in section 7.

B.1   Practical Distances

The maximum Lane flight time is defined at two nanoseconds. Assuming less than 100ps wiring delay within the RX-TX modules each, the physical distance that can be bridged with external interconnect is around 54cm/√ε. For most practical PCB and flex materials this corresponds to maximum distances around 25-30 cm.

B.2   RF Frequency Bands: Interference

On one side of the Lane there are the RF interference frequencies, which disturb the signals of the Lane. Most likely the dominant interferers are the transmit band frequencies of wireless interconnect standards. On the other side there are the frequencies for which generated EMI by the Lane should be as low as possible because very weak signals in these bands must be received by the radio IC. Some important frequency bands are:

Transmit Bands

- GSM 850 (824-849 MHz)
- GSM 900 (880-915 MHz)
- GSM DCS (1710-1785 MHz)
- GSM PCS (1850-1910 MHz)
- WCDMA (1920-1980 MHz)
- FLASH-OFDM, GSM (450 MHz)

Receive Bands:

- GSM 850 (869-894 MHz)
- GSM 900 (925-960 MHz)
- GSM DCS (1805-1880 MHz)
- GSM PCS (1930-1990 MHz)
- WCDMA (2110-2170 MHz)
- GPS (1574-1577 MHz)

It is important to identify the lowest interference frequency with significant impact, as this sets 'f_{INTMIN}'. For this specification, $f_{INT,MIN}$ is decided to be 450 MHz, because this frequency will most likely be used as the new WCDMA band in the USA in the future.

B.3   Transmission Line Design

In most cases the transmission lines will either be designed as striplines and/or micro-striplines. The coupling between neighboring lines within a pair is small if the distance between them is >2x the di-

1816   electrical thickness. For the separation of multiple pairs it is highly recommended to interleave the pairs
1817   with a ground or supply line in order to reduce coupling.

1818   ## B.4   Reference Layer

1819   In order to achieve good signal integrity and low EMI it is recommended that either a ground plane or a
1820   ground signal is in close proximity of any signal line.

1821   ## B.5   Printed-Circuit Board

1822   For boards with a large number of conductor layers the dielectric spacing between layers may become so
1823   small that it would be hard to meet the characteristic impedance requirements. In those cases a micro-
1824   stripline in the top or bottom layers may be a better solution.

1825   ## B.6   Flex-foils

1826   Either two conductor layers or a reasonable connected cover layer makes it much easier to meet the
1827   specifications

1828   ## B.7   Series Resistance

1829   The DC series resistance of the interconnect should be less then 5 Ohms in order to meet the specifications.
1830   It is strongly recommended to keep the resistance in the ground connection below 0.2 Ohm. Furthermore,
1831   the DC ground shift shall be less then 50mV, which may require an even lower value if a large current is
1832   flowing through this ground. The lower this ground series resistance value can be made, the better it is for
1833   reliability and robustness.

1834   ## B.8   Connectors

1835   Connectors usually cause some impedance discontinuity. It is important to carefully minimize these
1836   discontinuities by design, especially with respect to the through-connection of the reference layer.
1837   Although connectors are typically rather small in size, the wrong choice can mess-up signals completely.
1838   Please note that the contact resistance of connectors is part of the total series resistance budget and should
1839   therefore be sufficiently low.

1840

1841 Annex C 8b9b Line Coding for D-PHY (normative)

1842 Raw data transmission without constraining the data set does not allow in-band control signaling (control
1843 symbols inserted into the data stream) during transmission. Line coding conditions the possible bit
1844 sequences on the wires and provides reserved codes to include additional control features. Useful
1845 additional features may be, for example, idle symbols, specific-event identifiers, sync patterns, and
1846 protocol markers.

1847 Comma codes, bit sequences that do not appear anywhere in the data stream (in the absence of bit errors)
1848 unless these are intentionally transmitted, provide synchronization features and are very useful to increase
1849 robustness.

1850 Furthermore, a line-coding scheme that guarantees a minimum edge density improves the signaling quality
1851 and enables skew calibration in the PHY.

1852 Figure 63 shows how the line coding sub-layer fits into the standard hierarchy. The line coding can be
1853 considered as a separate sub-layer on top of the basic D-PHY. Optimizations by merging layers are allowed
1854 if the resulting solution complies with the PHY specification. These optimization choices are left to
1855 implementers.
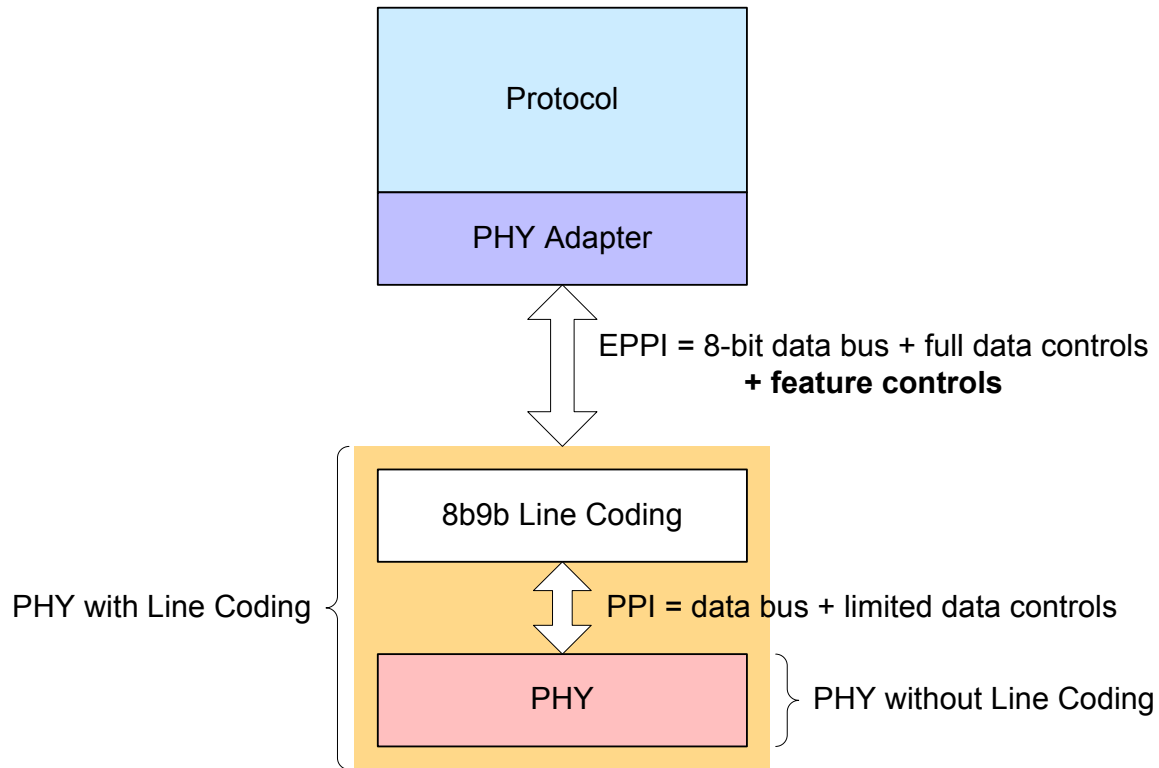
1856
1857 **Figure 63 Line Coding Layer**

1858 Note that the line coding sub-layer is optional. Protocols may exploit only the baseline PHY without line
1859 coding. This feature is provided for compatibility with existing protocols. However, in case a protocol
1860 decides to use line coding, it shall be implemented as described in this annex.

1861 The PHY-protocol interface above the line coding sub-layer (EPPI) is very similar to the PPI. Some
1862 additional signals enable a more functional and flexible control of the PHY with Line Coding. For details
1863 of the EPPI see section C.5.

1864 **C.1   Line Coding Features**

1865 The 8b9b line coding scheme provides features to both the PHY and protocol layers.

1866 **C.1.1   Enabled Features for the Protocol**

1867 • Comma code marker for special protocol features

1868 • Word synchronization/resynchronization during transmission bursts

1869 • Automatic idling support; no need for TX to always provide valid data during transmission

1870 • Possibility for future PHY compatible PHY-Protocol Interface (PPI)

1871 **C.1.2   Enabled Features for the PHY**

1872 • On-the-fly word resynchronization

1873 • Simplification of EoT signaling

1874 • Reduced latency

1875 • Automatic idle symbol insertion and removal in absence of data

1876 • Skew calibration in the RX possible

1877 **C.2   Coding Scheme**

1878 This section describes the details of the coding scheme.

1879 **C.2.1   8b9b Coding Properties**

1880 The 8b9b coding has the following properties:

1881 • All code words are nine bits long. Data is encoded byte-wise into 9-bit words, which corresponds
1882   to a 12.5% coding overhead.

1883 • Sixteen regular exception codes, i.e. code words that do not appear as regular data words, but
1884   require word sync for reliable recognition, are available.

1885 • Six unique exception codes, i.e. code words that do not appear within any sliding window except
1886   when that code word is transmitted, are available.

1887 • Guaranteed minimum edge density of at least two polarity transitions per word. Therefore, each
1888   word contains at least two ones and two zeros.

1889 • Simple logical functions for encoding and decoding

1890 • Run length is limited to a maximum of seven bits. Data codes have a maximum run length of five
1891   bits, unique exception codes have run lengths of six or seven bits.

1892 ## C.2.2   Data Codes: Basic Code Set

1893 Assume the following notation for the input data word and the coded data word:

1894 • 8-bit data byte: $[B_1\ B_2\ B_3\ X_1\ X_2\ Q_1\ Q_2\ Q_3]$

1895 • 9-bit code word: $[B_1\ X_1\ Y_1\ Y_2\ B_2\ B_3\ Y_3\ Y_4\ X_2]$

1896 The 256 data codes are denoted by Dxxx, where xxx is the value of the corresponding 8-bit data byte.

1897 The 8-bit data byte shall be the input for the encoding, and result of the decoding, function. There can be
1898 any arbitrary bijective 8b-to-8b logical transformation function between real source data bytes from the
1899 protocol and the input data bytes for encoding, as long as the inverse function is present at the receiver
1900 side. If such a function is used, it shall be defined in the protocol specification.

1901 The bits $\{B_1, B_2, B_3, X_1, X_2\}$ appear directly in the code words as can be seen in the code word structure.

1902 $\{Q_1, Q_2, Q_3\}$ are the remaining three bits in the data byte, which are encoded into $\{Y_1, Y_2, Y_3, Y_4\}$ using
1903 $\{X_1, X_2\}$. The decoding of $\{Y_1, Y_2, Y_3, Y_4\}$ into $\{Q_1, Q_2, Q_3\}$ does not require $\{X_1, X_2\}$.

1904 The relation between Q_i, X_i and Y_i is shown in Table 29.

1905 **Table 29 Encoding Table for 8b9b Line Coding of Data Words**

8-bit Data Byte								9-bit Code Word, Y bits			
B_1	B_2	B_3	X_1	X_2	Q_1	Q_2	Q_3	Y_1	Y_2	Y_3	Y_4
x			x	1	1	1	0	0	1	0	0
				0						1	1
				x	0	1	0			0	1
					1	0	0			1	0
x			x	1	1	1	1	1	0	0	0
				0						1	1
				x	0	1	1			0	1
					1	0	1			1	0
x			0	x	0	0	0	1	1	0	1
			1					0	0		
			0	x	0	0	1	1	1	1	0
			1					0	0		

1906 Notes:

1907 x = don't care

1908 The logical relation for encoding between $\{Q_1, Q_2, Q_3, X_1, X_2\}$ and $\{Y_1, Y_2, Y_3, Y_4\}$ is given by the
1909 following equations:

1910 $Y_1\quad = (\sim Q_1\ \&\ \sim Q_2\ \&\ \sim X_1)\ |\ (Q_1\ \&\ Q_3)\ |\ (Q_2\ \&\ Q_3)$

1911 $Y_2\quad = (\sim Q_1\ \&\ \sim Q_2\ \&\ \sim X_1)\ |\ (Q_1\ \&\ \sim Q_3)\ |\ (Q_2\ \&\ \sim Q_3)$

1912 $\qquad Y_3 \qquad = (Q_1 \And \sim Q_2) | (Q_1 \And Q_2 \And \sim X_2) | (\sim Q_2 \And Q_3)$

1913 $\qquad Y_4 \qquad = (\sim Q_1 \And Q_2) | (Q_1 \And Q_2 \And \sim X_2) | (\sim Q_1 \And \sim Q_3)$

1914 The logical relation for decoding between $\{Y_1, Y_2, Y_3, Y_4\}$ and $\{Q_1, Q_2, Q_3\}$ is:

1915 $\qquad Q_1 \qquad = (Y_1 \wedge Y_2) \And \sim (\sim Y_3 \And Y_4)$

1916 $\qquad Q_2 \qquad = (Y_1 \wedge Y_2) \And \sim (Y_3 \And \sim Y_4)$

1917 $\qquad Q_3 \qquad = (Y_1 \And \sim Y_2) | (Y_1 \And Y_2 \And Y_3) | (\sim Y_1 \And \sim Y_2 \And Y_3)$
1918 $\qquad\qquad\qquad = (Y_1 \And \sim Y_2) | (\sim (Y_1 \wedge Y_2) \And Y_3)$

1919 These logical functions show that the encoding and decoding can be implemented with a few dozen logic
1920 gates and therefore do not require additional hardware such as a lookup table or storage of history data.

1921 C.2.3 Comma Codes: Unique Exception Codes

1922 Unique means that these codes are uniquely identifiable in the data stream because these sequences do not
1923 occur in any encoding or across word boundaries, assuming no bits are corrupted. The data-encoding
1924 scheme described in section C.2.2 enables a very simple run-length limit based unique exception code
1925 mechanism.

1926 There are four code sequences available, called Type A Comma codes, with a run length of six bits, and
1927 two code sequences, called Type B Comma codes, with a run length of seven bits. Currently, four Comma
1928 codes are sufficient to cover the required features and therefore only Type A Comma codes are used. Type
1929 B Comma codes are reserved for future use.

1930   **Table 30 Comma Codes**

Type	Run Length, bits	Code Name	Comma code	Feature
Type A	6	C600	0 1111 1100	Protocol
		C611	1 0000 0011	EoT
		C610	1 0000 0010	Idle/Sync 1
		C601	0 1111 1101	Idle/Sync 2
Type B	7	C701	1 0000 0001	Reserved 1
		C710	0 1111 1110	Reserved 2

1931 C.2.4 Control Codes: Regular Exception Codes

1932 The normal data set does not use all codes with a maximum run-length of five bits. There are two
1933 combinations of the $\{X_i, Y_i\}$ bits that do not appear in any data code word that are available as regular
1934 exception codes. Since Comma Codes are defined to have a run-length of six or seven bits, this gives three
1935 freely usable bits per code word and results in $2*2^3=16$ different Regular Exception Codes. The syntax of
1936 the Regular Exception Code words is given in Table 31, where the bits B1, B2 and B3 can have any binary
1937 value.

1938   **Table 31 Regular Exception Code Structure**

	X_1	Y_1	Y_2			Y_3	Y_4	Y_2	Code Name
B_1	0	1	1	B_2	B_3	0	0	1	C410-C417
B_1	1	0	0	B_2	B_3	1	1	0	C400-C407

1939   These code words are not unique sequences like the Comma codes described in Table 30, but can only be
1940   used as exception codes if word sync is already accomplished. These codes are currently reserved and not
1941   yet allocated to any function.

C.2.5   Complete Coding Scheme

1943   The complete code table can be found in Table 33.

C.3   Operation with the D-PHY

1945   The line coding impacts the payload of transmission bursts. Section C.3.1 described the generic issues for
1946   both HS and LP transmission. Section C.3.2 and C.3.3 describe specific details for HS and LP
1947   transmission, respectively.

C.3.1   Payload: Data and Control

1949   The payload of a HS or LP transmission burst consists of concatenated serialized 9-bit symbols,
1950   representing both data and control information.

C.3.1.1   Idle/Sync Comma Symbols

1952   Idle/Sync Comma code words can be present as symbols within the payload of a transmission burst. These
1953   symbols are inserted either on specific request of the protocol, or autonomously when there is a
1954   transmission request but there is no valid data available either at the beginning, or anywhere, during
1955   transmission. The Idle pattern in the latter case is an alternating C601 and C610 sequence, until there is
1956   valid data available to transmit, or transmission has ended. Idle periods may begin with either of the two
1957   prescribed Idle symbols. The RX-side PHY shall remove Idle/Sync symbols from the stream and flag these
1958   events to the protocol.

C.3.1.2   Protocol Marker Comma Symbol

1960   Comma symbol C600 (Protocol Marker) is allocated for use by protocols on top of the D-PHY. This
1961   symbol shall be inserted in the stream on request of the TX-side protocol and flagged by the receiving PHY
1962   to the RX-side protocol.

C.3.1.3   EoT Marker

1964   Comma symbol C611 is allocated as the EoT Marker symbol.

1965 **C.3.2   Details for HS Transmission**

1966 **C.3.2.1   SoT**

1967 The SoT procedure remains the same as the raw data D-PHY SoT. See section 5.4.2. The SoT sequence
1968 itself is NOT encoded, but can be easily recognized.

1969 The first bit of the first transmitted code symbol of a burst shall be aligned with the rising edge of the DDR
1970 clock.

1971 **C.3.2.2   HS Transmission Payload**

1972 The transmitted burst shall consist of concatenated serialized 9-bit symbols as described in section C.3.1.

1973 The TX-side PHY can idle by sending the Idle sequences as described in section C.3.1.1

1974 **C.3.2.3   EoT**

1975 The TX-side PHY shall insert an EoT marker symbol at the moment the request for HS transmission is
1976 withdrawn. The transmitter can pad additional bits after this EoT-Marker symbol before actually switching
1977 to LP mode (EoT sequence).

1978 The RX-side PHY shall remove the EoT-Marker symbol and any additional bits appearing after it. Note
1979 that with line coding, EoT-processing by backtracking on LP-11 detection to avoid (unreliable) non-
1980 payload bits on the PPI is no longer required as the EoT marker symbol notifies the RX-side PHY before
1981 the End-of-Transmission.

1982 **C.3.3   Details for LP Transmission**

1983 **C.3.3.1   SoT**

1984 The start of LP transmission is identical to basic D-PHY operation.

1985 **C.3.3.2   LP Transmission Payload**

1986 The transmitted burst shall consist of concatenated serialized 9-bit symbols as described in section C.3.1.

1987 During LPDT, the TX-side PHY can idle in two ways: either it can send the Idle sequences as described in
1988 section C.3.1.1 and implicitly provide a clock signal to the RX-side PHY, or it can pause the transmission
1989 by keeping the Lines at LP-00 (Space) for a certain period of time between bits, which interrupts the clock
1990 on the RX side, but minimizes power consumption.

1991 **C.3.3.3   EoT**

1992 The TX-side PHY shall insert an EoT marker symbol at the moment the request for LP transmission is
1993 withdrawn. The TX-side PHY can pad additional (spaced-one-hot) bits after the EoT-Marker symbol
1994 before actually ending the transmission by switching via Mark to Stop state (End of LPDT procedure).

1995 The RX-side PHY shall remove the EoT-marker symbol and any additional bits appearing after it.

1996 ## C.4   Error Signaling

1997 The usage of a line code scheme enables the detection of many signaling errors. These errors include:

1998 - Non-existing code words

1999 - Non-aligned Comma symbols

2000 - EoT detection without detection of EoT-Marker

2001 Detection and flagging of errors is not required, but may help the protocol to recover faster from an error
2002 situation.

2003 ## C.5   Extended PPI

2004 The interface to the protocol shall be extended with functional handles (TX) and flags (RX) to manage the
2005 usage of Comma symbols. Whenever necessary, the transmitting PHY can hold the data delivery from the
2006 protocol to the TX PHY with the TxReadyHS or TxReadyEsc signal. This is already provided for in the
2007 current PPI.

2008 The PPI shall be extended with a TX Valid signal for HS data transmission, TxValidHS. Encoded
2009 operation allows for Idling of the Link when there is no new valid data. If the transmitter is ready and the
2010 provided data is not valid, an Idle symbol shall be inserted into the stream. Note, contrary to the basic PHY
2011 PPI, the Valid signals for a coded PHY can be actively used to manage the data on both TX and RX sides.
2012 This arrangement provides more flexibility to the PHY and Protocol layers. For LPDT, this Valid signaling
2013 already exists in the PPI. Addition of TxValidHS signal eliminates the constraint in the PPI description for
2014 TxRequestHS that the "protocol always provides valid data".

2015 On the RX side, errors may be flagged to the protocol in case unexpected sequences are observed.
2016 Although many different errors are detectable, it is not required that all these errors flags be implemented.
2017 The number of error flags implemented depends on the cost/benefit trade-off to be made by the
2018 implementer. These error features do not impact compliance of the D-PHY. The signals are mentioned here
2019 for informative purposes only.

2020 All control signals shall remain synchronous to the TxByteClk, or RxByteClk. The control signal clock
2021 frequency shall be equal to or greater than 1/9 of the serial bit rate.

2022 Table 32 lists the additional signals for the PPI on top of the coding sub-layer (EPPI).

2023 **Table 32 Additional Signals for (Functional) PPI**

Symbol	Dir	Categories	Description
TxProMarkerEsc	I	MXAX (SXXA)	Functional handle to insert a Protocol-marker symbol in the serial stream for LPDT. Active HIGH signal
TxProMarkerHS	I	MXXX (SRXX)	Functional handle to insert a Protocol-marker symbol in the serial stream for HS transmission. Active HIGH signal
TxValidHS	I	MXXX (SRXX)	Functional handle for the protocol to hold on providing data to the PHY without ending the HS transmission. In the case of a continued transmission request without Valid data, the PHY coding layer inserts Idle symbols. Active HIGH signal

Symbol	Dir	Categories	Description
RxAlignErrorEsc	O	SXAX (MXXA)	Flag to indicate that a Comma code has been observed in the LPDT stream that was not aligned with the assumed word boundary. Active HIGH signal (optional)
RxAlignErrorHS	O	SXXX (MRXX)	Flag to indicate that a Comma code has been observed during HS reception that was not aligned with the assumed word boundary. Active HIGH signal (optional)
RxBadSymbolEsc	O	SXAX (MXXA)	Flag to indicate that a non-existing symbol was received using LPDT. Active HIGH signal (optional)
RxBadSymbolHS	O	SXXX (MRXX)	Flag to indicate that a non-existing symbol was received in HS mode. Active HIGH signal (optional)
RxEoTErrorEsc	O	SXAX (MXXA)	Flag to indicate that at EoT, after LP transmission, a transition to LP-11 has been detected without being preceded by an EoT-marker symbol. Active HIGH signal (optional)
RxEoTErrorHS	O	SXXX (MRXX)	Flag to indicate that at EoT, after HS transmission, a transition to LP-11 has been detected without being preceded by an EoT-marker symbol. Active HIGH signal (optional)
RxIdleEsc	O	SXAX (MXXA)	Indication flag that Idle patterns are observed at the Lines during LPDT. Active HIGH signal (optional)
RxIdleHS	O	SXXX (MRXX)	Indication flag that Idle patterns are observed at the Lines in HS mode. Active HIGH signal (optional)
RxProMarkerEsc	O	SXAX (MXXA)	Functional flag to know that a Protocol-marker symbol occurred in the serial stream using LPDT. This is communicated to the protocol synchronous with the data, exactly at the position where it occurred. Therefore, the interface either shows a flag plus non-valid data or no-flag with valid data. Active HIGH signal
RxProMarkerHS	O	SXXX (MRXX)	Functional flag to know that a Protocol-marker symbol occurred in the serial stream for HS mode. This is communicated to the protocol synchronous with the ByteClk, exactly at the position where it occurred. Therefore, the interface either shows a flag plus non-valid data or no-flag with valid data. Active HIGH signal

2024 **C.6   Complete Code Set**

2025 Table 33 contains the complete code set.

2026   **Table 33 Code Set (8b9b Line Coding)**

Name	Type	8-bit Data Byte								9-bit Symbol								
		B_1	B_2	B_3	X_1	X_2	Q_1	Q_2	Q_3	B_1	X_1	Y_1	Y_2	B_2	B_3	Y_3	Y_4	X_2
D000	Data	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0
D001	Data	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	0	0
D002	Data	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	0
D003	Data	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0
D004	Data	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0
D005	Data	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	0	0
D006	Data	0	0	0	0	0	1	1	0	0	0	0	1	0	0	1	1	0
D007	Data	0	0	0	0	0	1	1	1	0	0	1	0	0	0	1	1	0
D008	Data	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0	1	1
D009	Data	0	0	0	0	1	0	0	1	0	0	1	1	0	0	1	0	1
D010	Data	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	1	1
D011	Data	0	0	0	0	1	0	1	1	0	0	1	0	0	0	0	1	1
D012	Data	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0	1
D013	Data	0	0	0	0	1	1	0	1	0	0	1	0	0	0	1	0	1
D014	Data	0	0	0	0	1	1	1	0	0	0	0	1	0	0	0	0	1
D015	Data	0	0	0	0	1	1	1	1	0	0	1	0	0	0	0	0	1
D016	Data	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0
D017	Data	0	0	0	1	0	0	0	1	0	1	0	0	0	0	1	0	0
D018	Data	0	0	0	1	0	0	1	0	0	1	0	1	0	0	0	1	0
D019	Data	0	0	0	1	0	0	1	1	0	1	1	0	0	0	0	1	0
D020	Data	0	0	0	1	0	1	0	0	0	1	0	1	0	0	1	0	0
D021	Data	0	0	0	1	0	1	0	1	0	1	1	0	0	0	1	0	0
D022	Data	0	0	0	1	0	1	1	0	0	1	0	1	0	0	1	1	0
D023	Data	0	0	0	1	0	1	1	1	0	1	1	0	0	0	1	1	0
D024	Data	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1
D025	Data	0	0	0	1	1	0	0	1	0	1	0	0	0	0	1	0	1
D026	Data	0	0	0	1	1	0	1	0	0	1	0	1	0	0	0	1	1
D027	Data	0	0	0	1	1	0	1	1	0	1	1	0	0	0	0	1	1
D028	Data	0	0	0	1	1	1	0	0	0	1	0	1	0	0	1	0	1
D029	Data	0	0	0	1	1	1	0	1	0	1	1	0	0	0	1	0	1
D030	Data	0	0	0	1	1	1	1	0	0	1	0	1	0	0	0	0	1

Name	Type	8-bit Data Byte								9-bit Symbol								
		B_1	B_2	B_3	X_1	X_2	Q_1	Q_2	Q_3	B_1	X_1	Y_1	Y_2	B_2	B_3	Y_3	Y_4	X_2
D031	Data	0	0	0	1	1	1	1	1	0	1	1	0	0	0	0	0	1
D032	Data	0	0	1	0	0	0	0	0	0	0	1	1	0	1	0	1	0
D033	Data	0	0	1	0	0	0	0	1	0	0	1	1	0	1	1	0	0
D034	Data	0	0	1	0	0	0	1	0	0	0	0	1	0	1	0	1	0
D035	Data	0	0	1	0	0	0	1	1	0	0	1	0	0	1	0	1	0
D036	Data	0	0	1	0	0	1	0	0	0	0	0	1	0	1	1	0	0
D037	Data	0	0	1	0	0	1	0	1	0	0	1	0	0	1	1	0	0
D038	Data	0	0	1	0	0	1	1	0	0	0	0	1	0	1	1	1	0
D039	Data	0	0	1	0	0	1	1	1	0	0	1	0	0	1	1	1	0
D040	Data	0	0	1	0	1	0	0	0	0	0	1	1	0	1	0	1	1
D041	Data	0	0	1	0	1	0	0	1	0	0	1	1	0	1	1	0	1
D042	Data	0	0	1	0	1	0	1	0	0	0	0	1	0	1	0	1	1
D043	Data	0	0	1	0	1	0	1	1	0	0	1	0	0	1	0	1	1
D044	Data	0	0	1	0	1	1	0	0	0	0	0	1	0	1	1	0	1
D045	Data	0	0	1	0	1	1	0	1	0	0	1	0	0	1	1	0	1
D046	Data	0	0	1	0	1	1	1	0	0	0	0	1	0	1	0	0	1
D047	Data	0	0	1	0	1	1	1	1	0	0	1	0	0	1	0	0	1
D048	Data	0	0	1	1	0	0	0	0	0	1	0	0	0	1	0	1	0
D049	Data	0	0	1	1	0	0	0	1	0	1	0	0	0	1	1	0	0
D050	Data	0	0	1	1	0	0	1	0	0	1	0	1	0	1	0	1	0
D051	Data	0	0	1	1	0	0	1	1	0	1	1	0	0	1	0	1	0
D052	Data	0	0	1	1	0	1	0	0	0	1	0	1	0	1	1	0	0
D053	Data	0	0	1	1	0	1	0	1	0	1	1	0	0	1	1	0	0
D054	Data	0	0	1	1	0	1	1	0	0	1	0	1	0	1	1	1	0
D055	Data	0	0	1	1	0	1	1	1	0	1	1	0	0	1	1	1	0
D056	Data	0	0	1	1	1	0	0	0	0	1	0	0	0	1	0	1	1
D057	Data	0	0	1	1	1	0	0	1	0	1	0	0	0	1	1	0	1
D058	Data	0	0	1	1	1	0	1	0	0	1	0	1	0	1	0	1	1
D059	Data	0	0	1	1	1	0	1	1	0	1	1	0	0	1	0	1	1
D060	Data	0	0	1	1	1	1	0	0	0	1	0	1	0	1	1	0	1
D061	Data	0	0	1	1	1	1	0	1	0	1	1	0	0	1	1	0	1
D062	Data	0	0	1	1	1	1	1	0	0	1	0	1	0	1	0	0	1
D063	Data	0	0	1	1	1	1	1	1	0	1	1	0	0	1	0	0	1
D064	Data	0	1	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0

Name	Type	8-bit Data Byte								9-bit Symbol								
		B_1	B_2	B_3	X_1	X_2	Q_1	Q_2	Q_3	B_1	X_1	Y_1	Y_2	B_2	B_3	Y_3	Y_4	X_2
D065	Data	0	1	0	0	0	0	0	1	0	0	1	1	1	0	1	0	0
D066	Data	0	1	0	0	0	0	1	0	0	0	0	1	1	0	0	1	0
D067	Data	0	1	0	0	0	0	1	1	0	0	1	0	1	0	0	1	0
D068	Data	0	1	0	0	0	1	0	0	0	0	0	1	1	0	1	0	0
D069	Data	0	1	0	0	0	1	0	1	0	0	1	0	1	0	1	0	0
D070	Data	0	1	0	0	0	1	1	0	0	0	0	1	1	0	1	1	0
D071	Data	0	1	0	0	0	1	1	1	0	0	1	0	1	0	1	1	0
D072	Data	0	1	0	0	1	0	0	0	0	0	1	1	1	0	0	1	1
D073	Data	0	1	0	0	1	0	0	1	0	0	1	1	1	0	1	0	1
D074	Data	0	1	0	0	1	0	1	0	0	0	0	1	1	0	0	1	1
D075	Data	0	1	0	0	1	0	1	1	0	0	1	0	1	0	0	1	1
D076	Data	0	1	0	0	1	1	0	0	0	0	0	1	1	0	1	0	1
D077	Data	0	1	0	0	1	1	0	1	0	0	1	0	1	0	1	0	1
D078	Data	0	1	0	0	1	1	1	0	0	0	0	1	1	0	0	0	1
D079	Data	0	1	0	0	1	1	1	1	0	0	1	0	1	0	0	0	1
D080	Data	0	1	0	1	0	0	0	0	0	1	0	0	1	0	0	1	0
D081	Data	0	1	0	1	0	0	0	1	0	1	0	0	1	0	1	0	0
D082	Data	0	1	0	1	0	0	1	0	0	1	0	1	1	0	0	1	0
D083	Data	0	1	0	1	0	0	1	1	0	1	1	0	1	0	0	1	0
D084	Data	0	1	0	1	0	1	0	0	0	1	0	1	1	0	1	0	0
D085	Data	0	1	0	1	0	1	0	1	0	1	1	0	1	0	1	0	0
D086	Data	0	1	0	1	0	1	1	0	0	1	0	1	1	0	1	1	0
D087	Data	0	1	0	1	0	1	1	1	0	1	1	0	1	0	1	1	0
D088	Data	0	1	0	1	1	0	0	0	0	1	0	0	1	0	0	1	1
D089	Data	0	1	0	1	1	0	0	1	0	1	0	0	1	0	1	0	1
D090	Data	0	1	0	1	1	0	1	0	0	1	0	1	1	0	0	1	1
D091	Data	0	1	0	1	1	0	1	1	0	1	1	0	1	0	0	1	1
D092	Data	0	1	0	1	1	1	0	0	0	1	0	1	1	0	1	0	1
D093	Data	0	1	0	1	1	1	0	1	0	1	1	0	1	0	1	0	1
D094	Data	0	1	0	1	1	1	1	0	0	1	0	1	1	0	0	0	1
D095	Data	0	1	0	1	1	1	1	1	0	1	1	0	1	0	0	0	1
D096	Data	0	1	1	0	0	0	0	0	0	0	1	1	1	1	0	1	0
D097	Data	0	1	1	0	0	0	0	1	0	0	1	1	1	1	1	0	0
D098	Data	0	1	1	0	0	0	1	0	0	0	0	1	1	1	0	1	0

Name	Type	8-bit Data Byte								9-bit Symbol								
		B_1	B_2	B_3	X_1	X_2	Q_1	Q_2	Q_3	B_1	X_1	Y_1	Y_2	B_2	B_3	Y_3	Y_4	X_2
D099	Data	0	1	1	0	0	0	1	1	0	0	1	0	1	1	0	1	0
D100	Data	0	1	1	0	0	1	0	0	0	0	0	1	1	1	1	0	0
D101	Data	0	1	1	0	0	1	0	1	0	0	1	0	1	1	1	0	0
D102	Data	0	1	1	0	0	1	1	0	0	0	0	1	1	1	1	1	0
D103	Data	0	1	1	0	0	1	1	1	0	0	1	0	1	1	1	1	0
D104	Data	0	1	1	0	1	0	0	0	0	0	1	1	1	1	0	1	1
D105	Data	0	1	1	0	1	0	0	1	0	0	1	1	1	1	1	0	1
D106	Data	0	1	1	0	1	0	1	0	0	0	0	1	1	1	0	1	1
D107	Data	0	1	1	0	1	0	1	1	0	0	1	0	1	1	0	1	1
D108	Data	0	1	1	0	1	1	0	0	0	0	0	1	1	1	1	0	1
D109	Data	0	1	1	0	1	1	0	1	0	0	1	0	1	1	1	0	1
D110	Data	0	1	1	0	1	1	1	0	0	0	0	1	1	1	0	0	1
D111	Data	0	1	1	0	1	1	1	1	0	0	1	0	1	1	0	0	1
D112	Data	0	1	1	1	0	0	0	0	0	1	0	0	1	1	0	1	0
D113	Data	0	1	1	1	0	0	0	1	0	1	0	0	1	1	1	0	0
D114	Data	0	1	1	1	0	0	1	0	0	1	0	1	1	1	0	1	0
D115	Data	0	1	1	1	0	0	1	1	0	1	1	0	1	1	0	1	0
D116	Data	0	1	1	1	0	1	0	0	0	1	0	1	1	1	1	0	0
D117	Data	0	1	1	1	0	1	0	1	0	1	1	0	1	1	1	0	0
D118	Data	0	1	1	1	0	1	1	0	0	1	0	1	1	1	1	1	0
D119	Data	0	1	1	1	0	1	1	1	0	1	1	0	1	1	1	1	0
D120	Data	0	1	1	1	1	0	0	0	0	1	0	0	1	1	0	1	1
D121	Data	0	1	1	1	1	0	0	1	0	1	0	0	1	1	1	0	1
D122	Data	0	1	1	1	1	0	1	0	0	1	0	1	1	1	0	1	1
D123	Data	0	1	1	1	1	0	1	1	0	1	1	0	1	1	0	1	1
D124	Data	0	1	1	1	1	1	0	0	0	1	0	1	1	1	1	0	1
D125	Data	0	1	1	1	1	1	0	1	0	1	1	0	1	1	1	0	1
D126	Data	0	1	1	1	1	1	1	0	0	1	0	1	1	1	0	0	1
D127	Data	0	1	1	1	1	1	1	1	0	1	1	0	1	1	0	0	1
D128	Data	1	0	0	0	0	0	0	0	1	0	1	1	0	0	0	1	0
D129	Data	1	0	0	0	0	0	0	1	1	0	1	1	0	0	1	0	0
D130	Data	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	0
D131	Data	1	0	0	0	0	0	1	1	1	0	1	0	0	0	0	1	0
D132	Data	1	0	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0

Name	Type	8-bit Data Byte								9-bit Symbol								
		B_1	B_2	B_3	X_1	X_2	Q_1	Q_2	Q_3	B_1	X_1	Y_1	Y_2	B_2	B_3	Y_3	Y_4	X_2
D133	Data	1	0	0	0	0	1	0	1	1	0	1	0	0	0	1	0	0
D134	Data	1	0	0	0	0	1	1	0	1	0	0	1	0	0	1	1	0
D135	Data	1	0	0	0	0	1	1	1	1	0	1	0	0	0	1	1	0
D136	Data	1	0	0	0	1	0	0	0	1	0	1	1	0	0	0	1	1
D137	Data	1	0	0	0	1	0	0	1	1	0	1	1	0	0	1	0	1
D138	Data	1	0	0	0	1	0	1	0	1	0	0	1	0	0	0	1	1
D139	Data	1	0	0	0	1	0	1	1	1	0	1	0	0	0	0	1	1
D140	Data	1	0	0	0	1	1	0	0	1	0	0	1	0	0	1	0	1
D141	Data	1	0	0	0	1	1	0	1	1	0	1	0	0	0	1	0	1
D142	Data	1	0	0	0	1	1	1	0	1	0	0	1	0	0	0	0	1
D143	Data	1	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0	1
D144	Data	1	0	0	1	0	0	0	0	1	1	0	0	0	0	0	1	0
D145	Data	1	0	0	1	0	0	0	1	1	1	0	0	0	0	1	0	0
D146	Data	1	0	0	1	0	0	1	0	1	1	0	1	0	0	0	1	0
D147	Data	1	0	0	1	0	0	1	1	1	1	1	0	0	0	0	1	0
D148	Data	1	0	0	1	0	1	0	0	1	1	0	1	0	0	1	0	0
D149	Data	1	0	0	1	0	1	0	1	1	1	1	0	0	0	1	0	0
D150	Data	1	0	0	1	0	1	1	0	1	1	0	1	0	0	1	1	0
D151	Data	1	0	0	1	0	1	1	1	1	1	1	0	0	0	1	1	0
D152	Data	1	0	0	1	1	0	0	0	1	1	0	0	0	0	0	1	1
D153	Data	1	0	0	1	1	0	0	1	1	1	0	0	0	0	1	0	1
D154	Data	1	0	0	1	1	0	1	0	1	1	0	1	0	0	0	1	1
D155	Data	1	0	0	1	1	0	1	1	1	1	1	0	0	0	0	1	1
D156	Data	1	0	0	1	1	1	0	0	1	1	0	1	0	0	1	0	1
D157	Data	1	0	0	1	1	1	0	1	1	1	1	0	0	0	1	0	1
D158	Data	1	0	0	1	1	1	1	0	1	1	0	1	0	0	0	0	1
D159	Data	1	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	1
D160	Data	1	0	1	0	0	0	0	0	1	0	1	1	0	1	0	1	0
D161	Data	1	0	1	0	0	0	0	1	1	0	1	1	0	1	1	0	0
D162	Data	1	0	1	0	0	0	1	0	1	0	0	1	0	1	0	1	0
D163	Data	1	0	1	0	0	0	1	1	1	0	1	0	0	1	0	1	0
D164	Data	1	0	1	0	0	1	0	0	1	0	0	1	0	1	1	0	0
D165	Data	1	0	1	0	0	1	0	1	1	0	1	0	0	1	1	0	0
D166	Data	1	0	1	0	0	1	1	0	1	0	0	1	0	1	1	1	0

Name	Type	8-bit Data Byte								9-bit Symbol								
		B_1	B_2	B_3	X_1	X_2	Q_1	Q_2	Q_3	B_1	X_1	Y_1	Y_2	B_2	B_3	Y_3	Y_4	X_2
D167	Data	1	0	1	0	0	1	1	1	1	0	1	0	0	1	1	1	0
D168	Data	1	0	1	0	1	0	0	0	1	0	1	1	0	1	0	1	1
D169	Data	1	0	1	0	1	0	0	1	1	0	1	1	0	1	1	0	1
D170	Data	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	1
D171	Data	1	0	1	0	1	0	1	1	1	0	1	0	0	1	0	1	1
D172	Data	1	0	1	0	1	1	0	0	1	0	0	1	0	1	1	0	1
D173	Data	1	0	1	0	1	1	0	1	1	0	1	0	0	1	1	0	1
D174	Data	1	0	1	0	1	1	1	0	1	0	0	1	0	1	0	0	1
D175	Data	1	0	1	0	1	1	1	1	1	0	1	0	0	1	0	0	1
D176	Data	1	0	1	1	0	0	0	0	1	1	0	0	0	1	0	1	0
D177	Data	1	0	1	1	0	0	0	1	1	1	0	0	0	1	1	0	0
D178	Data	1	0	1	1	0	0	1	0	1	1	0	1	0	1	0	1	0
D179	Data	1	0	1	1	0	0	1	1	1	1	1	0	0	1	0	1	0
D180	Data	1	0	1	1	0	1	0	0	1	1	0	1	0	1	1	0	0
D181	Data	1	0	1	1	0	1	0	1	1	1	1	0	0	1	1	0	0
D182	Data	1	0	1	1	0	1	1	0	1	1	0	1	0	1	1	1	0
D183	Data	1	0	1	1	0	1	1	1	1	1	1	0	0	1	1	1	0
D184	Data	1	0	1	1	1	0	0	0	1	1	0	0	0	1	0	1	1
D185	Data	1	0	1	1	1	0	0	1	1	1	0	0	0	1	1	0	1
D186	Data	1	0	1	1	1	0	1	0	1	1	0	1	0	1	0	1	1
D187	Data	1	0	1	1	1	0	1	1	1	1	1	0	0	1	0	1	1
D188	Data	1	0	1	1	1	1	0	0	1	1	0	1	0	1	1	0	1
D189	Data	1	0	1	1	1	1	0	1	1	1	1	0	0	1	1	0	1
D190	Data	1	0	1	1	1	1	1	0	1	1	0	1	0	1	0	0	1
D191	Data	1	0	1	1	1	1	1	1	1	1	1	0	0	1	0	0	1
D192	Data	1	1	0	0	0	0	0	0	1	0	1	1	1	0	0	1	0
D193	Data	1	1	0	0	0	0	0	1	1	0	1	1	1	0	1	0	0
D194	Data	1	1	0	0	0	0	1	0	1	0	0	1	1	0	0	1	0
D195	Data	1	1	0	0	0	0	1	1	1	0	1	0	1	0	0	1	0
D196	Data	1	1	0	0	0	1	0	0	1	0	0	1	1	0	1	0	0
D197	Data	1	1	0	0	0	1	0	1	1	0	1	0	1	0	1	0	0
D198	Data	1	1	0	0	0	1	1	0	1	0	0	1	1	0	1	1	0
D199	Data	1	1	0	0	0	1	1	1	1	0	1	0	1	0	1	1	0
D200	Data	1	1	0	0	1	0	0	0	1	0	1	1	1	0	0	1	1

Name	Type	8-bit Data Byte								9-bit Symbol								
		B₁	B₂	B₃	X₁	X₂	Q₁	Q₂	Q₃	B₁	X₁	Y₁	Y₂	B₂	B₃	Y₃	Y₄	X₂
D201	Data	1	1	0	0	1	0	0	1	1	0	1	1	1	0	1	0	1
D202	Data	1	1	0	0	1	0	1	0	1	0	0	1	1	0	0	1	1
D203	Data	1	1	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1
D204	Data	1	1	0	0	1	1	0	0	1	0	0	1	1	0	1	0	1
D205	Data	1	1	0	0	1	1	0	1	1	0	1	0	1	0	1	0	1
D206	Data	1	1	0	0	1	1	1	0	1	0	0	1	1	0	0	0	1
D207	Data	1	1	0	0	1	1	1	1	1	0	1	0	1	0	0	0	1
D208	Data	1	1	0	1	0	0	0	0	1	1	0	0	1	0	0	1	0
D209	Data	1	1	0	1	0	0	0	1	1	1	0	0	1	0	1	0	0
D210	Data	1	1	0	1	0	0	1	0	1	1	0	1	1	0	0	1	0
D211	Data	1	1	0	1	0	0	1	1	1	1	1	0	1	0	0	1	0
D212	Data	1	1	0	1	0	1	0	0	1	1	0	1	1	0	1	0	0
D213	Data	1	1	0	1	0	1	0	1	1	1	1	0	1	0	1	0	0
D214	Data	1	1	0	1	0	1	1	0	1	1	0	1	1	0	1	1	0
D215	Data	1	1	0	1	0	1	1	1	1	1	1	0	1	0	1	1	0
D216	Data	1	1	0	1	1	0	0	0	1	1	0	0	1	0	0	1	1
D217	Data	1	1	0	1	1	0	0	1	1	1	0	0	1	0	1	0	1
D218	Data	1	1	0	1	1	0	1	0	1	1	0	1	1	0	0	1	1
D219	Data	1	1	0	1	1	0	1	1	1	1	1	0	1	0	0	1	1
D220	Data	1	1	0	1	1	1	0	0	1	1	0	1	1	0	1	0	1
D221	Data	1	1	0	1	1	1	0	1	1	1	1	0	1	0	1	0	1
D222	Data	1	1	0	1	1	1	1	0	1	1	0	1	1	0	0	0	1
D223	Data	1	1	0	1	1	1	1	1	1	1	1	0	1	0	0	0	1
D224	Data	1	1	1	0	0	0	0	0	1	0	1	1	1	1	0	1	0
D225	Data	1	1	1	0	0	0	0	1	1	0	1	1	1	1	1	0	0
D226	Data	1	1	1	0	0	0	1	0	1	0	0	1	1	1	0	1	0
D227	Data	1	1	1	0	0	0	1	1	1	0	1	0	1	1	0	1	0
D228	Data	1	1	1	0	0	1	0	0	1	0	0	1	1	1	1	0	0
D229	Data	1	1	1	0	0	1	0	1	1	0	1	0	1	1	1	0	0
D230	Data	1	1	1	0	0	1	1	0	1	0	0	1	1	1	1	1	0
D231	Data	1	1	1	0	0	1	1	1	1	0	1	0	1	1	1	1	0
D232	Data	1	1	1	0	1	0	0	0	1	0	1	1	1	1	0	1	1
D233	Data	1	1	1	0	1	0	0	1	1	0	1	1	1	1	1	0	1
D234	Data	1	1	1	0	1	0	1	0	1	0	0	1	1	1	0	1	1

Name	Type	8-bit Data Byte								9-bit Symbol								
		B_1	B_2	B_3	X_1	X_2	Q_1	Q_2	Q_3	B_1	X_1	Y_1	Y_2	B_2	B_3	Y_3	Y_4	X_2
D235	Data	1	1	1	0	1	0	1	1	1	0	1	0	1	1	0	1	1
D236	Data	1	1	1	0	1	1	0	0	1	0	0	1	1	1	1	0	1
D237	Data	1	1	1	0	1	1	0	1	1	0	1	0	1	1	1	0	1
D238	Data	1	1	1	0	1	1	1	0	1	0	0	1	1	1	0	0	1
D239	Data	1	1	1	0	1	1	1	1	1	0	1	0	1	1	0	0	1
D240	Data	1	1	1	1	0	0	0	0	1	1	0	0	1	1	0	1	0
D241	Data	1	1	1	1	0	0	0	1	1	1	0	0	1	1	1	0	0
D242	Data	1	1	1	1	0	0	1	0	1	1	0	1	1	1	0	1	0
D243	Data	1	1	1	1	0	0	1	1	1	1	1	0	1	1	0	1	0
D244	Data	1	1	1	1	0	1	0	0	1	1	0	1	1	1	1	0	0
D245	Data	1	1	1	1	0	1	0	1	1	1	1	0	1	1	1	0	0
D246	Data	1	1	1	1	0	1	1	0	1	1	0	1	1	1	1	1	0
D247	Data	1	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	0
D248	Data	1	1	1	1	1	0	0	0	1	1	0	0	1	1	0	1	1
D249	Data	1	1	1	1	1	0	0	1	1	1	0	0	1	1	1	0	1
D250	Data	1	1	1	1	1	0	1	0	1	1	0	1	1	1	0	1	1
D251	Data	1	1	1	1	1	0	1	1	1	1	1	0	1	1	0	1	1
D252	Data	1	1	1	1	1	1	0	0	1	1	0	1	1	1	1	0	1
D253	Data	1	1	1	1	1	1	0	1	1	1	1	0	1	1	1	0	1
D254	Data	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0	1
D255	Data	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	1
C400	Rsvd	Does not represent data								0	1	0	0	0	0	1	1	0
C401	Rsvd	Does not represent data								0	1	0	0	0	1	1	1	0
C402	Rsvd	Does not represent data								0	1	0	0	1	0	1	1	0
C403	Rsvd	Does not represent data								0	1	0	0	1	1	1	1	0
C404	Rsvd	Does not represent data								1	1	0	0	0	0	1	1	0
C405	Rsvd	Does not represent data								1	1	0	0	0	1	1	1	0
C406	Rsvd	Does not represent data								1	1	0	0	1	0	1	1	0
C407	Rsvd	Does not represent data								1	1	0	0	1	1	1	1	0
C410	Rsvd	Does not represent data								0	0	1	1	0	0	0	0	1
C411	Rsvd	Does not represent data								0	0	1	1	0	1	0	0	1
C412	Rsvd	Does not represent data								0	0	1	1	1	0	0	0	1
C413	Rsvd	Does not represent data								0	0	1	1	1	1	0	0	1
C414	Rsvd	Does not represent data								1	0	1	1	0	0	0	0	1

Name	Type	8-bit Data Byte								9-bit Symbol								
		B_1	B_2	B_3	X_1	X_2	Q_1	Q_2	Q_3	B_1	X_1	Y_1	Y_2	B_2	B_3	Y_3	Y_4	X_2
C415	Rsvd	Does not represent data								1	0	1	1	0	1	0	0	1
C416	Rsvd	Does not represent data								1	0	1	1	1	0	0	0	1
C417	Rsvd	Does not represent data								1	0	1	1	1	1	0	0	1
C600	Protocol	Does not represent data								0	1	1	1	1	1	1	0	0
C611	EoT	Does not represent data								1	0	0	0	0	0	0	1	1
C601	Idle/Sync 1	Does not represent data								0	1	1	1	1	1	1	0	1
C610	Idle/Sync 2	Does not represent data								1	0	0	0	0	0	0	1	0
C701	Reserved	Does not represent data								1	0	0	0	0	0	0	0	1
C710	Rsvd	Does not represent data								0	1	1	1	1	1	1	1	0

2027   Notes:

2028   Rsvd = Reserved

Participants

The following is a list of individuals that have contributed to the development of this document.

Mario Akers, Toshiba Corporation

Giovanni Angelo, Freescale Semiconductors, Inc.

Cedric Bertholom, STMicroelectronics N.V.

Gerrit den Besten, NXP Semiconductors

Ignatius Bezzam, Arasan Chip Systems, Inc.

Mark Braun, Motorola

Kuochin Chang, OmniVision Technologies, Inc.

Laurent Claramond, STMicroelectronics N.V.

Frederic Hasbani, STMicroelectronics N.V.

Ken Hunt, Micron Technology, Inc.

Henrik Icking, Infineon Technologies AG

Kiyoshi Kase, Freescale Semiconductors, Inc.

Deepak Khanchandani, Texas Instruments Inc.

SeungLi Kim, Samsung

Thomas Langer, Toshiba Corporation

Ricky Lau, ATI Technologies, Inc.

Ed Liu, NVIDIA Corporation

David Meltzer, Seiko Epson Corp.

Marcus Muller, Nokia Corporation

Akira Nakada, Seiko Epson Corp.

Jim Ohannes, National Semiconductor

Harold Perik, NXP Semiconductors

Tim Pontius, NXP Semiconductors

Jim Rippie, IEEE-ISTO (staff)

Jose Sarmento, Synopsys, Inc.

DC Sessions, NXP Semiconductors

Vikas Sinha, Texas Instruments Inc.

Ashraf Takla, Mixel, Inc.

Peter Vinson, Texas Instruments Inc.

Martti Voutilainen, Nokia Corporation

Kunihiko Yamagishi, Toshiba Corporation

Seiji Yamamoto, Renesas Technology Corp.

Yunfeng Zhuo, Intel Corporation

Christoph Zimmermann, Toshiba Corporation