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RESEARCH ARTICLE

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Implantation-based passivating contacts for crystalline silicon front/rear contacted solar cells

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Abstract

In this work, we develop SiO_x/poly-Si carrier-selective contacts grown by low-pressure chemical vapor deposition and boron or phosphorus doped by ion implantation. We investigate their passivation properties on symmetric structures while varying the thickness of poly-Si in a wide range (20-250 nm). Dose and energy of implantation as well as temperature and time of annealing were optimized, achieving implied open-circuit voltage well above 700 mV for electron-selective contacts regardless the poly-Si layer thickness. In case of hole-selective contacts, the passivation quality decreases by thinning the poly-Si layer. For both poly-Si doping types, forming gas annealing helps to augment the passivation quality. The optimized doped poly-Si layers are then implemented in c-Si solar cells featuring SiO_2/poly-Si contacts with different polarities on both front and rear sides in a lean manufacturing process free from transparent conductive oxide (TCO). At cell level, open-circuit voltage degrades when thinner p-type poly-Si layer is employed, while a consistent gain in short circuit current is measured when front poly-Si thickness is thinned down from 250 to 35 nm (up to +4 mA/cm^2). We circumvent this limitation by decoupling front and rear layer thickness obtaining, on one hand, reasonably high current ($J_{SC\text{-}EQE}$ = 38.2 mA/cm^2) and, on the other hand, relatively high V_{OC} of approximately 690 mV. The best TCO-free device using Ti-seeded Cu-plated front contact exhibits a fill factor of 75.2% and conversion efficiency of 19.6%.

KEYWORDS

doping, ion implantation, passivating contacts, poly-silicon, silicon solar cells

1 | INTRODUCTION

Very low surface recombination velocity at the c-Si/metal interface is required to enhance the conversion efficiency of a c-Si solar cell.[1] This task is successfully achieved by inserting a layer separating the c-Si absorber from the metal contact, which properly passivates the c-Si surface and, at the same time, selectively collects one type of carriers.[2] A first type of such *carrier-selective passivating contact* (CSPC) employs a stack of intrinsic and doped hydrogenated amorphous silicon (a-Si:H) grown on both sides of c-Si wafer, enabling open-circuit voltages (V_{OCs}) up to 750 mV.[3] Kaneka has recently reported a conversion efficiency (η) above 25% for a front-/back-contacted (FBC) c-Si solar cell[4] and a world record efficiency of 26.7% for an interdigitated back-contacted (IBC) architecture] [4,5]. However,

due to electrical degradation of a-Si:H layers for temperature above 250°C,[6] such device concept has limited compatibility with standard solar cell manufacturing processes. An alternative type of CSPC featuring higher thermal budget was proposed by Yablonovich et al[7]and is the so-called semi-insulating polycrystalline silicon (SIPOS) heterostructure as a mixture of microcrystalline silicon and silicon oxide. Several research groups [8,9] have recently further developed such device scheme consisting of an ultra-thin silicon oxide (SiO_2) (<2 nm) layer grown on the c-Si surfaces [10] coated by in situ or ex situ doped polycrystalline silicon (poly-Si) layer deposited via low-pressure/plasma-enhanced chemical vapor deposition (LP/PECVD) techniques.[11] The thin SiO_2 provides excellent chemical passivation of c-Si interface defects and also acts as a barrier that allows the collection of only majority carriers at poly-Si contact.[12] The transport principle at this junction may occur via tunneling[13,14] and/or via pin-holes present at c-Si/SiO_2 interface.[15] This passivation scheme has proved to give excellent passivation properties[16] with implied open-circuit voltage (iV_{OC}) obtained up to 730 mV and saturation current density (J_0) well below 10 fA/cm^2. Moreover, as typical process temperatures are above approximately 900°C, such devices exhibit high thermal stability and are, in principle, compatible with conventional metallization techniques.

Poly-silicon based CSPCs are successfully applied at cell level using different device architectures, such as IBC solar cells[17-22]with a remarkable efficiency over 26%[23] or bifacial[24] and FBC solar cells.[25] Similarly, promising hybrid concepts combining homo-junction with poly-Si CSPC are under research as front homo-junction and CSPC at the back side[26] with experimental η very close to 26% and selective front surface field (FSF) architecture and rear poly-Si CSPC[27] with modelled η also in the range of 26%.

Poly-Si has been applied at the front side of FBC solar cells with transparent conductive oxide (TCO)[28] or with SiN_x as anti-reflection coating[29] for tandem device applications or at the rear side of industrial n-type wafer-based FBC cells[30,31] However, placing thick poly-Si layers at the front side of a solar cell induces consistent parasitic absorption[32] estimated in the range of 1.5 mA/cm^2 each 30 nm of poly-Si.[33] Furthermore, poly-Si accounts for free carrier absorption (FCA) in the near infrared (NIR) wavelength range.[34] Therefore, into an attempt to obtain more transparent high-thermal budget CSPCs, poly-Si layer has been alloyed with oxygen[35,36] or carbon[37] and applied in FBC devices in combination with a-Si:H–based CSPC at the textured front side.[38,39] Notwithstanding the promising results at both passivation level and cell level, these alloys are still not optically optimal[35,40] presenting higher absorption coefficient than c-Si in the visible range and FCA in the NIR range, just like poly-Si.[41] Thus, to minimize these optical losses due to poly-Si layers while keeping high their passivation quality, a careful surface engineering has to be performed.

In this work, we present the optimization of n- and p-type implanted poly-Si contacts deposited by LPCVD on top of ultra-thin chemical SiO_2. We optimize both implantation dose/energy and annealing time/temperature while thinning the poly-Si layer thickness from 250 to 20 nm. The effect of the layer thickness on the passivation quality is investigated monitoring effective carriers' lifetime (τ_{eff}), implied open-circuit voltage (iV_{OC}), and saturation current density (J_0). Supported by TCAD simulations, we also evaluate the effects of doping profile in poly-Si/SiO_2/c-Si stack on passivation quality and band alignment for carrier collection. The investigated layers are tested on completed devices in a rear emitter configuration with a textured-front and a flat-rear side in a lean and TCO-free manufacturing process. We discuss the relation among short-circuit current density (J_{SC}), open-circuit voltage (V_{OC}), and fill factor (FF) for different poly-Si thicknesses.

2 | EXPERIMENTAL DETAILS

Double side polished, <100>-oriented, 280-μm-thick, n-type c-Si float-zone (FZ) wafers with a resistivity of 2.5 Ω·cm (Doping concentration of $1.8{\cdot}10^{15}$ cm^{-3}) are used as starting material to prepare both symmetric lifetime samples and solar cells. Firstly, the substrates are cleaned in 99% and 69.5% nitric acid (HNO_3) both for 10 minutes in order to remove organic and metallic particles, respectively. Some wafers are chemically textured on both sides in an alkaline solution containing H_2O, TMAH, and Alkatex to obtain random pyramids. Before processing, we remove the native oxide via a short HF dip, and afterwards, we wet-chemically oxidize the c-Si surfaces using a nitric acid solution to grow an approximately 1.5-nm-thick SiO_2 buffer layer as described in Yang et al.[17] The samples are then coated with intrinsic amorphous silicon layer deposited by a Tempress LPCVD reactor at a temperature of 580°C, pressure of 150 mTorr, and SiH_4 flow of 45 sccm. The deposition time is adapted to obtain layers with thickness of 250, 75, 35, and 20 nm. Ex situ doping of the poly-Si layers is performed via ion implantation using a Varian EHP500 implanter. Phosphorous (P) and boron (B) are implanted, selecting an energy of 10 keV and 5 keV, respectively, with variable dose from $5{\cdot}10^{15}$ to $1.2{\cdot}10^{16}$ ions/cm^2. Figure 1A,B sketches the symmetric samples fabricated in this work.

Afterwards, the samples are annealed in a tube furnace to activate and diffuse the implanted dopants within the a-Si lattice and, concurrently, to obtain poly-Si layer. Annealing temperature for samples in Figure 1A,B is either 950°C or 850°C, and annealing time is variable between 5 and 90 minutes, depending on the thickness of the poly-Si layer. Eventually, a forming gas annealing (FGA) at 400°C for 2 hours (10% H_2 in N_2) is performed to enhance chemical passivation at c-Si/SiO_2 interface.[42] Quasi-steady-state photoconductance lifetime measurements (QSSPC)[43] are performed using a Sinton Instruments WCT-120 on the symmetric samples in Figure 1A,B to assess the surface passivation quality of the fabricated structures. Effective carriers' lifetime (τ_{eff}) is evaluated at low injection level ($\Delta n = 10^{15}$ cm^{-3}); implied open-circuit voltage (iV_{OC}) and recombination current density (J_0) are extracted from the measured curves at high injection level ($\Delta n = 10^{16}$ cm^{-3}). Furthermore, electrocapacitance voltage (ECV) technique is employed on the same samples to investigate the active doping concentration profile from the doped layers into the c-Si substrate.

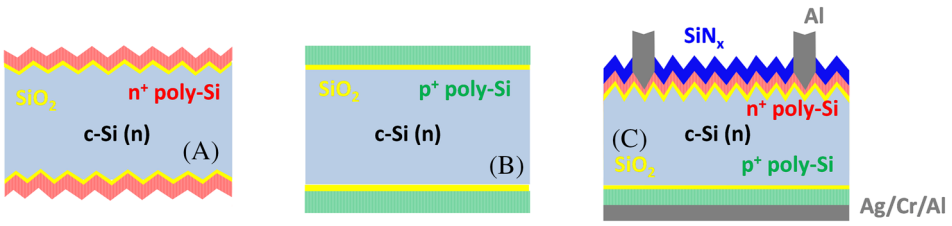

FIGURE 1 Symmetric samples with (A) SiO_2/n-type poly-Si on textured c-Si wafer, (B) SiO_2/p-type poly-Si on flat c-Si wafer, and (C) *poly-poly* solar cell sketch with variable front/rear poly-Si thicknesses between 250 and 20 nm [Colour figure can be viewed at wileyonlinelibrary.com]

Solar cells are fabricated by combining the layer stacks optimized in a *poly-poly* configuration (see Figure 1C). The process is shown in Figure 2. Because our p-type poly-Si layer for textured surface is still under development, we locate the hole contact at rear side on a flat interface. The choice of rear-emitter architecture additionally improves the transport of minority carriers inside c-Si bulk as discussed by Larionova et al[44] and Bivour et al[45] for the case of silicon heterojunction solar cells. Only the front side of the c-Si wafer is textured (see Figure 2A), by covering the other side with 100-nm-thick SiN_x protective layer. After SiN_x removal and cleaning, SiO_2 and doped poly-Si stack are deposited as described above. In particular, we fabricate devices with 250, 75, and 35 nm of poly-Si layer on both the front and the rear side.

After tunneling SiO_2 formation (see Figure 2B), the LPCVD intrinsic amorphous silicon layers are implanted with P or B and co-annealed at the optimal temperature according to the passivation study (see Figure 2C). To minimize reflection losses, a 75-nm-thick SiN_x layer is deposited by PECVD on the textured front side (see Figure 2D) and finally, the cells are completed with metal contacts (see Figure 2E). At rear side, a stack of Ag/Cr/Al (200 nm/30 nm/2 μm) is evaporated through a hard mask to define the cell area of 2.8 cm × 2.8 cm (7.84 cm^2), while, at the front side, a 2-μm-thick e-beam evaporated Al metal grid (5% metal coverage) is structured via photolithography, etching of SiN_x ARC, evaporation, and lift-off.[27] Additionally, the front grid of some solar cells is Cu-plated by means of a mask-less process (plating current density of 576 mA/cm^2 for 1500 s) using evaporated titanium as seed layer.[46] For solar cells with decoupled front/rear poly-Si thicknesses, the fabrication process consists in repeating twice the SiO_2/poly-Si deposition using a SiN_x layer to protect one of the wafer's surface and a poly-Si etching in between. Poly-Si layer is etched in a mixture of HF/HNO_3 and H_2O. We keep the rear side thickness at 250 nm while the front layer is varied from 250 nm down to 20 nm. The cell precursors are then processed as described above for implantation and annealing performed at optimized temperature/time depending on the poly-Si thickness. Forming gas annealing at 400°C for 2 hours is eventually deployed to increase chemical passivation. The solar cells are characterized using a calibrated, class AAA, Wacom WXS-156S solar simulator to extract the following cell parameters: V_{oc}, FF, J_{sc}, and η. External quantum efficiency (EQE) is measured by an in-house built setup, and a calibrated mono-silicon diode with known spectral response was used as a reference. Sinton SunsV_{OC} setup allows to measure pseudo parameters, such as pseudo-FF (pFF), which excludes the series resistance contribution.

Accurate opto-electrical simulations of poly-poly solar cells are performed using a modelling framework based on TCAD Sentaurus,[47-51] combining thin film optics and opto-electrical properties, such as free carrier absorption. The simulated structure is reported in Figure 1C using experimentally extracted wavelength-dependent refractive index of poly-Si.[52] From each simulated absorption profile, equivalent photocurrent densities are calculated. We assume here that all the light absorbed in the front or rear layers (except the c-Si absorber) is parasitically absorbed and contributes therefore to current losses.

3 | RESULTS AND DISCUSSION

3.1 | c-Si surface passivation by poly-Si selective contacts

From Raman spectrum reported in Figure 3, it is clear that before high temperature annealing at 950°C, silicon is deposited in an amorphous state (black curve). After high temperature annealing (red curve), the crystallinity fraction increases up to 90%.

Table 1 summarizes the implantation parameters tested for the SiO_2/n-type poly-Si stack on textured substrates with the symmetric

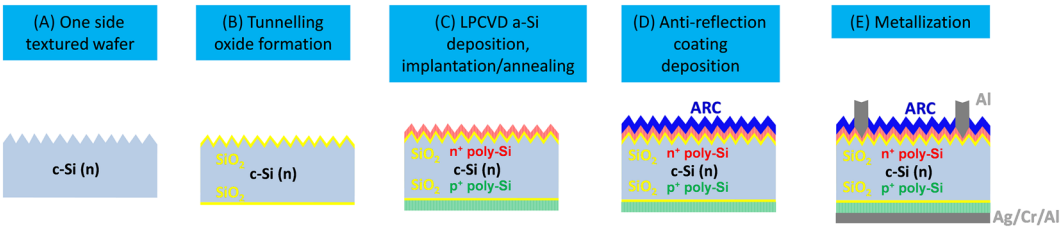

FIGURE 2 Steps for fabrication of poly-poly solar cell; (A) starting material one sided textured wafer, (B) tunneling oxide formation; (c) LPCVD a-Si deposition, implantation, and annealing, (D) anti-reflection coating deposition, and (E) front/rear metallization [Colour figure can be viewed at wileyonlinelibrary.com]

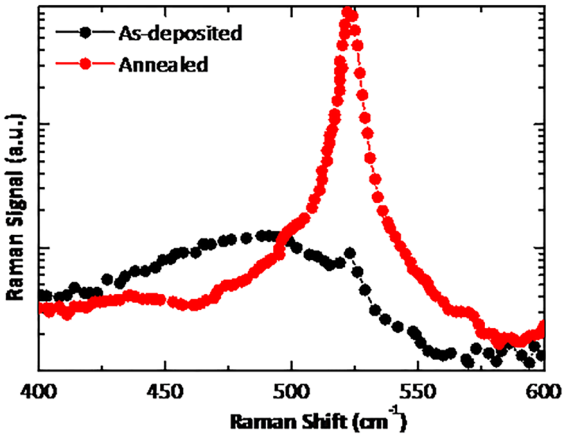

FIGURE 3 Raman spectra of as-deposited LPCVD a-Si and annealed poly-Si at 950°C [Colour figure can be viewed at wileyonlinelibrary.com]

structure reported in Figure 1A. The poly-Si layer thickness is kept constant at 250 nm for the three samples fabricated while the P implantation is performed at an energy of 10 keV. Sample *n1* receives a dose of $7.5{\cdot}10^{15}$ ions/cm^2, while for samples *n2* and *n3*, implantation dose is 10^{16} ions/cm^2. All the samples undergo the same annealing process for 5 minutes at temperature of 950°C, and the FGA is tested only for sample *n3*. Surface passivation quality of the fabricated samples is reported in the same Table 1. Sample *n1*, implanted at lower dose, exhibits relatively low performance with τ_{eff} = 0.8 ms, J_0 = 72 fA/cm^2, and iV_{OC} = 664 mV. When implantation dose is increased up to $1{\cdot}10^{16}$ ions/cm^2 (sample *n2*), lifetime increases up to 1.8 milliseconds, and J_0 decreases to 39 fA/cm^2 with improved iV_{OC} up to 688 mV. The better passivation properties observed for increased implantation dose can be explained by the higher doping concentration into poly-Si layer that enhances carrier selectivity inducing a stronger electrical field across the junction.[53] A similar trend has been observed in literature by other researchers.[14,54,55] Finally, we test the effect of FGA on the investigated stack (sample *n3*), measuring a significant improvement in the passivation properties. In particular, we measured τ_{eff} = 4.6 ms, J_0 = 14.5 fA/cm^2, and iV_{OC} > 700 mV. Sample *n3* benefits from the FGA treatment owing to the diffusion of H^+ atoms into the stack, enhancing chemical passivation at the c-Si/SiO_2 interface.[42,56] Similar results about FGA have been reported in Peibst et al,[57] although in our case, the implantation dose is higher than typical literature values[58,59] with similar annealing conditions.

Next, we investigate the effect of poly-Si layer thickness on passivation. Figure 4 depicts the phosphorous concentration profile across the SiO_2/poly-Si structure for the case of 75-nm-thick poly-Si implanted with fixed dose of 10^{16} ions/cm^2 and annealed at 950°C for 5 minutes and 850°C for 90 minutes, respectively. The sample annealed at 950°C (green curve in Figure 4) confines 10^{20} P atoms into poly-Si layer, and a similar amount is diffused into c-Si bulk. For the case of 850°C (red curve in Figure 4), the junction depth is shallower with approximately 10^{20} P atoms confined into the poly-Si layer. The doping profile decreases with a sharp tail into the c-Si with 10^{18} atoms near the c-Si/SiO_2 interface. This doping diffusion into c-Si bulk facilitates carrier transport across the junction[60,61] Consequently, different doping profiles lead to a different passivation properties thanks to the higher Auger recombination contribution that is estimated to be 40% higher in case of 950°C annealed sample. We measure τ_{eff} = 0.8 ms and τ_{eff} = 2.2 ms for the sample annealed at 950°C and 850°C, respectively. The difference in passivation performance is due to different distribution of dopants inside crystalline silicon at the interface with tunneling oxide. Indeed, the electrical field across the junction depends on spatial variation of potential energy by incorporating dopant species. In case of constant doping before/after the interface with tunneling oxide, the electrical field is negligible, explaining the lack of field-effect passivation in case of sample annealed 950°C (see Figure 4).

After the optimal temperature is found, we optimize the doping level for the 75-nm-thick n-type poly-Si by sweeping implantation

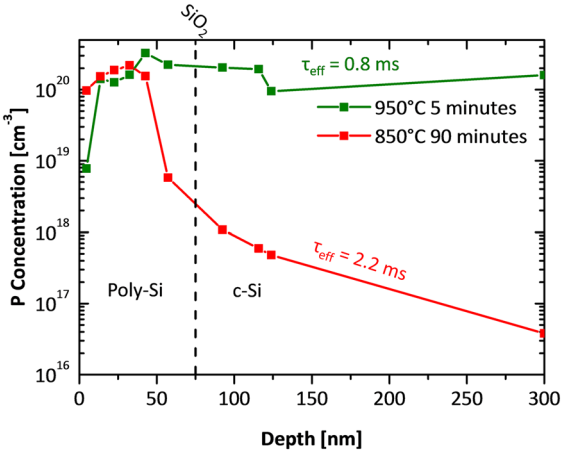

FIGURE 4 ECV measurement of phosphorous doping concentration profile as function of the depth in 75-nm-thick n-type poly-Si contact implanted with a dose of 10^{16} cm^{-2} and energy of 10 keV and annealed at different temperatures and times. Reported τ_{eff} indicated for each sample is probed at $\Delta n = 10^{15}$ cm^{-3} [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 1 Lifetime measurements on symmetric samples based on textured wafers and passivated by SiO_2/poly-Si (250-nm-thick, n-type) as shown in Figure 1A

			Annealing		FGA				R_{SH}, Ω/sq
Sample	Energy, keV	Dose, ions/cm^2	Temp, °C	Time, min		τ_{eff} @ 10^{15} cm^{-3}, ms	J_0, fA/cm^2	iV_{oc}, mV	
n1	10	$7.5{\cdot}10^{15}$	950	5	No	0.8	72.0	664	150
n2	10	$1.0{\cdot}10^{16}$	950	5	No	1.8	39.0	688	135
n3	10	$1.0{\cdot}10^{16}$	950	5	Yes	4.6	14.5	709	130

dose in the range from $0.5{\cdot}10^{16}$ ions/cm^2 to $1.2{\cdot}10^{16}$ ions/cm^2. Annealing temperature is kept at 850°C for 90 minutes. The corresponding carrier lifetime curves versus minority carrier density are reported in Figure 5. The layer implanted with a dose of $5{\cdot}10^{15}$ ions/cm^2 exhibited the lowest τ_{eff} (0.5 ms), with a poor behavior at low injection level. By increasing the dose up to $7.5{\cdot}10^{15}$ and $1{\cdot}10^{16}$ ions/cm^2, the lifetime curves shift up in the entire injection level with a τ_{eff} ~ 2 ms. Further increasing the dose up to $1.2{\cdot}10^{16}$ ions/cm^2, τ_{eff} degrades down to 0.5 milliseconds with a severe effect on the surface passivation (iV_{oc} = 663 mV). In these cases, sheet resistance is varying from 310 Ω/sq (D = $5{\cdot}10^{15}$ cm^2) to 200 Ω/sq (D = 10^{16} cm^2). As for the case of 250-nm-thick poly-Si, implantation dose lower than 10^{16} ions/cm^2 does not induce such strong electric field across the junction to increase carrier-selectivity. On the other hand, a dose higher than 10^{16} ions/cm^2 induces lower lifetime. This is because the resulting junction is Auger-limited with a J_0 = 95 fA/cm^2, according to a qualitative simulation run by EDNA 2.[62] The optimum for 75-nm-thick poly-Si layer is found indeed for a dose of $1{\cdot}10^{16}$ ions/cm^2. In this case, J_0 = 14 fA/cm^2 and iV_{OC} = 703 mV indicate a trade-off between optimal surface vs Auger recombination mechanisms.

Figure 6A shows optimal doping profile for 250-, 75-, and 35-nm-thick poly-Si layers and their corresponding τ_{eff} and J_0. For the 35-nm-thick poly-Si layer, we obtain a sharp doping profile for an annealing performed at 850°C for 45 minutes. We obtain a not fully-optimized 75-nm-thick layer because its doping profile (shown in Figure 6A), albeit decaying as steeply as the other two cases into c-Si bulk, does not keep high concentration as close as possible to the poly-Si/SiO_2 interface. Therefore, a less effective field-effect passivation is in place for this sample. Consequently, both 250- and 35-nm-thick poly-Si layers exhibit τ_{eff} above 4.5 milliseconds, while the 75-nm-thick one is limited at 2.3 milliseconds. Sheet resistance of 35-nm-thick poly-Si layer is 270 Ω/sq. The three samples depicted in Figure 6A have approximately 10^{20} phosphorous atoms/cm^3 into the poly-Si layer, while the doping tail in the c-Si bulk becomes not significant after about 100 nm. Figure 6B summarizes these τ_{eff} results

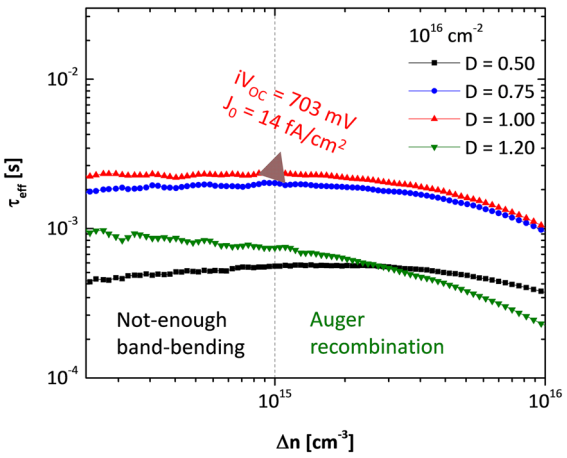

FIGURE 5 QSSPC lifetime measurements of 75-nm-thick n-type poly-Si symmetric samples on textured wafer sweeping implantation dose (D) from $0.5{\cdot}10^{16}$ to $1.2{\cdot}10^{16}$ ions/cm^2 [Colour figure can be viewed at wileyonlinelibrary.com]

while measuring a fairly constant J_0 = 14.5 fA/cm^2, independently from the poly-Si thickness. This means that the chemical passivation is excellent in all the three samples. A similar trend has been observed in literature.[33,63]

A similar study is performed on B-implanted poly-Si CSPC on flat substrate. Table 2 shows τ_{eff}, J_0, and iV_{OC} in as-annealed condition and after FGA treatment for the case of 250-nm-thick poly-Si layer. The samples are implanted with 5 keV as ion energy and a dose of $5{\cdot}10^{15}$ ions/cm^2. Annealing is at temperature of 950°C and time is 5 minutes.

For sample *p1*, after annealing for dopants activation and crystallization, we measure τ_{eff} = 3.8 ms, J_0 = 19 fA/cm^2, and iV_{OC} = 704 mV. For sample *p2*, which subsequently received also FGA, it is evident that hydrogenation treatment via FGA is capable of increasing lifetime by 25% relative with respect to *p1* with τ_{eff} = 5.2 ms and J_0 = 12.5 fA/cm^2. Furthermore, iV_{OC} increases by more than 10 mV, up to 716 mV. As in case of the electron-selective contact, we investigate the effect of thinning the p-type poly-Si layer on passivation properties. When the p-type poly-Si layer is 75 nm thick, an annealing at 950°C is not suitable to perfectly confine the boron doping into poly-Si layer. For this reason, annealing temperature is scaled down to 850°C and time is increased to 90 minutes. As for n-type poly-Si layers, a series of different implantation doses from $5{\cdot}10^{15}$ to 10^{16} ions/cm^2 is performed.

Figure 7 shows QSSPC lifetime curves of symmetric samples passivated by SiO_2/p-type poly-Si stack with different implantation doses and ion energy = 5 keV. By increasing implantation dose, the curves shift towards higher carrier lifetimes. The highest passivation quality is measured for 10^{16} ions/cm^2 with τ_{eff} = 2.3 ms, J_0 = 23 fA/cm^2, and iV_{OC} = 691 mV. In this case, sheet resistance is 285 Ω/sq. For lower doses, as the doping level into poly-Si is not optimal, lifetime is limited at approximately 1 millisecond.

Figure 8A shows doping profiles of 250-, 75-, and 35-nm-thick p-type poly-Si samples. In the case of 250-nm-thick layer, 10^{20} B atoms/cm^3 are confined well into the poly-Si layer and its doping tail in c-Si bulk, ensuring τ_{eff} > 5 ms. For the 75-nm-thick sample (see Figure 8A, red line), the doping level into poly-Si is around approximately $3{\cdot}10^{20}$ B atoms/cm^3, and it decreases in c-Si bulk such that after 100 nm in c-Si bulk, there are 10^{18} B atoms/cm^3, giving a weaker field-effect passivation (τ_{eff} = 2.3 ms) than the case of 250-nm-thick poly-Si. When 35-nm-thick poly-Si is deposited, the B-doping concentration at c-Si/SiO_2/poly-Si junction is on the order of 10^{20} cm^{-3} on both sides of the SiO_2 tunneling layer, causing almost no field-effect passivation, and therefore, lifetime is 0.5 milliseconds. In this case, sheet resistance is 263 Ω/sq. In this case, also Auger recombination plays a role in the recombination processes. Since boron is a light atom (atomic mass unit of 11), its diffusivity into silicon is greater than that of phosphorous[64]; therefore, having already limited the annealing temperature to 850°C to prevent unwanted diffusion of boron into the c-Si bulk, the annealing time could be reduced further. On the other hand, boron typically needs higher activation temperatures than phosphorous,[64] thus narrowing the optimization window of B-implanted poly-Si. In the two thicker layers, junction

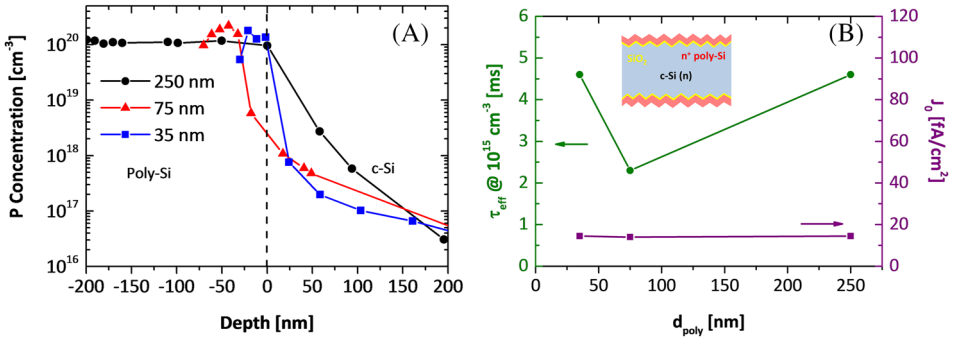

FIGURE 6 (A) ECV measurement of phosphorous doping concentration profile as function of the depth in 250-, 75-, and 35-nm-thick n-type poly-Si; (B) τ_{eff} and J_0 versus poly-Si thickness [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 2 Implantation and annealing parameters for symmetric samples on polished wafers with 250-nm-thick B-doped poly-Si

			Annealing		FGA				
Sample	Energy, keV	Dose, ions/cm^2	Temp, °C	Time, min		τ_{eff} @ 10^{15} cm^{-3}, ms	J_0, fA/cm^2	iV_{oc}, mV	R_{SH}, Ω/sq
p1	5	$5{\cdot}10^{15}$	950	5	No	3.8	19.0	704	134
p2	5	$5{\cdot}10^{15}$	950	5	Yes	5.2	12.5	716	130

Note. Measured passivation quality parameters: τ_{eff}, J_0, and iV_{OC}.

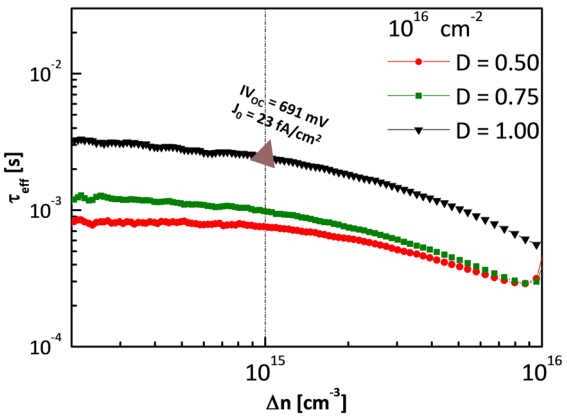

FIGURE 7 QSSPC lifetime curves of 75-nm-thick p-type poly-Si on flat wafer sweeping implantation dose (D) for a fixed ion energy at 5 keV. The samples are annealed at 850°C for 90 minutes [Colour figure can be viewed at wileyonlinelibrary.com]

depths are optimized such that doping unbalance at the junction is high enough to induce strong electrical field, while in the 35-nm-thick case, diffusion of dopants is rather high causing weak electrical field at the junction and also high Auger recombination. Furthermore, we observe that the optimized implantation dose for thinner poly-Si layer is higher than the one used for 250-nm-thick layer. This might be caused by a more complicated incorporation of B dopants into thinner poly-Si layers. A possible way to minimize junction depth is to use lower implantation energy,[65] which is unfortunately not possible in our setup. Figure 8B summarizes all the results obtained so far about p-type poly-Si passivating contact for different thicknesses. It shows that τ_{eff} increases when poly-Si thickness increases with an opposite trend for J_0. For the 35-nm-thick B-doped poly-Si layer, low lifetime of 0.5 milliseconds, iV_{OC} of 655 mV, and J_0 ~ 100 fA/cm^2 are obtained, indicating overall that also chemical passivation is affected, most likely by inactive clusters of B atoms acting as recombination centers. For both hole-selective and electron-selective contacts, annealing temperature is higher when the poly-Si thickness is in the range of 250 nm. This is also partially confirmed in Yan et al[66],where a BBr_3 diffusion instead of ion implantation is used as ex situ doping technique. Finally, also for our hole-selective poly-Si contacts, implantation doses are much higher than the state of the art.[67],We believe that this might be due to different density of the poly-Si layers.

For a deeper understanding of our results, we simulated, by means of our TCAD Sentaurus modelling platform,[51] the energy band diagrams of both n-type and p-type poly-Si CSPCs based on the measured doping concentration profiles shown in Figures 6A and 8A of

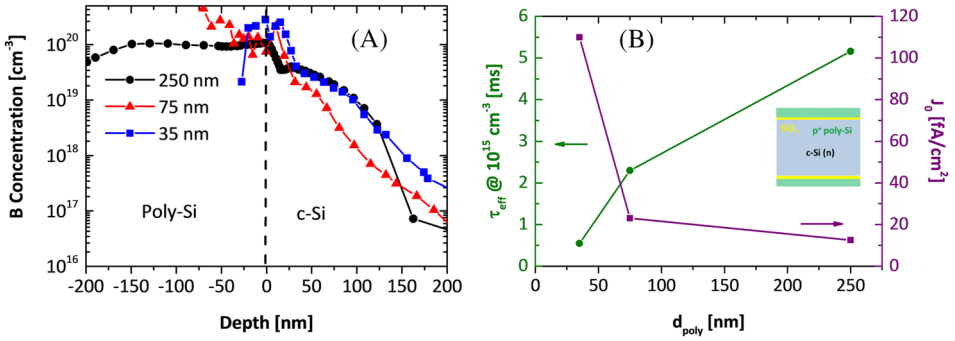

FIGURE 8 (A) ECV measurement of boron doping concentration in 250-, 75-, and 35-nm-thick B-doped poly-Si and (B) corresponding τ_{eff} and J_0 measured on symmetric samples on double side polished wafer as function of poly-Si thickness [Colour figure can be viewed at wileyonlinelibrary.com]

n-type and p-type poly-Si contacts, respectively. Figure 9A reports in the top panel the measured phosphorous doping concentration profiles and in the bottom panel the corresponding conduction energy level together with the Fermi energy level in equilibrium of n-type poly-Si/SiO_2/c-Si junction simulated for different poly-Si thicknesses. For n-type contact, a strong band bending is observed for the 250- and 35-nm-thick samples, revealing a stronger field-effect passivation than that related to the 75-nm-thick sample. This is compatible with the measured lifetime achieved by n-type poly-Si (see Figure 6B). In particular, strong electrical field across the junction is induced by high electron density at the interface. This has the effect to place the conduction band energy level below the Fermi level in c-Si. This mechanism is the effect of the optimized doping profile across the junction. This effect, together with high doping level at poly-Si side, leads to a band alignment which is crucial for transport through tunneling oxide.[51] In the case of 75 nm (red curves in Figure 8A), the conduction band is above the Fermi level. This leads a relatively weak electrical field across the junction and less efficient tunneling. It is important to highlight that, in c-Si bulk, high doping profile potentially boosts transport through tunneling oxide, but also increases Auger recombination. Therefore, the doping tail in c-Si bulk should be kept such sharp to obtain the effect of higher electron accumulation only at c-Si/SiO_2 interface.

A similar analysis has been carried out regarding the p-type poly-Si contact. Figure 9B shows in the top panel the measured doping profile and in the bottom panel the corresponding valence energy level together with the Fermi energy level in equilibrium of p-type poly-Si/SiO_2/c-Si junction simulated for different poly-Si thicknesses. In this case, the doping profiles of 250- and 75-nm-thick cases induce a strong valence band bending and, therefore, a strong electrical field. Similarly, the valence bands of poly-Si and c-Si exhibit an alignment above the Fermi energy level, for which tunneling is expected to be efficient for all the samples. However, the depth of the doping profile tail inside c-Si limits the passivation as Auger recombination is higher for deeper doping profiles. Accordingly, 250-, 75-, and 35-nm-thick poly-Si samples exhibit doping profiles as deep as 100 nm, 250 nm, and 300 nm inside c-Si, respectively. The passivation quality observed in Figure 8B highlights the effect of Auger recombination on the passivation in terms of τ_{eff} and J_0. Therefore, in our experimental framework, the 250-nm-thick poly-Si sample exhibits the best potential for p-type poly-Si contact in solar cells.

We can conclude that an ideal doping profile should have high doping concentration at c-Si/SiO_2 interface to enhance collection of carriers, but at the same time, it should have a relatively shallow doping tail such that Auger recombination is minimized. Accordingly, reduced layer thickness in both electron and hole-selective contact requires a careful tuning of implantation dose, annealing temperature and time to confine the dopants atoms into poly-Si layer, leaving a sufficiently high doping tail that results in better passivation quality.

3.2 | Solar cells

The optimized carrier-selective contacts discussed in Section 3.1 are integrated into *poly-poly* solar cells. We combine the n-type and p-type poly-Si layers with different thicknesses at the front and rear side of the device, respectively.

Table 3 summarizes the different *poly-poly* solar cells fabricated and the external parameters of the devices. *SC1* with 250-nm-thick poly-Si on both front and rear sides exhibits V_{OC} = 684 mV, J_{SC} = 32 mA/cm^2, and FF = 68.7%. As this cell has not received the FGA treatment, it appears to be limited by the n-type poly-Si. In fact, its V_{OC} is in line with the iV_{OC}s values shown in Table 1 for sample *n2* ($iV_{OCn,poly,250nm}$ = 688 mV before FGA), which was used for this device. FF lies below 70%, most likely because lateral transport is mostly supported by the large doping tail in c-Si at the front electron contact. Also, the lack of a TCO as transport layer plays an important role in FF values. In a similar solar cell architecture[29] with a 200-nm-thick poly-Si, V_{OC} was found 10 mV lower than ours and FF 4% absolute higher than ours. Those parameters were obtained by screen-printed front contacts that introduce higher recombination but also ensure lower contact resistivity than our PVD-evaporated contacts. In our case, contact resistivity of poly-Si layer with Al contacts, measured via transfer length method (TLM), is 0.1 mΩ·cm^2. This relatively low value does not have impact on series resistance of our devices. By decreasing front and rear poly-Si thicknesses to 75 nm (*SC2* in Table 2), V_{OC} decreases to 663 mV, but FF goes up to 72.8%. This result is also obtained without FGA treatment. When 35-nm-thick poly-Si is employed (*SC3* in Table 2), we measure an improved V_{OC} up to 675 mV with a gain of 12 mV as compared with *SC2*. This improvement in V_{OC} is due to the FGA treatment, as demonstrated in the case of passivation tests of both electron- and hole-selective contacts.

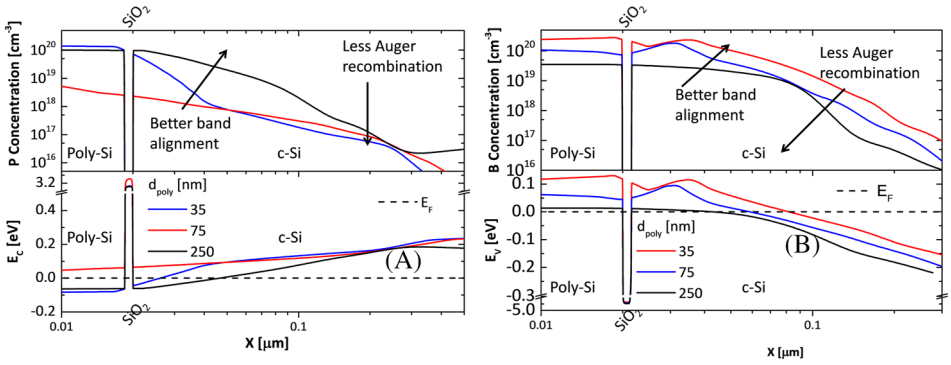

FIGURE 9 (A) Top panel: measured doping profile (in log-log scale) in the stack n-type poly-Si/SiO_2/c-Si; bottom panel: corresponding band diagram for different poly-Si thicknesses; (B) top panel: measured doping profile (in log-log scale) in the stack p-type poly-Si/SiO_2/c-Si; bottom panel: corresponding band diagram for different poly-Si thicknesses [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 3 *Poly-poly* solar cells results with different combination of front/rear poly-Si thickness and eventual FGA

Solar cell	FGA	$d_{front/rear}$ [nm]	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]	η [%]	η_{active} [%]	pFF [%]
SC1	No	250/250	684	32.0	68.7	15.0	15.8	82.9
SC2	No	75/75	663	36.0	72.8	17.3	18.2	82.0
SC3	Yes	35/35	675	36.5	71.0	17.5	18.4	82.5
SC4	Yes	35/250	701	35.1	72.8	17.9	18.8	82.3
SC5	Yes	20/250	689	36.5	73.0	18.4	19.3	82.1
SC6[a]	Yes	20/250	682	36.3	75.2	18.7	19.6	84.0

Note. Reported external parameters are for Al-based front contacted solar cells; The cell sketch is reported in Figure 1C.
[a]Ti-seeded Cu-plated front contacts.

Accordingly, we highlight that FGA treatment is critical to improve both passivation and transport properties of this type of selective contacts. In this case, FF is reduced to 71%. We speculate that this FF reduction is due to a different lateral transport through the front contact owing to different doping profile in poly-Si layers. Short circuit current density is very poor for *SC1* (32 mA/cm^2). We measure an improvement of approximately 4 mA/cm^2 when 75-nm-thick poly-Si layers are employed. Further improvement up to 36.5 mA/cm^2 is observed in case of *SC3*. When front and rear thicknesses are decoupled to 35 nm at the front and 250 nm at the back (*SC4*), V_{OC} is 701 mV (the gain is 17 mV compared to *SC1*), short current density is 35.1 mA/cm^2, and FF is again at 72.8 %, as in *SC2*. The lower current might be due to not optimized texturing and anti-reflection coating thickness. By further thinning the front poly-Si to approximately 20 nm and keeping the rear side poly-Si thickness to 250 nm (*SC5*), V_{OC} slightly decreases to 689 mV with respect to *SC4*, but an increase in J_{SC} is noted up to 36.5 mA/cm^2 and FF is equal to 73% (η_{active} = 19.3%). Finally, the same solar cell as *SC5* has been fabricated with Ti-seeded Cu-plated front contacts (*SC6*), resulting in FF = 75.2% (approximately 2% absolute higher than *SC5*) and V_{OC} = 682 mV (7 mV lower compared with *SC5*). J_{SC} is 36.3 mA/cm^2, which is slightly lower than *SC5*. The overall η_{active} is 19.6%. The gain in FF is due to more conductive Ti/Cu stack respect to the previously used 2-μm-thick e-beam evaporated Al.[68] The reduction in V_{OC} of 7 mV might be explained by the so-called background-plating[69] that consists in Cu growing outside the designed fingers areas and acting as deep impurity in Si.[70]

Figure 10 reports the EQE spectra of *SC1*, *SC2*, and *SC3*, clearly showing the losses in the short-wavelength part of the spectrum due to parasitic absorption in the front poly-Si layer. *SC2* and *SC3* devices show higher current collection than *SC1*, because of the reduced parasitic absorption in the front poly-Si layer. In this respect, there is a substantial improvement in collection from 380 to 800 nm. Furthermore, maximum EQE reached is approximately 90% in both *SC1* and *SC2*. This can be explained by electrical recombination occurring at the front and rear Si surfaces since no FGA treatment is performed. In case of *SC3*, instead, we observe an improved carrier collection across the whole spectral range up to approximately 97%. This is not only due to thinner poly-Si layers but also owing to the FGA treatment. Regardless the poly-Si layers thickness, these layers suffer from

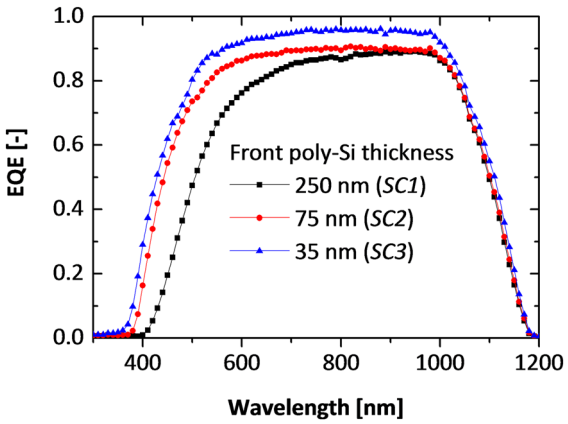

FIGURE 10 External quantum efficiency of *SC1*, *SC2*, and *SC3* (see Table 1) [Colour figure can be viewed at wileyonlinelibrary.com]

parasitic absorption in the long wavelength range between 1000 nm and 1200 nm,[33,34] which, together with the additional parasitic absorption due to the rear metal contact, contributes to current losses. From these experiments, we can demonstrate that the front poly-Si layer should primarily be kept as thin as possible in order to limit parasitic absorption.

We performed opto-electrical simulations of the abovementioned *SC1*, *SC2*, and *SC3* devices with TCAD Sentaurus[47,51] using experimentally-extracted optical properties of poly-Si layers.[52] Figure 11A shows the simulated absorptance in front and rear poly-Si layers. The device with 250-nm-thick poly-Si layers shows a consistent absorption of the incoming light that peaks up to 0.8 in the short-wavelength range and decays to a negligible value at around 800 nm. When the thickness of poly-Si layers is reduced to 75 nm and 35 nm, the absorption strongly decreases in the ultraviolet and visible parts of the spectrum but still peaks to values close to 0.6. For the rear poly-Si layer, we observe a weak dependence of absorption against poly-Si thickness. It is noteworthy to mention that our simulations take into consideration both front texturing[48] and free carrier absorption into poly-Si given by high doping. By integrating these absorption profiles with the AM1.5 photon flux,[71] we obtain the equivalent photocurrent density losses (J_L) for different *poly-poly* solar cell configurations. The values are shown in Figure 11B, where we observe a strong dependence of front poly-Si thickness on photocurrent density losses (J_L ~ 8.5 mA/cm^2 for *SC1* configuration). If the front poly-Si layer is

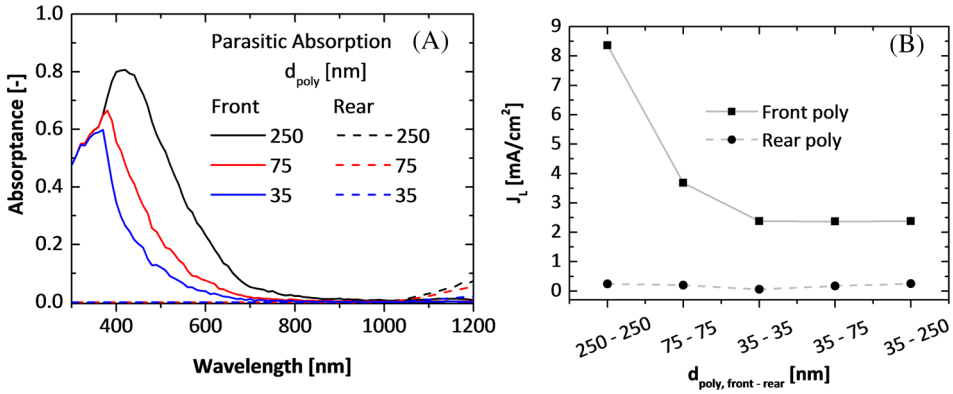

FIGURE 11 (A) Simulated absorptance in front poly-Si (continuous line) and rear poly-Si (dashed line) layers for different thicknesses as used in *SC1*, *SC2*, and *SC3*; (B) simulated equivalent photocurrent density losses (J_L) related to different front and rear poly-Si layer thicknesses [Colour figure can be viewed at wileyonlinelibrary.com]

kept at 35 nm, J_L decreases to approximately 2.5 mA/cm^2. Regarding absorption in the rear poly-Si, we obtain J_L < 1 mA/cm^2 with a weak dependency on the backside layer thickness. Therefore, in order to reach, on one hand, relatively high short circuit current density and, on the other hand, high V_{OC} (see Figure 8), it is necessary to decouple the front thickness from the rear one. Focusing on the rear side only, Figure 12 describes the J_L of rear poly-Si and rear metal in the abovementioned cell configurations. Losses due to metal absorption are limited between 0.4 and 0.5 mA/cm^2, while the losses into rear poly-Si account for less than 0.25 mA/cm^2. By adding those two losses, the total rear losses differ by only about 0.15 mA/cm^2 between the configurations 35 nm/35 nm and 35 nm/250 nm. Therefore, we justify the decoupling of front/rear poly-Si thicknesses.

Based on these results, we performed a TCAD simulation of *SC1*, *SC2*, *SC3*, and *SC4* solar cells to predict their ultimate efficiencies. The purpose of these simulations is to have an idea of the pitfalls of our fabricated *poly-poly* solar cells. It is also important to note that these simulations are not optimally calibrated, since they represent a qualitative indication of the routes to pursue to achieve higher efficiencies with these devices.

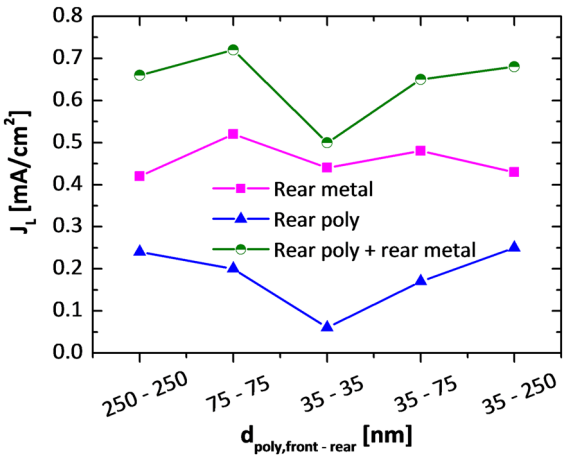

FIGURE 12 Simulated equivalent photocurrent density losses in backside poly-Si and back Ag contact, depending on *poly-poly* solar cell configuration [Colour figure can be viewed at wileyonlinelibrary.com]

Figure 13 shows the simulated and the measured external parameters of the first four solar cells indicated in Table 3. The simulation replicates the same conditions as the fabricated solar cells (SiN_x antireflection coating, 5% coverage metal grid at the front side, Ag/Cr/Al stack at the rear side). In some cases, measured J_{SC} overcomes simulated one (see Figure 13 top-left panel), as a not-optimal calibration of the model might underestimate the J_{SC}. Regarding V_{OC} (bottom left graph in Figure 13), measured values are significantly lower than the simulated ones. In the case of *SC1* and *SC2*, ideal V_{OC} is around 710 mV, for *SC3* V_{OC} ~ 695 mV while for *SC4* V_{OC} ~ 720 mV. This confirms our claim of a weak passivation of the 35-nm-thick p-type poly-Si layer due to its not optimal doping distribution. Indeed, when we switch from *SC3* to *SC4*, simulated V_{OC} increases of approximately 30 mV. Regarding FF (top-right panel in Figure 13), values of our fabricated solar cells are behind the ideal values. All the simulated values are above 80%, while measured ones are between 68% and 73%. We ascribe this major difference to high sheet resistance of poly-Si layers together with the lack of a TCO layer. Moreover, the use of (e-beam) evaporation for realizing the metallization as well as the not-optimal thickness of deposited metals also contribute to FF losses. At the end, the ultimate efficiencies (Figure 13 bottom-right panel) are estimated to increase from 17.7% (*SC1*) to 21.7% (*SC4*).

Finally, we also simulated *SC5* to recognize its ultimate efficiency. We performed this simulation in two different cases: (a) front electron selective contact with an ideal doping profile taken from Procel et al[51] and rear hole-selective contact with the measured doping profile (see Figure 8) and (b) both front and rear poly-Si contacts with ideal doping profiles shown in Procel et al.[51]

Table 4 highlights the external parameters of such simulated solar cells. In the case of front-ideal and rear-measured doping distributions (*SC5-1*), V_{OC} is expected to be equal to 723 mV, J_{SC} to 38.3 mA/cm^2, and FF to 80.3%. The simulated efficiency is thus 22.3%. By employing an ideal doping profile also at rear (*SC5-2*), the J_{SC} stays at the same level as for *SC5-1*, V_{OC} improves by 2 mV, but most importantly, FF increases by 1.5% absolute. This improvement in FF is ascribed to an optimal hole transport at the rear side due to the steeper doping distribution across the junction compared to SC5-1, which allows an improved hole accumulation at c-Si/SiOx interface for enhancing the tunneling current. The ideal efficiency is therefore 22.7%. In perspective, these results are important to understand what

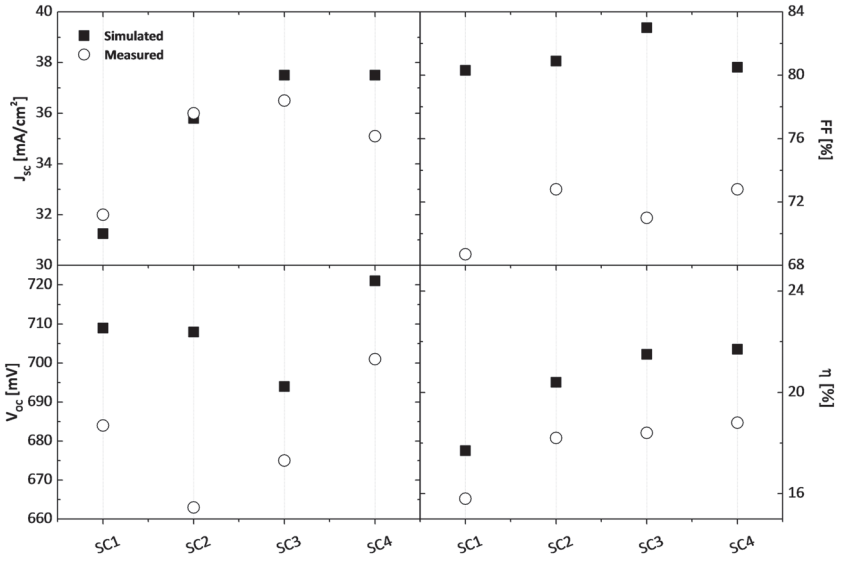

FIGURE 13 Simulated and measured external parameters of *SC1*, *SC2*, *SC3*, and *SC4*. Note that the purpose of these simulations is to have a qualitative idea of the pitfalls of our fabricated solar cells

TABLE 4 External parameters of simulated solar cell SC5 with ideal/measured doping profiles

Solar Cell	Front Poly-Si Doping Profile	Rear Poly-Si Doping Profile	V_{OC}, mV	J_{SC}, mA/cm^2	FF, %	η, %
SC5-1	Ideal	Measured	723	38.3	80.3	22.3
SC5-2	Ideal	Ideal	725	38.3	81.8	22.7

to improve in our fabricated solar cells. Indeed, FF losses are the main limiting factor of efficiency of our TCO-free *poly-poly* solar cells. To tackle these losses, the outlook is to (a) optimize front metal grid, (b) lower series resistance by enhancing lateral transport with in-diffusion in c-Si bulk,[72] (c) realize an efficient metallization scheme (this has already, partially, been demonstrated by Cu-plating), and (d) develop rear edge-isolation of poly-Si layer to decrease edge effects on the solar cell operation. Moreover, also, V_{OC} of our solar cells is affected by non-ideal doping profile. In Procel et al,[51] it is shown how a semi-squared doping profile across c-Si/SiO_2/poly-Si junction leads to optimal selectivity. In an expansion of this work, this ideal doping profile (used for simulations shown in Table 4) can be achieved by in situ doped epitaxially grown layers, LPCVD or PE-CVD techniques. It is noteworthy to mention that recently, reported *poly-poly* cells based on the PECVD route show V_{OC} beyond 720 mV and FF very close to 80%.[73] However, from such experimental results as well as our simulations, it is possible to recognize that the limit of these solar cells is the J_{SC} that, even for front poly-Si thickness of 20 nm, does not overcome approximately 38 mA/cm^2. This is due to strong parasitic absorption at the front poly-Si layer. To avoid these losses, there are several different solutions. The first one is to reduce front poly-Si thickness to d_{poly} < 10 nm. At that point, a TCO transport layer will be necessary to ensure good fill-factor.[74-76] Another possible solution is to change the front side structure with either amorphous silicon or a lightly doped homojunction front surface field with poly-Si passivating contacts only underneath the contacts. Figure 14 shows the EQE of *SC3*, a hybrid solar cell from,[39] and a PeRFeCT solar cell from.[27] With both the hybrid and the PeRFeCT architectures

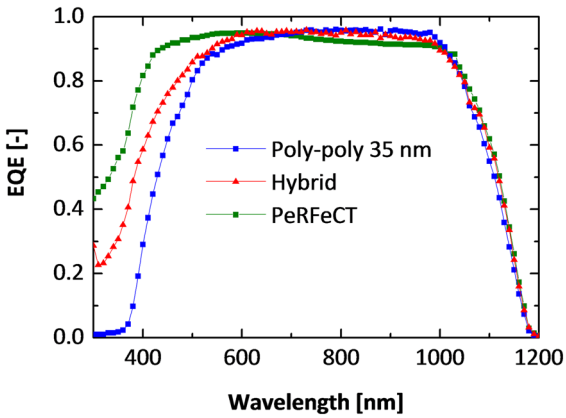

FIGURE 14 External quantum efficiency of poly-poly *SC3*, a hybrid solar cell with front side based on intrinsic amorphous silicon passivation and rear p-type poly-Si[34] and PERFeCT solar cell[22] [Colour figure can be viewed at wileyonlinelibrary.com]

losses in the blue part of the spectrum can be mitigated. The poor responsivity at the short-wavelength of our *poly-poly* cell is much less problematic if such architecture is deployed in a tandem configuration together with a thin-film top cell such as perovskite,[29] either in a monolithic configuration or in a four-terminal configuration.[77]

4 | CONCLUSION

In this paper, we optimize poly-Si layers as carrier-selective passivating contacts prepared by LPCVD and boron- or phosphorous-

doped via ion implantation. With the aim to reduce parasitic absorption in the poly-Si layers, their thickness is drastically reduced from 250 to 35 nm, and both passivation quality and junction profile are investigated on symmetric samples by varying ion dose and annealing treatment (ie, temperature/time). For SiO_2/n-type poly-Si fabricated on textured c-Si wafers, we obtain J_0 < 15 fA/cm^2 regardless the deposited poly-Si thickness. For these samples, carrier lifetimes above 4 milliseconds are measured for both the thickest and thinnest investigated poly-Si layers. On the contrary, 75-nm-thick layer exhibits τ_{eff} ~ 2 ms, due to not-optimized doping profile that leads to a degraded field-effect passivation. ECV measurements confirm this hypothesis indicating, for an acceptable passivation quality, a shallow junction depth into c-Si bulk and 10^{20} P atoms/cm^3 confined into poly-Si layer for the 250-nm and 35-nm-thick samples. Regarding the SiO_2/p-type poly-Si, passivation quality increases with poly-Si thickness. This result is the consequence of an easier doping confinement in 250-nm-thick poly-Si. Although we changed implantation dose and annealing temperature/time, doping profile has a wide junction depth when thinner poly-Si is employed, leading to weaker field-effect passivation.

We evaluated the effect of doping profile on field-effect passivation and band alignment on the basis of TCAD simulations. Accordingly, the experimentally optimized doping profile maximizes the trade-off between electrical field and Auger recombination by means of high doping concentration at c-Si surface and thinner buried doping profile inside c-Si, concurrently. The optimized p- and n-type SiO_2/poly-Si contacts are tested in completed TCO-free FBC *poly-poly* solar cells with SiN_x as anti-reflection coating. It is important to remark that the fabrication process is lean, such that it has only four steps. By decreasing front/rear poly-Si thicknesses, as expected, more incoming light can reach the c-Si without being parasitically absorbed in the front stack. We measure a gain in J_{SC} up to 4 mA/cm^2 when switching from 250- to 35-nm-thick front poly-Si. Moreover, we have shown that most of the optical losses are in the short-wavelength range. In fact, according to TCAD simulations, equivalent photo current density losses are highly dependent on front poly-Si thickness, while the equivalent photocurrent density lost at the rear side in the long-wavelength range is only 0.15 mA/cm^2 when switching the rear side poly-Si thickness from 250 to 35 nm. Therefore, we decouple the front/rear poly-Si thicknesses, keeping the p-type on the rear side at 250 nm and thinning the film on the front down to 35 nm to concurrently optimize transparency of the front film and p-type passivation at rear. This cell (*SC4*) exhibits a V_{OC} of 701 mV with a gain of 17 mV as compared with the device with thicker p-type poly-Si (*SC1*). Further decrease in the front n-poly-Si layer down to 20 nm leads to a trade-off between V_{OC} (decreased to 689 mV) and J_{SC} (increased to approximately 36 mA/cm^2). Finally, using Ti-Cu plated front contacts, FF increases up to 75.2% while V_{OC} decreases to 682 mV, ascribed to background plating outside the designated grid area. A TCAD simulation of our *poly-poly* solar cells shows that the efficiency of our solar cells is mainly limited by FF losses coming from various sources: (a) not-optimized front metal grid, (b) series resistance given by poor lateral transport due the small in-diffusion in c-Si bulk, (c) thin metallization scheme, and (d) no rear edge-isolation of poly-Si structure. With all these adjustments, we forecast efficiencies greater than 21% in single junction configuration. It is remarkable that processing of this solar cell consists in only four steps, and therefore, it is suitable for industrial up taking with further engineering. The authors believe that this solar cell architecture is a good candidate for a bottom cell in tandem configuration with emerging technologies such as perovskite. Indeed, given its high thermal budget and the poor responsivity in the blue part of the spectrum, it matches all the requirements for a fabrication of both two and four terminal tandem devices.

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