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| 浙江大学信息与电子工程学院 | **集成电路原理与设计** | 2023年5月 |
| 2022-2023学年春夏学期 |

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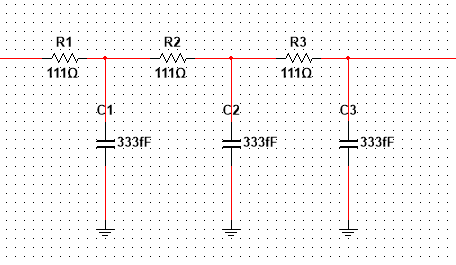
**Exercise 9**

* 1. Consider a 5 mm-long, 4 λ-wide metal2 wire in a 0.6 μm process. The sheet resistance is 0.08 Ω/□ and the capacitance is 0.2 fF/μm. Construct 3-segment L-model and 3-segment π-model for the wire. (Please present models and calculate delay).

Answer

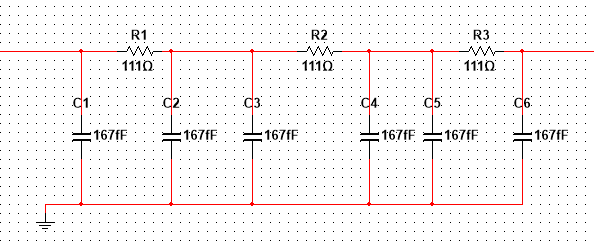
The wire width is 1.2𝜇m so the wire is 5000𝜇m/1.2𝜇m= 4167 squares in length

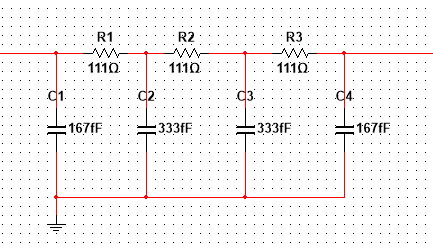
So, the total resistance is (0.08 sq)4167 sq) = 333 The total capacitance is (0.2 fF/)5000m) = 1 pF



3-segment L-model

+ =





3-segment 𝝅-model

=

* 1. Assume an inverter is designed with a PMOS/NMOS ratio of 3.6 and the NMOS transistor is minimum size. (W = 0.375m, L = 0.25m, W/L =1.5). 𝑉𝑀=1.25V, 𝑉𝐷𝐷=2.5V. Please describe the voltage transfer characteristic and noise margins of CMOS inverter. (use , , , and g). The parameters shown in table 9.1.

Table9.1

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|  | VT0 (V) | γ  (V1/2) | VDSAT  (V) | K  (μA/V2) | λ  (V-1) |
| NMOS | 0.7 | 0.45 | 0.83 | 134 | 0.1 |
| PMOS | -0.8 | -0.4 | -1 | -50 | -0.2 |

Answer