

Modeling and Control of Grid-following Single-phase Voltage-sourced Converter

List of authors: Huazhao Ding, Zhengyu Wang, Lingling Fan, Zhixin Miao

Presenter: Huazhao Ding



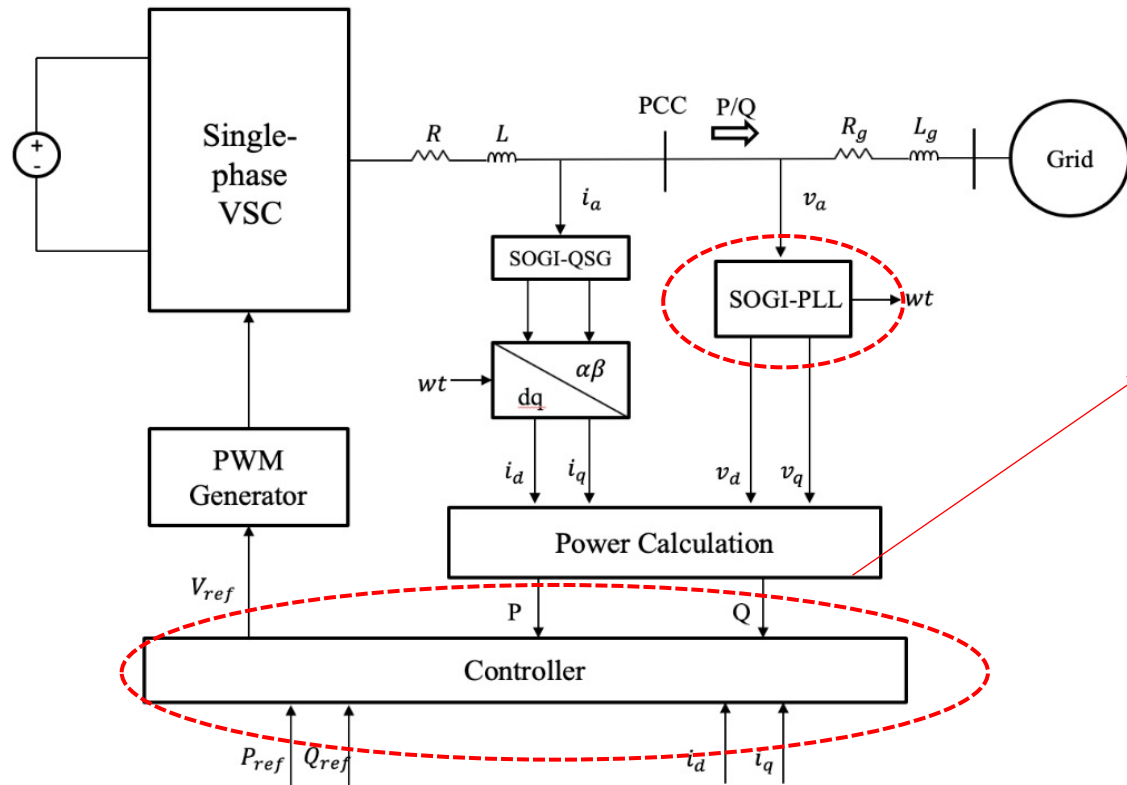
Overview

- Introduction
- Structure of the system and control algorithm
- Second-order Generalized Integrator (SOGI) -based PLL Case study
- Case study
- Conclusion

Introduction

- In North America, some rural areas where no three-phase supply is available, single-phase distribution are widely used among farmers and households even some small commercial environment.
- Compared with three-phase system, modeling and control of single-phase system was conducted less by researchers and scholars.
- Second-order generalized integrator based Phase-Locked loop has low computation cost and good performance against hostile grid condition.
- Weak grid analysis is very important and of practical to test the operation limit of a system.

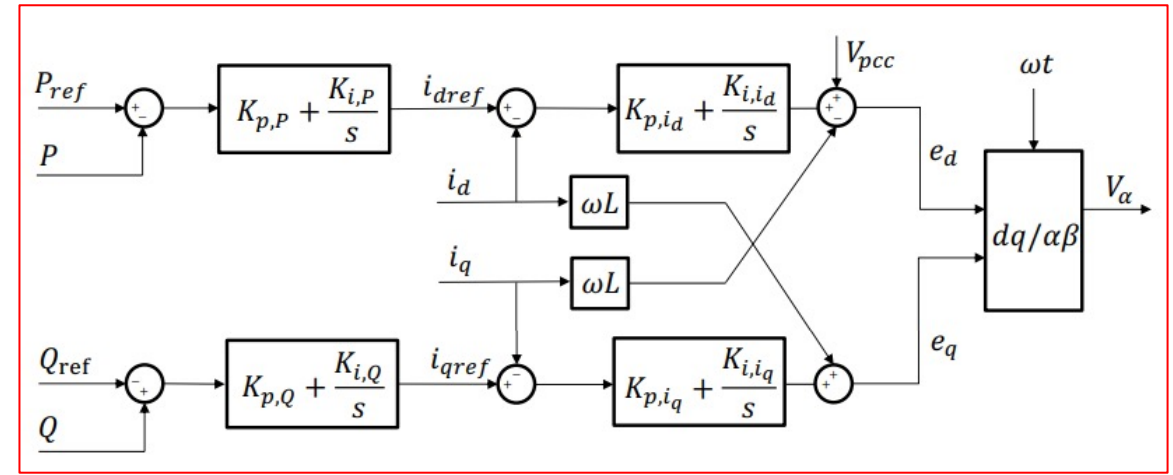
Structure of the system and control algorithm



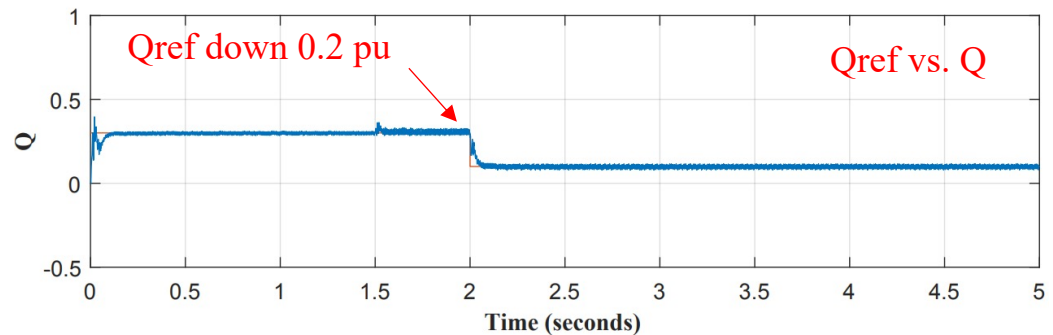
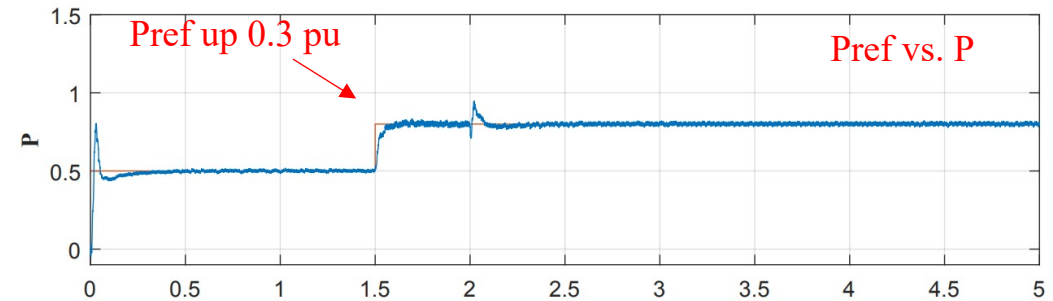
Item	Value	Item	Value
S _{base}	4000 VA	V _n	190.52 V
R	1.1E-5 pu	X	1.142 pu
R _g	0.05 pu	X _g	0.25 pu

TABLE III: Parameters of the controller

Item	Value	Item	Value
K _{p,P}	0.4	K _{i,P}	45
K _{p,Q}	0.4	K _{i,Q}	40
K _{p,i_d}	0.4758	K _{i,i_d}	3.2655
K _{p,i_q}	4	K _{i,i_q}	15



PQ Control



Second-order Generalized Integrator (SOGI) -based PLL

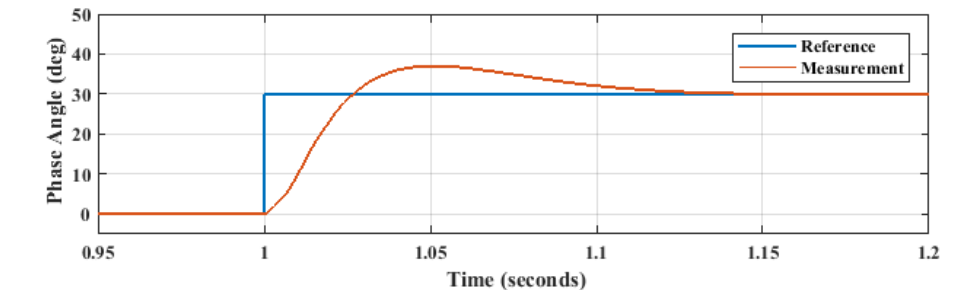
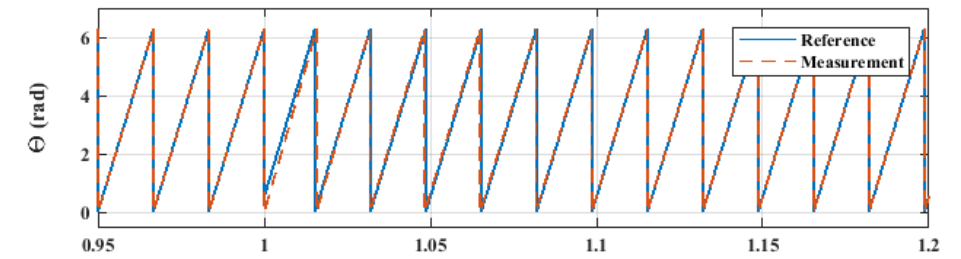
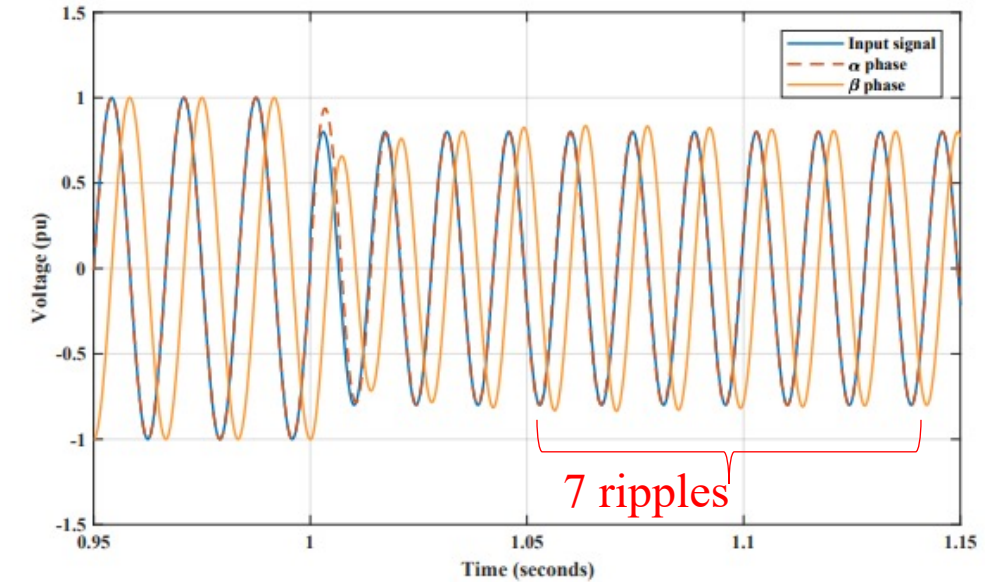
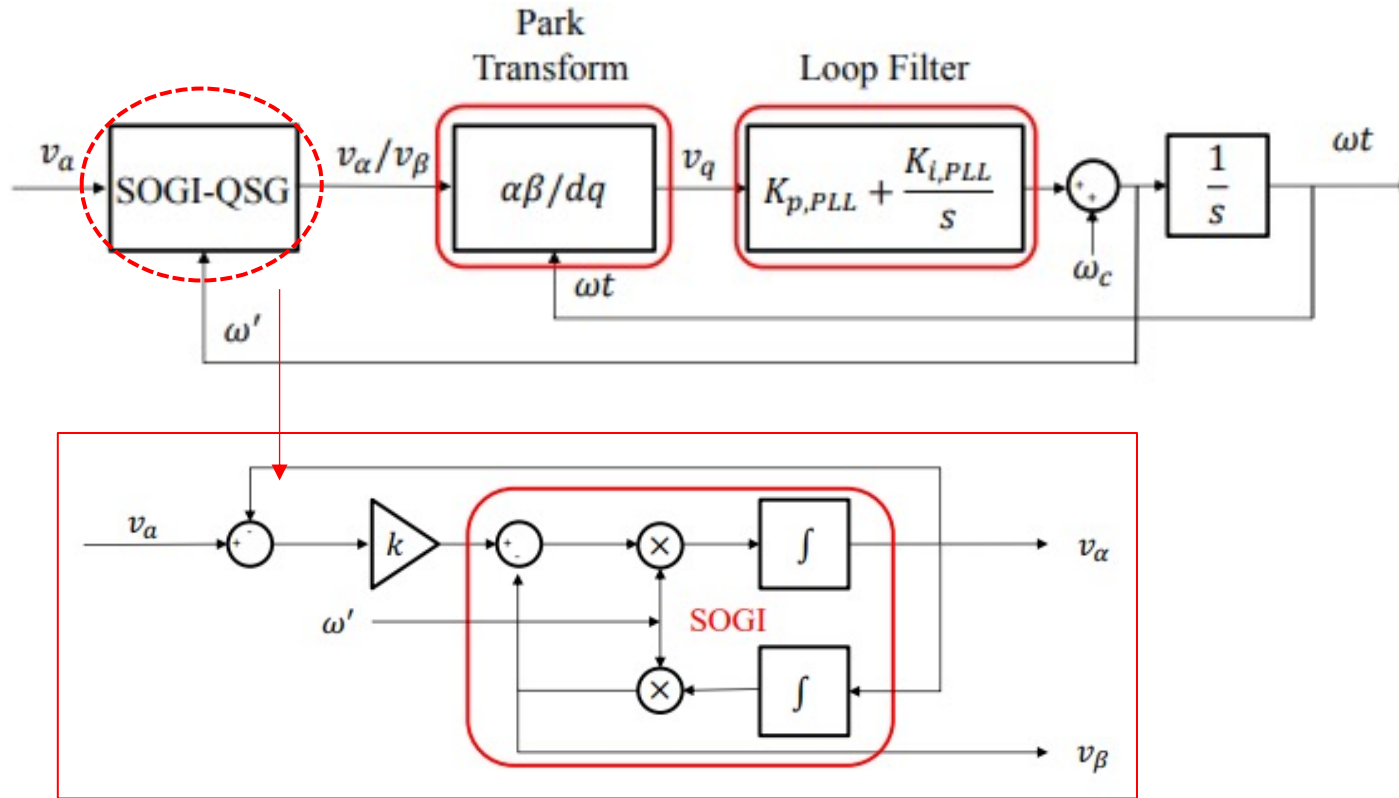


TABLE II: Parameters of SOGI-PLL

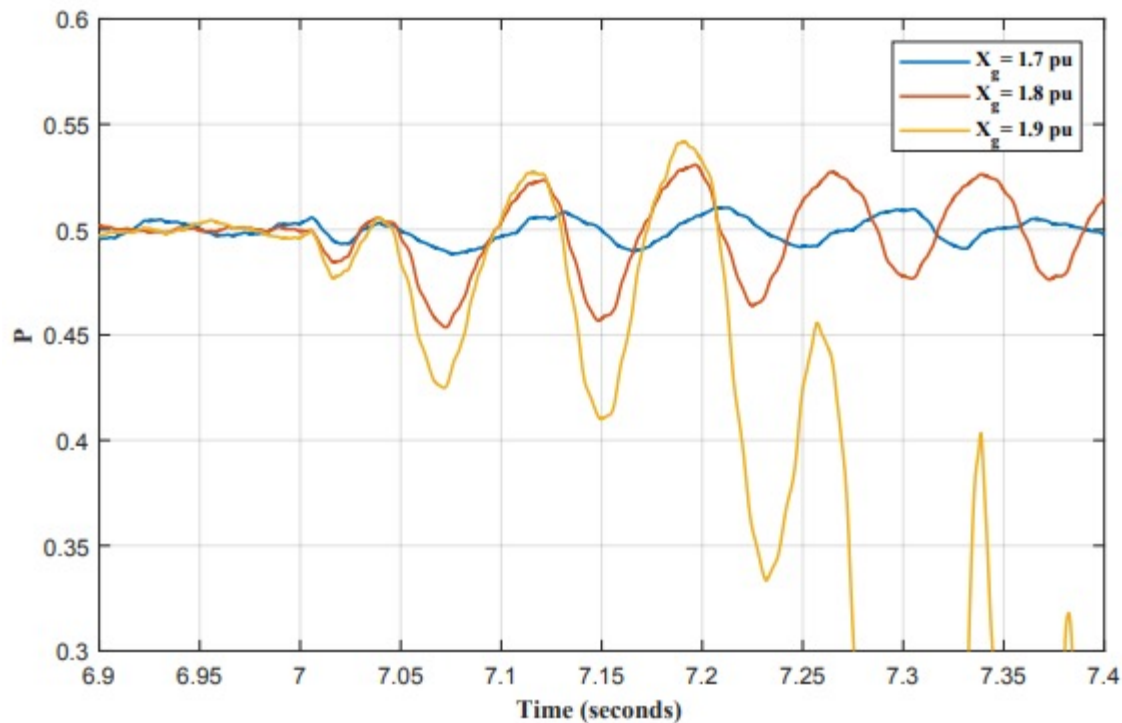
Item	Value	Item	Value
$K_{p,PLL}$	60	ω_c	376.9 rad/s
$K_{i,PLL}$	1400	k	$\sqrt{2}$

SOGI-PLL Tracking

1. Magnitude drops by 0.2 pu
2. Frequency increases by 10 Hz
3. Phase jumps by 30 degrees

Case studies – Weak grid condition

- Event 1: Line impedance increases from 1.6 to 1.7 pu
- Event 1: Line impedance increases from 1.6 to 1.8 pu
- Event 1: Line impedance increases from 1.6 to 1.9 pu



```
Vd = Vpcc;
Vq = 0;
vpcc = Vd+1i*Vq;
vg = exp(-1i*theta);
Xg = 0.25+1.6i;
I = (vpcc-vg)/(0.05+1i*Xg);
Id = real(I);
Iq = imag(I);
Pg = Vd*Id+Vq*Iq;
Qg = Vq*Id-Vd*Iq;
```

```
Vd = Vpcc;
Vq = 0;
vpcc = Vd+1i*Vq;
vg = exp(-1i*theta);
Xg = 0.25+1.61i;
I = (vpcc-vg)/(0.05+1i*Xg);
Id = real(I);
Iq = imag(I);
Pg = Vd*Id+Vq*Iq;
Qg = Vq*Id-Vd*Iq;
```

```
Constraints = [ Pg == 0.5;
               Qg == 0.3;];
Objective = 0;% decrease error to ;
```

```
Constraints = [ Pg == 0.5;
               Qg == 0.3;];
Objective = 0;% decrease error to zero
```

Total CPU secs in IPOPT (w/o function evaluations)	=	0.320
Total CPU secs in NLP function evaluations	=	0.060

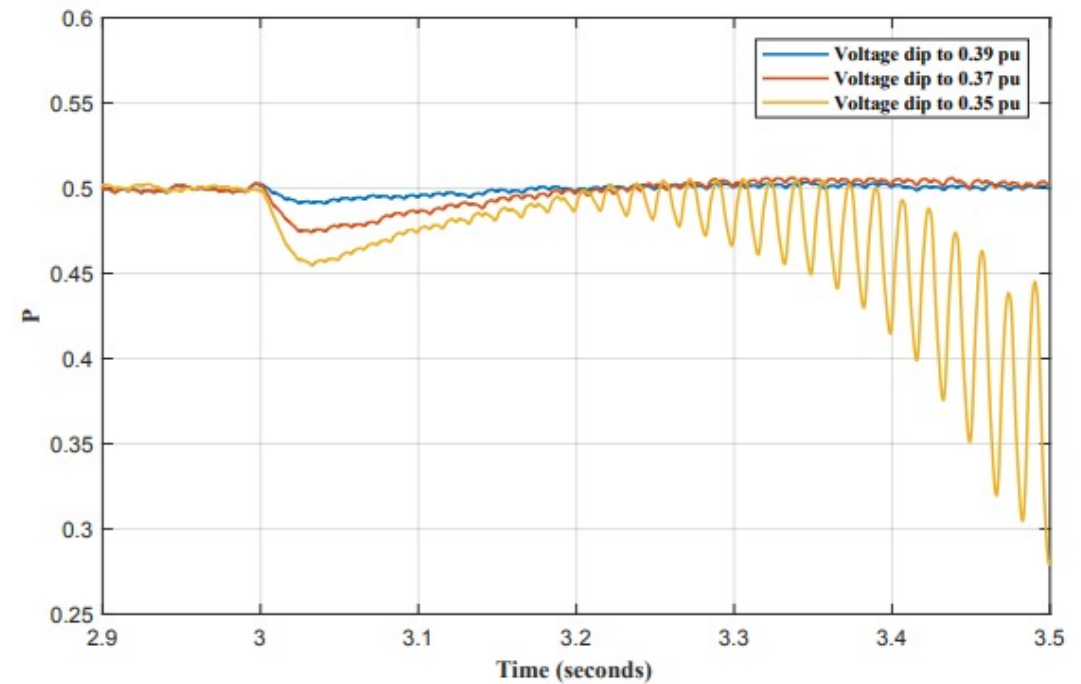
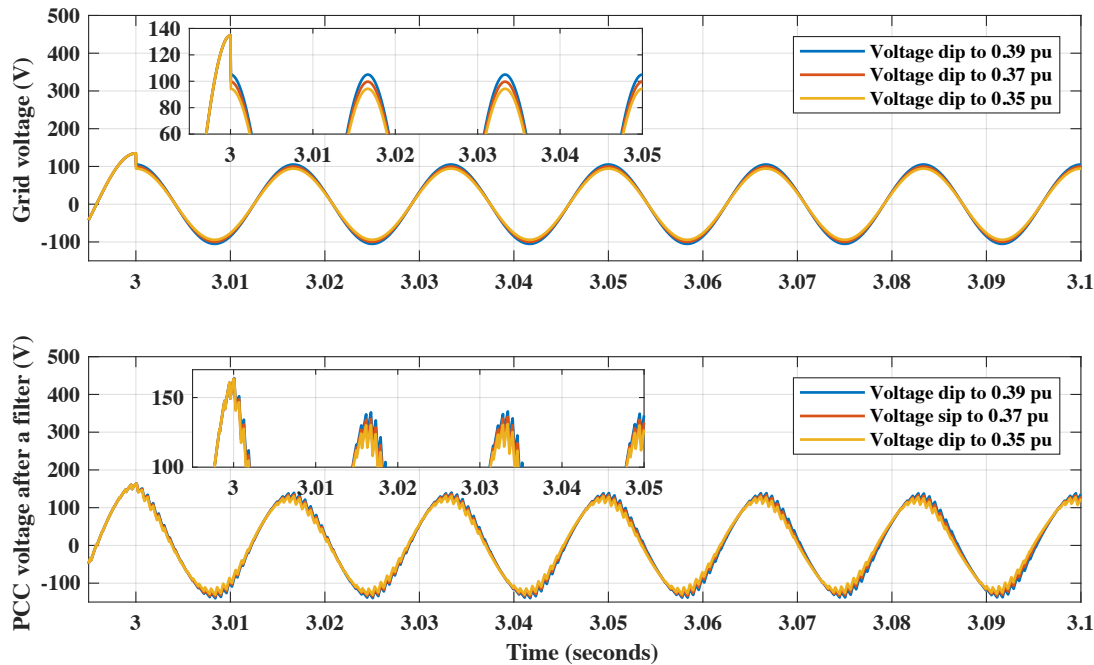
EXIT: Optimal Solution Found.

Total CPU secs in IPOPT (w/o function evaluations)	=	0.362
Total CPU secs in NLP function evaluations	=	0.347

EXIT: Converged to a point of local infeasibility. Problem may be infeasible.

Increases the line impedance to push system to unstable condition. Line impedance is increased by switching on additional RL branch (series connected).

Case studies – Grid voltage changes

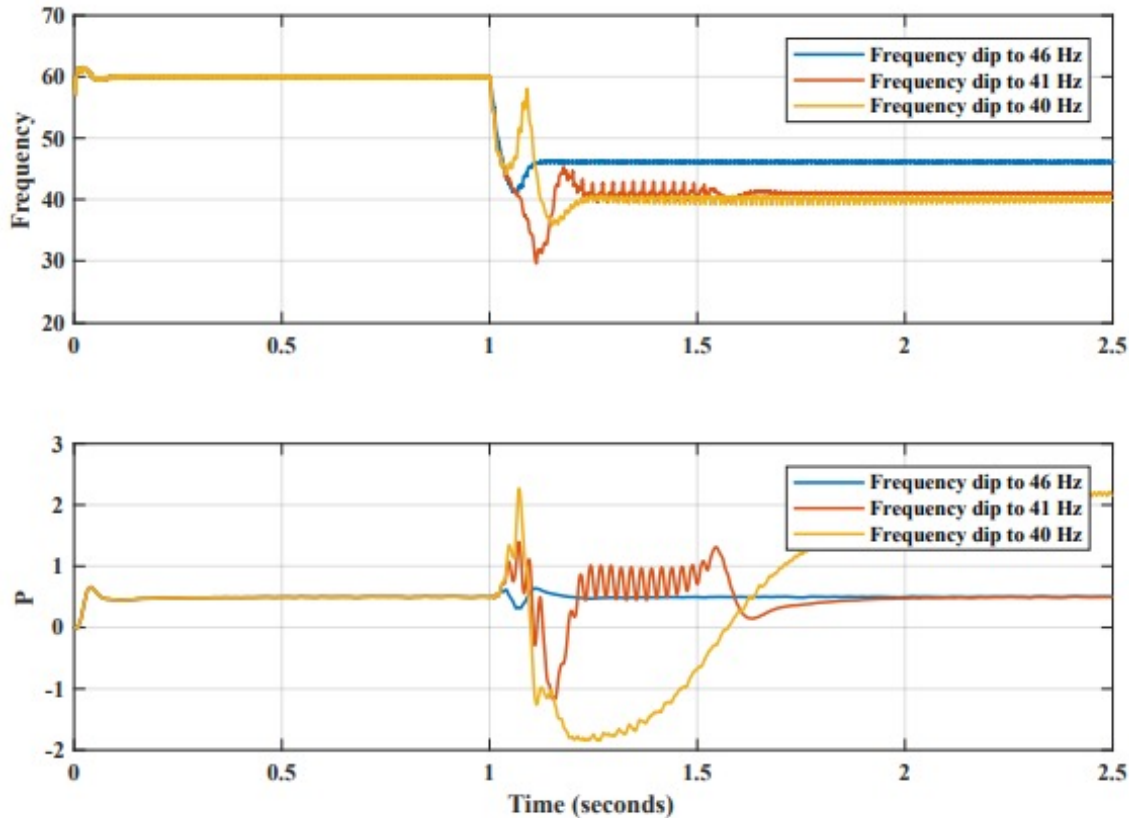


Grid voltage magnitude dips:

1. Dips to 0.39 pu
2. Dips to 0.37 pu
3. Dips to 0.35 pu - unstable

Grid voltage and PCC voltage are measured to show the voltage dip result. The above figure shows that PCC voltage seems still stable when grid voltage dips to 0.35 pu. However, the real power at PCC bus cannot track the reference value.

Case studies – Grid frequency changes



Three events are given to test the grid frequency dip.

Frequency of SOGI-PLL was examined. Figures in left shows SOGI-PLL could work more tolerate that the main system. SOGI-PLL could work when the grid frequency dips to 40 Hz, while the real power shows that the testbed is not stable.

Grid frequency dips:

1. Dips to 46 Hz
2. Dips to 41 Hz
3. Dips to 40 Hz - unstable

Conclusion

- An EMT testbed of single-phase VSC in grid following mode is modeled and tested.
- SOGI-PLL is examined. Three events are given to measure and test its performance. SOGI is implemented to generate the dq-component by using single-phase component.
- Weak grid analysis, grid voltage dip and grid frequency dip is conducted to test the system's limit operation condition. YALMIP is applied to validate the result.