Karlsruher Institut für Technologie

New camera platform for science

Collaboration meeting for phase contrast Camera, DESY, 01 March 2017

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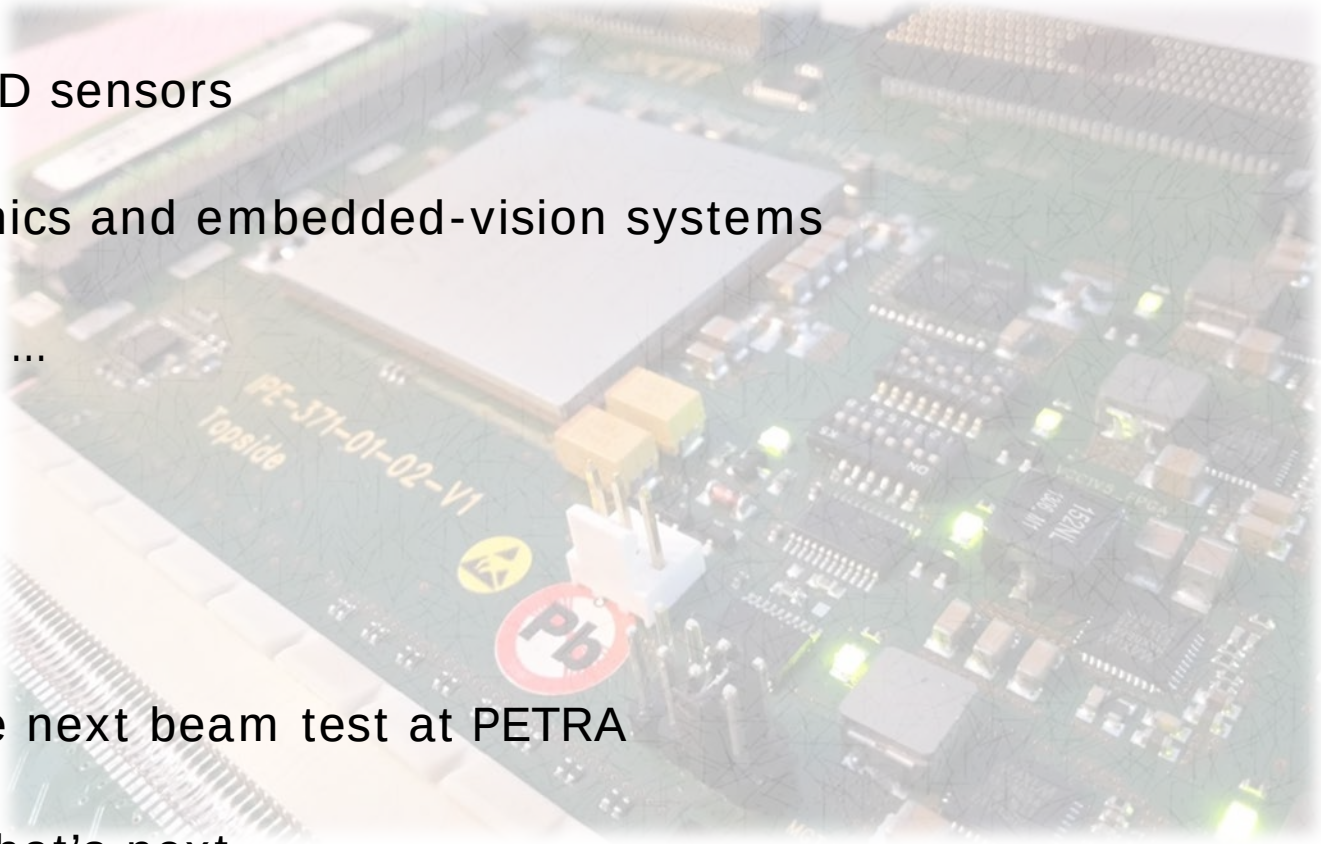
KIT, Institut für Prozessdatenverarbeitung und Elektronik
CMS periodical meeting

Outline

- Motivations
- New CMOS – CCD sensors
- Readout electronics and embedded-vision systems
- New solution for …
- Preparing for the next beam test at PETRA
- Conclusions & what's next

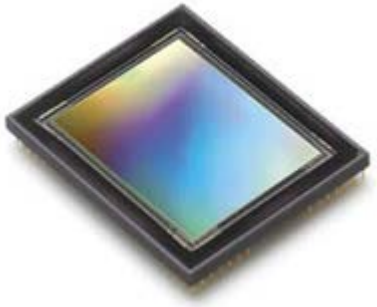


IPE- Readout board - "High-Flex"

Motivation

- **Increasing demand of high-resolution and/or high-speed cameras for X-ray:**
  - High-resolution and low-noise → large CCD (60 Mpixel)
  - High-speed tomography → 1 Mpixel @ minimum frame rate of 5 kfps
- **Technology trend ➔ FPGA with integrated Distributed Multi-processor systems**
  - Heterogeneous systems based on FPGA – GPUs – CPUs - SoC
- **Move FPGA "development code" from "engineering" → to "physics"**
  - On-line data processing on FPGA with partial re-programming written C/C++ or OpenCL
  - Embedded-vision → camera control, calibration, data-processing algorithm, etc. by Multi-Processor SoC and FPGA on same device
- **High-performance data-processing applications**
  - PCIe-DMA based on GPUDirect technology
  - High-performance UFO-framework for GPUs data-processing

New CCD – 60 Mpixel for phase contrast



Well-capability
> 40 ke⁻

- Large Image format (53.8 x 40.3 mm²)
- 60 Mpixel (8956H x 6708V) pixels pitch of 6x6 µm² has a 4:3 aspect ratio
- Fast variable electronic shuttering
- Vertical sub-sampling → ROI algorisms
- >95% fill factor
- High sensitivity, high dynamic range (> 70dB)
- Low dark current and low fixed pattern noise, low readout noise

Architecture:

The device has four identical low-noise output amplifiers, one at each corner of the chip, to allow simultaneous readout through one, two or four outputs.

The Dynamic Range is >11 true bits at 60° C and 25 MHz pixel frequency.

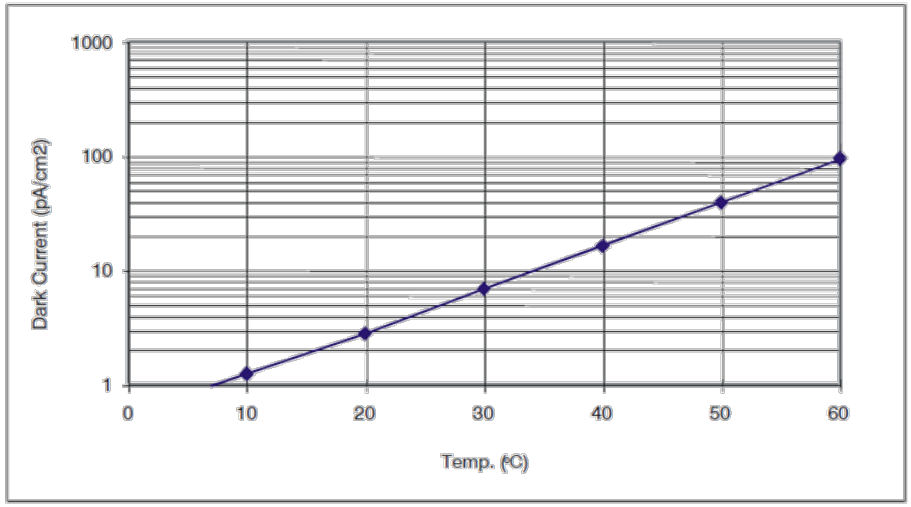
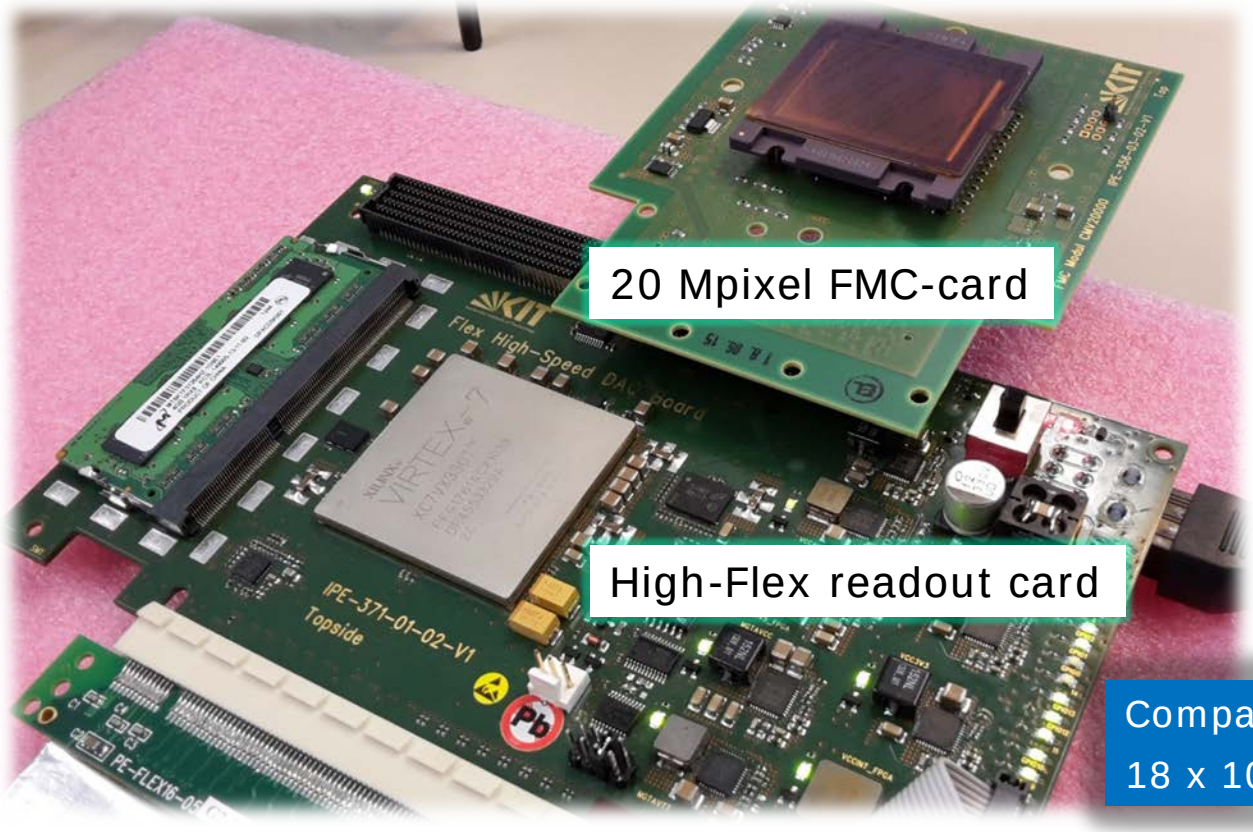


Figure 11: Dark current versus temperature.

Good operation point over the dew point (15° C)

Current readout system

Readout system based on IPE card so-called “High-Flex” and not ML605



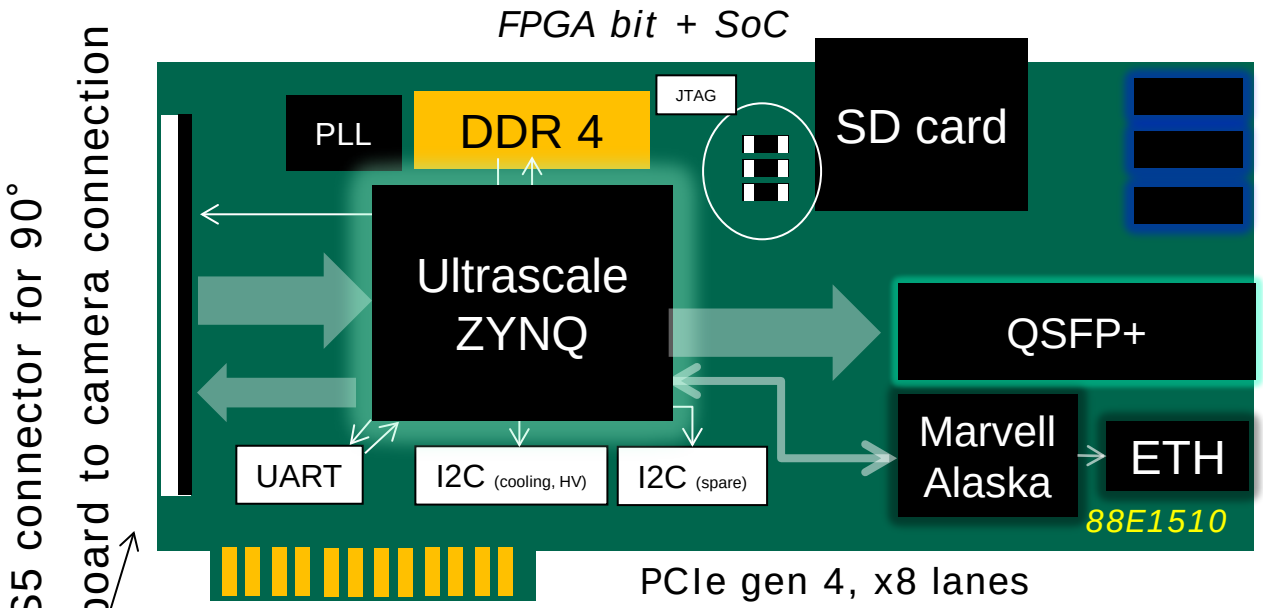
High-Flex is a multi-purpose high-performance readout card for:

- X-ray camera
- Photo science

based on Virtex 7

It uses the *KIT-DMA* based on “*GPUDirect*” technology for a fast data transfer from data source to GPU up to 120 Gb/s

Futures readout system – under design



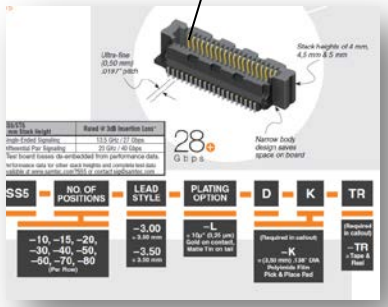
External trigger and programmable I/Os

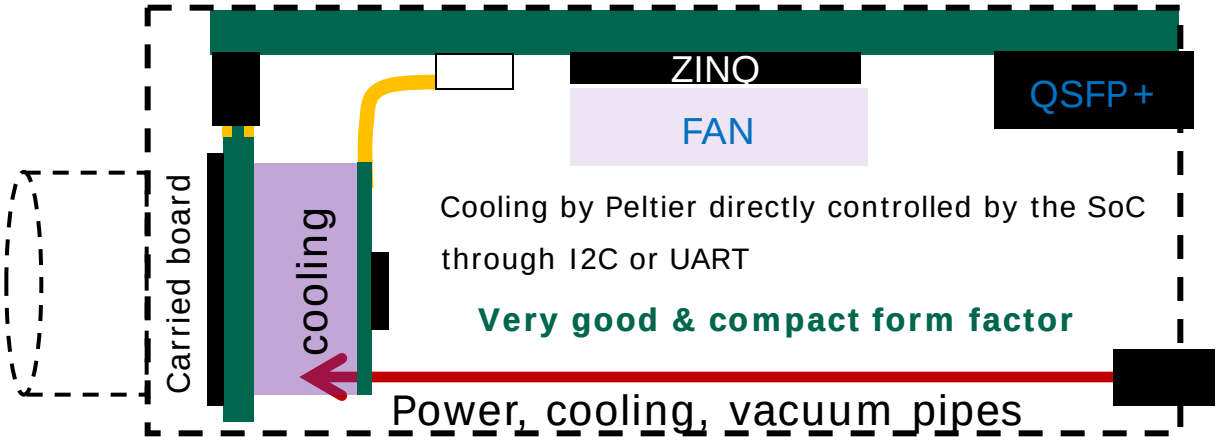
High-speed DAQ

4 x 28 Gb/s - Full-duplex

Control and on-line data check

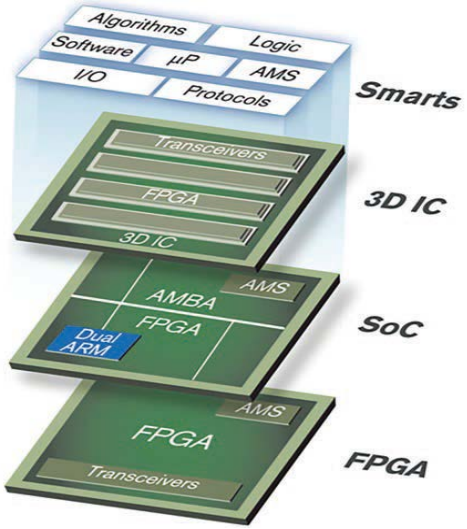
TCP/IP – RJ45





Next readout infrastructure – MP SoC

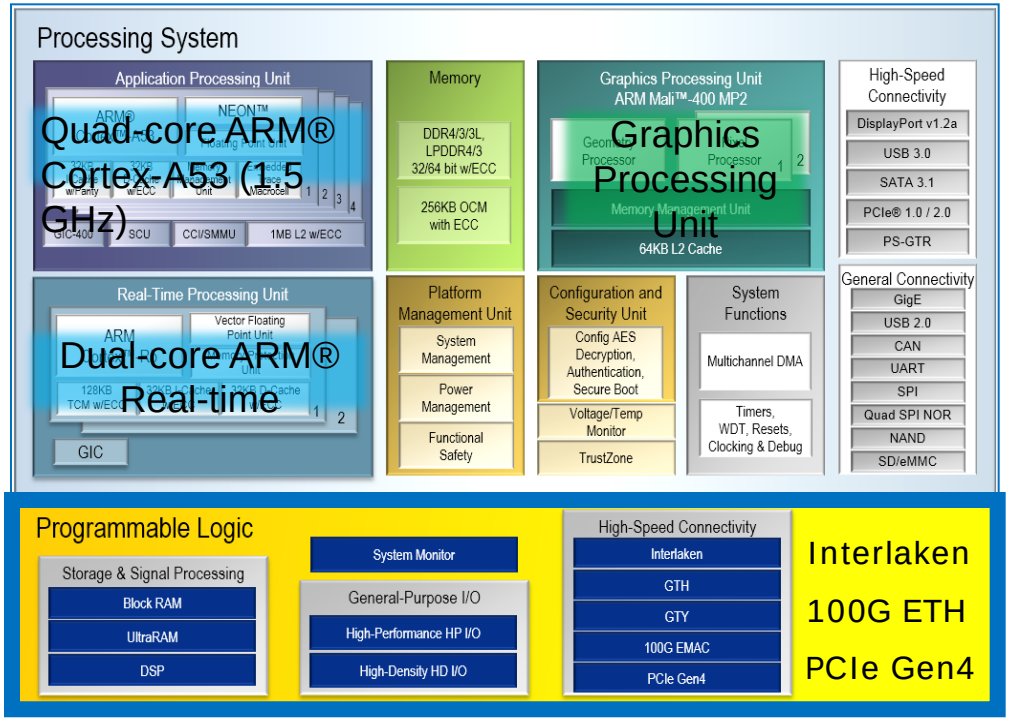
Future KIT-readout infrastructure: Heterogeneous (FPGA -> MPSoC -> GPUs)



Zynq UltraScale+ CG

FPGA today based on 3D-ASICs technology:

1) Power ARM Processors for Application program and Real-time
2) Large and high performance FPGA
3) High Bandwidth Memory (URAM)



How optimize a heterogeneous FPGA + MPSoC + GPU system in according to specific applications ?

Common programming language for FPGA and GPUs ... ?

PhD: Weijia Wang

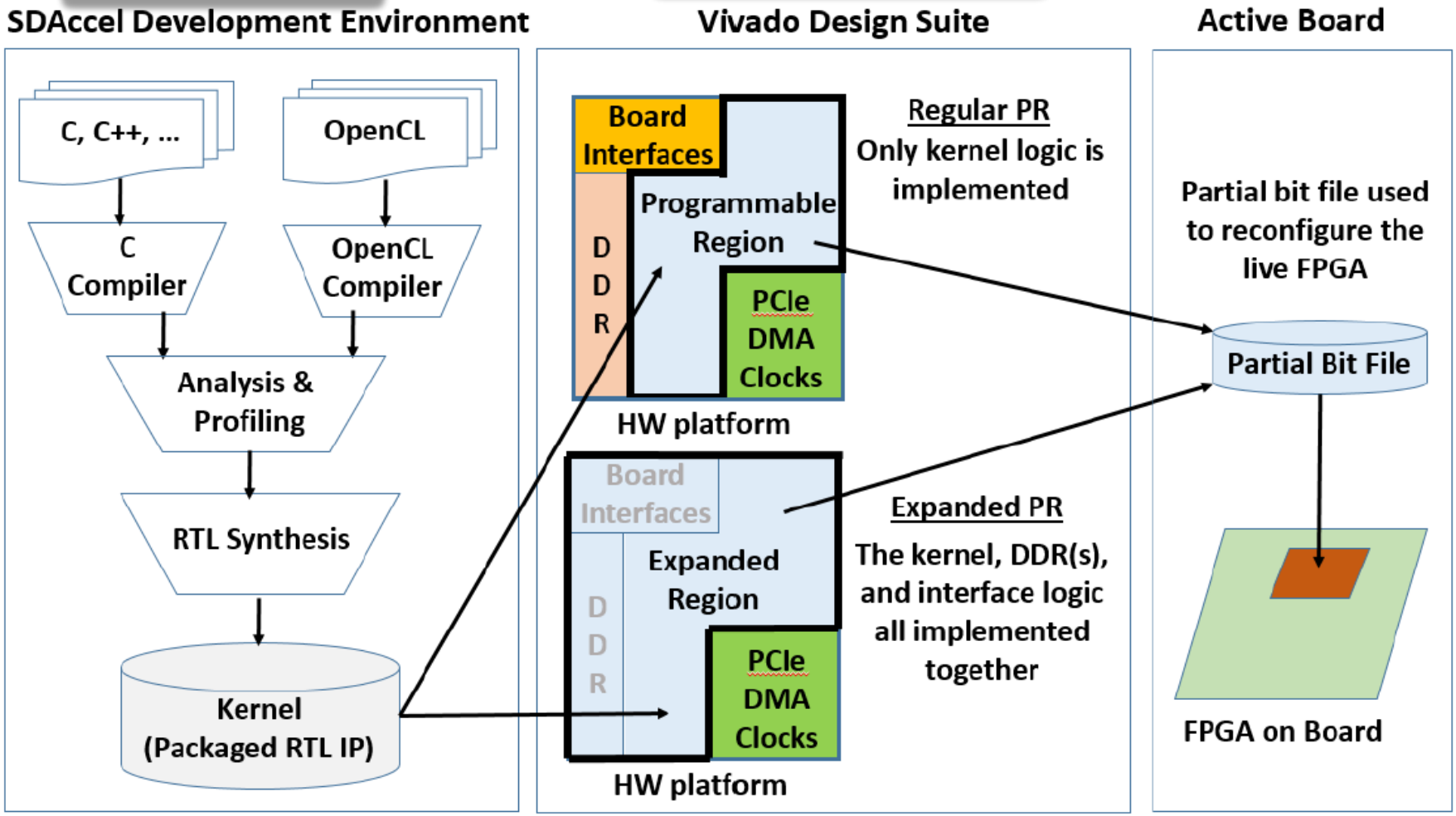
SDx development tools

Which enables software developers with no FPGA experience to create systems in C or C++ targeting Zynq, FPGA - SoC devices

Workflow

"Scientific"
New algorithm
(many times)

"Engineering"
Basic infrastructure
(only one time)



OpenCL on FPGA – working principle

OpenCL applications consist of two parts: Host program + Kernels

Kernel Program

```
__kernel void
sum(__global const float *a,
__global const float *b,
__global float *answer)
{
int xid = get_global_id(0);
answer[xid] = a[xid] + b[xid];
}
```

OpenCL
Host Program + Kernels

Xilinx
SDAccel

Standard
C Compiler

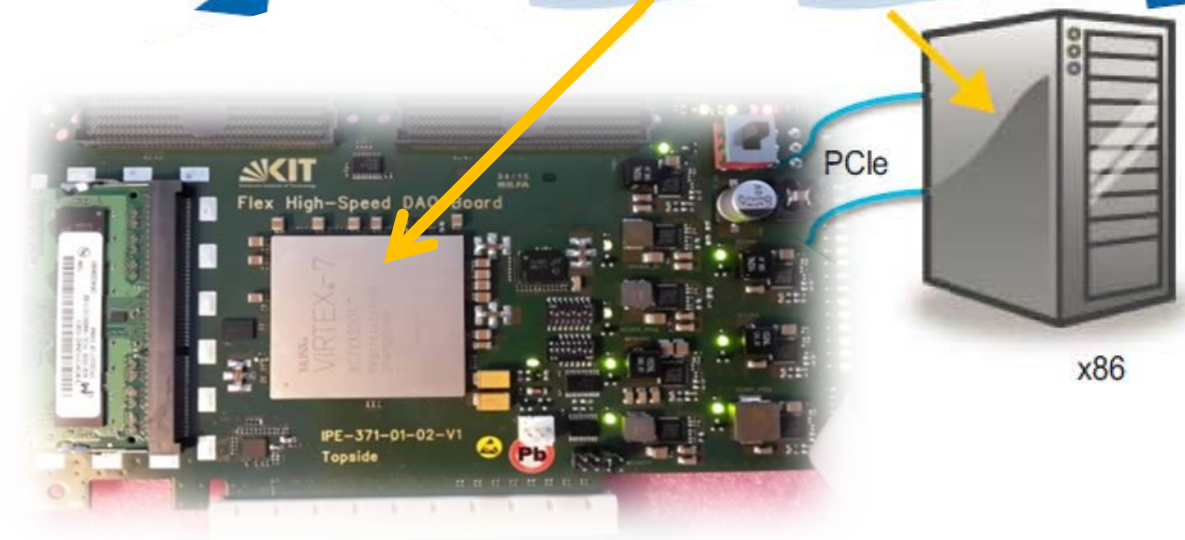
SOF

X86 binary

```
main( )
{
    read_data_from_file( ... );
    maninpulate_data( ... );

    clEnqueueWriteBuffer( ... );
    clEnqueueTask( ..., my_kernel, ...);
    clEnqueueReadBuffer( ... );

    display_result_to_user( ... );
}
```

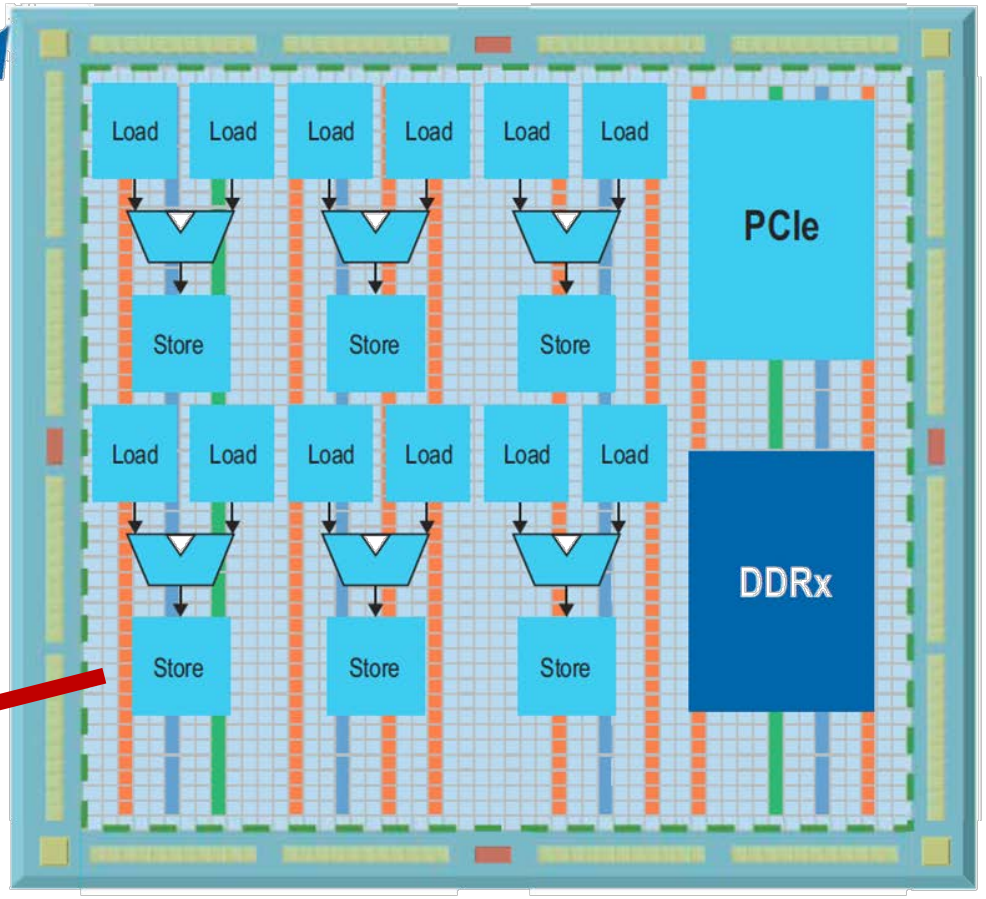


Host software routine call a computationally expensive function.

This function to be accelerated is referred to as an OpenCL kernel

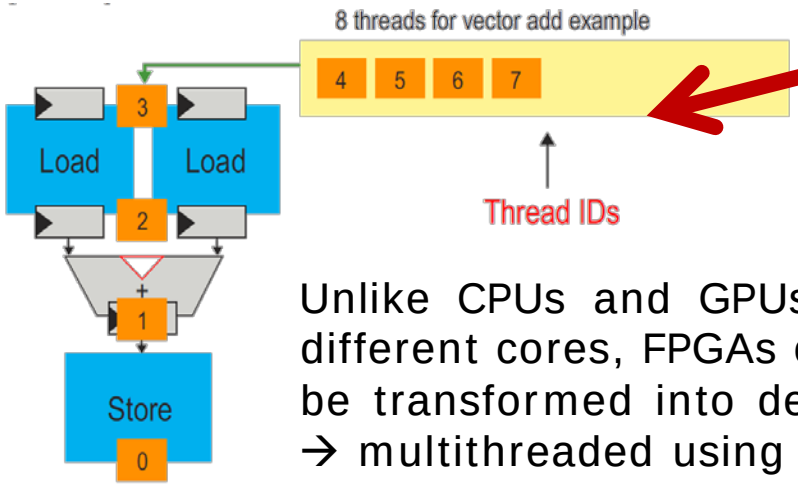
Kernel in the FPGA

```
__kernel void
sum(__global const float *a,
__global const float *b,
__global float *answer)
{
int xid = get_global_id(0);
answer[xid] = a[xid] + b[xid];
}
```



Example: performs the vector addition of two arrays, *a* and *b*, while writing the results back to an output array answer.

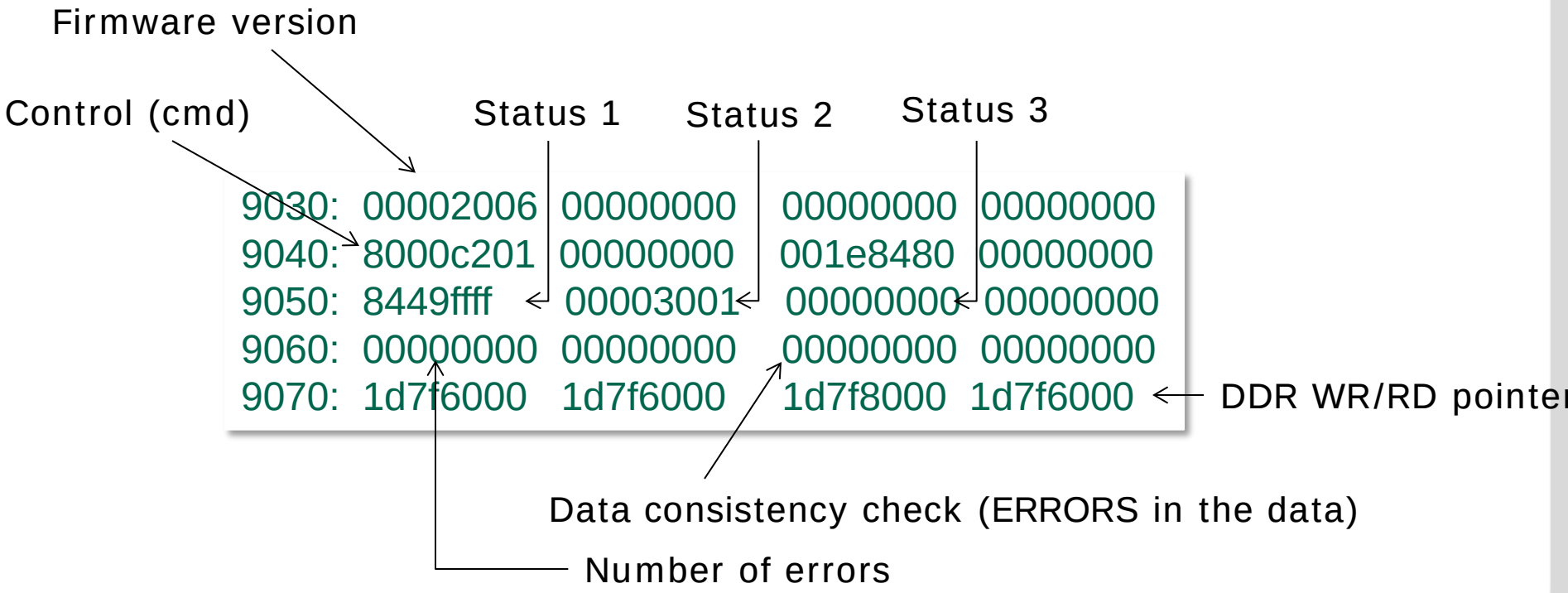
FPGA offers massive amounts of fine-grained parallelism



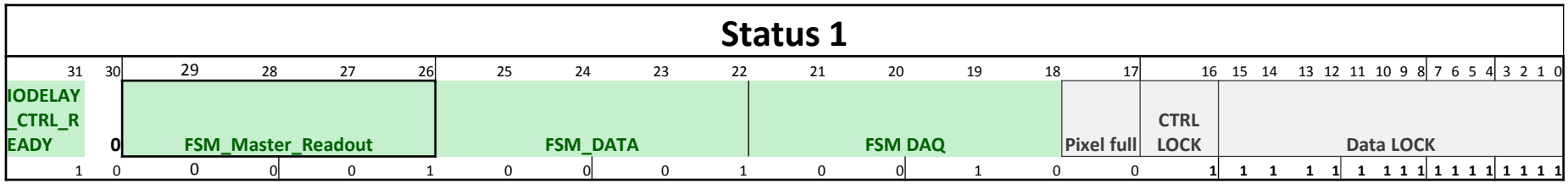
Unlike CPUs and GPUs, where parallel threads can be executed on different cores, FPGAs offer a different strategy → Kernel functions can be transformed into dedicated and deeply pipelined hardware circuits → multithreaded using the concept of pipeline parallelism

20 Mpixels camera for next beam test @ PETRA

User Bank Register



Status and errors – 20Mpix camera



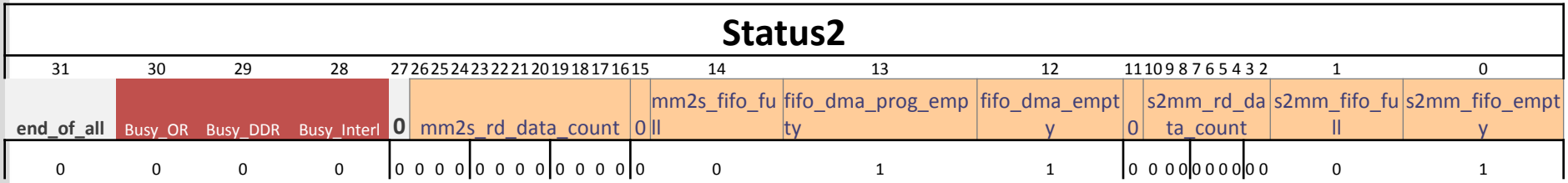
Camera speed-grade = 1

Main FSMs

Control lock =1

Data LOCK must be=FFFF

Before an after readout must be = 8449FFFF



Busy OR logic, DDR and Interleaving-special

Status FIFO DDR -> DMA

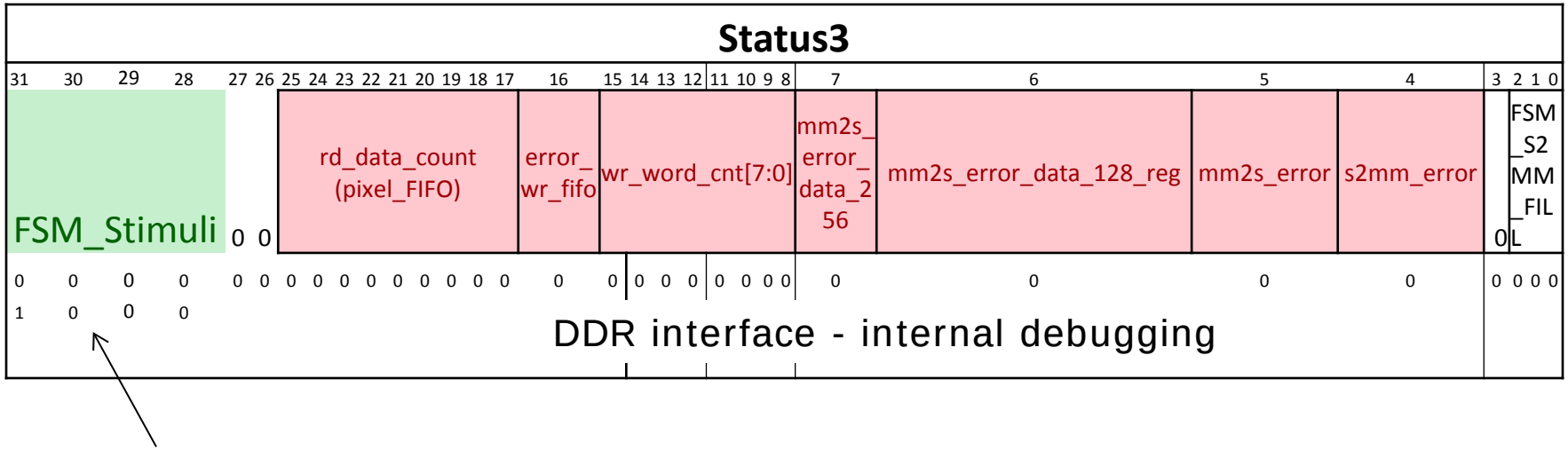
Status FIFO SENSOR -> DDR

Single or sequence frames acquired

Before an after readout must be = 00003001

Status and errors – 20Mpix camera (II)

Before an after readout must be = 00000000



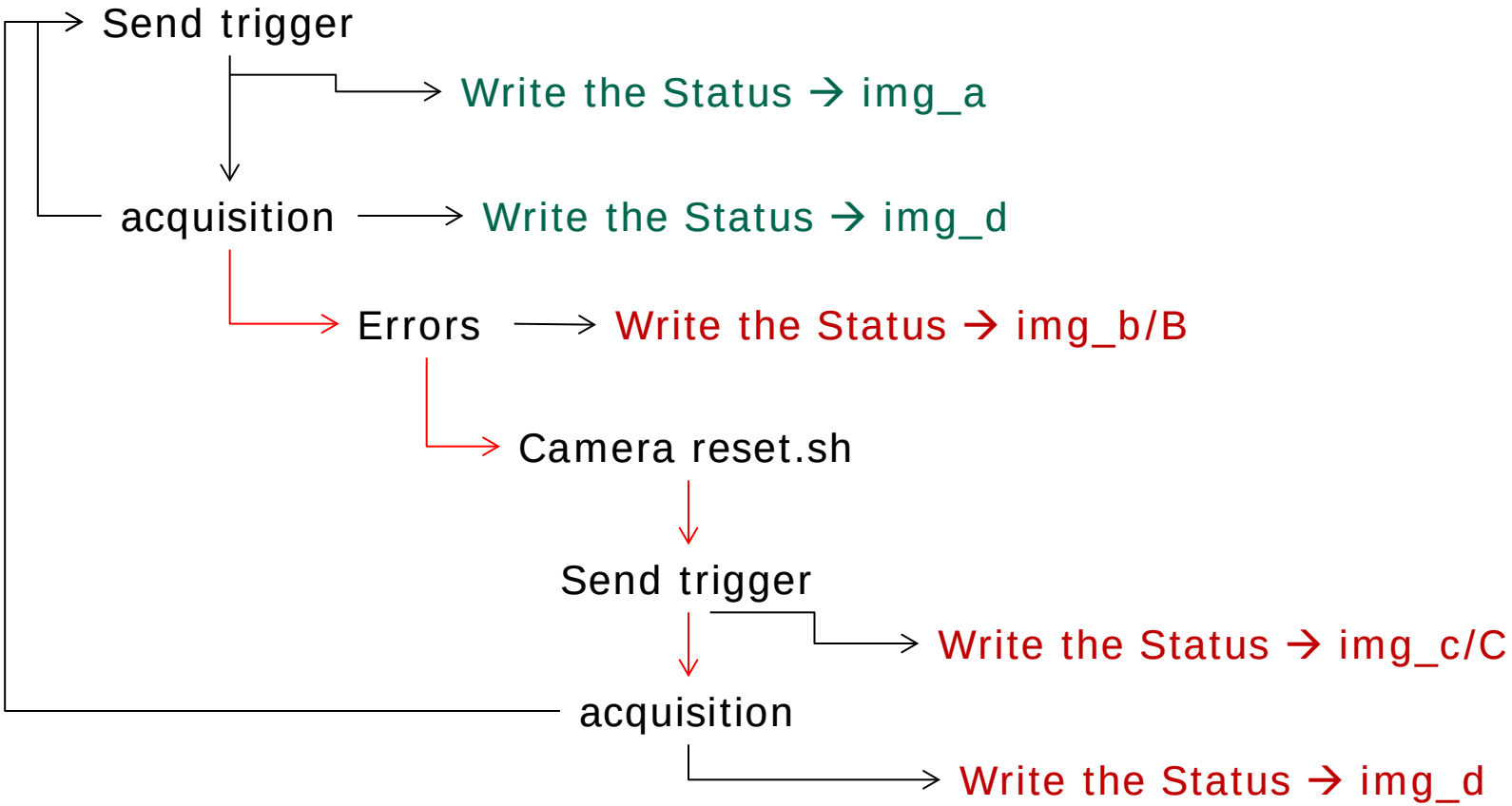
FSM Stimuli ➔ Here you can find if the trigger has been accepted by the camera and under-processing

FSM_Stimuli	
FSM_Stimuli_idle	= 4'h0;
FSM_Stimuli_check_num_trig	= 4'h1;
FSM_Stimuli_check_for_ex_trigger	= 4'h2;
FSM_Stimuli_counting_time	= 4'h3;
FSM_Stimuli_check_busy	= 4'h4;
FSM_Stimuli_check_new_frame_req	= 4'h5;
FSM_Stimuli_generate_end_of_all_FR	= 4'h6;
FSM_Stimuli_wait_all_done	= 4'h7;
FSM_Stimuli_wait_until_readout_start	= 4'h8;
FSM_Stimuli_wait_until_readout_finished	= 4'h9;

Status and Errors – feedback

Test procedure

1000 frames acquired with external edge-trigger configuration



Status and Errors – feedback (II)

Img_a004 files: S_1 = 8449ffff, S_2 = 40003001 and S_3 = 80000000

Readout FSMs =OK

Camera in Busy^, Camera wait for readout → still during the integration time

Img_d004 files: S_1 = 8449ffff, S_2 = 00003001 and S_3 = 00000000

NO ERRORs

Case of TANGO HW-timeout, errors 005, 234, 381, 390 …

Img_b005 files: S_1 = 8449ffff, S_2 = 00003001 and S_3 = 00000000

NO ERRORs

Img_a005 files: S_1 = 8449ffff, S_2 = 00003001 and S_3 = 00000000

NO trigger sent !!!!

Img_c005 files: S_1 = 8449ffff, S_2 = 40003001 and S_3 = 80000000

trigger received

Img_d005 files: S_1 = 8449ffff, S_2 = 00003001 and S_3 = 00000000

NO ERRORs

No errors, seems no data because no trigger !!!!!!

Status and Errors – B_896, 904, 928, 953

Case of TANGO SW-timeout

Img_a896 files: S_1 = 8449ffff, S_2 = 40003001 and S_3 = 80000405

Readout FSMs =OK

DDR filling to be check

Camera in Busy (because processing a trigger)

Camera wait for readout → still during the integration time

Img_b896 files: S_1 = 8449ffff, S_2 = 00003001 and S_3 = 00000000

User bank register

9050	8449ffff	00003001	00000000	00000000
9060:	00000000	00000000	00000000	00000000
9070:	00000000	00000000	00000000	00000000
9080:	00000000	00000000	00000000	00000000
9090:	00000000	00000000	00000000	00000000
90a0:	00000000	00000000	00000000	00000000
90b0:	00000000	00000000	00000000	00000000
90c0:	00000000	00000000	00000000	00000000
90d0:	00000000	00000000	00000000	00000000
90e0:	00000000	00000000	00000000	00000000

Camera completely reset ….

Should be in readout ?

How is it possible ?

Cont'd

Status and Errors – B_896, 904, 928, 953

Img_c896 files: S_1 = 8449ffff, S_2 = 40003001 and S_3 = 80000000

trigger received

Img_d896 files: S_1 = 8449ffff, S_2 = 07fd4001 and S_3 = 00000000

No errors, just the data are not full transferred to PC because **PC not ready**

Status and Errors – B_949

Case of TANGO SW-timeout

Img_a949

```
9050:     8449ffff  40003001   80000000  00000000
9060:  00000000  00000000   00000000  00000000
```

Trigger received

Img_b949

```
9050:  8449ffff     00003001   00000000  00000000
9060:  00000001  00000000   50f00000  00000000
```

One error in the data

Img_d949

```
9050    8449ffff     00003001   00000000  00000000
9060:  00000002  00000000   50f00000  00000000
```

Got same error

Next Run number # 950 → OK

Status and Errors – B_988

Case of TANGO SW-timeout

Img_a988

```
9050:  8449ffff  40003001  80000000  00000000
9060:  00000000  00000000  00000000  00000000
9070:  122d3000  122d3000  122d5000  122d3000
```

Trigger received

Img_B988

```
9050:  8449ffff  00003001  00000000  00000000
9060:  00000000  00000000  00000000  00000000
9070:  14864000  14864000  14866000  14864000
```

NO errors

Readout DONE

Img_C988

```
9050:  8449ffff  40003001  80000000  00000000
9060:  00000000  00000000  00000000  00000000
9070:  14864000  14864000  14866000  14864000
```

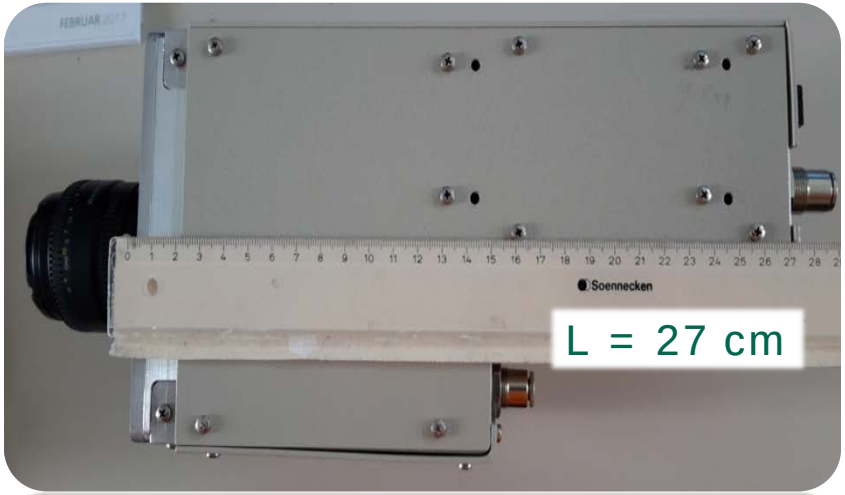
New trigger received

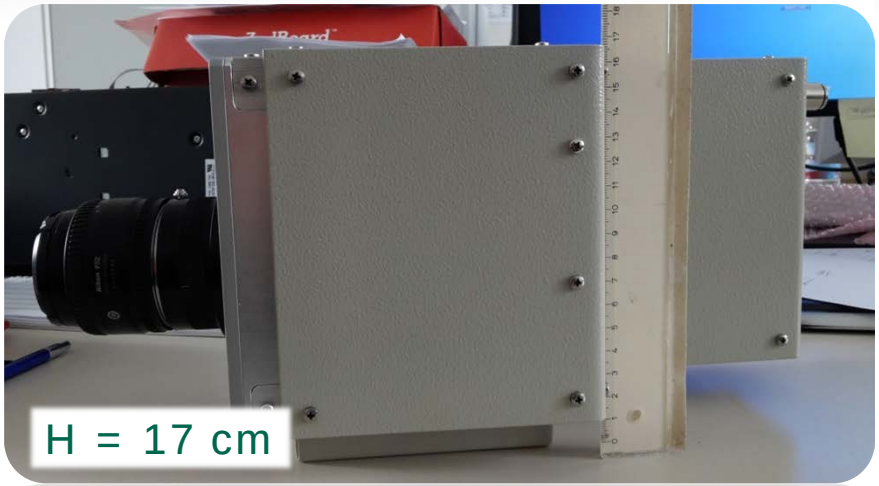
Img_d988

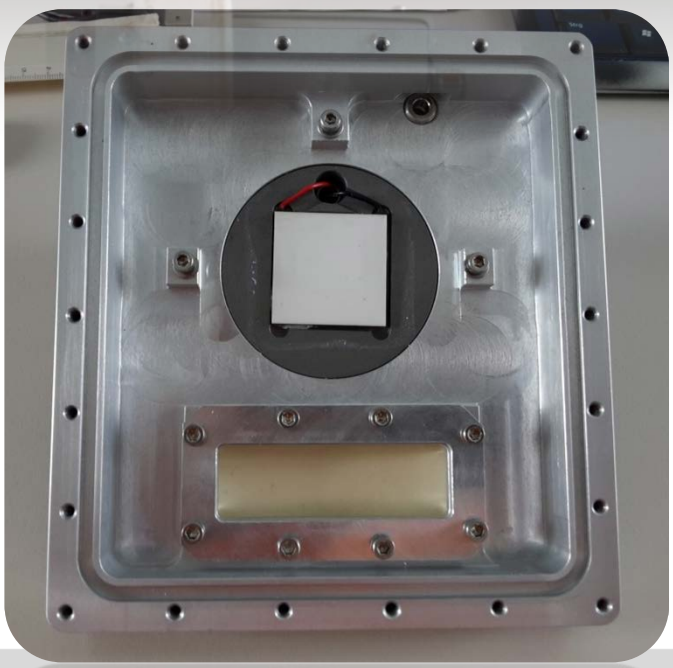
```
9050:  8449ffff  00003001  00000000  00000000
9060:  00000000  00000000  00000000  00000000
9070:  14864000  14864000  14866000  14864000
```

NO READOUT

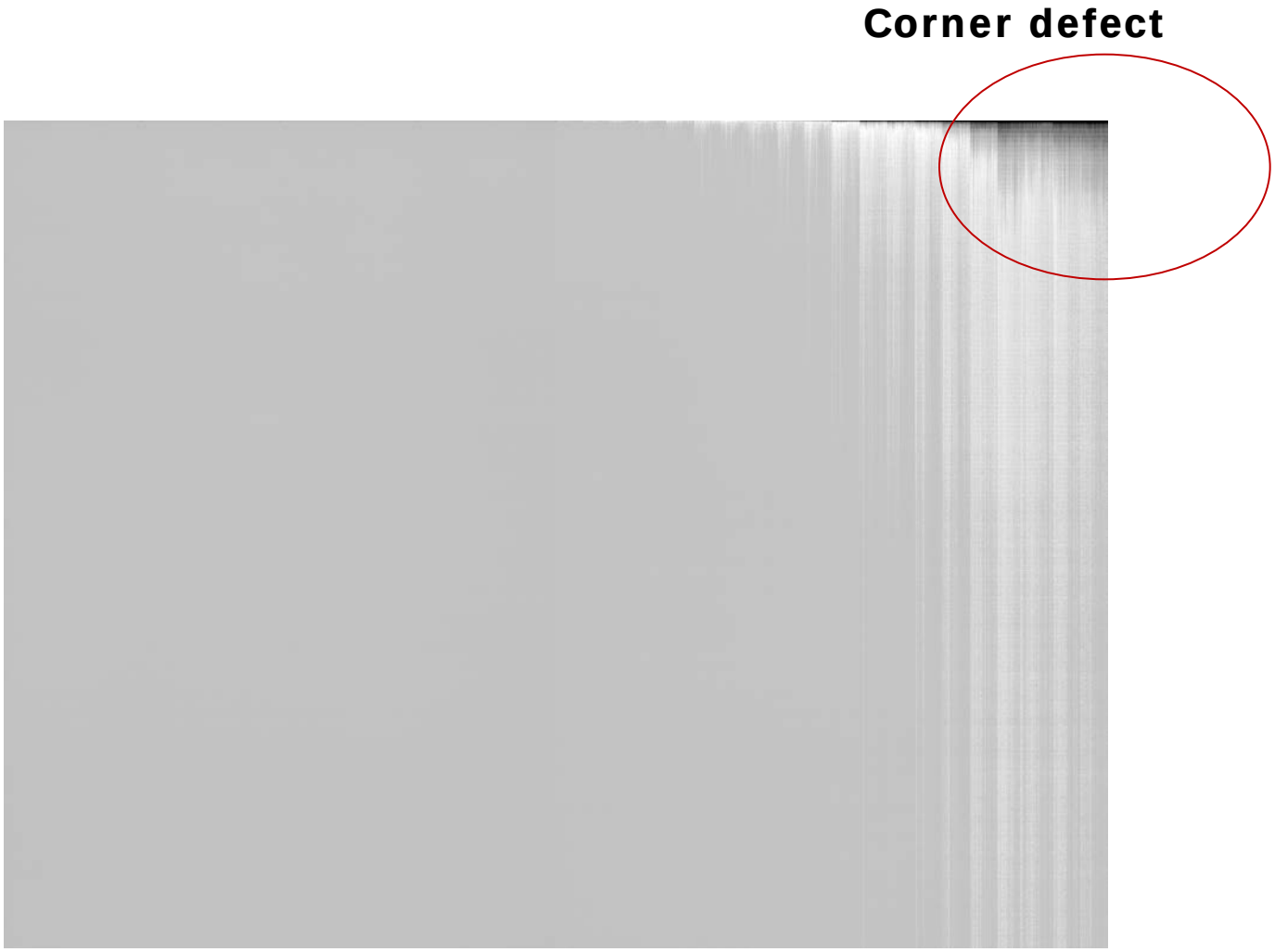
IPE-Camera







Current 20Mpix – FMC



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Thank you for your attention