

AMSTRAD CPC / CRTC 1

SHAKER V1.8 OUTPUT

LOGON SYSTEM 2021 / LONGSHOT

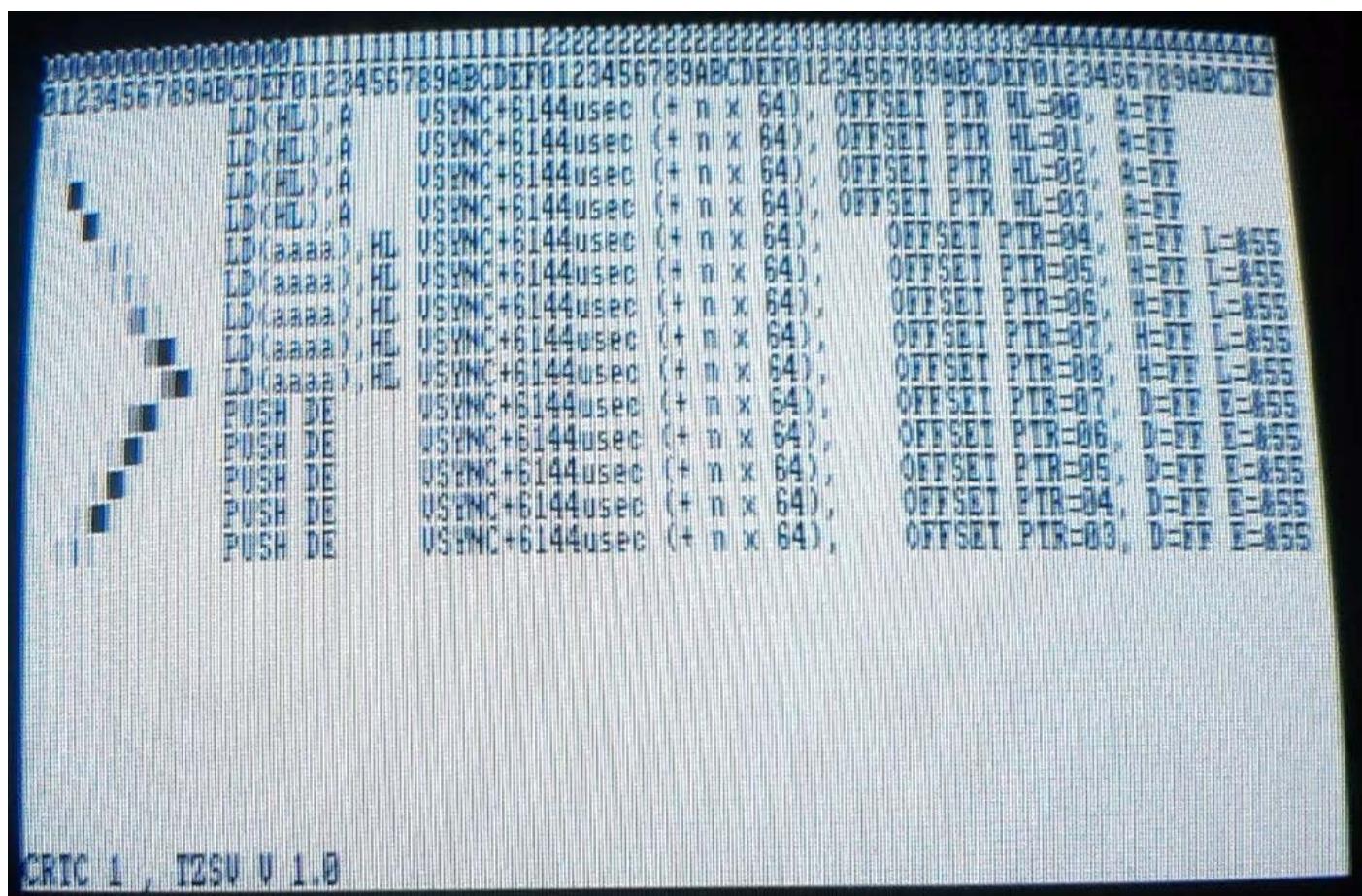
More information about CRTC in Amstrad Cpc Crtc Compendium
("con de chat canadien")

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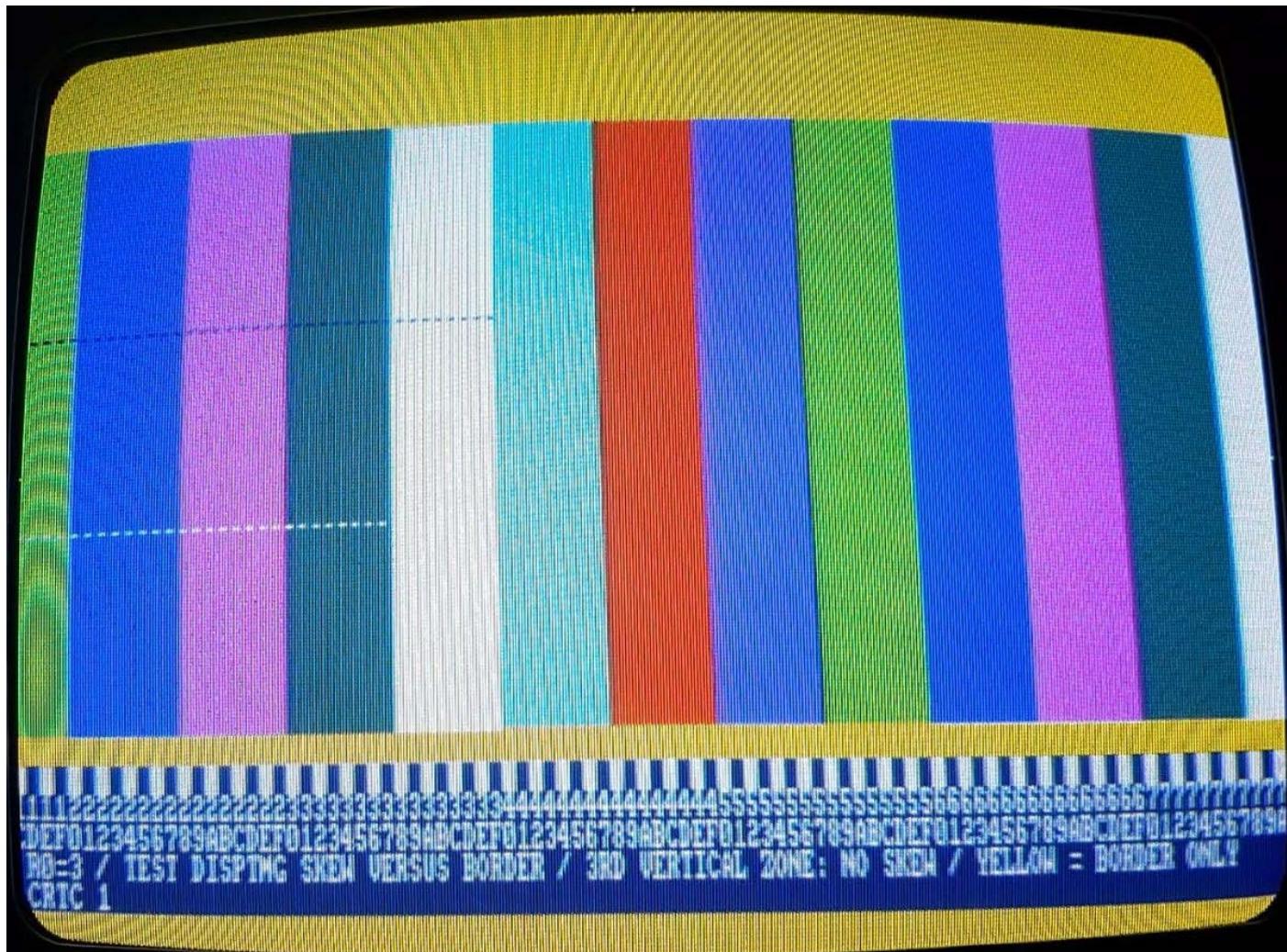
UPDATE VRAM VS CRTC

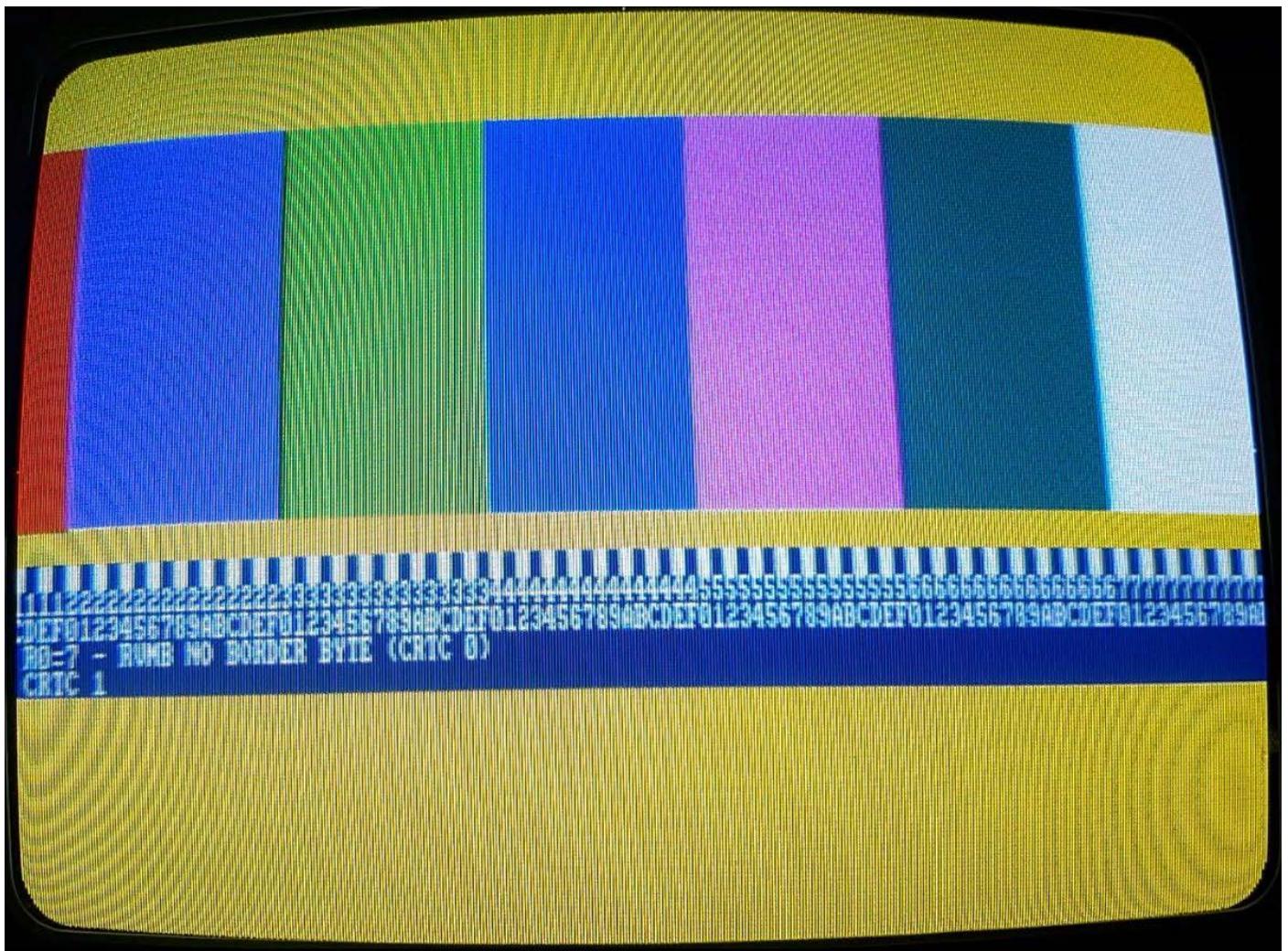
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST) (0) CRTC 2 RUMB
(2) SKEW DISP ON R0 RUPTURE (5 TST) (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC) (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!



SKEW DISP ON R0 RUPTURE

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM US CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
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(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
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(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
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(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC USYNC FROM PPI.PORTB.0=1 !!





INTERRUPT DELAY FROM R2

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE URAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
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(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT < CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```

```
DELAY BETWEEN SEND (ODER2) AND INTERRUPTION (INT)
WHEN R3=00, INTERRUPT OCCURS #0F USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=00, INTERRUPT OCCURS #0E USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=0C, INTERRUPT OCCURS #0D USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=0B, INTERRUPT OCCURS #0C USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=0A, INTERRUPT OCCURS #0B USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=09, INTERRUPT OCCURS #0A USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=08, INTERRUPT OCCURS #09 USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=07, INTERRUPT OCCURS #08 USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=06, INTERRUPT OCCURS #07 USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=05, INTERRUPT OCCURS #06 USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=04, INTERRUPT OCCURS #05 USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=03, INTERRUPT OCCURS #04 USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=02, INTERRUPT OCCURS #03 USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=01, INTERRUPT OCCURS #02 USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=00, INTERRUPT OCCURS #FF USEC AFTER CB=R2 (#FF=NO INT)
```

VSYNC DURATION (S=8180 ON CRT 0,3,4)(B=8480 ALL CRT / n=8480 CRT 1,2)
B3 High=6)) SIZE=80400 uSEC
B3 High=0)) SIZE=80400 uSEC

DELAY OF 'CALL TO #38' ON INTERRUPTION IS 05 uSEC (RST#38=4 uSEC)

CRTC 1

DELAY BETWEEN HSYNC (CODE R2) AND INTERRUPTION (IM2)

WHEN R3=0E, INTERRUPT OCCURS #0F USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=0D, INTERRUPT OCCURS #0E USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=0C, INTERRUPT OCCURS #0D USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=0B, INTERRUPT OCCURS #0C USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=0A, INTERRUPT OCCURS #0B USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=09, INTERRUPT OCCURS #0A USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=08, INTERRUPT OCCURS #09 USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=07, INTERRUPT OCCURS #08 USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=06, INTERRUPT OCCURS #07 USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=05, INTERRUPT OCCURS #06 USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=04, INTERRUPT OCCURS #05 USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=03, INTERRUPT OCCURS #04 USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=02, INTERRUPT OCCURS #03 USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=01, INTERRUPT OCCURS #02 USEC AFTER CB=R2 (#FF=NO INT)
WHEN R3=00, INTERRUPT OCCURS #FF USEC AFTER CB=R2 (#FF=NO INT)

HORIZONTAL SYNC DURATION (S=8180 ON CRT 0,3,4)(B=8400 ALL CRT / n=8400 CRT 1,2)

R3 High=0)) SIZE=80400 USEC

R3 High=1)) SIZE=80400 USEC

DELAY OF INTERRUPTION CALL (IM2) IS 07 USEC

CRTC 1

UPDATE CRTC R0 TIMING

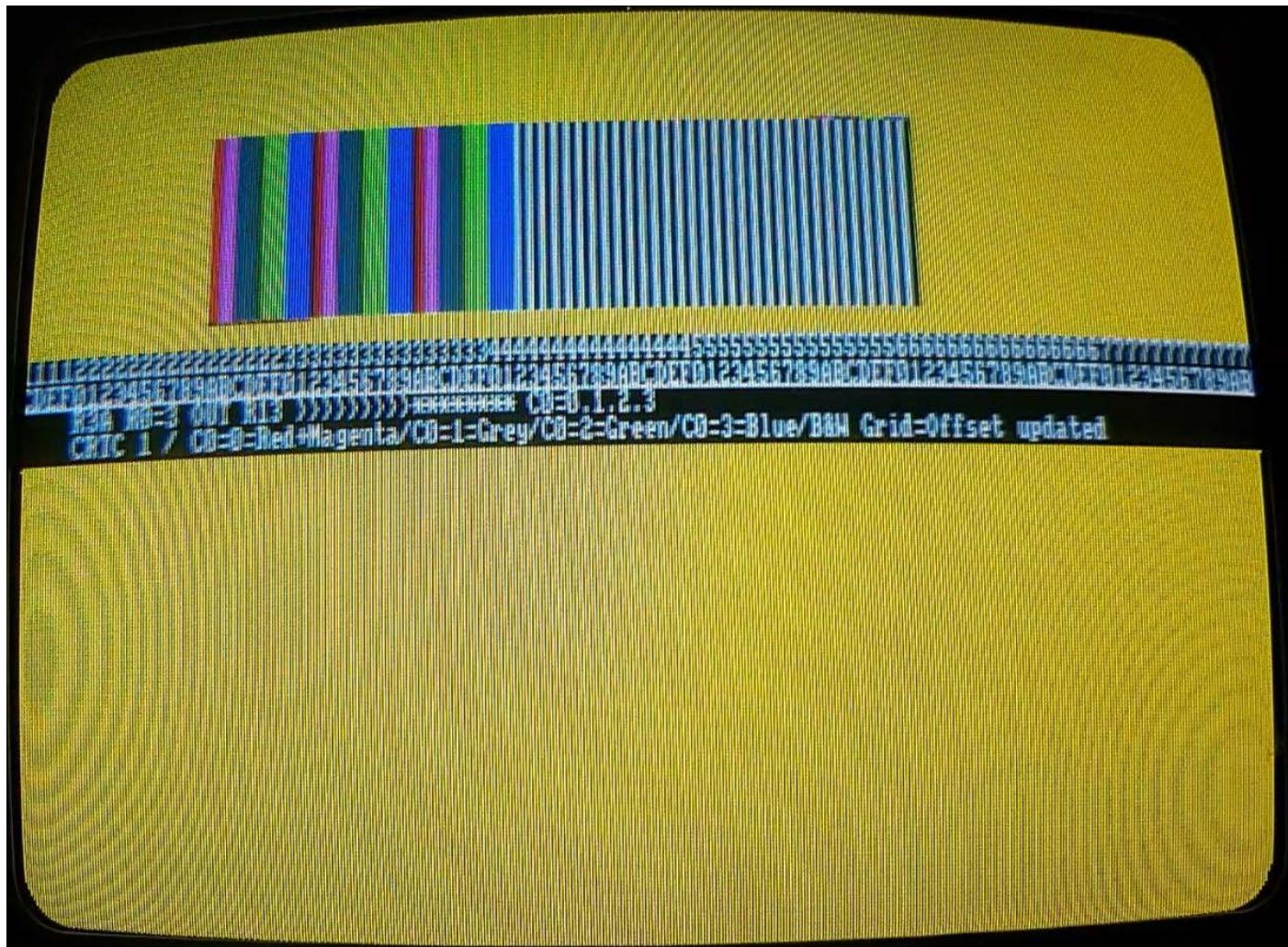
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CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
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(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD_UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
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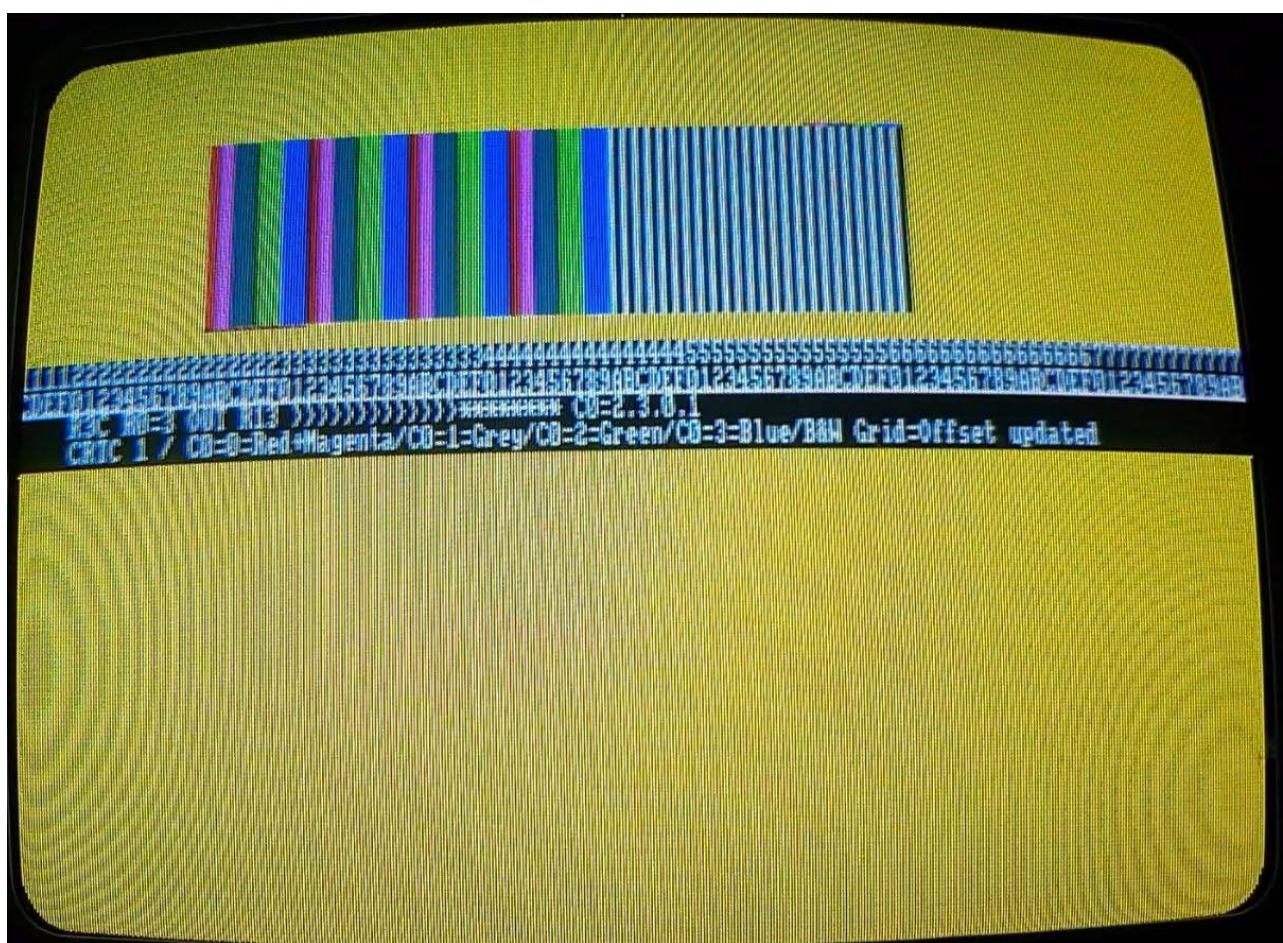
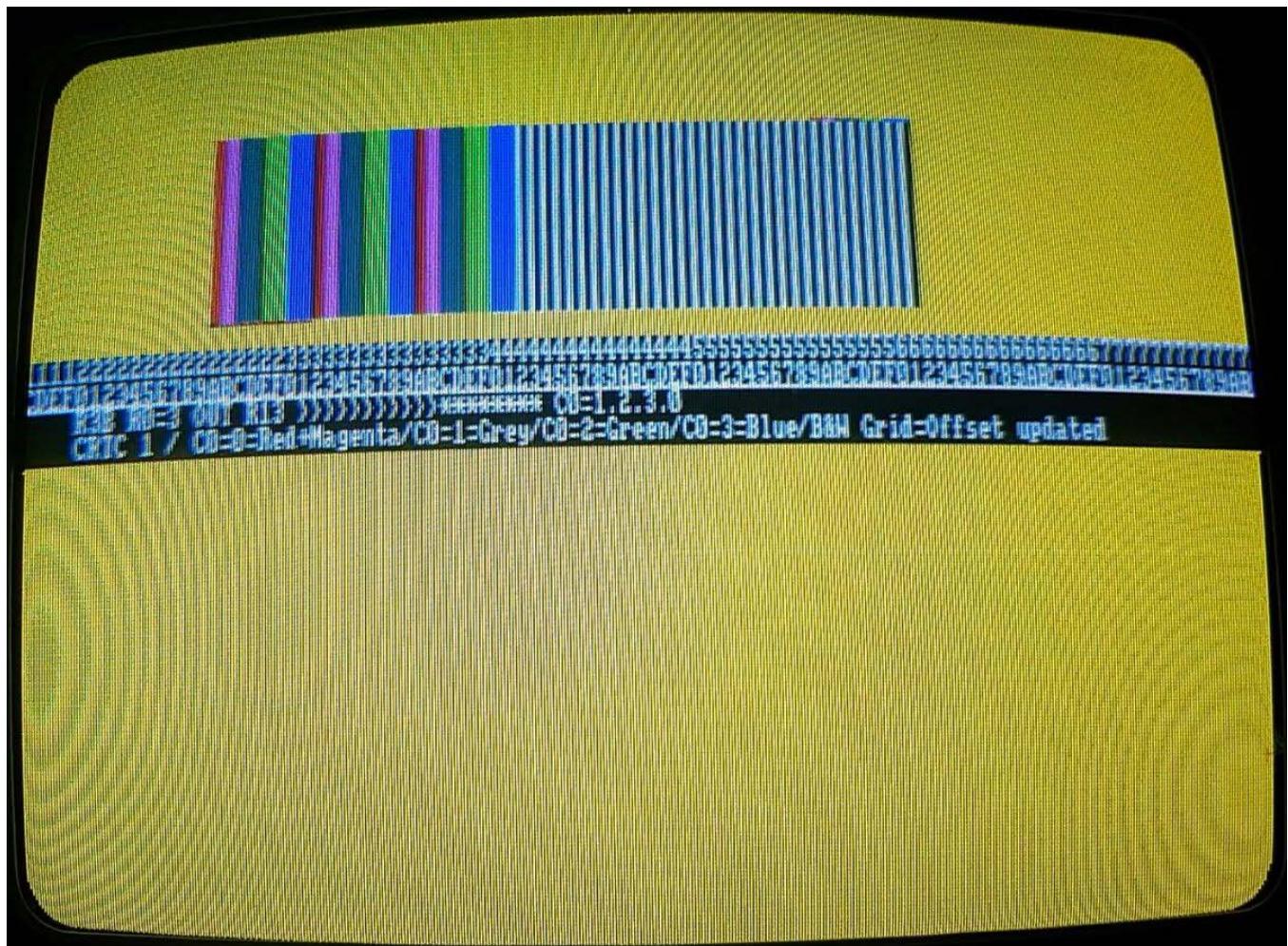
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00-0F / CRTC 10 ON R0 (01)(C) C
01: CB=..0F, AB=..41.. / X0: 00=..3F..00..01..
UPDATE R0=0F, OUT OM H0C=3F :OK
UPDATE R0=0F, OUT OM H0C=3E :OK
UPDATE R0=0F, OUT OM H0C=3D :OK
UPDATE R0=0F, OUT OM H0C=3C :OK
UPDATE R0=0F, OUT OM H0C=3B :OK
UPDATE R0=0F, OUT OM H0C=3A :NO
UPDATE R0=0F, OUT OM H0C=39 :NO
UPDATE R0=0F, OUT OM H0C=38 :NO
OUTI OM C0vs=#3c:01 (01:IO ON 5TH MOP / 00:IO ON 4TH MOP)
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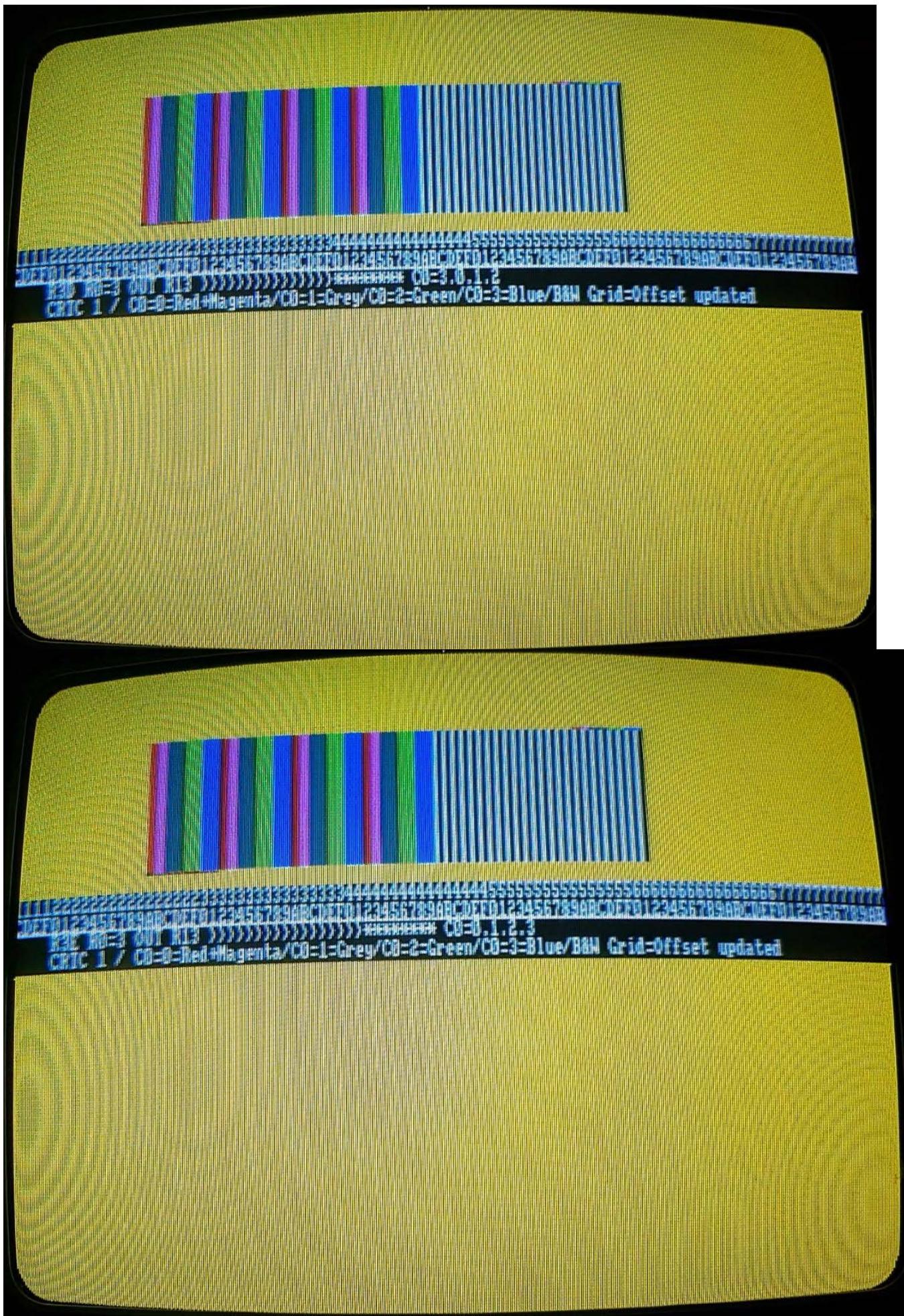
CRTC 1

R13 UPDATE IN 4 USEC SCREENS (R0=3)

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CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
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(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD_UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
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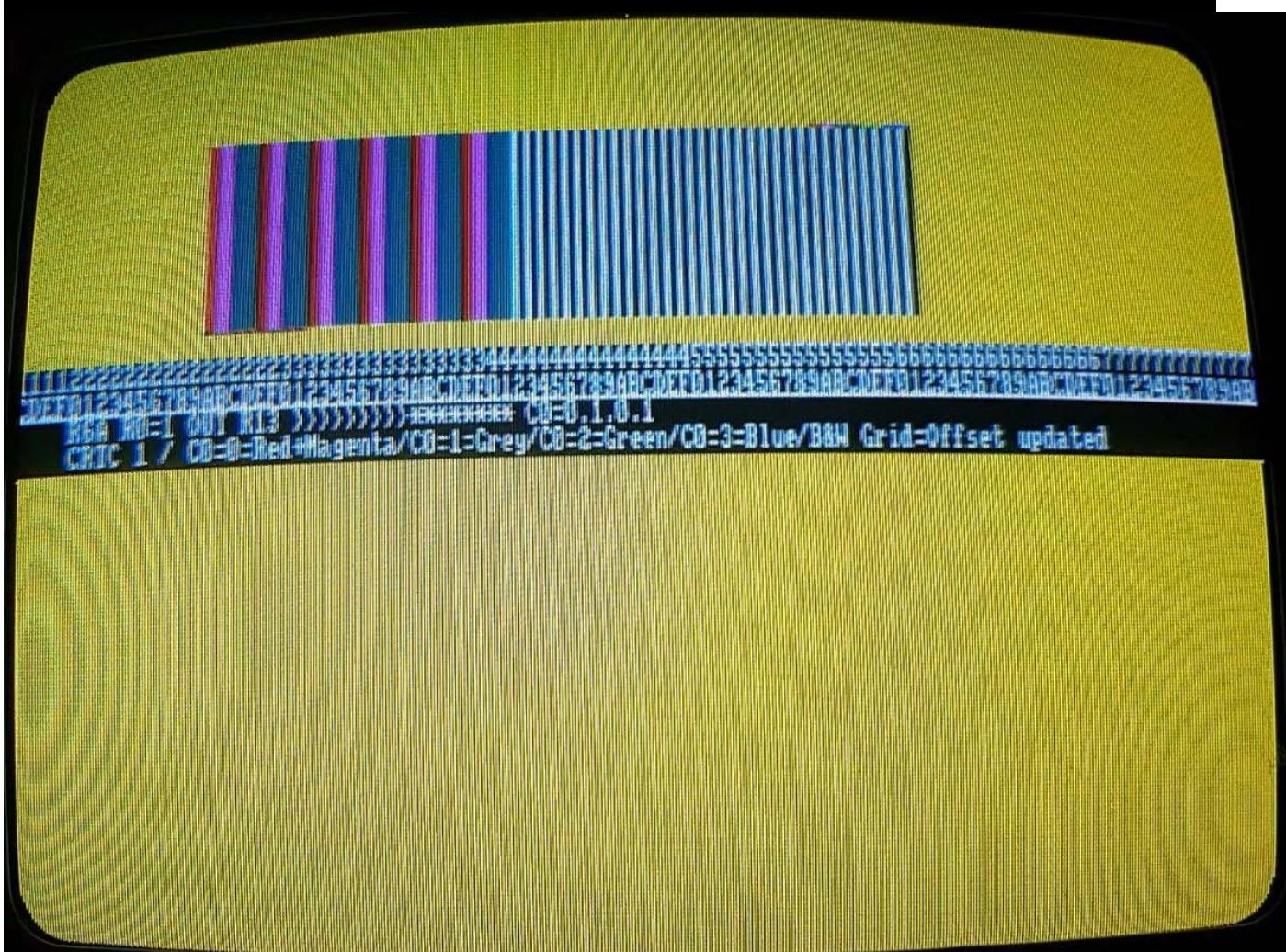


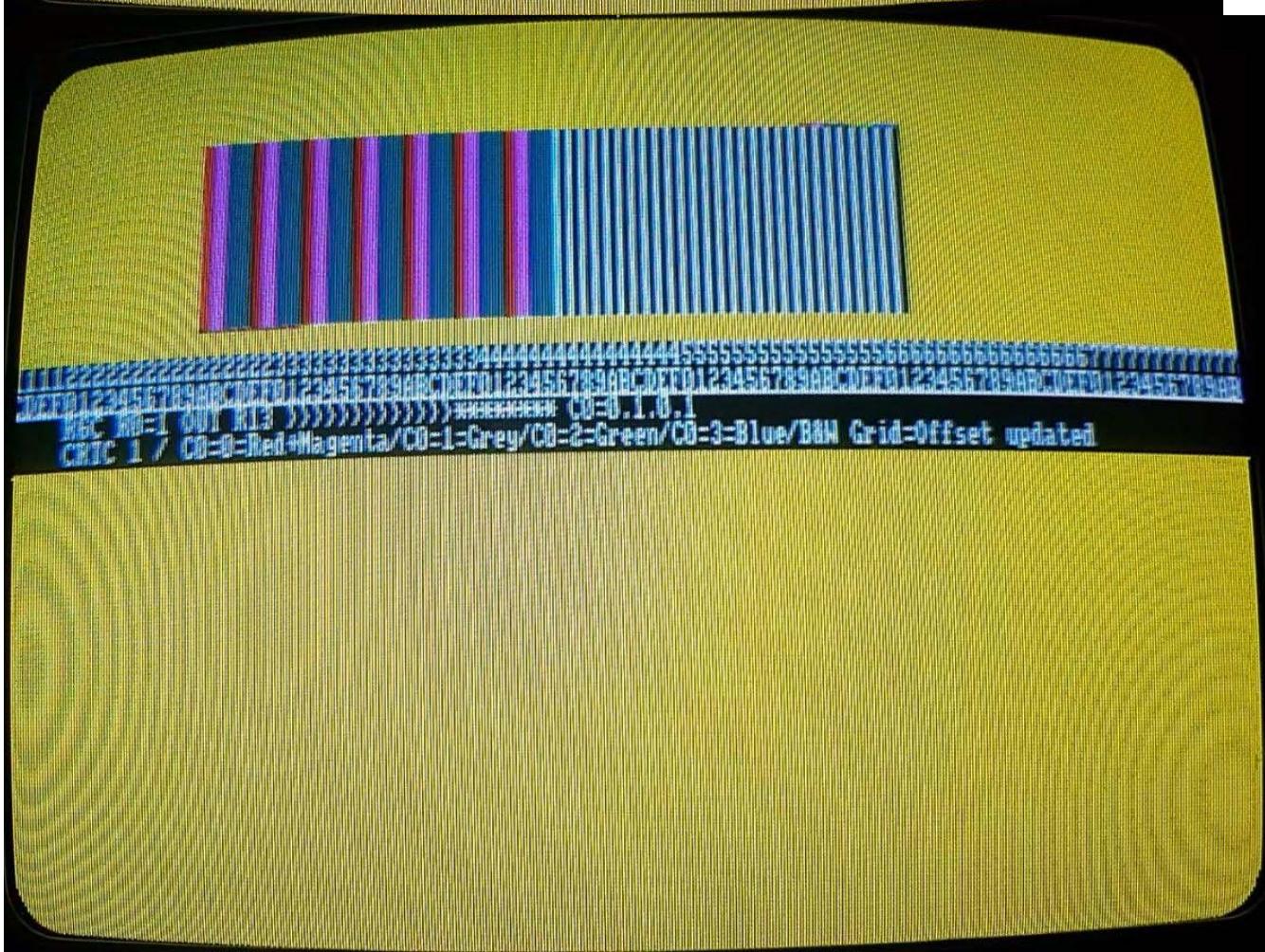
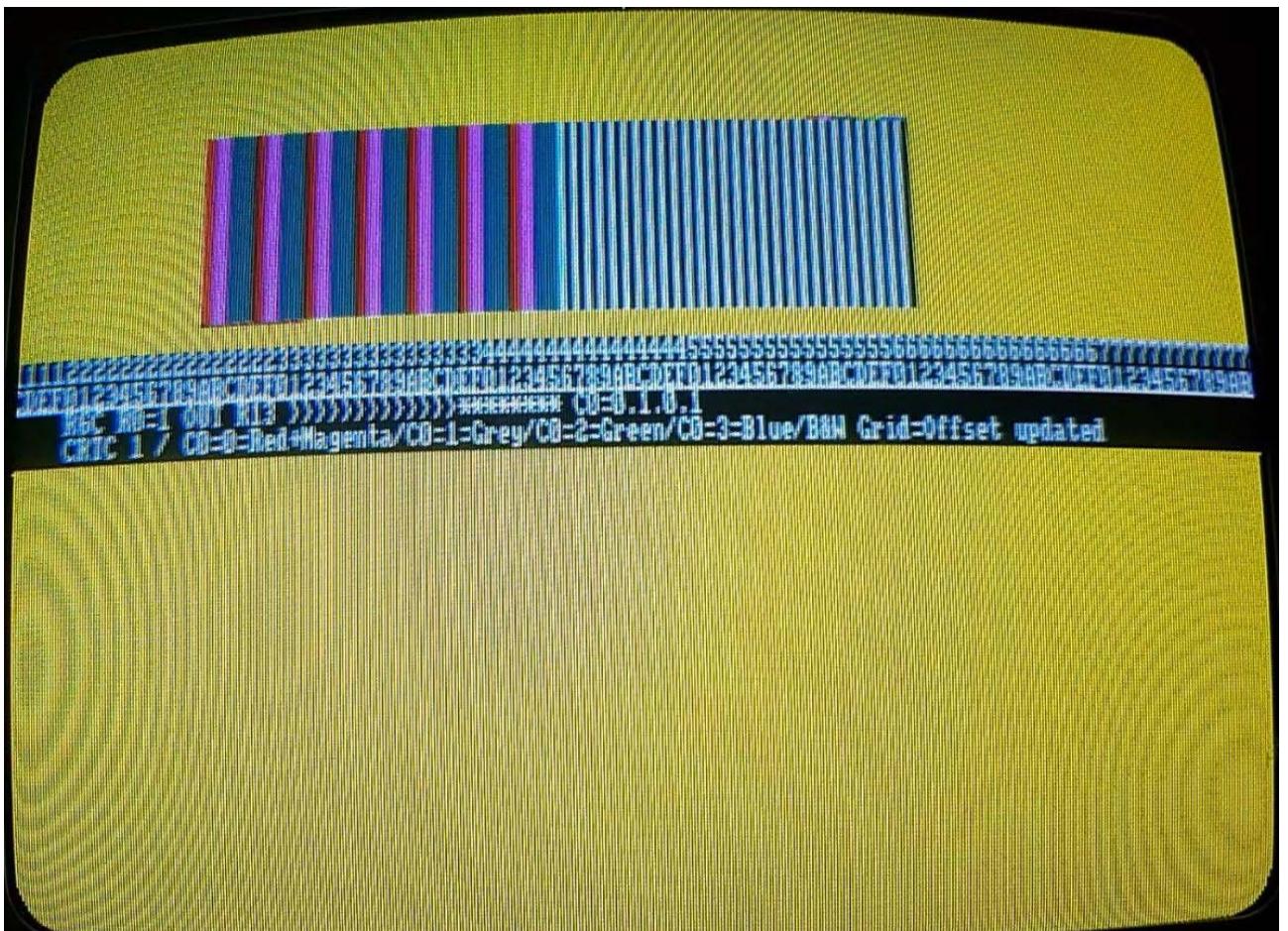


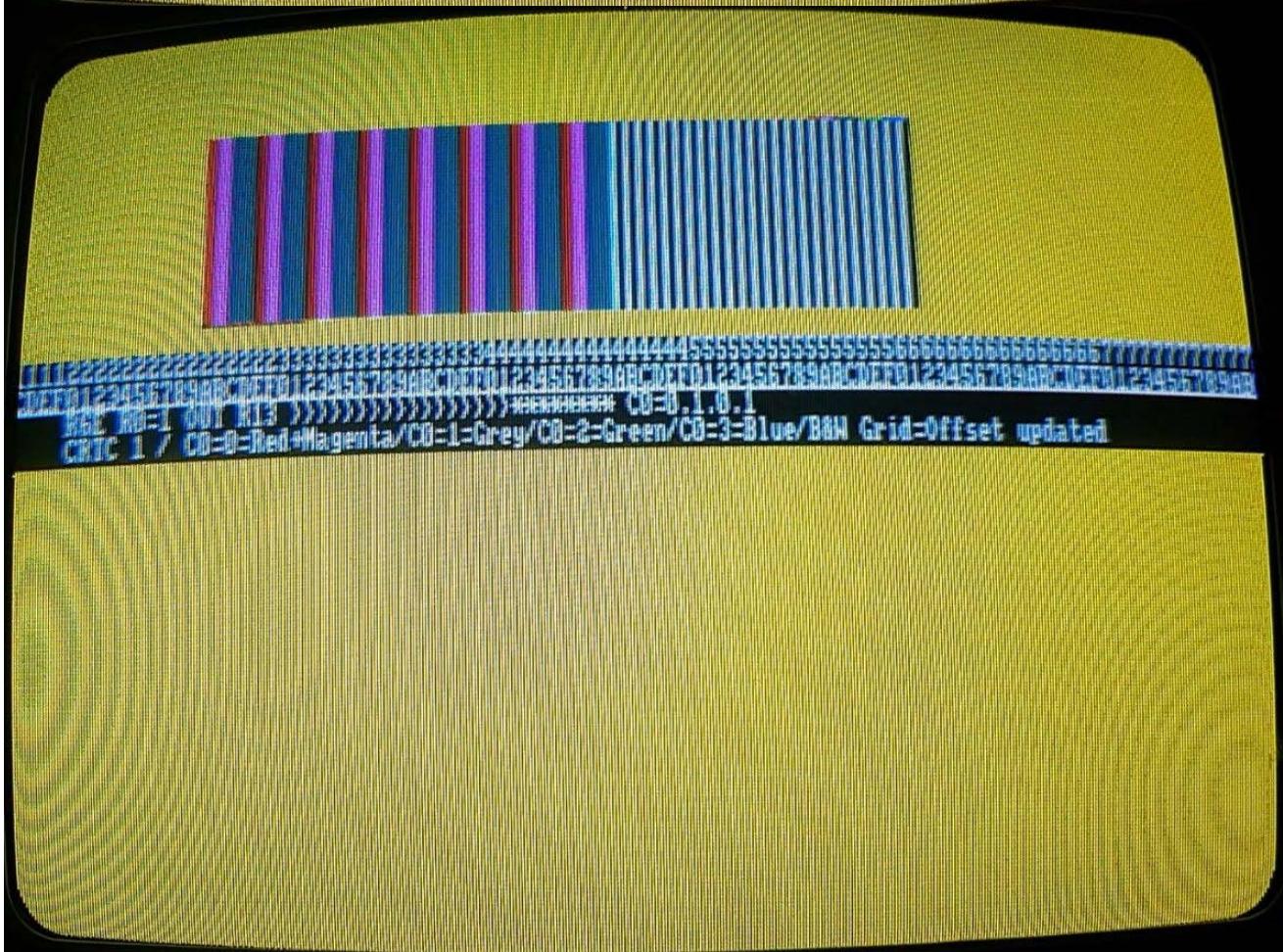
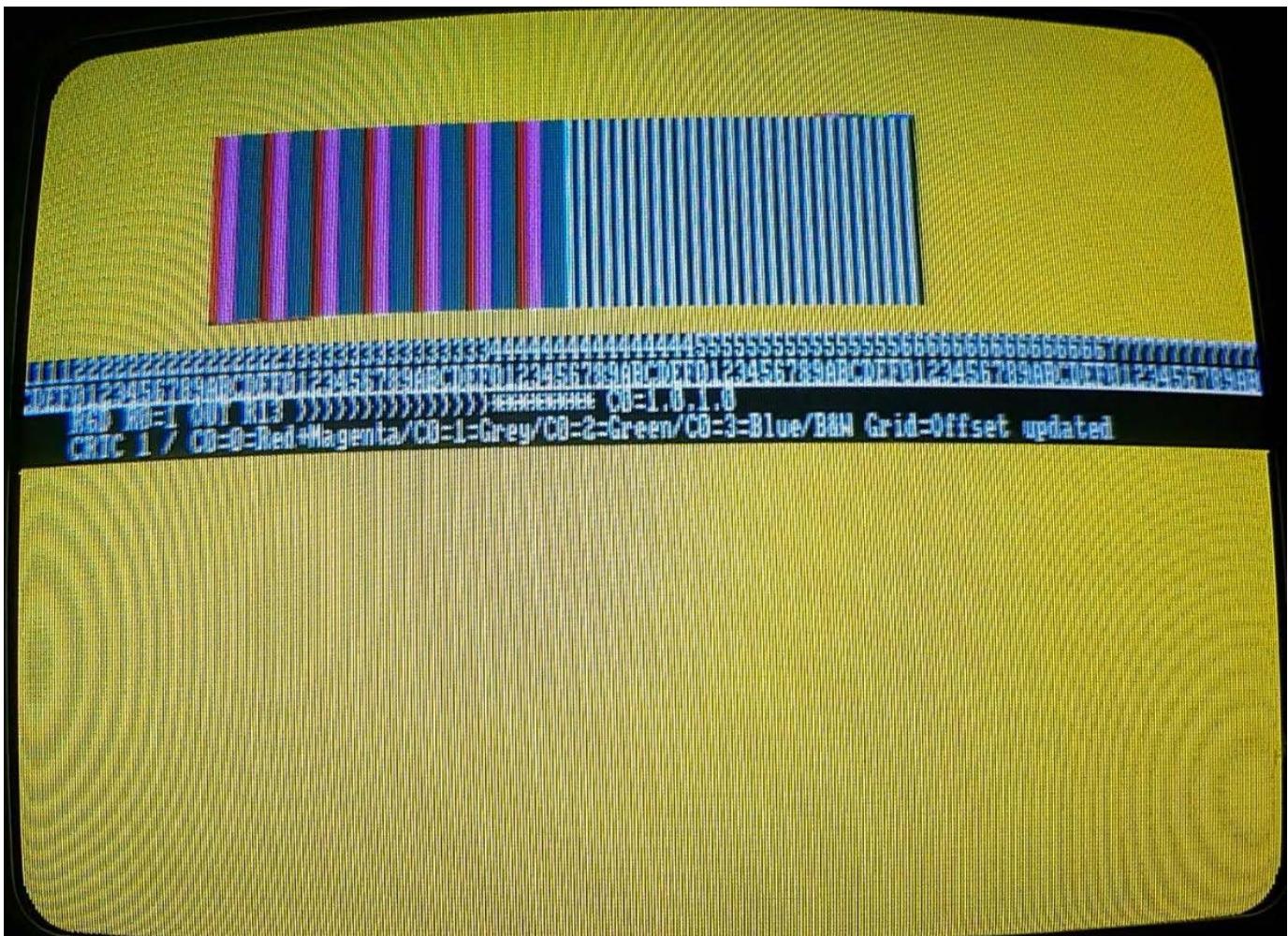


R13 UPDATE IN 2 USEC SCREENS (R0=1)

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD, UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!

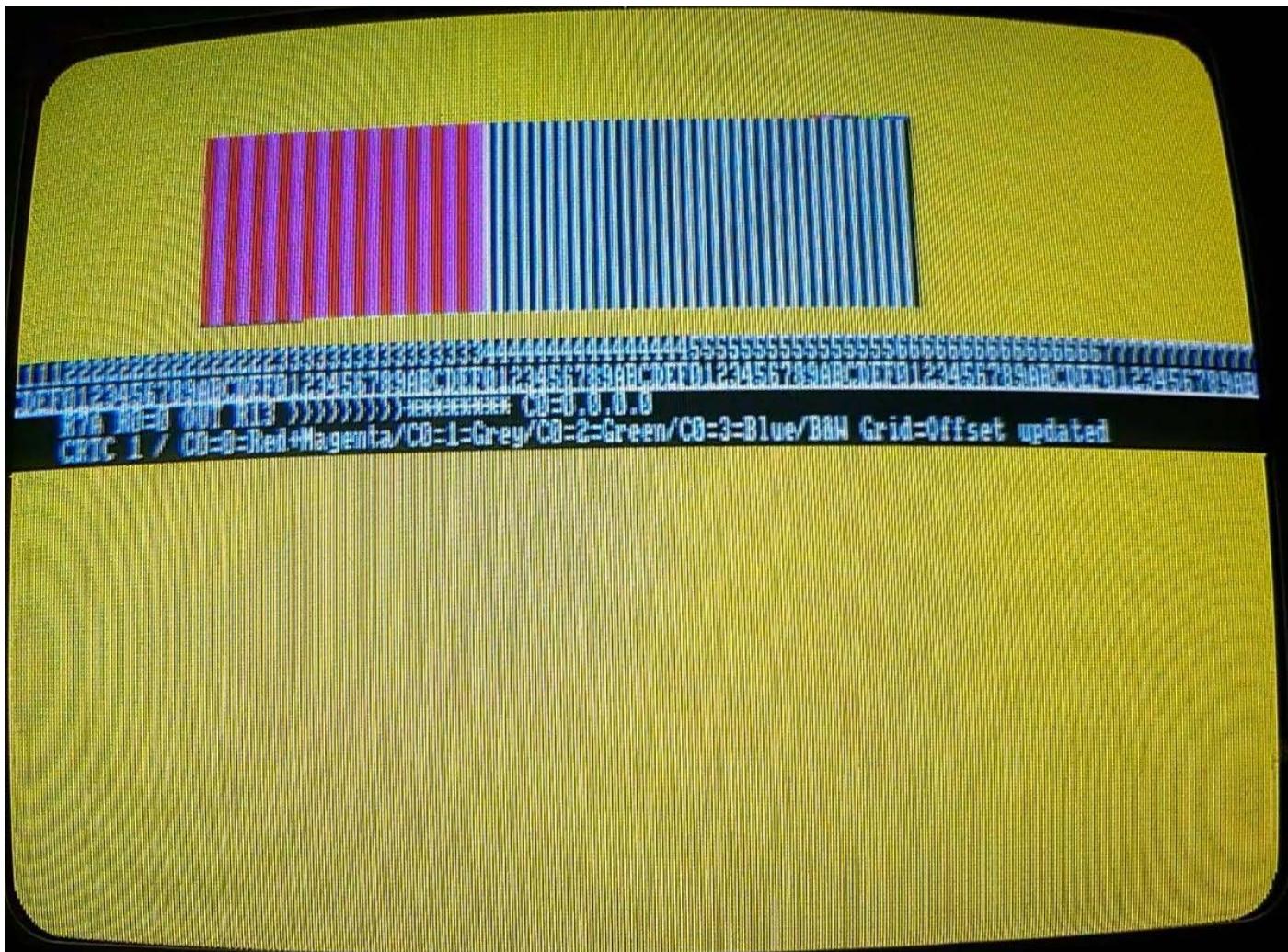


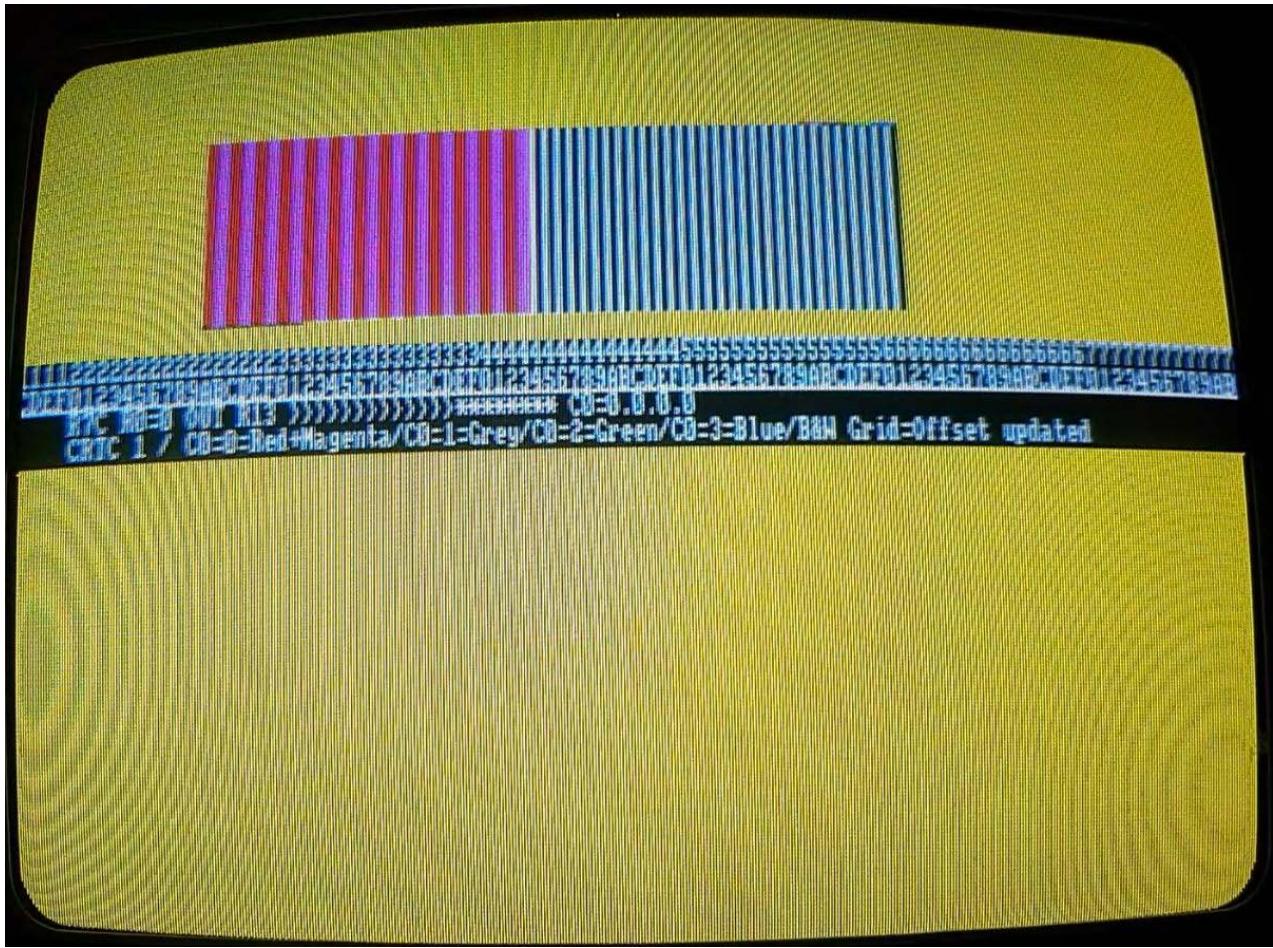
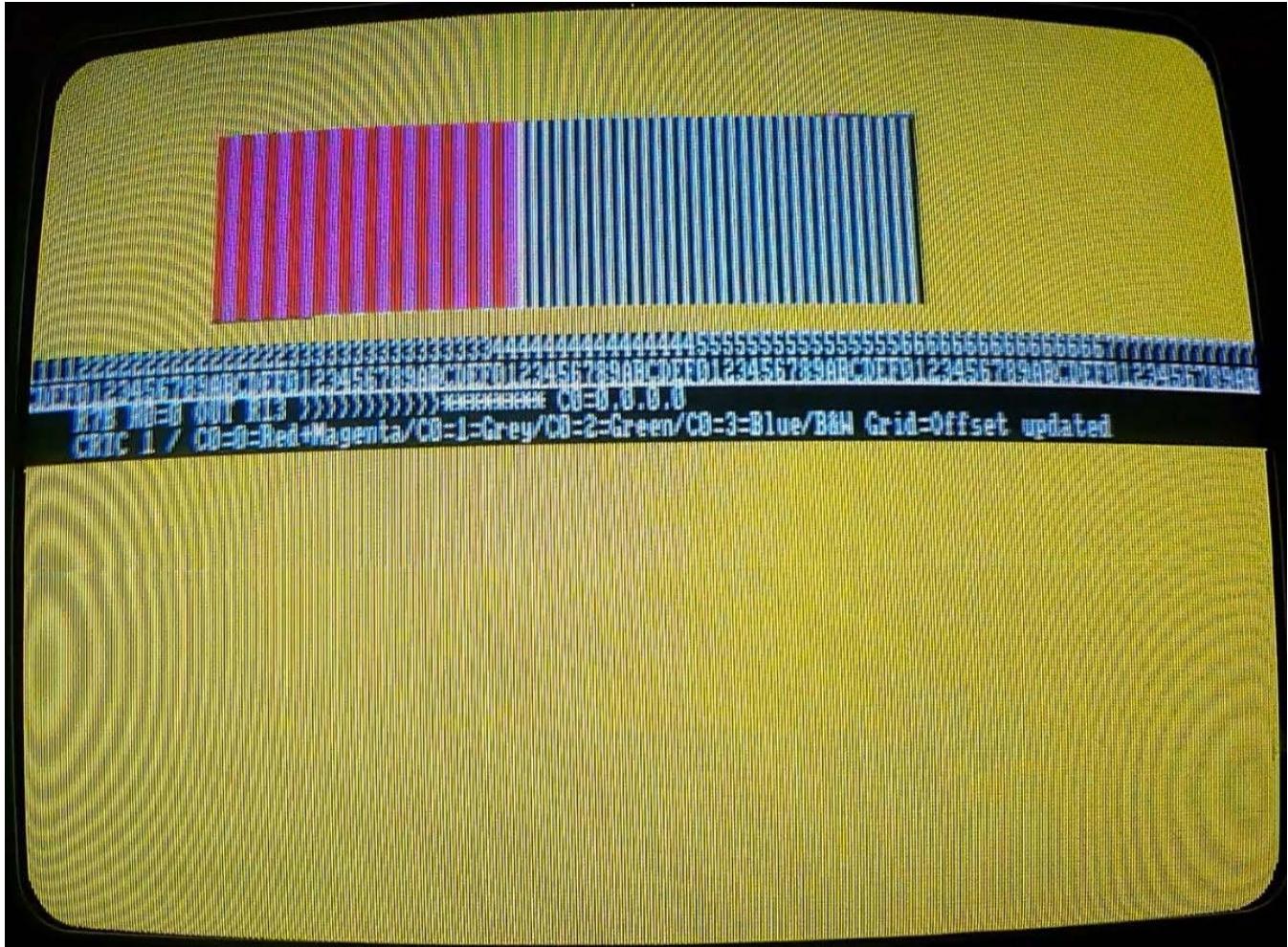


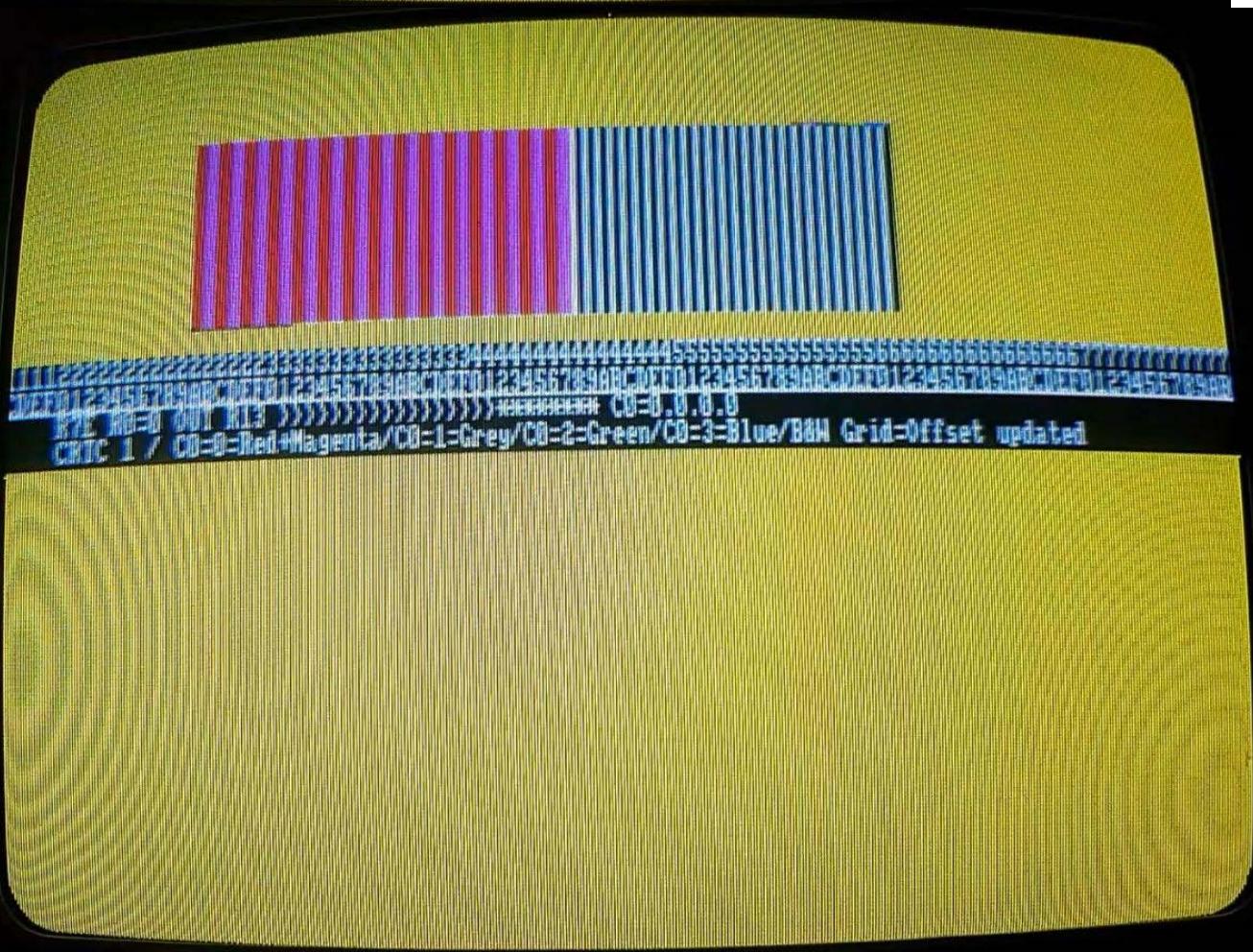
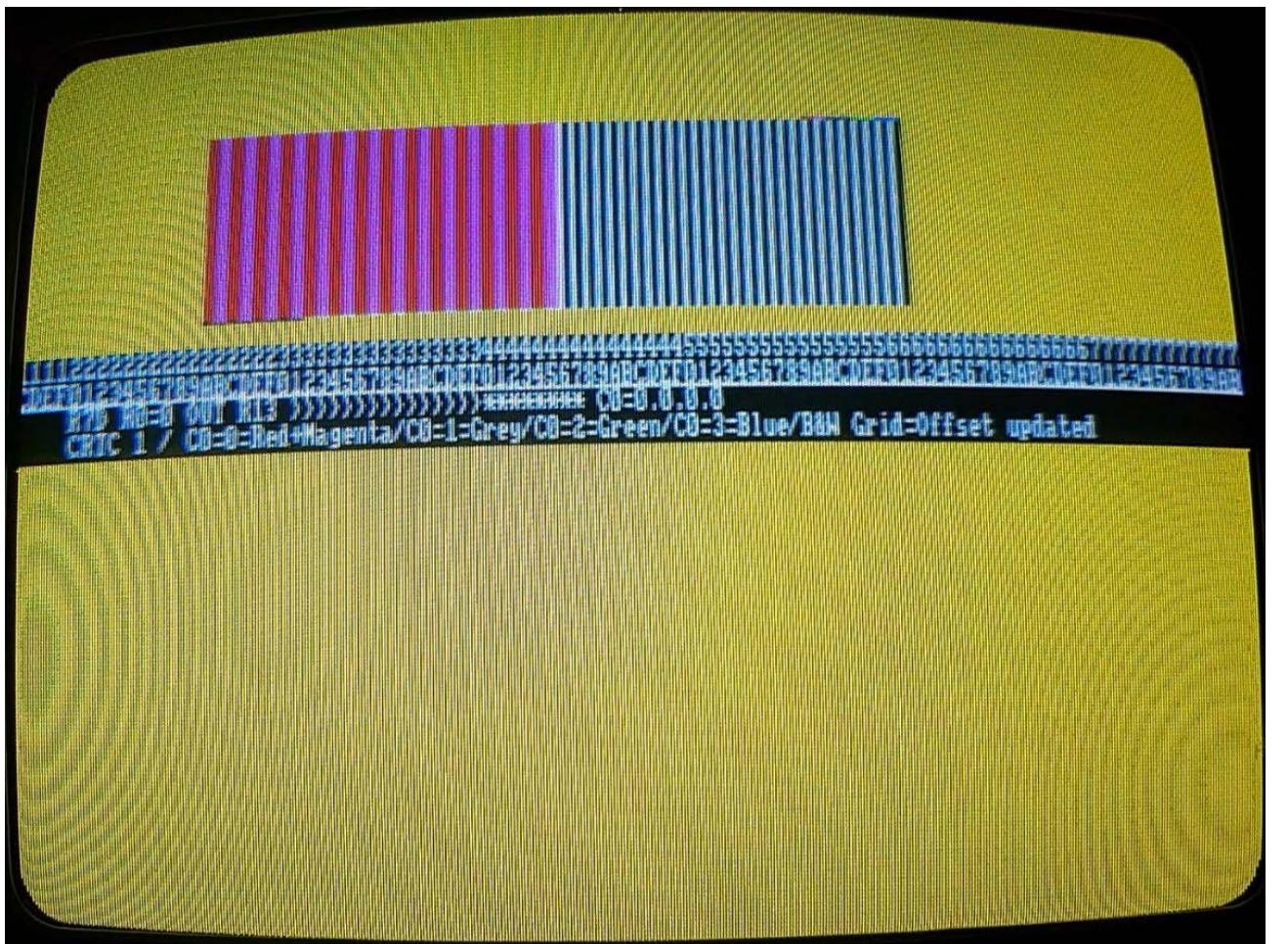


R13 UPDATE IN 1 USEC SCREENS (R0=0)

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST) (0) CRTC 2 RUMB
(2) SKEW DISP ON R0 RUPTURE (5 TST) (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC) (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
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(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
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(I) VSYNC CONDITIONS (16 TST)
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(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!

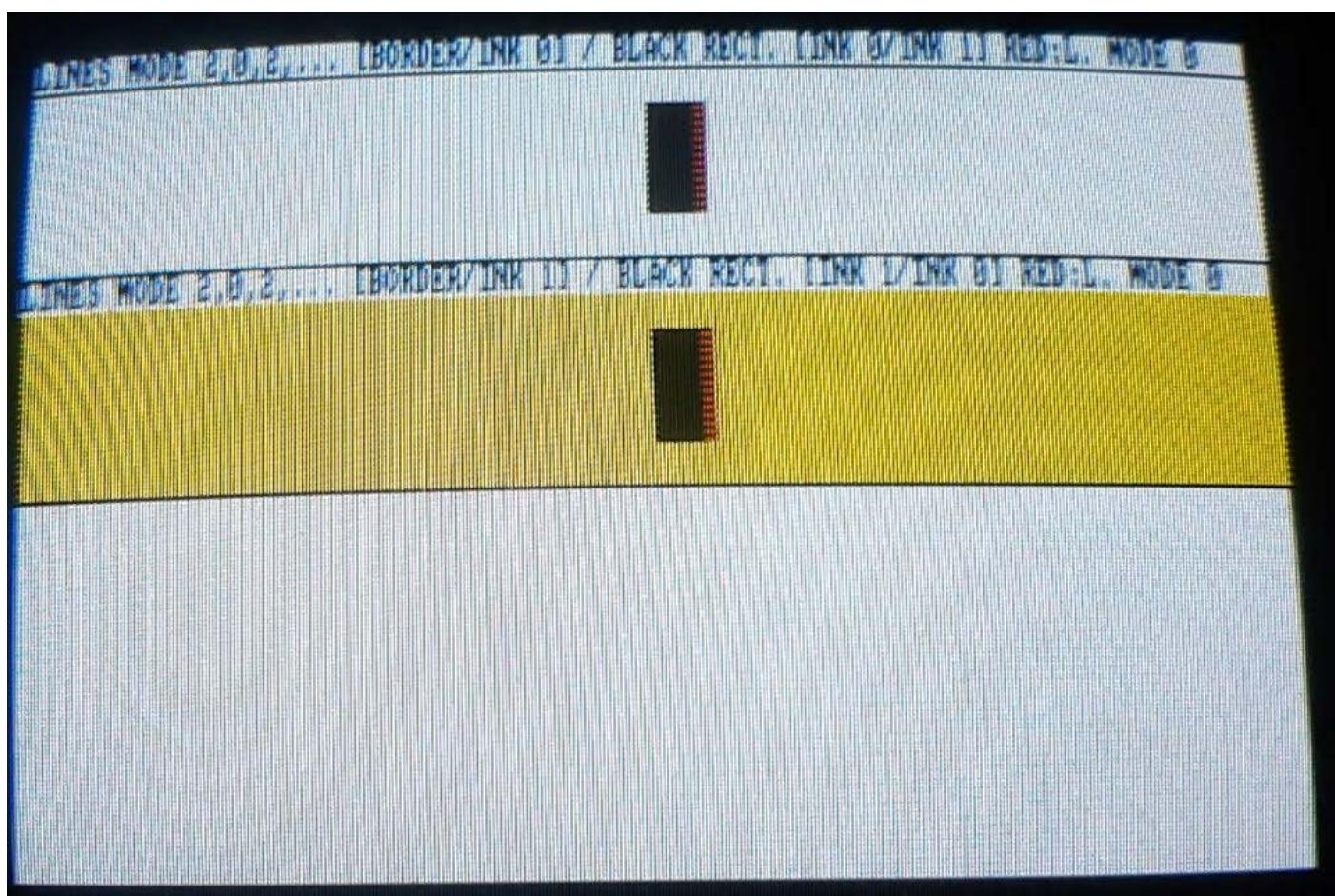






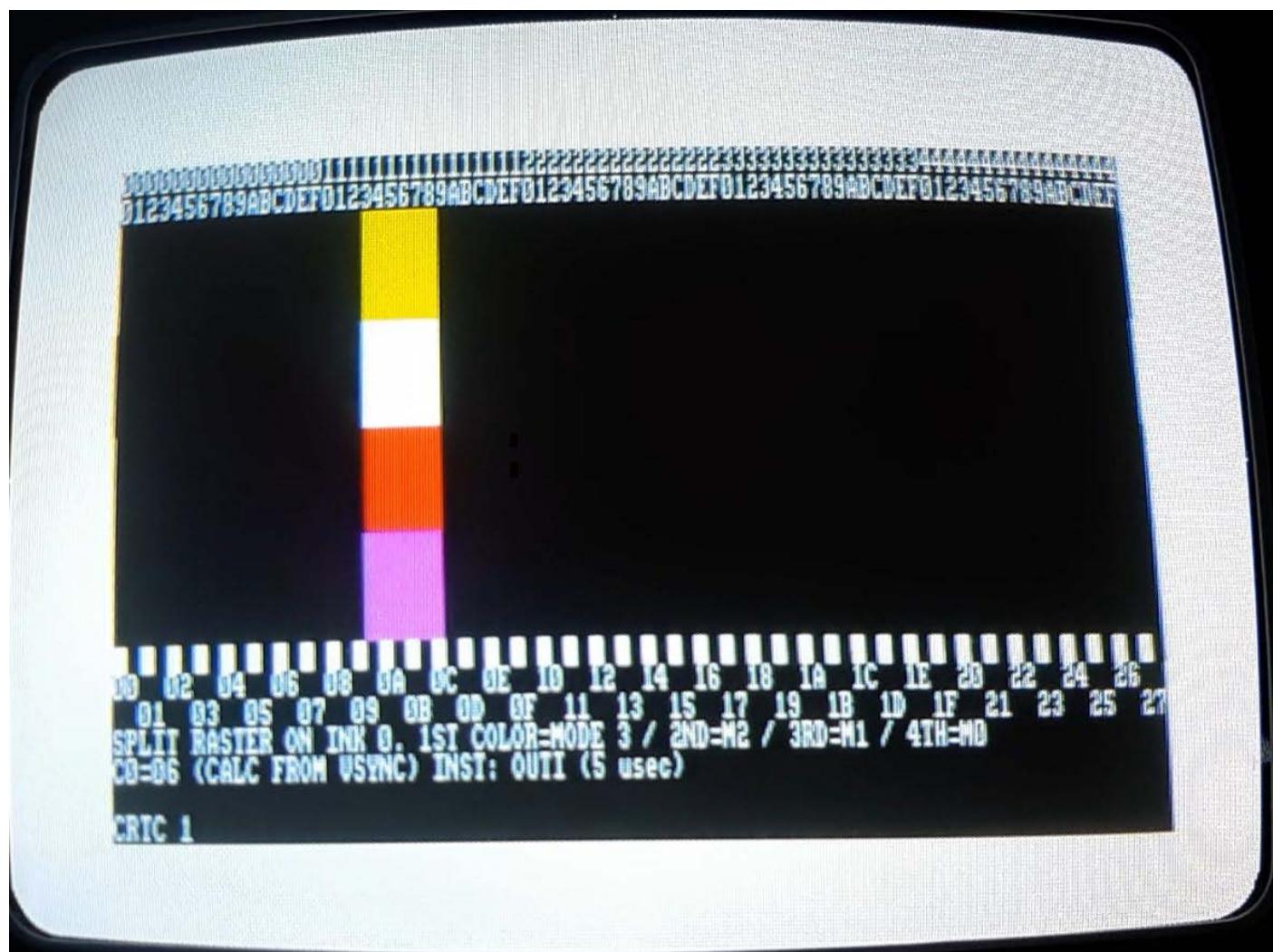
GATE ARRAY PIXELISATION

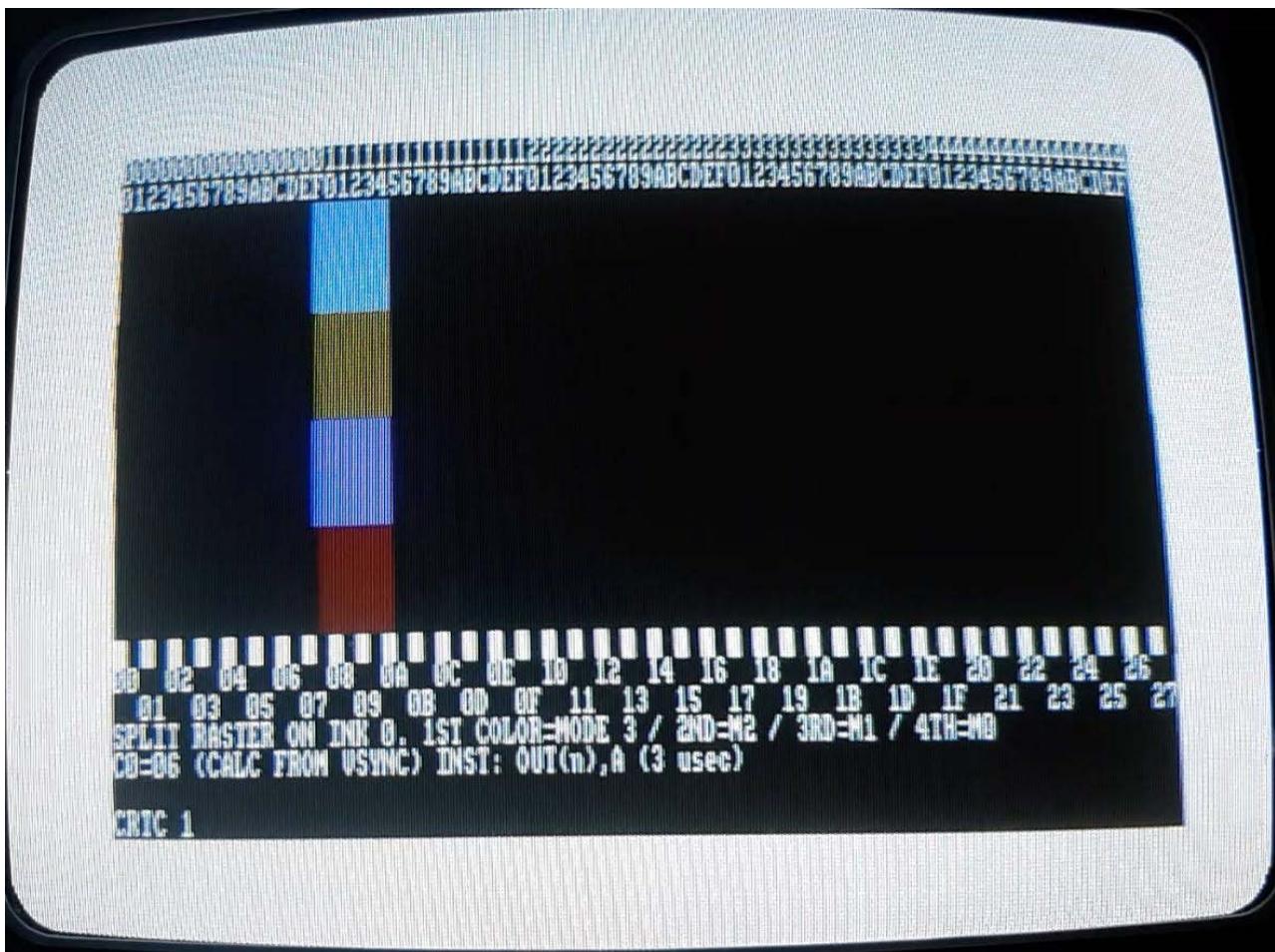
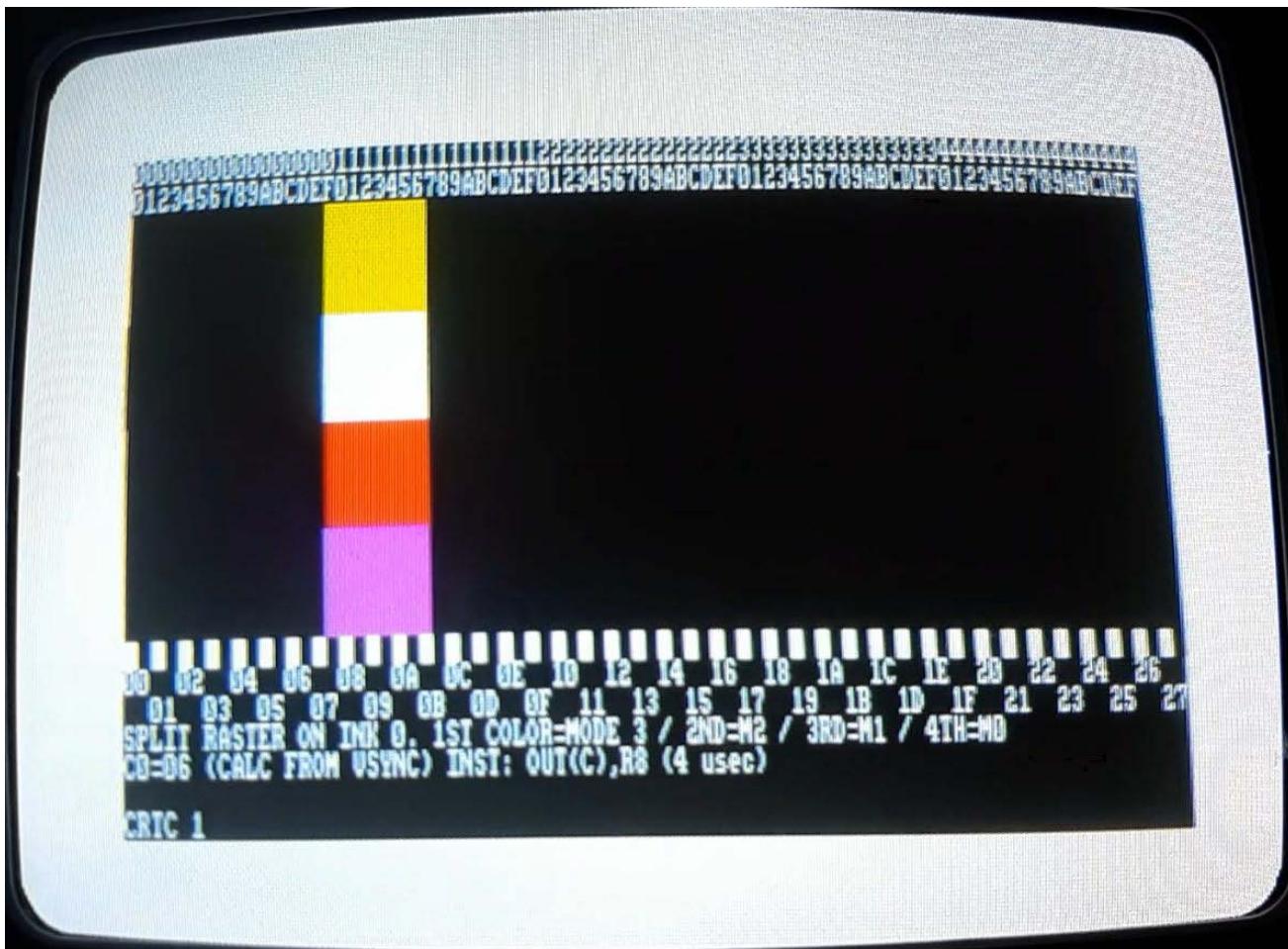
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CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
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(9) GATE ARRAY INKERISATION (3 TST)
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(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC USYNC FROM PPI.PORTB.0=1 !!
```



GATE ARRAY INKERISATION

```
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(1) UPDATE VRAM VS CRTC (14 TST)
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(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
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(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
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(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```





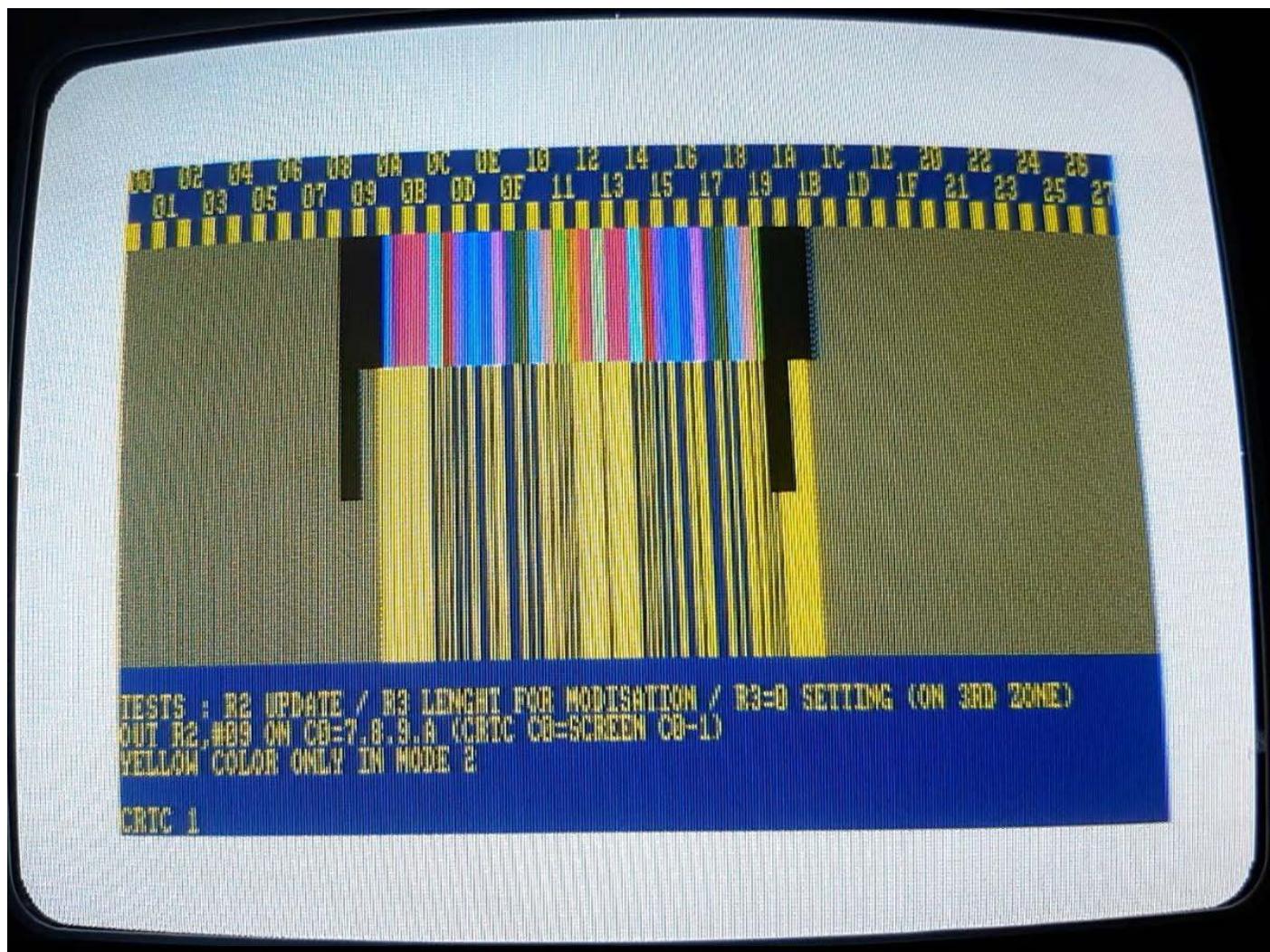
GATE ARRAY MODERISATION

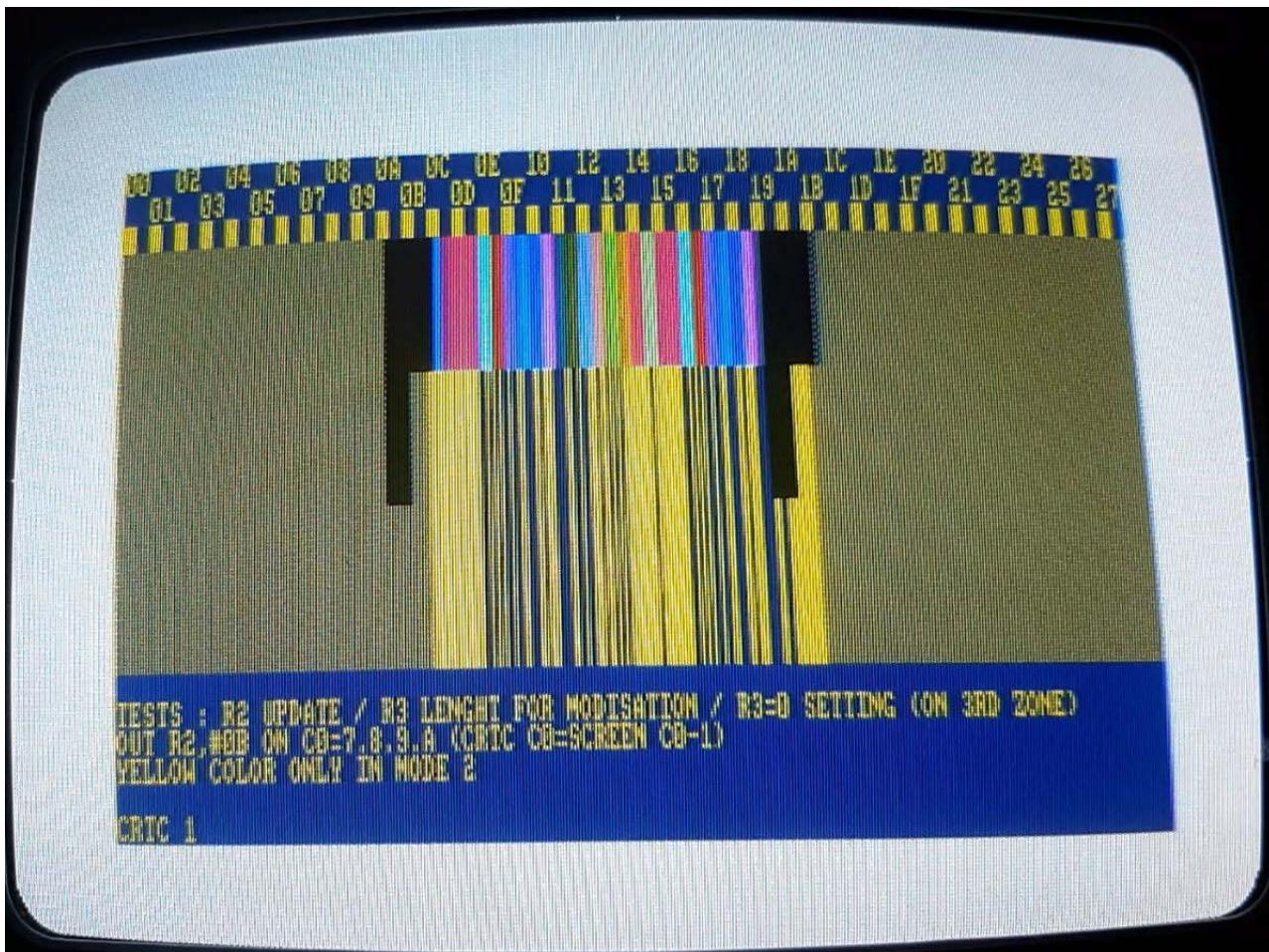
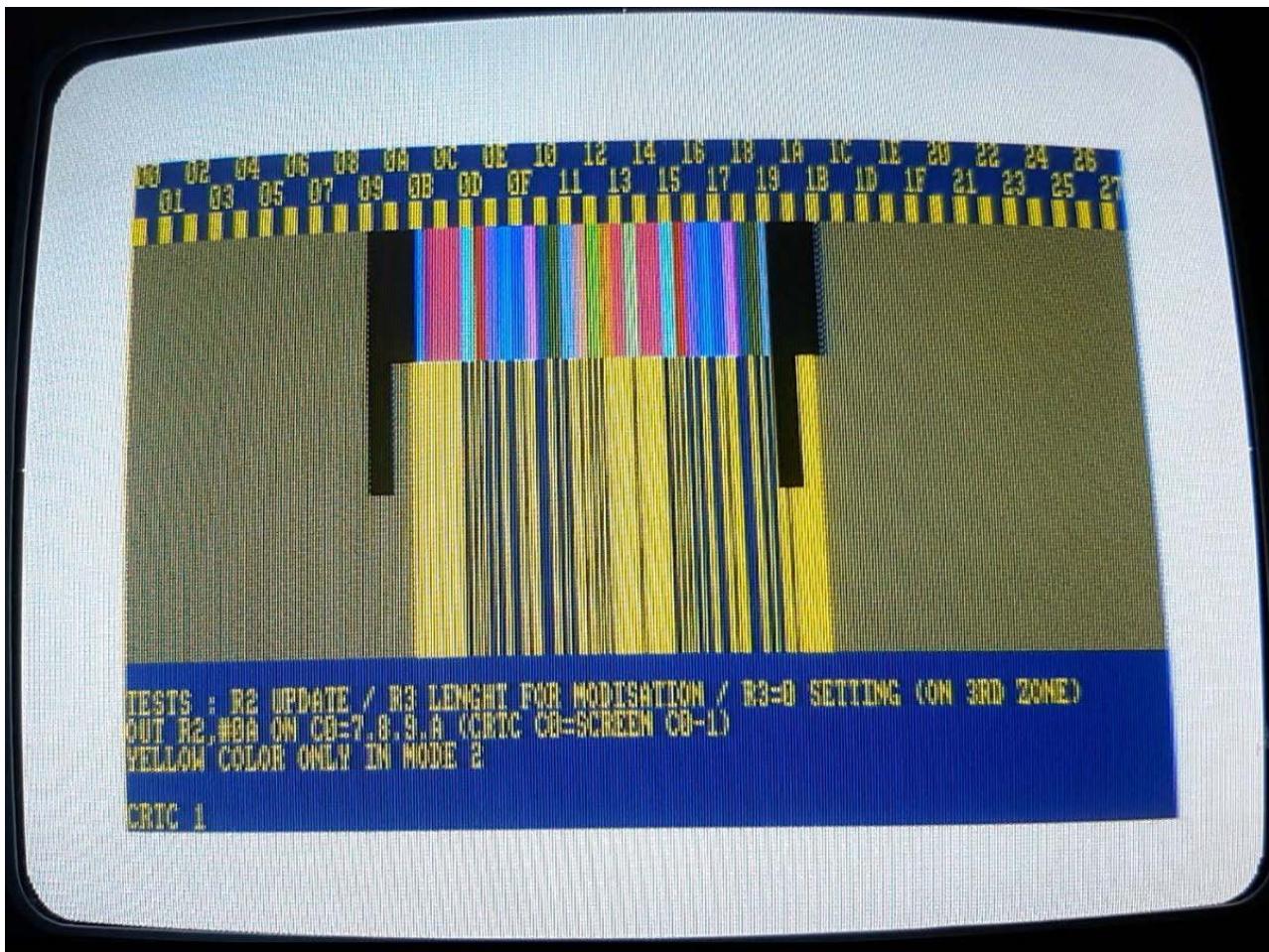
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
 (1) UPDATE VRAM VS CRTC (14 TST) (0) CRTC 2 RUMB
 (2) SKEW DISP ON R0 RUPTURE (5 TST) (F0) BOUNGA:CRTC 2 ZERO!
 (3) INTERRUPT DELAY FROM R2 (18 CALC) (F1) INTERLACE VM (27 TST)
 (4) UPDATE CRTC R0 TIMING (7 TST)
 (5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
 (6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
 (7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
 (8) GATE ARRAY PIXELISATION
 (9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
 (R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
 (T) R2 UPD DURING & AFTER HSYNC (6 TST)
 (Y) R3 UPD DURING HSYNC (8 TST)
 (U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
 (I) VSYNC CONDITIONS (16 TST)
 (O) R1 STORIES (7 TST)
 (P) R6 STORIES (11 TST)
 (RETURN) RUNI LTD
 (CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
 (CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
 (COPY) CRTC 2 OFFSET
 (DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
 !! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!



HSYNC DELAY ON MODE UPDATE, R2 UPDATE/R3 LENGTH 2 to 0

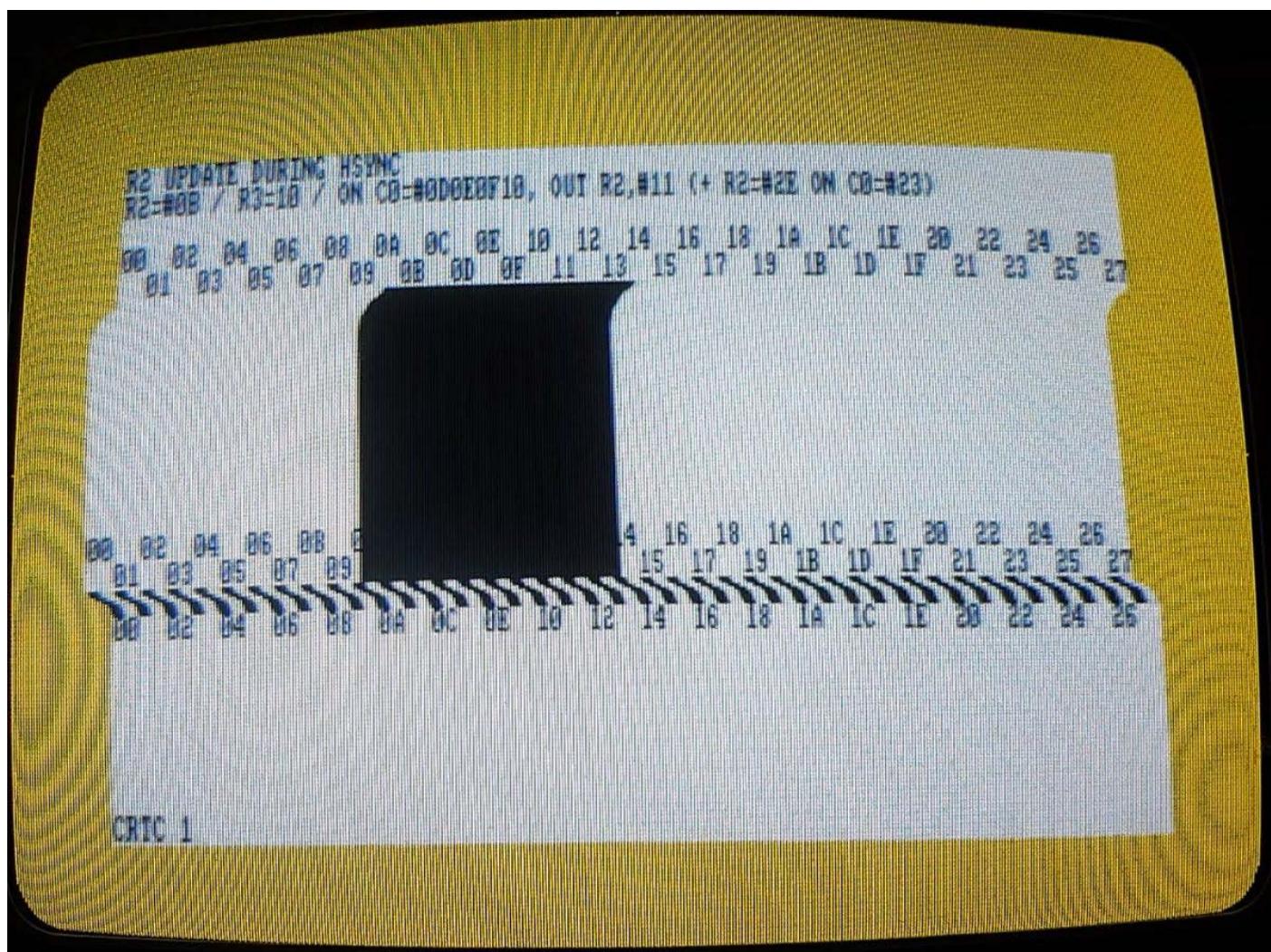
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD, UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!





R2 UPDATE DURING & AFTER HSYNC

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST) (0) CRTC 2 RUMB
(2) SKEW DISP ON R0 RUPTURE (5 TST) (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC) (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!



R2 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON CB=#0D0E0F10, OUT R2,#12 (+ R2=#2E ON CB=#23)

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

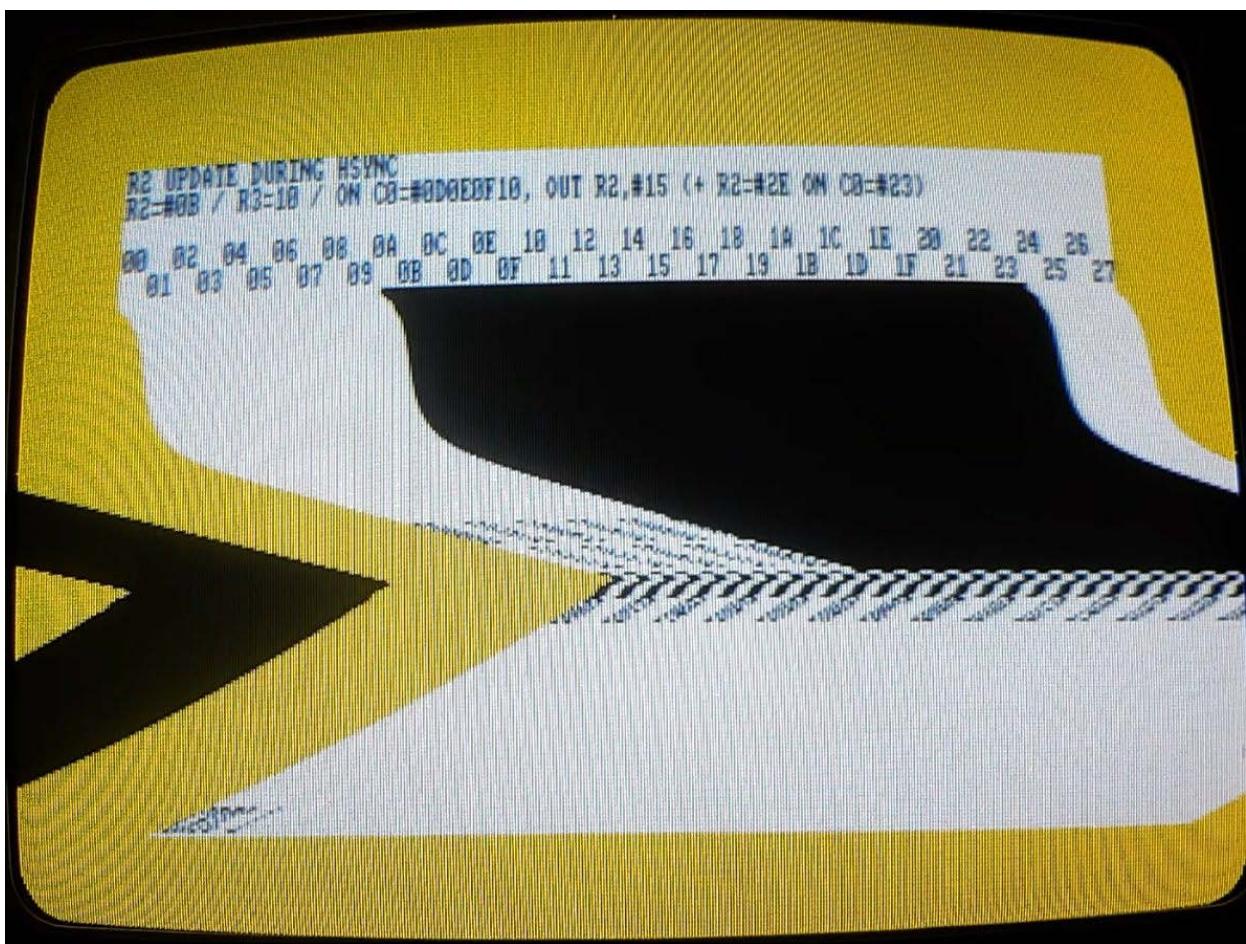
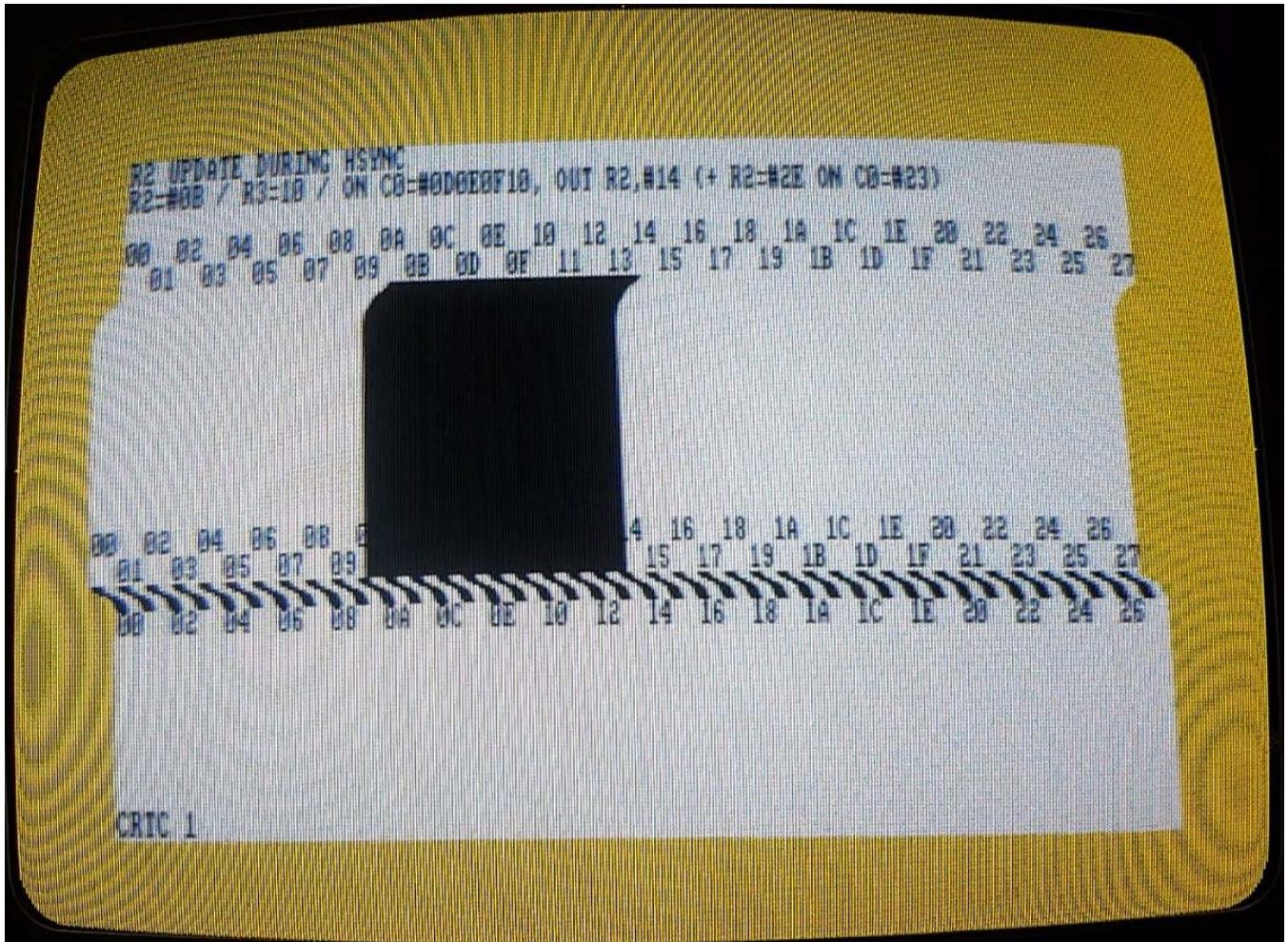
CRTC 1

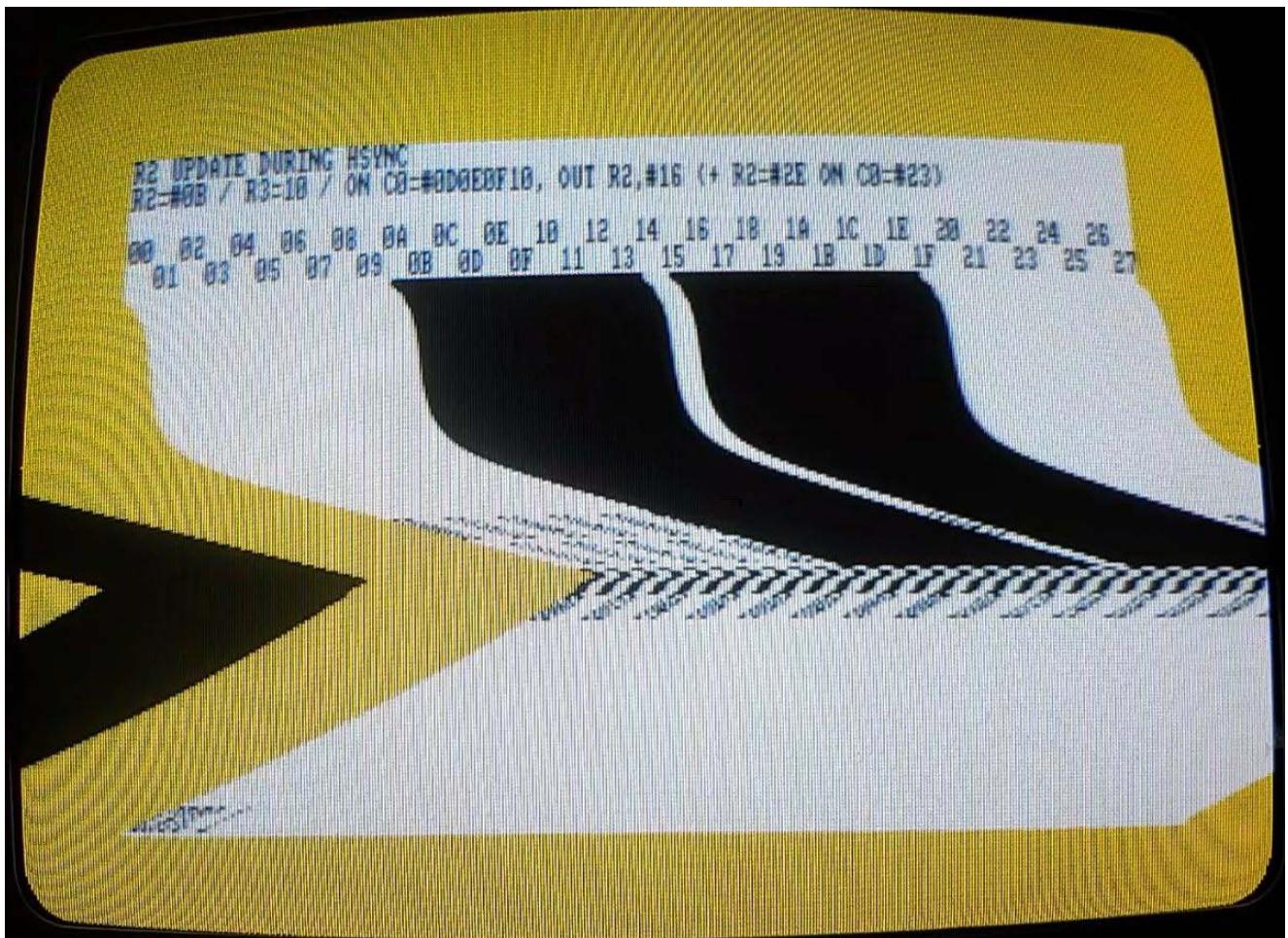
R2 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON CB=#0D0E0F10, OUT R2,#13 (+ R2=#2E ON CB=#23)

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26

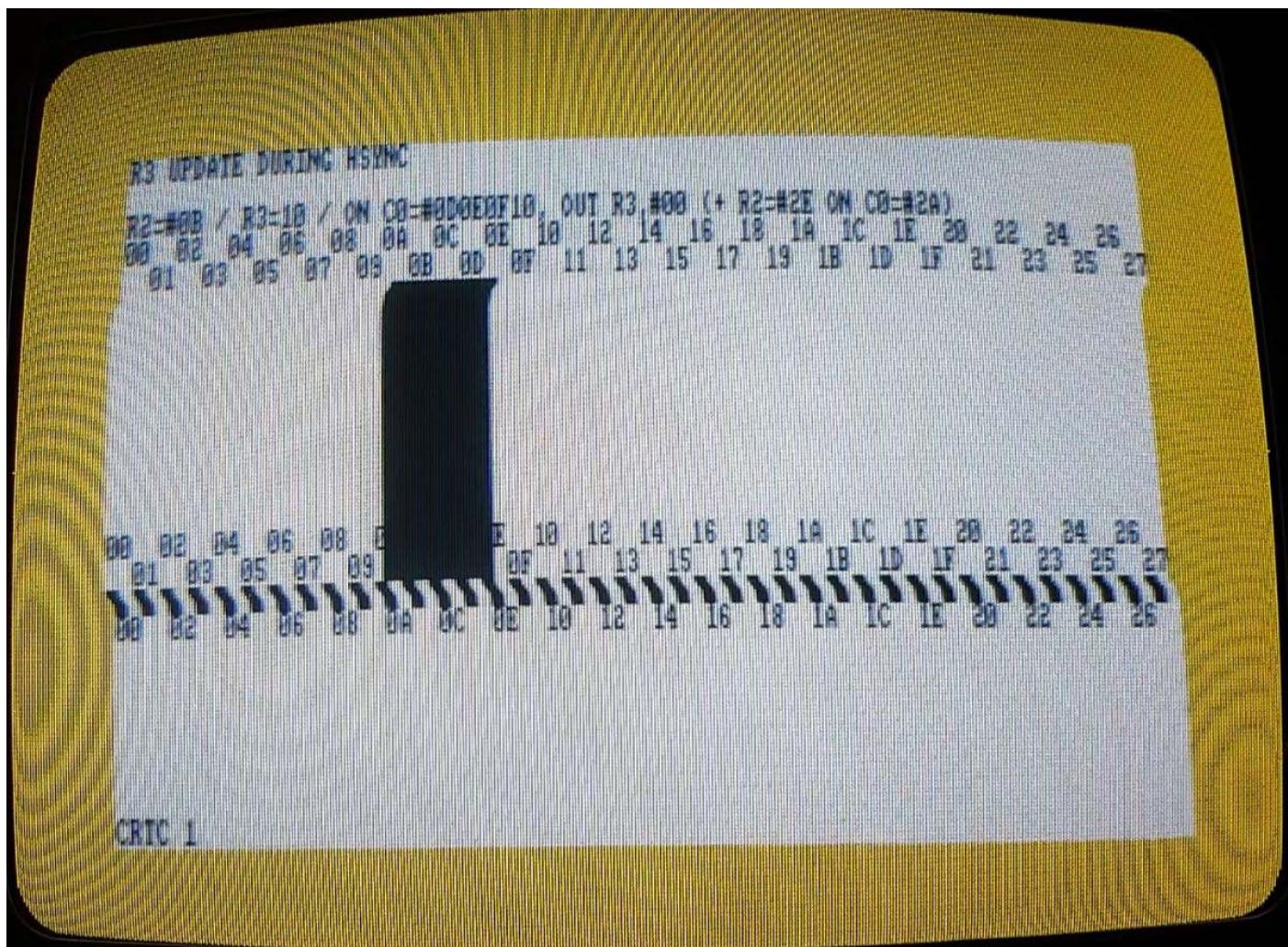
CRTC 1





R3 UPDATE DURING HSYNC

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD_UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!



R3 UPDATE DURING HSYNC

R2=#0B / R3=10 / ON CO=#0D0E0F10 OUT R3 #01 (+ R2:#2E ON CO:#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A
01 03 05 07 09
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26

1C 1E 20 22 24 26
1D 1F 21 23 25 27

CRTC 1

R3 UPDATE DURING HSYNC

R2=#0B / R3=10 / ON CO=#0D0E0F10 OUT R3 #02 (+ R2:#2E ON CO:#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A
01 03 05 07 09
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26

1C 1E 20 22 24 26
1D 1F 21 23 25 27

CRTC 1

R3 UPDATE DURING HSYNC

R2=#03 / R3=10 / ON CO=#0D0E0F10, OUT R3 #03 (+ R2=#2E ON CO=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

CRTC 1

R3 UPDATE DURING HSYNC

R2=#03 / R3=10 / ON CO=#0D0E0F10, OUT R3 #04 (+ R2=#2E ON CO=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 25
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

CRTC 1

R3 UPDATE DURING HSYNC

R2=#0B / R3=10 / ON CO=#0D0E0F10 OUT R3,#05 (+ R2=#2E ON CO=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26

CRTC 1

R3 UPDATE DURING HSYNC

R2=#0B / R3=10 / ON CO=#0D0E0F10 OUT R3,#06 (+ R2=#2E ON CO=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26

CRTC 1

R3 UPDATE DURING HSIMC

R2=##0B / R3=10 / ON CB=#0D0E0F10, OUT R3,#87 (+ R2=#25 ON CB=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

CRIC 1

R4 & R9 CHECKING

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST) (0) CRTC 2 RUMB
(2) SKEW DISP ON R0 RUPTURE (5 TST) (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC) (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) USYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC USYNC FROM PPI.PORTB.0=1 !!

SEARCHED SERIALIZED INDEXED CHECKED

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PRIV R9=7 )) UPD R9=1 WHEN C9=3))>C9=0 (OK FOR CRT 3+4 ONLY):>x80x
PRIV R9=7 R4=38 )) UPD R4=1 WHEN C4=1 & C9=7 )) C4=0 :OK
PRIV R9=7 R4=38 )) UPD R4=0 WHEN C4=1 & C9=7 )) C4=2 (0wf) :OK
PRIV R9=7 R4=38 )) UPD R9=0 WHEN C4=1 & C9=0 (UPD FROM CPvs10) 08=Upd 0W
PRIV R9=7 R4=38 )) UPD R4=1 WHEN C4=1 & C9=7 (UPD FROM CPvs10) 01=C4 0wf
)) 3E=00/3D=00/3E=00/3F=00/00=01/01=01/02=01/03=01/04=01/05=01
PRIV R9=7 R4=38 )) UPD R4=1 WHEN C4=1 & C9=7 (UPD FROM CPvs10) 01=C4 0wf
)) 3E=00/3D=00/3E=00/3F=00/00=01/01=01/02=01/03=01/04=01/05=01
PRIV R9=7 R4=1 )) UPD R9=1 WHEN C4=1 C9=7 LASTLINE FROM CB=29 R2=420(01:C9=0)
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
PRIV R9=7 R4=1 )) UPD R4=3 WHEN C4=1 & C9=7 (LAST LINE):00 (00:C4wf 01:C4=0)
PRIV R9=7 R4=1 )) UPD R4=0 WHEN C4=1 & C9=7 (UPD FROM CPvs10) 01:C4=0 00:C4 wf
)) 3E=00/3D=00/3E=00/3F=00/00=01/01=01/02=01/03=01/04=01/05=01

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100

VSYNC CONDITIONS

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD, UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!

VSYNC MANAGEMENT DURING R3

R3 APPLIED ON ALL VALUES OF C4
R2=50, R3=12, R0=63 : V1=#5E, V2=#5F
R2=50, R3=13, R0=63 : V1=#5E, V2=#5F
R2=50, R3=14, R0=63 : V1=#5E, V2=#5F
R2=50, R3=15, R0=63 : V1=#5E, V2=#5F

R3 APPLIED ON ALL VALUES OF C4, EXCEPTED WHEN C4=R7 (C9=0)(THEN R3=12)

R2=50, R3=12, R0=63 : V1=#5E, V2=#5F
R2=50, R3=13, R0=63 : V1=#5E, V2=#5F
R2=50, R3=14, R0=63 : V1=#5E, V2=#5F
R2=50, R3=15, R0=63 : V1=#5E, V2=#5F

R2=50, R3=15, R0=63 : V1=#5E, V2=#5F ON PREVIOUS LINE

VSING CONDITIONS IN HSYNC (R2=12B/R3=14)

>> UPD R7=04 ON C9=0, C0v=#35 PPI.B ON C9=0, C0v=#3A:#5F

>> UPD R7=04 ON C9=0, C0v=#35 PPI.B ON C9=0, C0v=#3B:#5F

>> UPD R7=04 ON C9=0, C0v=#35 PPI.B ON C9=1, C0v=#3A:#5F

>> UPD R7=04 ON C9=0, C0v=#35 PPI.B ON C9=1, C0v=#3B:#5F

PPI.STATUS 5us BEFORE R7=04 : #5E

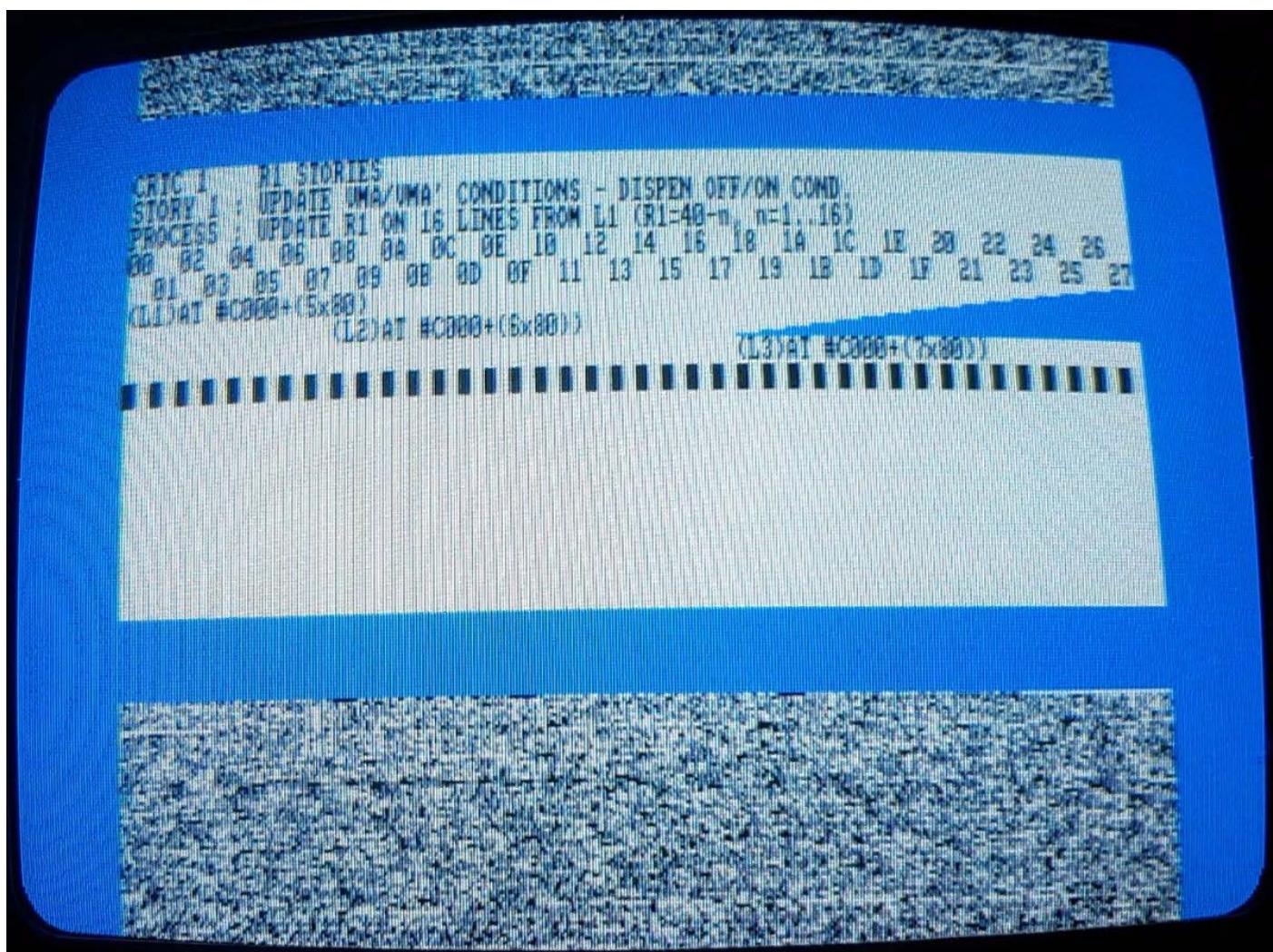
PPI.STATUS 5us AFTER UPD R7=04 (R7=04 BEFORE) (VSYNC CANCEL) (C9=0) : #5E

PPI.ST C0=46 15 LINES AFTER R7=04 ON C0vsio=#1E:5F,5F,5F,5F,5E

CRTC 1

R1 STORIES

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST) (0) CRTC 2 RUMB
(2) SKEW DISP ON R0 RUPTURE (5 TST) (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC) (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD_UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!



CRTC - #115 : 04-96-1, C9E9, PREV R1=40, OUT R1>0 IN '00vs=21

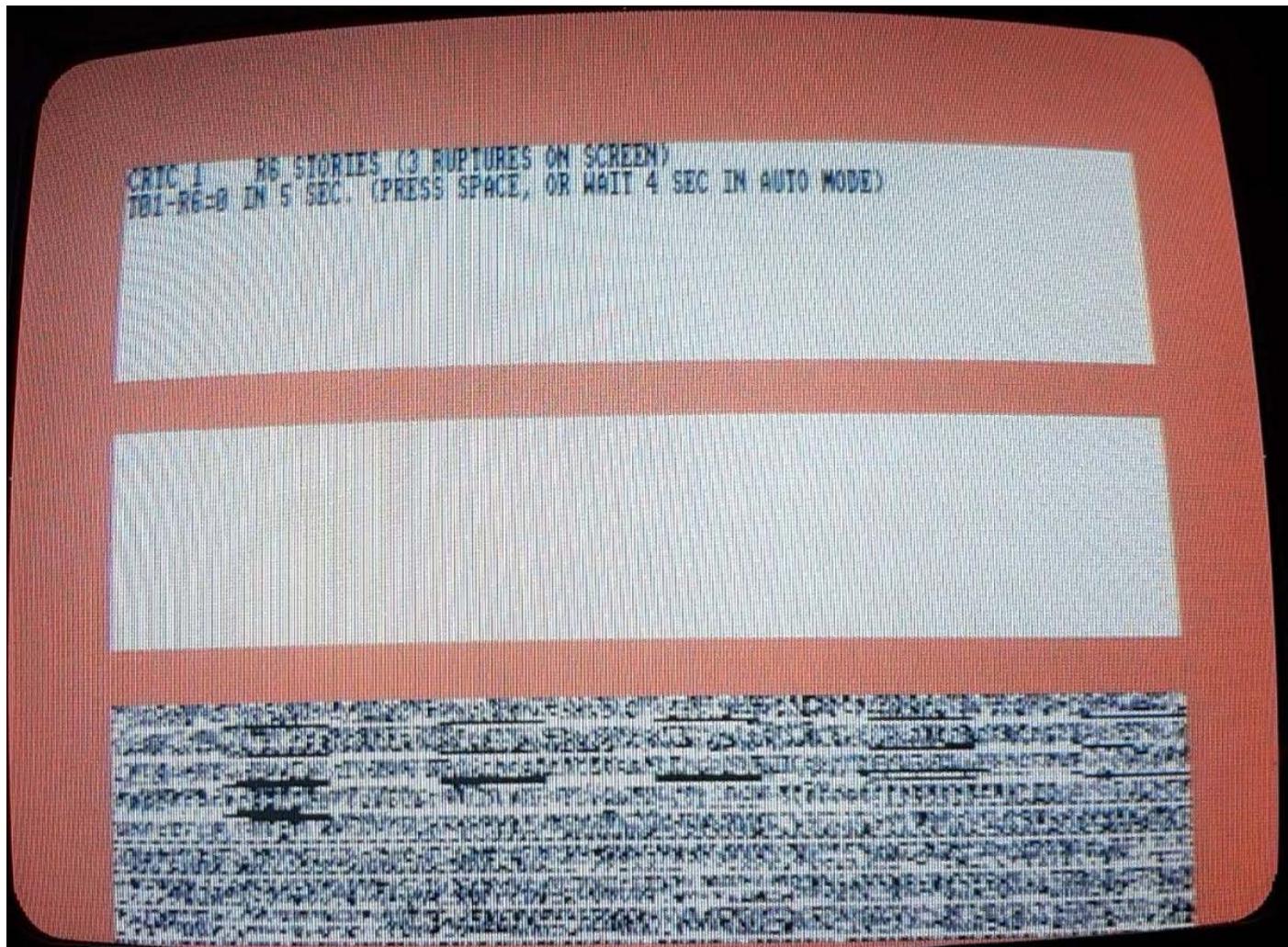
CRTC-UVA :=#0000+(80x24)
CRTC-UVA :=#0000+(80x24)

CRTC - #115 : 04-96-1, C9E9, PREV R1=40, OUT R1>0 IN '00vs=28

CRTC-UVA :=#0000+(80x24)
CRTC-UVA :=#0000+(80x24)

R6 STORIES

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)          (0) CRTC 2 RUMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)        (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)      (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```



CRTC 1 R6 STORIES (3 RUPTURES ON SCREEN)
102-50 L. PATCHWORK R6-B/B FROM VERY 1ST LINE OF MIDDLE SCREEN RUPTURE (C4=0,C3=0)



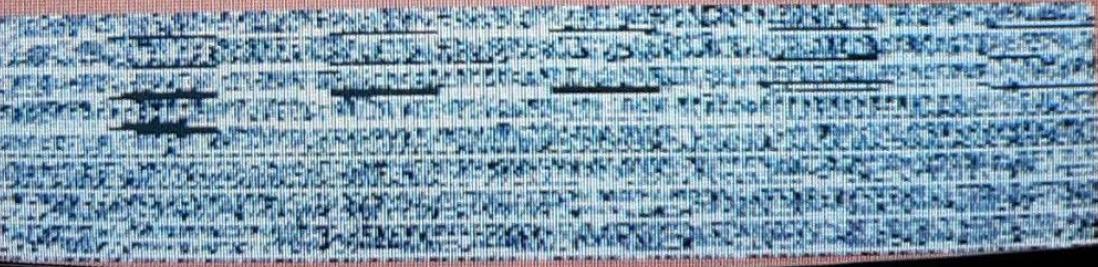
CRTC 1 R6 STORIES (3 RUPTURES ON SCREEN)
103-50 L. PATCHWORK R6-B/B FROM 2ND LINE OF MIDDLE SCREEN RUPTURE (C4=0,C3=1)



CRIC 1 RS STORIES (3 RUPTURES ON SCREEN)
T04-191 LINE IN DISPLAY AREA : SEQUENCE R6=8/R6=8/ WHEN R1>R0



CRIC 1 RS STORIES (3 RUPTURES ON SCREEN)
T05-50 L. FROM 2ND LINE IN DISP AREA : PATCHWORK R6=0/R6=8 WHEN R1>R0



ERIC 1 R6 STORIES - AGAIN-
TO6A-ON C4=9/C9=0 PATCHWORK R6=9/25 IN DISP AREA FOR 64 LINES

ERIC 1 R6 STORIES - AGAIN-
TO6B-ON C4=9/C9=1 PATCHWORK R6=9/25 IN DISP AREA FOR 64 LINES

CRTC 1 R6 STORIES -LAST LINE-
TOBC-ON C4=9/C9=1 PATCHWORK R6=R/25 IN DISP AREA FOR 64 LINES

CRTC 1 R6 STORIES -LAST LINE-
R6=0/FF FROM C8=2 ON C4=R4, C9=0..7, PREVIOUS R6=R4+1

CRTC 1 R6 STORIES -LAST LINE-
R6=0/FF FROM C8=2 ON C4=R4, C9=0..7, PREVIOUS R6=R4+1

CRTC 1 R6 STORIES -LAST LINE-
R6=R4+1/TF FROM CB=2 IN V.ADJ ZONE (RS=16) (C4=fnc(CRTC)) PREVIOUS RS=R4+3

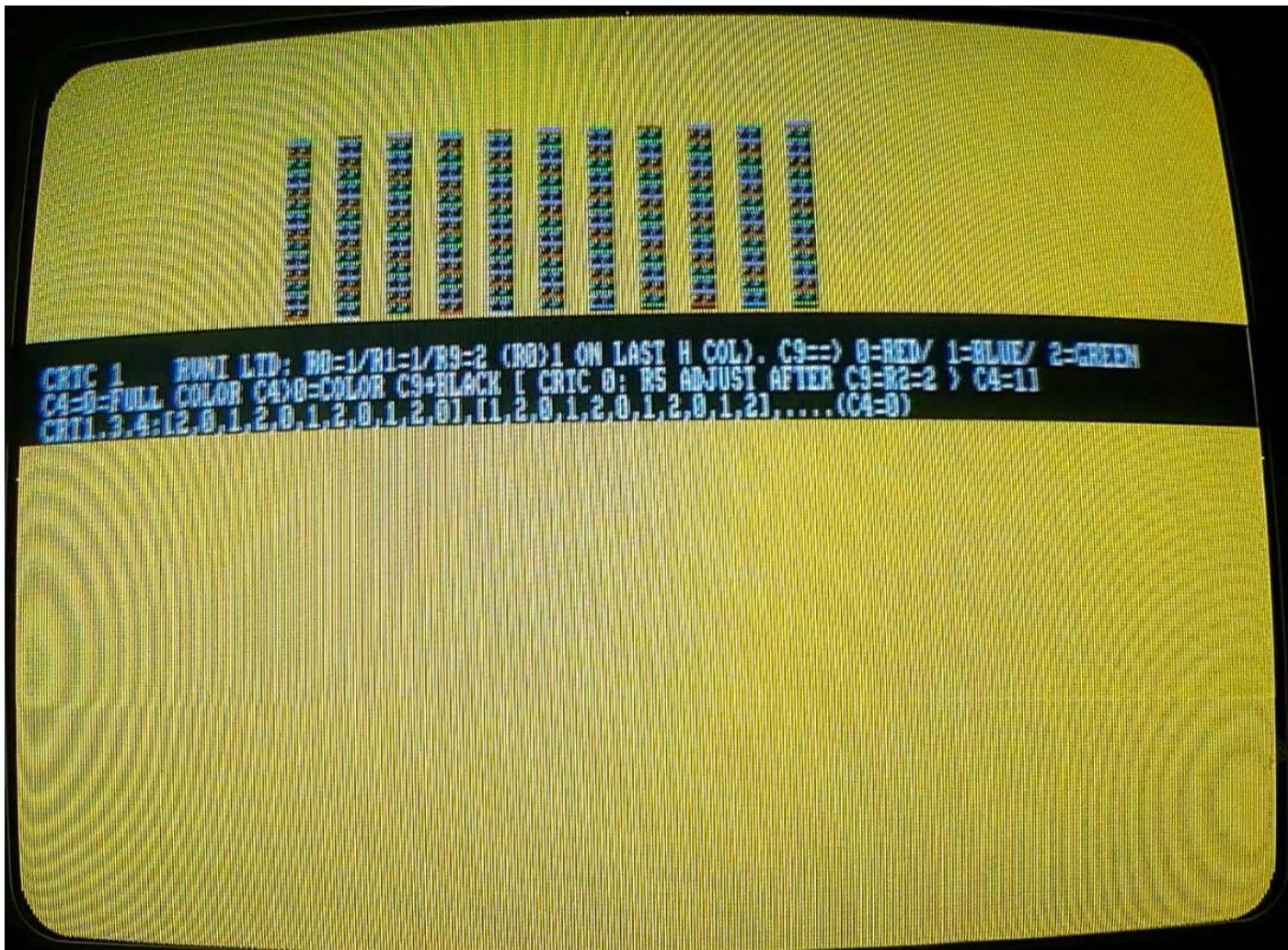
CRTC 1 R6 STORIES -LAST LINE-
R6=R4+1/TF FROM CB=2 IN V.ADJ ZONE
(RS=16) (C4=fnc(CRTC)) PREVIOUS RS=R4+3

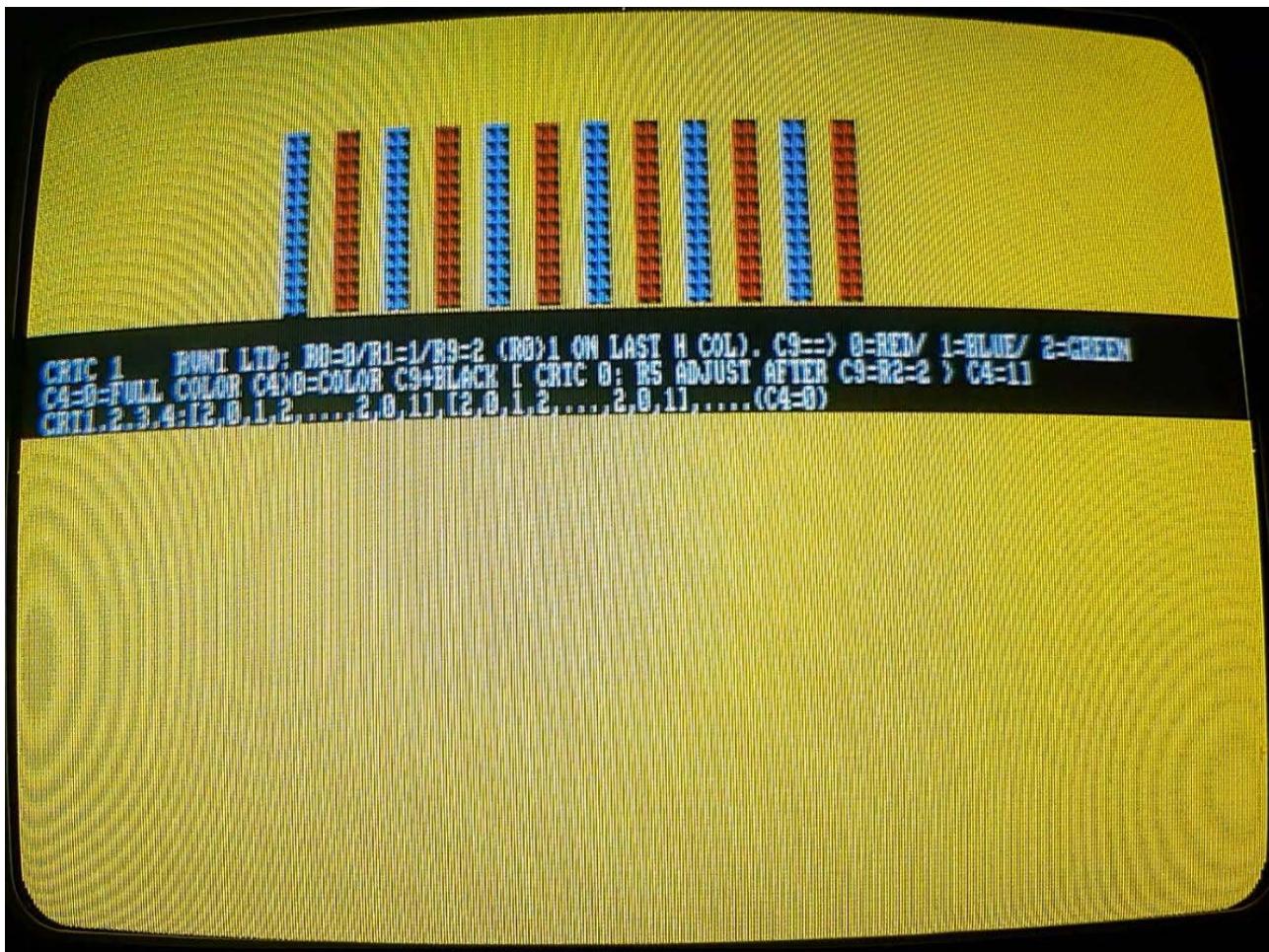
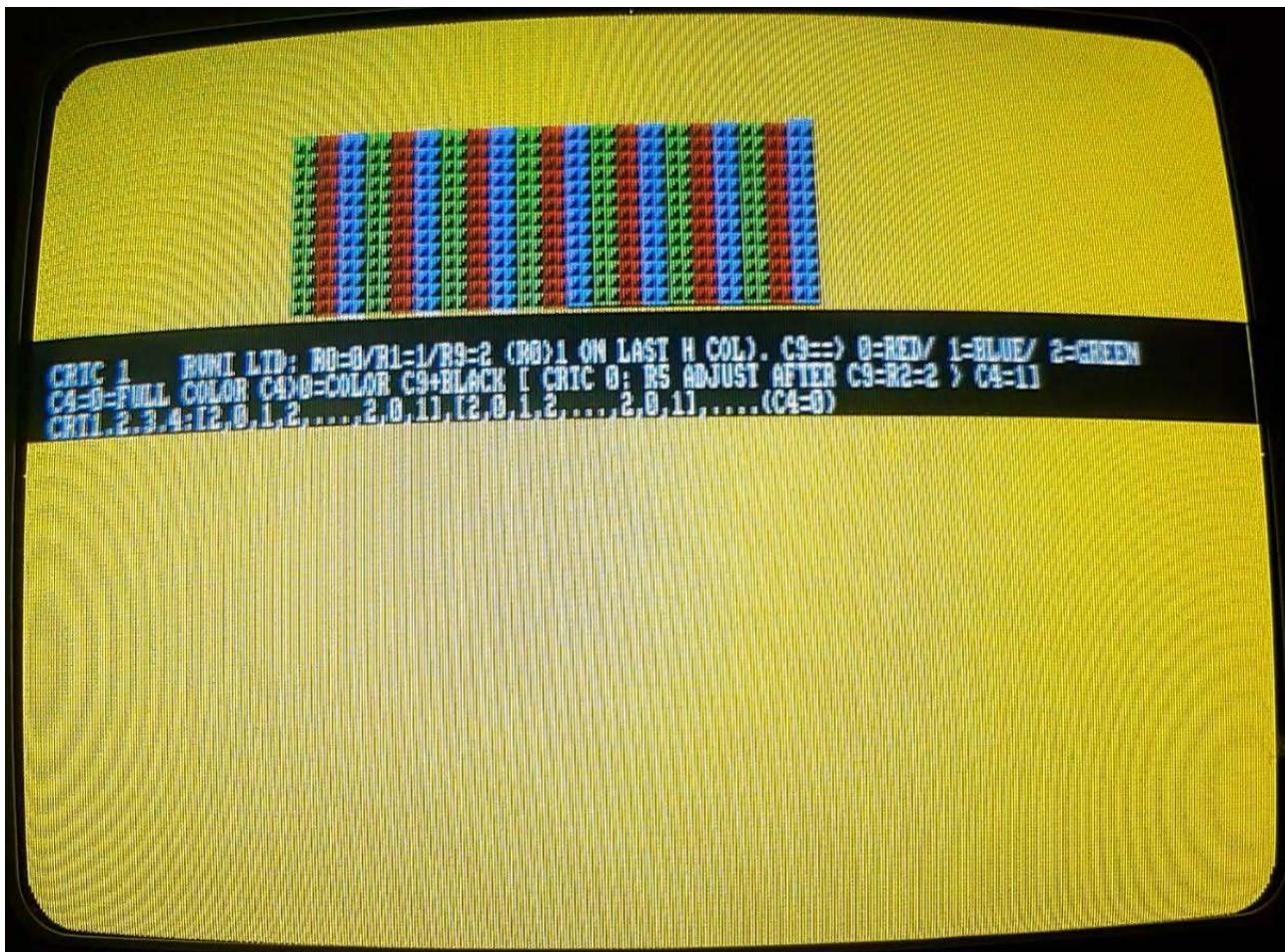
CRTC 1 R6 STORIES -LAST LINE-
R6=R4+1/TF FROM CB=2 IN V.ADJ ZONE (RS=16) (C4=fnc(CRTC)) PREVIOUS RS=R4+3

CRTC 1 R6 STORIES -LAST LINE-
R6=R4+1/TF FROM CB=2 IN V.ADJ ZONE
(RS=16) (C4=fnc(CRTC)) PREVIOUS RS=R4+3

RVNI (NON INVISIBLE VERTICAL RUPTURE)

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST) (0) CRTC 2 RUMB
(2) SKEW DISP ON R0 RUPTURE (5 TST) (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC) (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) USYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC USYNC FROM PPI.PORTB.0=1 !!





ANALYZER / FORCED STABILISATION ON R0=0

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST) (0) CRTC 2 RUMB
(2) SKEW DISP ON R0 RUPTURE (5 TST) (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC) (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
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(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!





R5 SCANNER (for CRTC 1)

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM US CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD_UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```

CRTC 1 R5 SHAKER : MAGIC COCKTAIL / KEY 1 10 8 10 MODIFY SCANNER TEST

```
UPDATE R5 FROM 0 TO 1 ON CD= #18, C9=5
A00401A02A03A04A05A06A07A08A09A10A11A12A13A14A15A16A17A18A19A20A21A22A23A24A25A
B00B01B02B03B04B05B06B07B08B09B10B11B12B13B14B15B16B17B18B19B20B21B22B23B24B25B
C00CB1C02C03C04C05C06C07C08C09C10C11C12C13C14C15C16C17C18C19C20C21C22C23C24C25C
D00D01D02D03D04D05D06D07D08D09D10D11D12D13D14D15D16D17D18D19D20D21D22D23D24D25D
E00E01E02E03E04E05E06E07E08E09E10E11E12E13E14E15E16E17E18E19E20E21E22E23E24E25E
F00F01F02F03F04F05F06F07F08F09F10F11F12F13F14F15F16F17F18F19F20F21F22F23F24F25F
G00G01G02G03G04G05G06G07G08G09G10G11G12G13G14G15G16G17G18G19G20G21G22G23G24G25G
H00H01H02H03H04H05H06H07H08H09H10H11H12H13H14H15H16H17H18H19H20H21H22H23H24H25H
I00I01I02I03I04I05I06I07I08I09I10I11I12I13I14I15I16I17I18I19I20I21I22I23I24I25I
J00J01J02J03J04J05J06J07J08J09J10J11J12J13J14J15J16J17J18J19J20J21J22J23J24J25J
K00K01K02K03K04K05K06K07K08K09K10K11K12K13K14K15K16K17K18K19K20K21K22K23K24K25K
L00L01L02L03L04L05L06L07L08L09L10L11L12L13L14L15L16L17L18L19L20L21L22L23L24L25L
M00M01M02M03M04M05M06M07M08M09M10M11M12M13M14M15M16M17M18M19M20M21M22M23M24M25M
N00N01N02N03N04N05N06N07N08N09N10N11N12N13N14N15N16N17N18N19N20N21N22N23N24N25N
O00O01O02O03O04O05O06O07O08O09O10O11O12O13O14O15O16O17O18O19O20O21O22O23O24O25O
P00P01P02P03P04P05P06P07P08P09P10P11P12P13P14P15P16P17P18P19P20P21P22P23P24P25P
Q00Q01Q02Q03Q04Q05Q06Q07Q08Q09Q10Q11Q12Q13Q14Q15Q16Q17Q18Q19Q20Q21Q22Q23Q24Q25Q
R00R01R02R03R04R05R06R07R08R09R10R11R12R13R14R15R16R17R18R19R20R21R22R23R24R25R
S00S01S02S03S04S05S06S07S08S09S10S11S12S13S14S15S16S17S18S19S20S21S22S23S24S25S
T00T01T02T03T04T05T06T07T08T09T10T11T12T13T14T15T16T17T18T19T20T21T22T23T24T25T
U00U01U02U03U04U05U06U07U08U09U10U11U12U13U14U15U16U17U18U19U20U21U22U23U24U25U
V00V01V02V03V04V05V06V07V08V09V10V11V12V13V14V15V16V17V18V19V20V21V22V23V24V25V
```


R5 STORIES / INTERACTIVE TEST

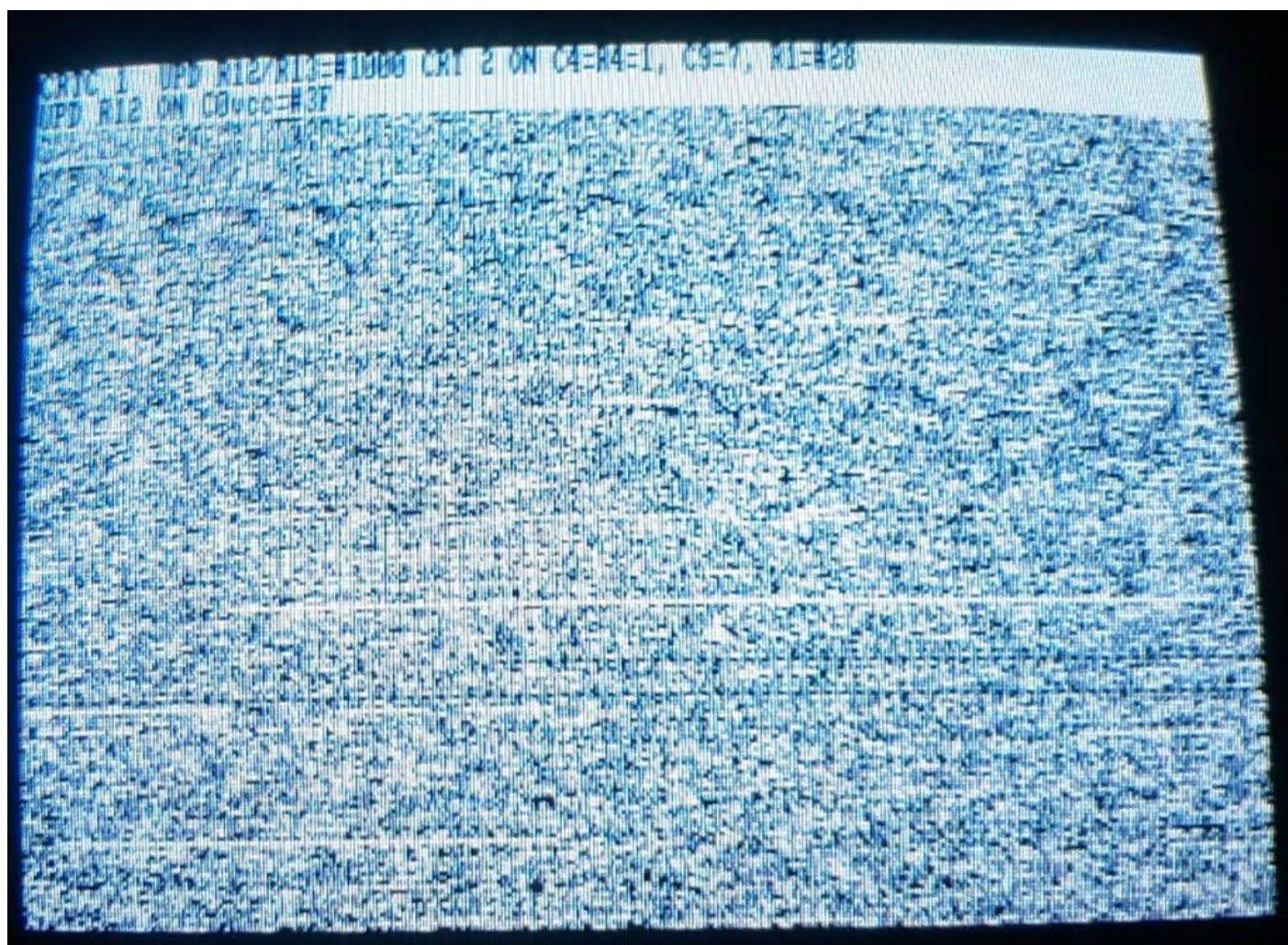
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST) (0) CRTC 2 RUMB
(2) SKEW DISP ON R0 RUPTURE (5 TST) (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC) (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
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(9) GATE ARRAY INKERISATION (3 TST)
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(R) HSYNC DELAY MODE UPD_UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) USYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC USYNC FROM PPI.PORTB.0=1 !!

2025 RELEASE UNDER E.O. 14176

R5 VALUE=14 LINE=39, R12/13=107F
Key L/2/3/4=Video Page, S/6:Offset Inc On-Off, 7/8:Offs H/L=0 (+shift=speed)
A00A01A02A03A04A05A06A07A08A09A10A11A12A13A14A15A16A17A18A19A20A21A22A23A24A25C
B00B01B02B03B04B05B06B07B08B09B10B11B12B13B14B15B16B17B18B19B20B21B22B23B24B25C
C00C01C02C03C04C05C06C07C08C09C10C11C12C13C14C15C16C17C18C19C20C21C22C23C24C25C
D00D01D02D03D04D05D06D07D08D09D10D11D12D13D14D15D16D17D18D19D20D21D22D23D24D25C
E00E01E02E03E04E05E06E07E08E09E10E11E12E13E14E15E16E17E18E19E20E21E22E23E24E25C
F00F01F02F03F04F05F06F07F08F09F10F11F12F13F14F15F16F17F18F19F20F21F22F23F24F25C
G00G01G02G03G04G05G06G07G08G09G10G11G12G13G14G15G16G17G18G19G20G21G22G23G24G25C
H00H01H02H03H04H05H06H07H08H09H10H11H12H13H14H15H16H17H18H19H20H21H22H23H24H25C
I00I01I02I03I04I05I06I07I08I09I10I11I12I13I14I15I16I17I18I19I20I21I22I23I24I25C
J00J01J02J03J04J05J06J07J08J09J10J11J12J13J14J15J16J17J18J19J20J21J22J23J24J25C
K00K01K02K03K04K05K06K07K08K09K10K11K12K13K14K15K16K17K18K19K20K21K22K23K24K25C
L00L01L02L03L04L05L06L07L08L09L10L11L12L13L14L15L16L17L18L19L20L21L22L23L24L25C
M00M01M02M03M04M05M06M07M08M09M10M11M12M13M14M15M16M17M18M19M20M21M22M23M24M25C
N00N01N02N03N04N05N06N07N08N09N10N11N12N13N14N15N16N17N18N19N20N21N22N23N24N25C
P00P01P02P03P04P05P06P07P08P09P10P11P12P13P14P15P16P17P18P19P20P21P22P23P24P25C
Q00Q01Q02Q03Q04Q05Q06Q07Q08Q09Q10Q11Q12Q13Q14Q15Q16Q17Q18Q19Q20Q21Q22Q23Q24Q25C
R00R01R02R03R04R05R06R07R08R09R10R11R12R13R14R15R16R17R18R19R20R21R22R23R24R25C
S00S01S02S03S04S05S06S07S08S09S10S11S12S13S14S15S16S17S18S19S20S21S22S23S24S25C
T00T01T02T03T04T05T06T07T08T09T10T11T12T13T14T15T16T17T18T19T20T21T22T23T24T25C
U00U01U02U03U04U05U06U07U08U09U10U11U12U13U14U15U16U17U18U19U20U21U22U23U24U25C
V00V01V02V03V04V05V06V07V08V09V10V11V12V13V14V15V16V17V18V19V20V21V22V23V24V25C

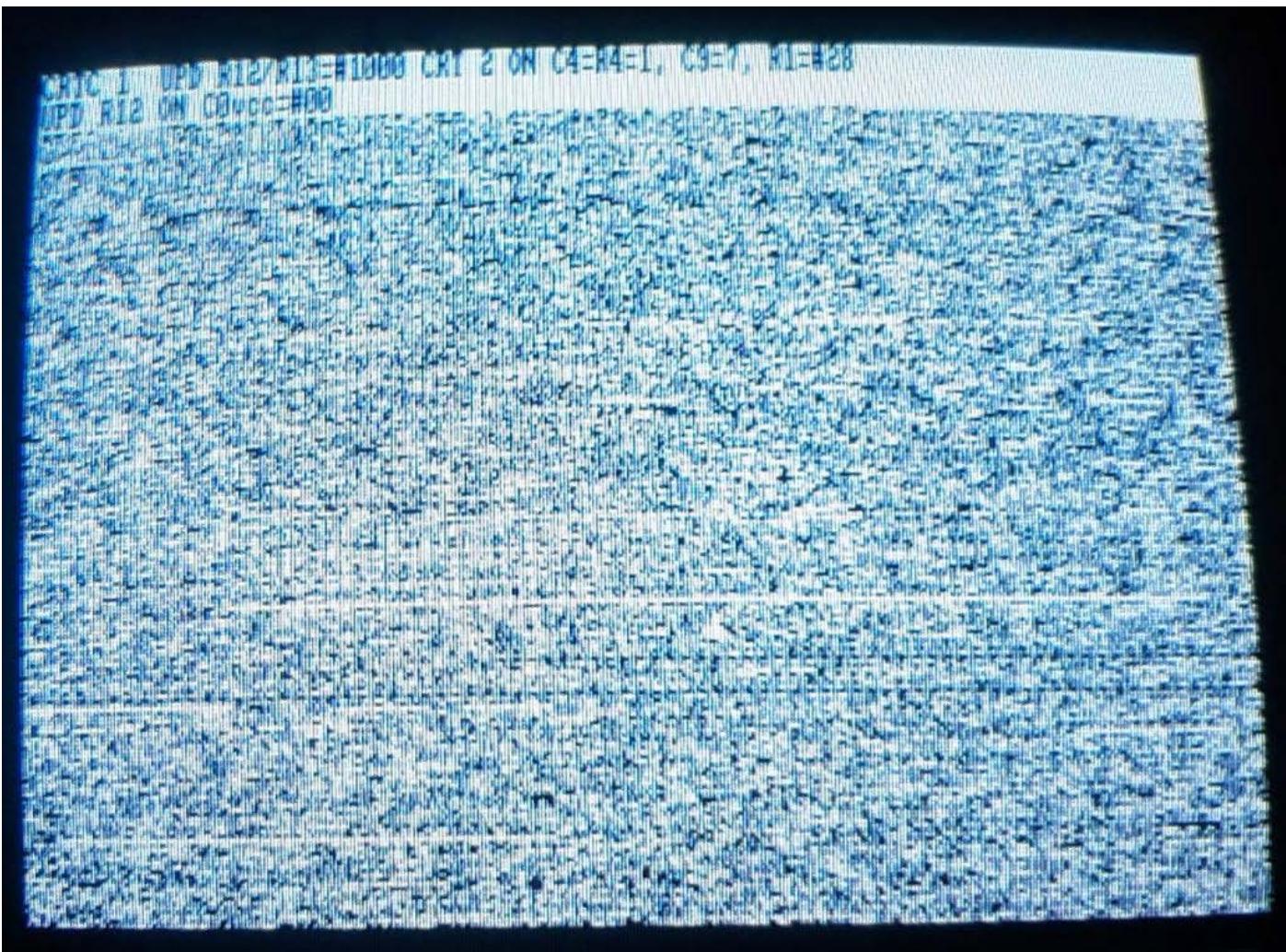
OFFSET UPDATE

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD_UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!



CRTC 1 UPD R12/R1000=1000 CRI 2 ON C4=R4=1, C9=1, R1=28

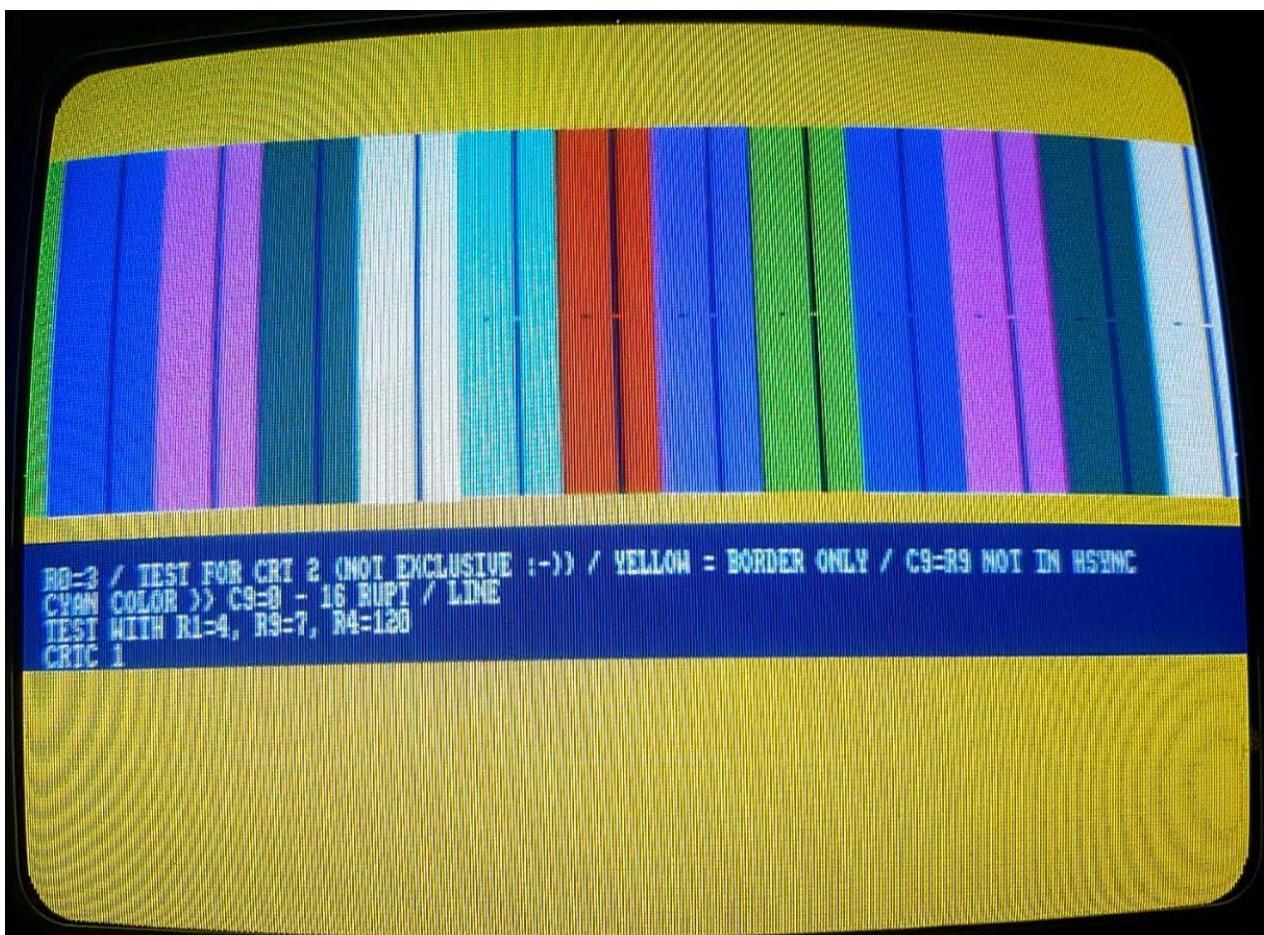
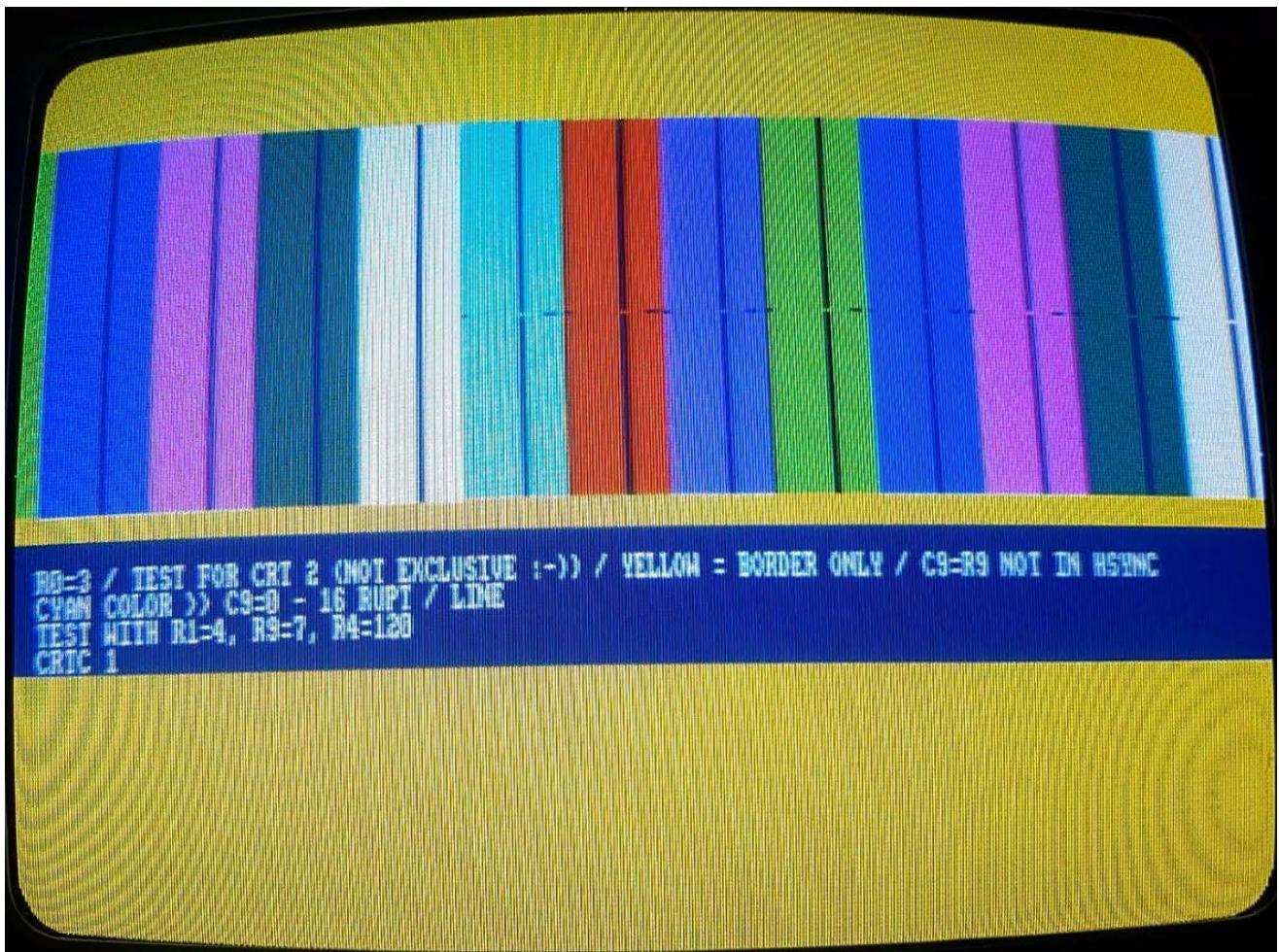
UPD R12 ON C0=C0=00



« RVMB »

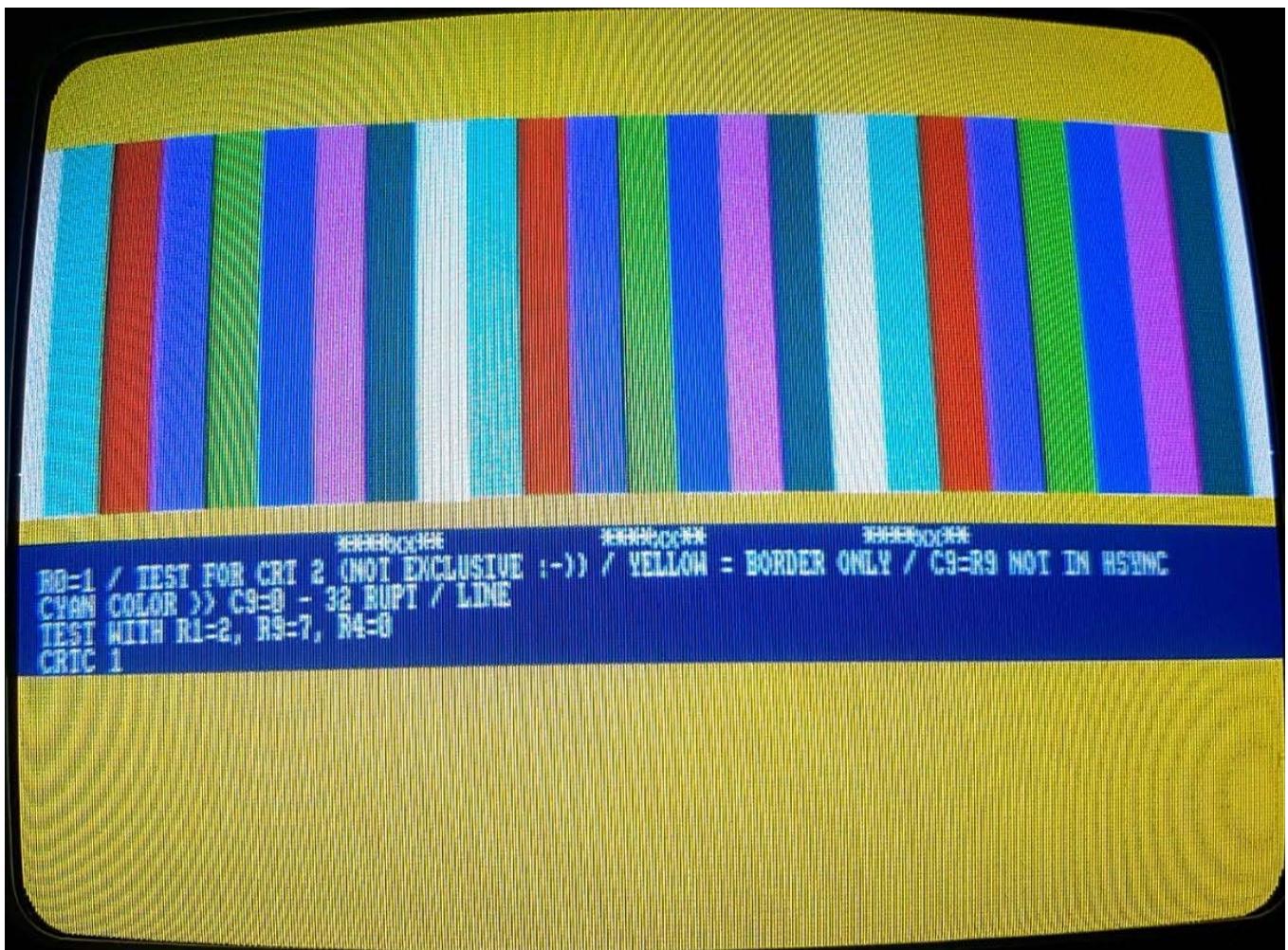
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
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(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!

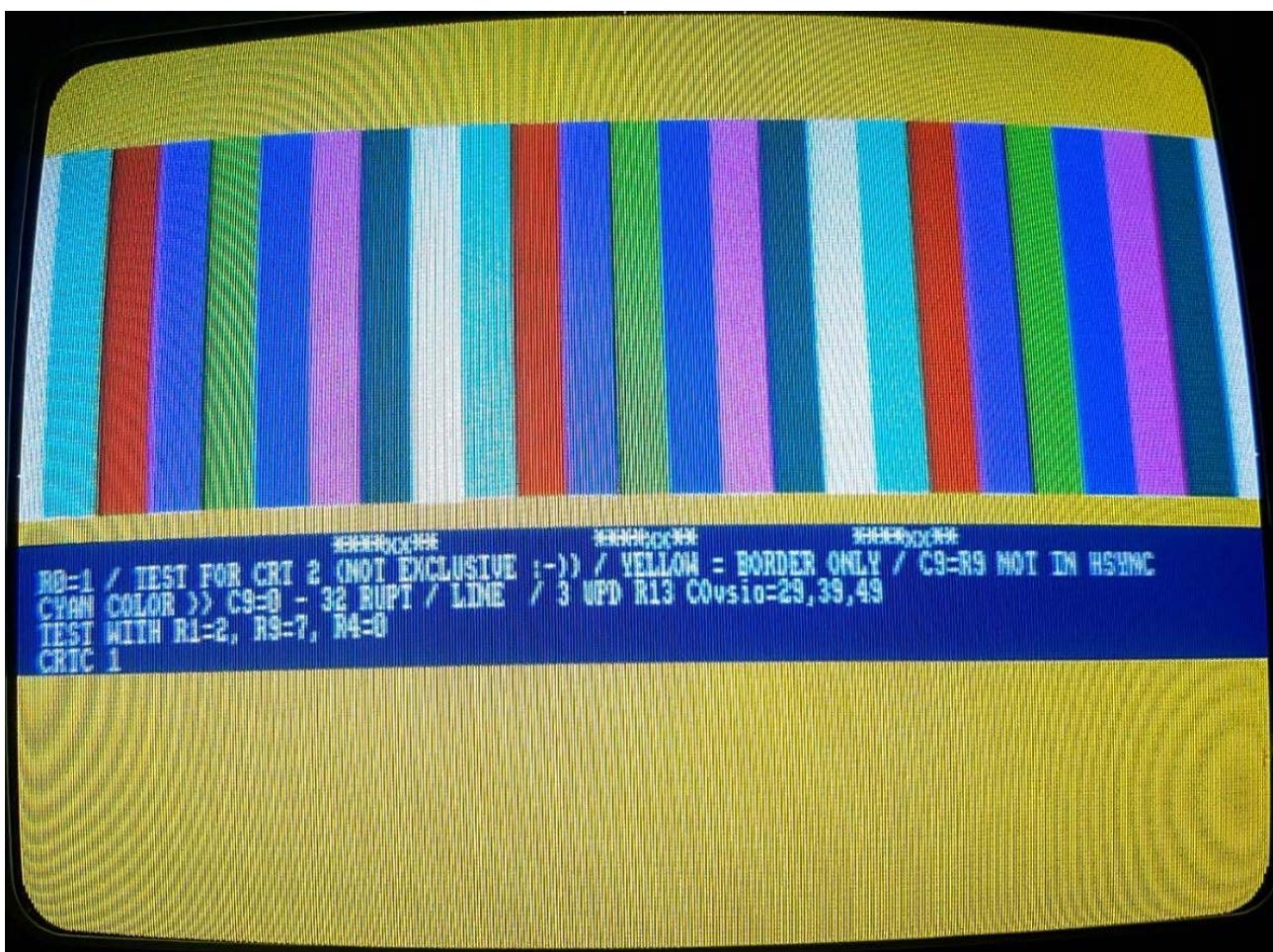
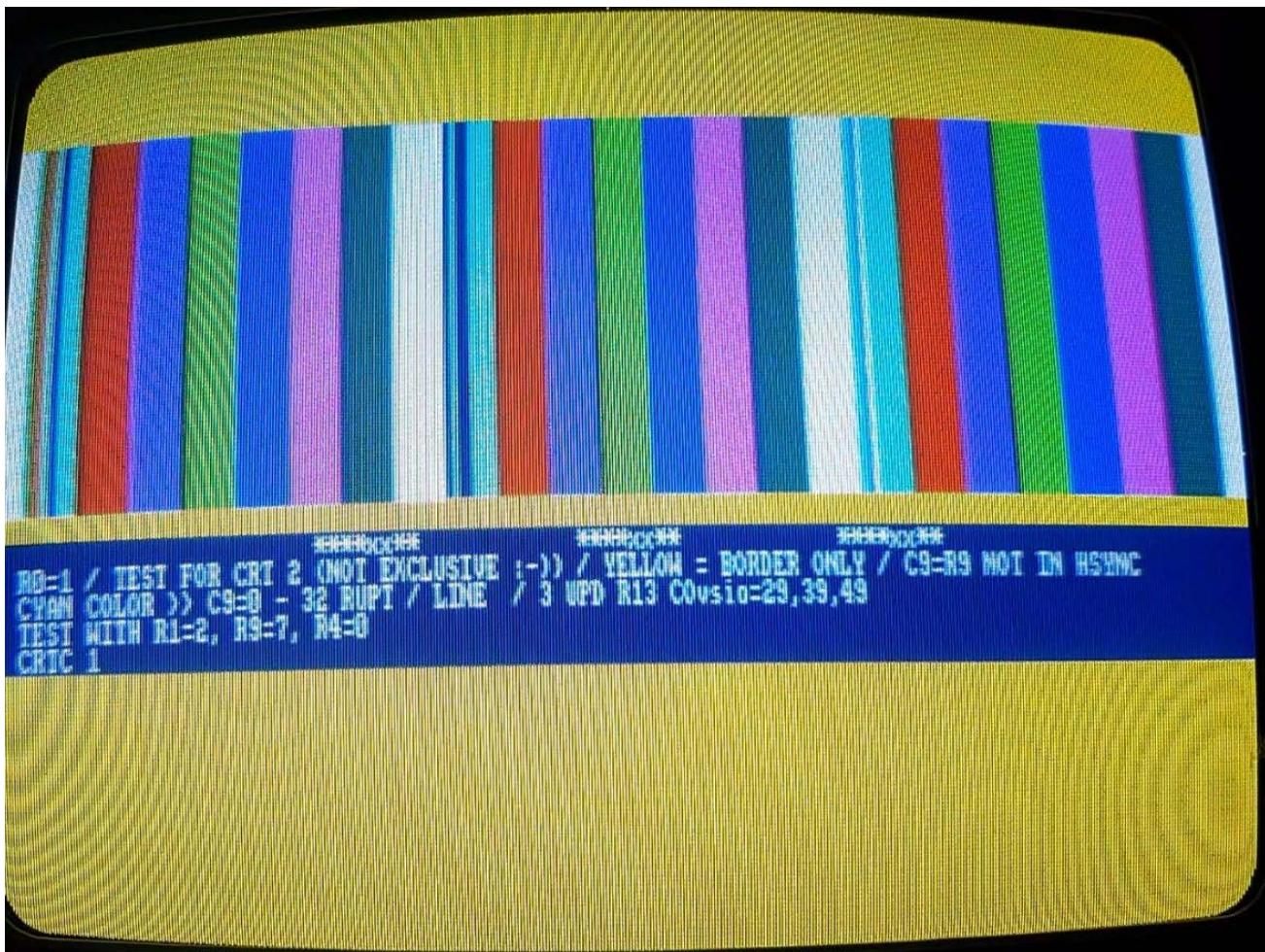






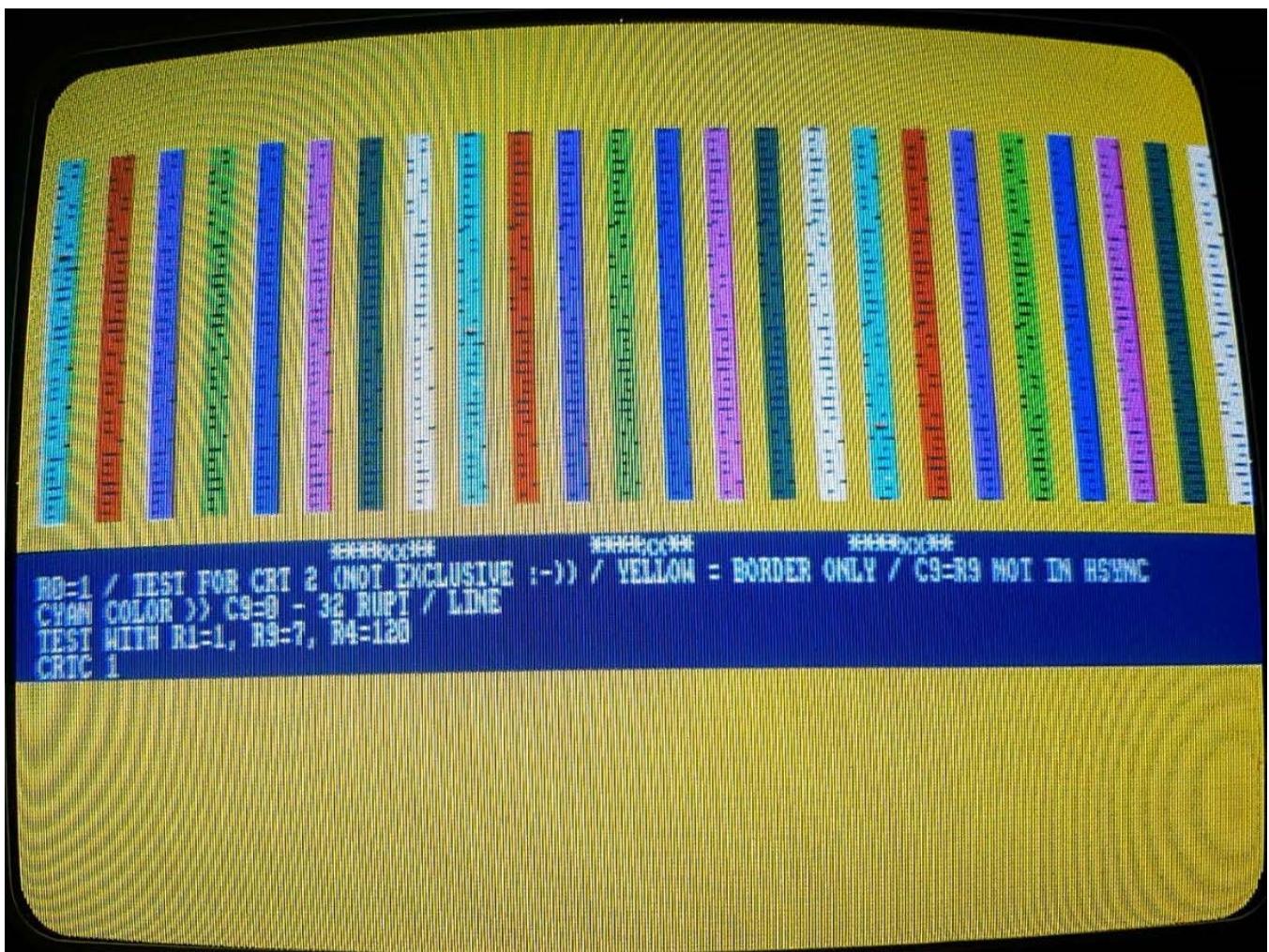


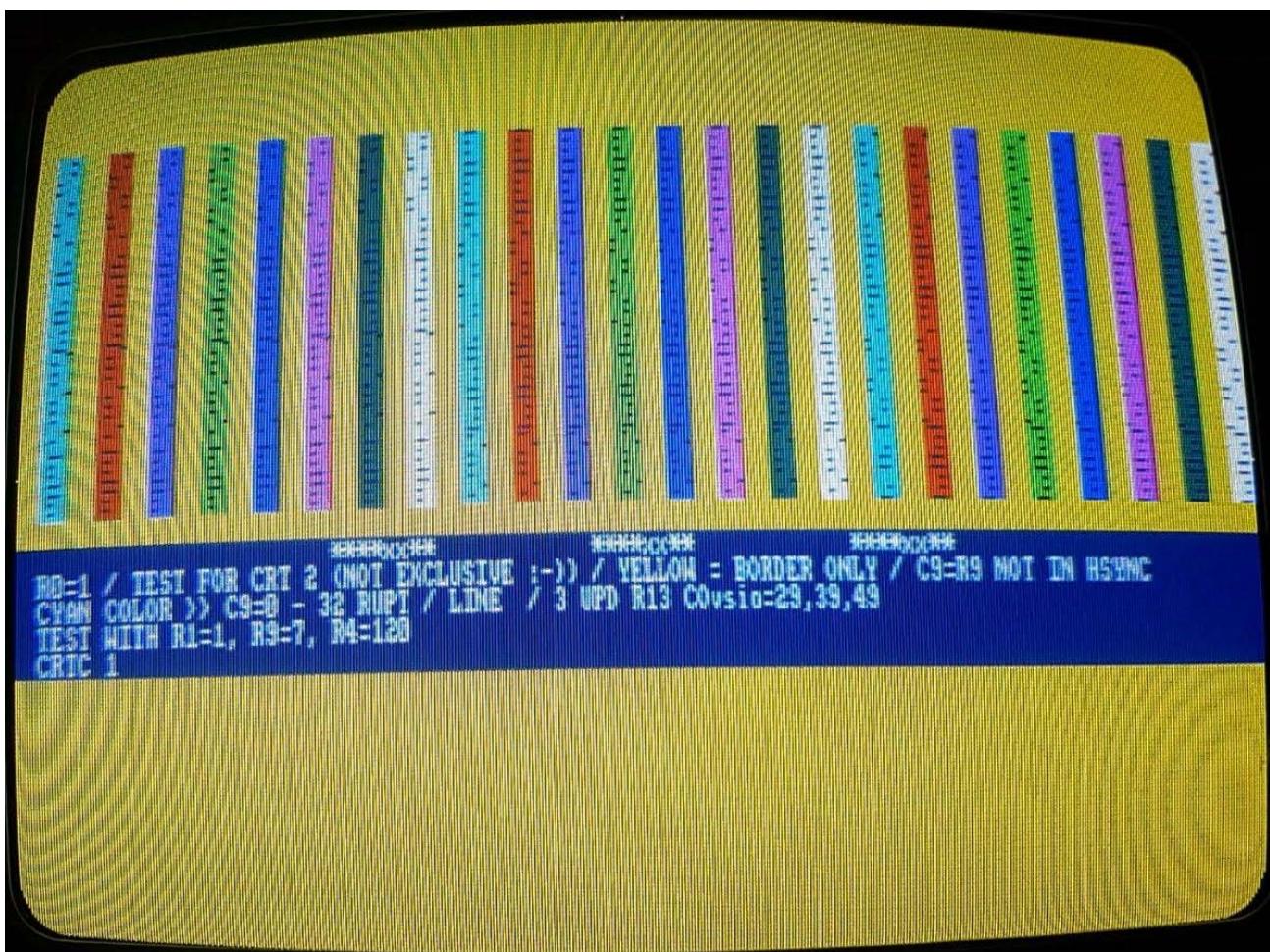


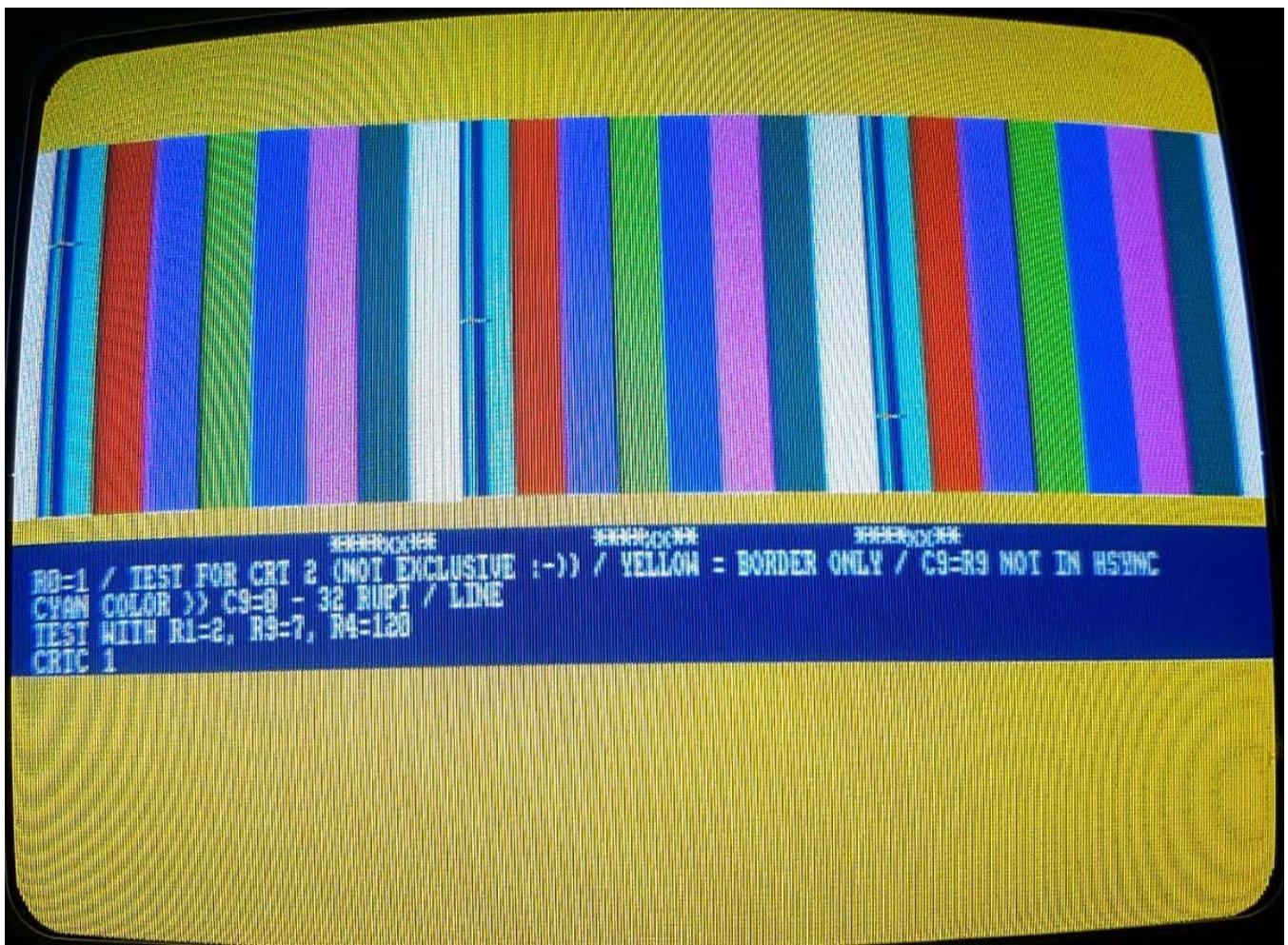
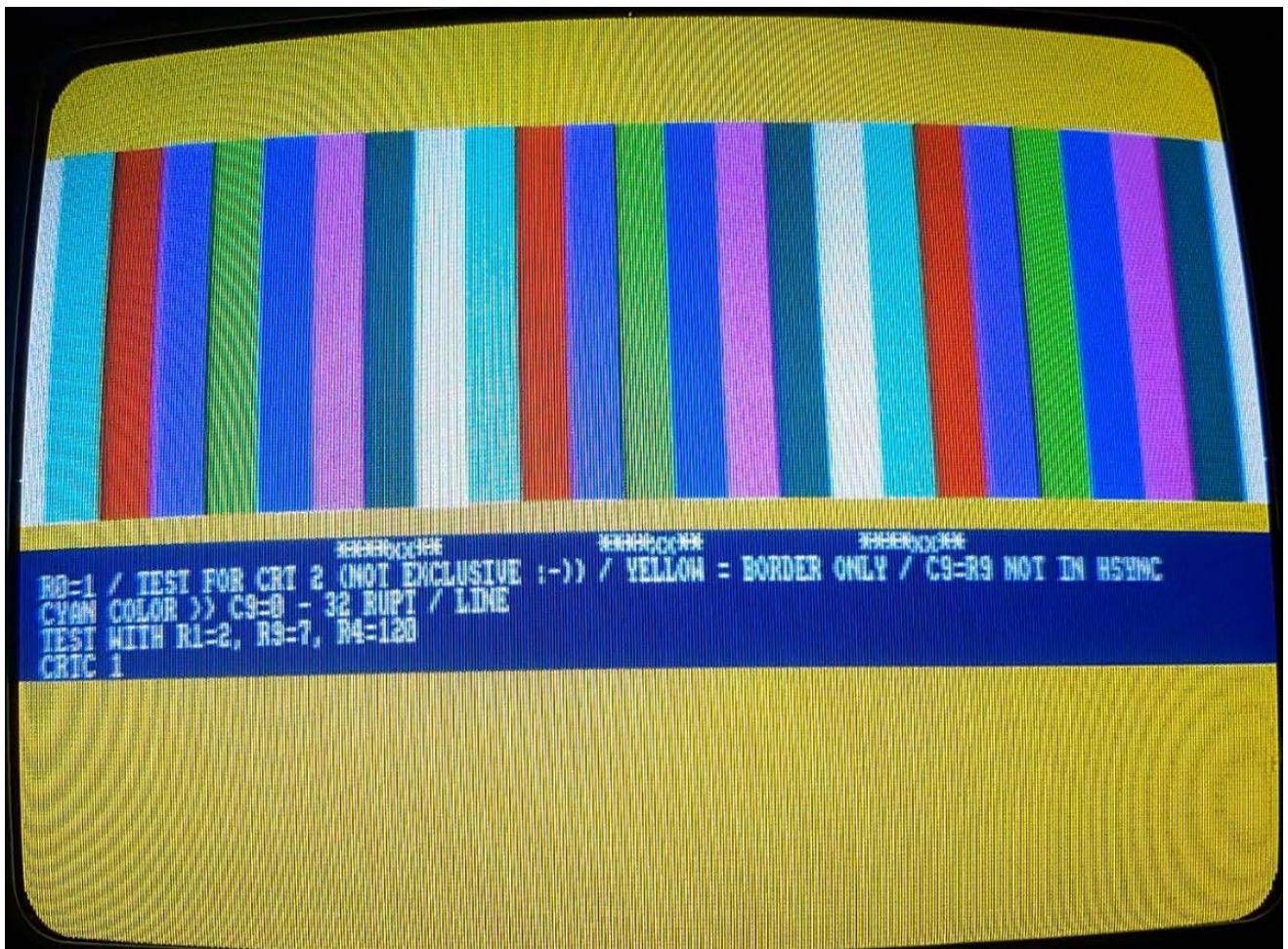


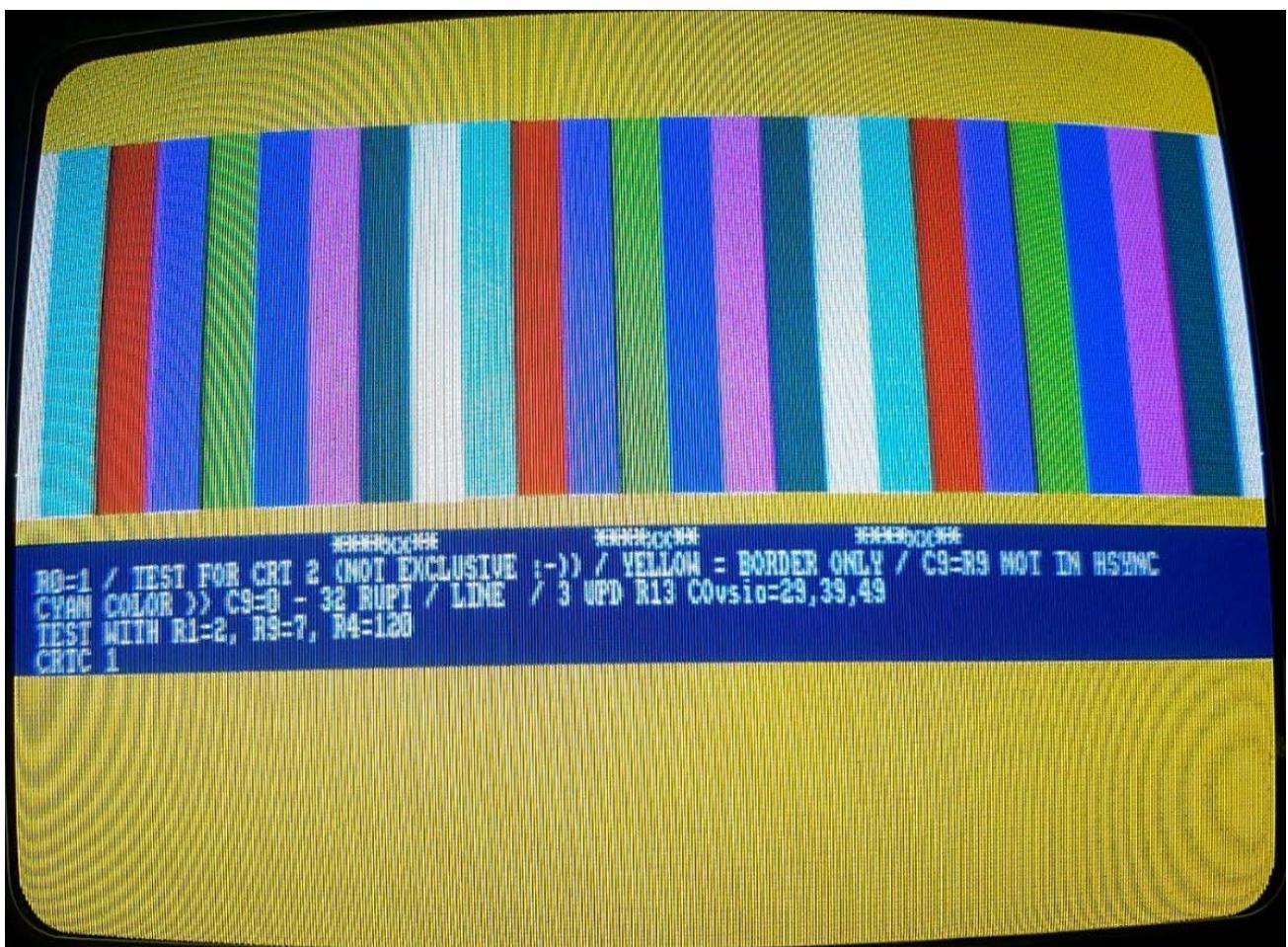
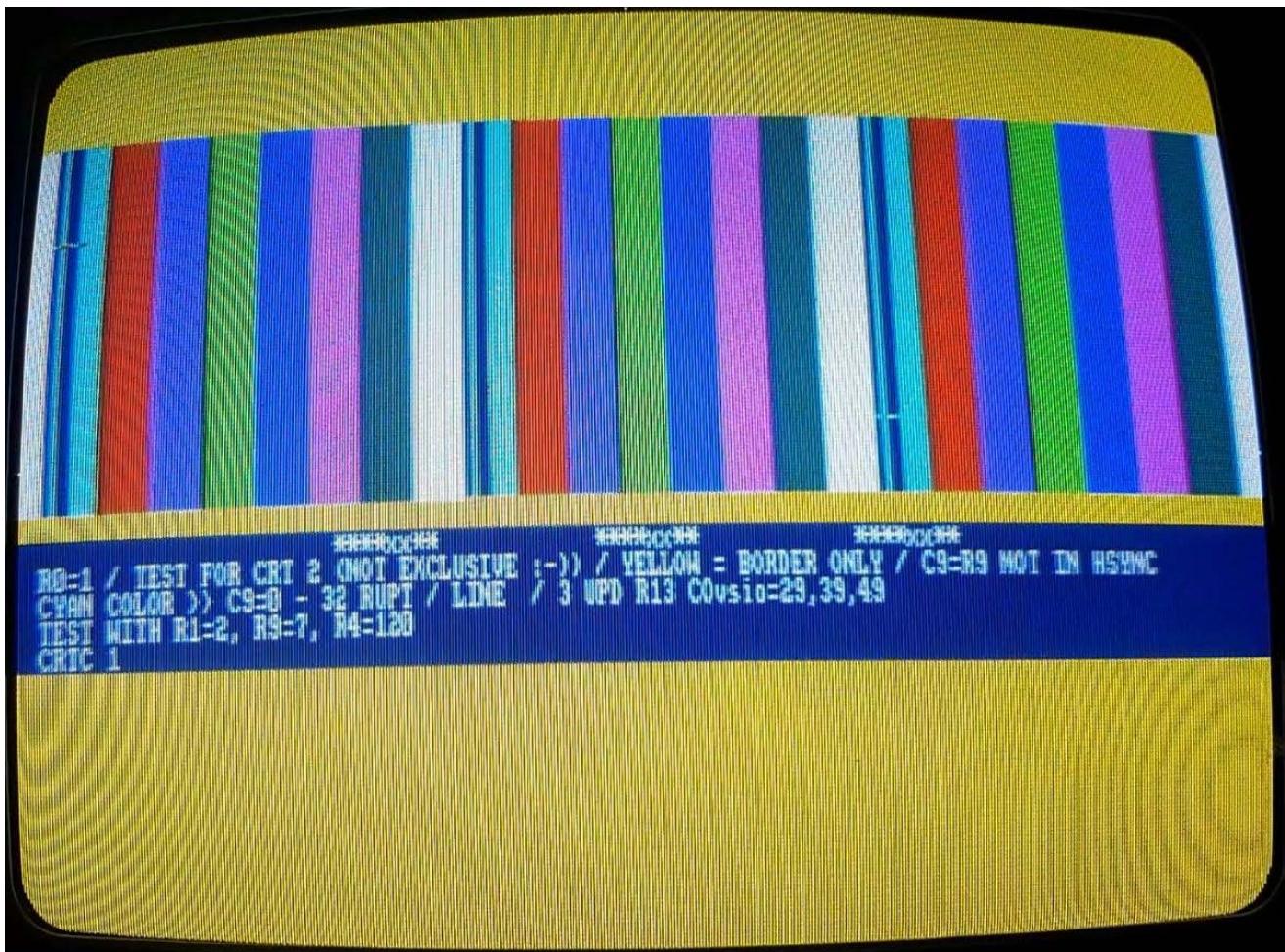






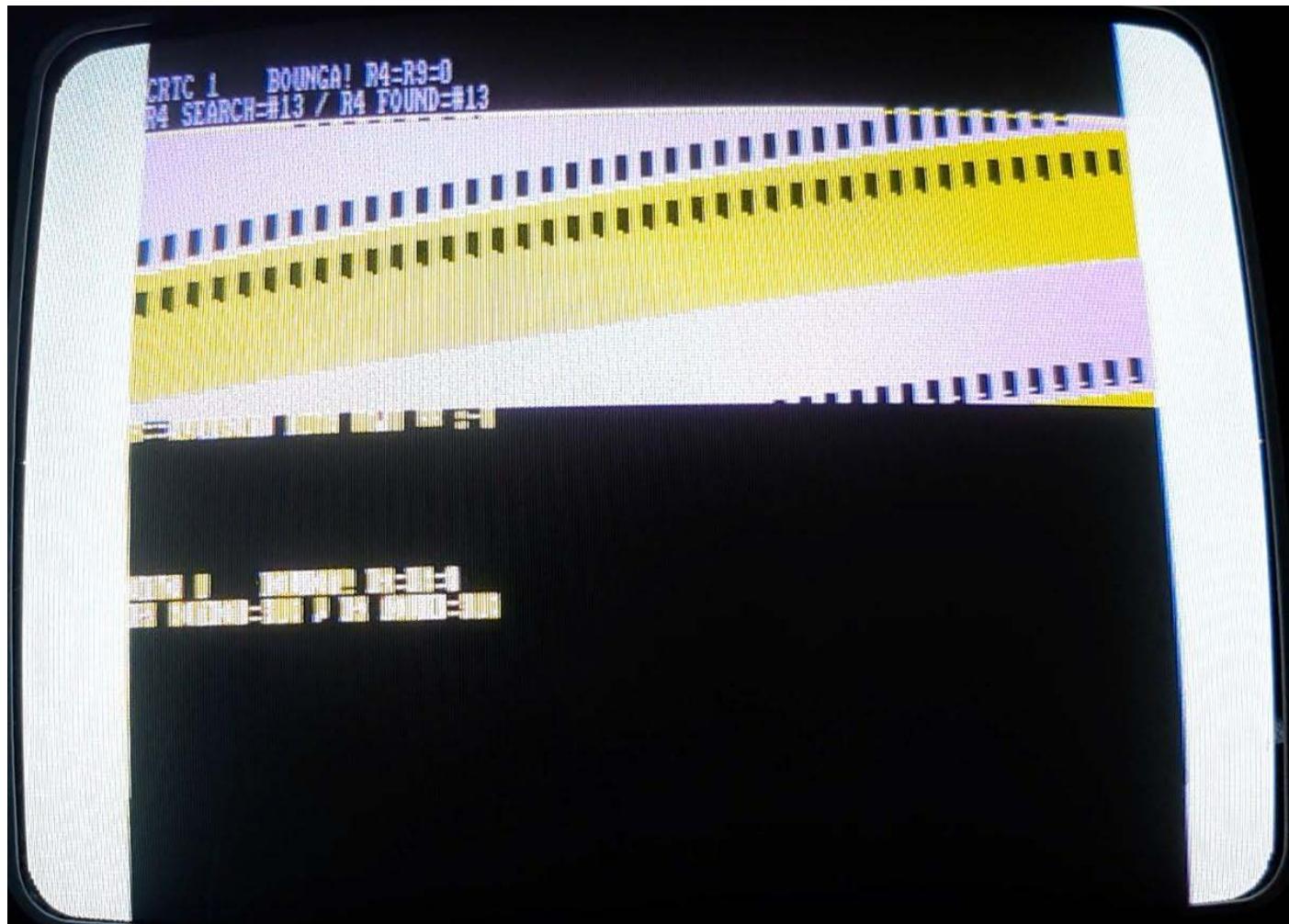






BOUNGA : CRTC 2 R4=R9=0 FORCED

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM  
(1) UPDATE VRAM VS CRTC (14 TST)  
(2) SKEW DISP ON R0 RUPTURE (5 TST)  
(3) INTERRUPT DELAY FROM R2 (18 CALC)  
(4) UPDATE CRTC R0 TIMING (7 TST)  
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)  
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)  
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)  
(8) GATE ARRAY PIXELISATION  
(9) GATE ARRAY INKERISATION (3 TST)  
(E) GATE ARRAY MODERISATION  
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)  
(T) R2 UPD DURING & AFTER HSYNC (6 TST)  
(Y) R3 UPD DURING HSYNC (8 TST)  
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))  
(I) VSYNC CONDITIONS (16 TST)  
(O) R1 STORIES (7 TST)  
(P) R6 STORIES (11 TST)  
(RETURN) RUNI LTD  
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)  
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)  
(COPY) CRTC 2 OFFSET  
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY  
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
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INTERLACE VM

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CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD_UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!

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MPC 1.1 INTERLACE VIDEO MODE
CALC WITH R6=#19:
R8=3 ON LINE 0 : FRAME SIZE=#2740 usec (R9=7)(R7=0)
R8=3 ON LINE 1 : FRAME SIZE=#2760 usec (R9=7)(R7=0)
R8=3 ON LINE 2 : FRAME SIZE=#2780 usec (R9=7)(R7=0)
R8=3 ON LINE 3 : FRAME SIZE=#2740 usec (R9=7)(R7=0)
R8=3 ON LINE 4 : FRAME SIZE=#2700 usec (R9=7)(R7=0)
R8=3 ON RASTER LINE 2 / R8=0 ON LINE 43 / FRAME SIZE=#4300 usec (R9=7)(R7=0)

CALC WITH R6=#79:
R8=3 ON LINE 0 : FRAME SIZE=#2740 usec (R9=7)(R7=0)
R8=3 ON LINE 1 : FRAME SIZE=#2760 usec (R9=7)(R7=0)
R8=3 ON LINE 2 : FRAME SIZE=#2780 usec (R9=7)(R7=0)
R8=3 ON LINE 3 : FRAME SIZE=#2740 usec (R9=7)(R7=0)
R8=3 ON LINE 4 : FRAME SIZE=#2700 usec (R9=7)(R7=0)
R8=3 ON RASTER LINE 2 / R8=0 ON LINE 43 / FRAME SIZE=#4300 usec (R9=7)(R7=0)

R7=18 BEFORE R6
CALC WITH R6:#19:
R8=3 ON LINE 0 : FRAME SIZE=#1820 usec (R9=7)(R7=0)
R8=3 ON LINE 1 : FRAME SIZE=#1860 usec (R9=7)(R7=0)
R8=3 ON LINE 2 : FRAME SIZE=#1860 usec (R9=7)(R7=0)
R8=3 ON LINE 3 : FRAME SIZE=#1840 usec (R9=7)(R7=0)
R8=3 ON LINE 4 : FRAME SIZE=#1840 usec (R9=7)(R7=0)
R8=3 ON RASTER LINE 2 / R8=0 ON LINE 43 / FRAME SIZE=#2500 usec (R9=7)(R7=0)

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MCU_1 INTERLACE VIDEO MODE

R8 UPDATE DELAY + 0 FRAME DELAY
R8-3 ON CB=0, CB=30 : FRAME SIZE=#2740 usec (R9=7)
R8-3 ON CB=0, CB=31 : FRAME SIZE=#2740 usec (R9=7)
R8-3 ON CB=0, CB=32 : FRAME SIZE=#2740 usec (R9=7)
R8-3 ON CB=1, CB=30 : FRAME SIZE=#2780 usec (R9=7)
R8-3 ON CB=1, CB=31 : FRAME SIZE=#2760 usec (R9=7)

R8 UPDATE DELAY + 1 FRAME DELAY
R8-3 ON CB=0, CB=30 : FRAME SIZE=#2740 usec (R9=7)
R8-3 ON CB=0, CB=31 : FRAME SIZE=#2740 usec (R9=7)
R8-3 ON CB=0, CB=32 : FRAME SIZE=#2740 usec (R9=7)
R8-3 ON CB=1, CB=30 : FRAME SIZE=#2780 usec (R9=7)
R8-3 ON CB=1, CB=31 : FRAME SIZE=#2760 usec (R9=7)

UPDATE DELAY + 1 FRAME DELAY

R8-3 ON CB=0, CB=30 : FRAME SIZE=#2740 usec (R9=7)
R8-3 ON CB=0, CB=31 : FRAME SIZE=#2740 usec (R9=7)
R8-3 ON CB=0, CB=32 : FRAME SIZE=#2740 usec (R9=7)
R8-3 ON CB=1, CB=30 : FRAME SIZE=#2780 usec (R9=7)
R8-3 ON CB=1, CB=31 : FRAME SIZE=#2760 usec (R9=7)

DELAY FOR EVEN+ODD FRAME (E/O R6=50/50, 7F/50, 50/7F, 7F/7F)

R8-3 ON LINE 0 : FRAME SIZE=#9060 usec (R9=7)(R7=0)
R8-3 ON LINE 0 : FRAME SIZE=#9060 usec (R9=7)(R7=0)
R8-3 ON LINE 0 : FRAME SIZE=#9060 usec (R9=7)(R7=0)
R8-3 ON LINE 0 : FRAME SIZE=#9060 usec (R9=7)(R7=0)

INTERLACE C4/C9 COUNTERS

CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM
(1) INTERLACE C4/C9 COUNTERS
(2) INTERLACE CRTC 2 C9 STRANGER THING
(3) FAKE VSYNC ON CRTC 2
(4) CRTC 2 FIND C0 MIN
(5) CRTC 2 RLAL
(6) CRTC 1 BUG OUTI R0

(S) BE00 CHECK (CRTC 1)

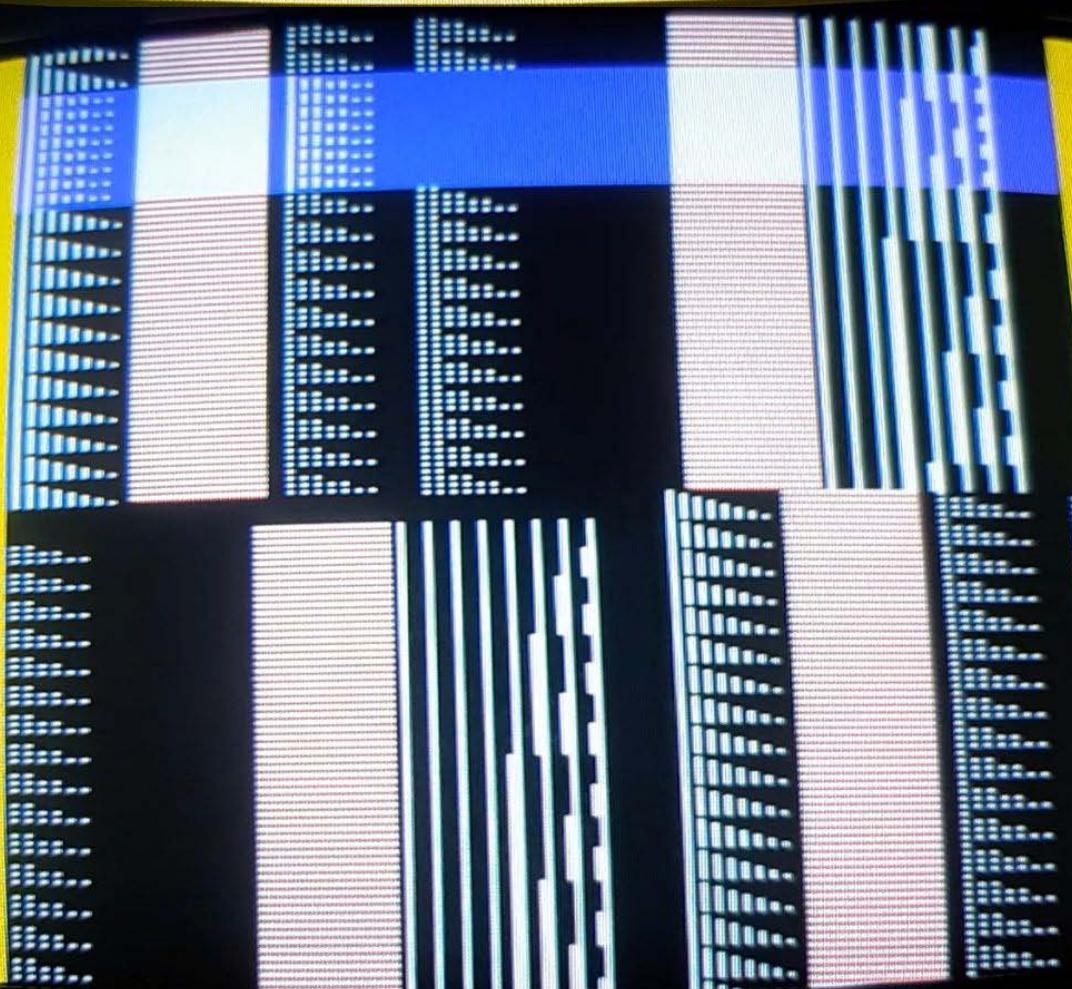
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!

CHIC 1 INTERFACE UN TESTS - C4/C9 COUNTING IN IWM PERIOD (NUMBER 2000)

NEXT SCREEN : C4=6, C9=0)) UPD R9=7, R8=3 (+3105)

EXIT IWM MODE ON C9=0)) UPD R9=7, R8=0

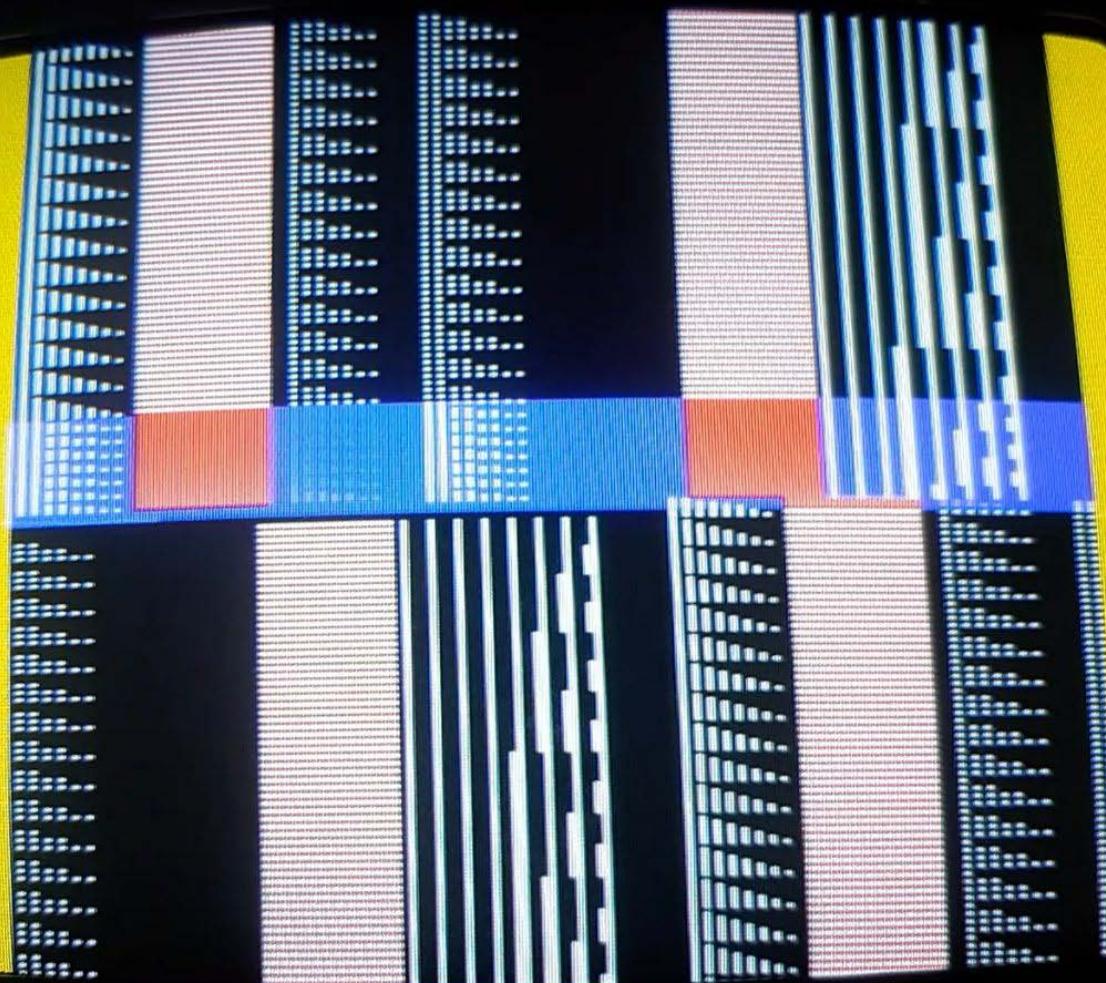
AUTOSHINC ON PREVIOUS SCREEN TEST: R4=bx R5=bx



CNIC 1 INTERFACE TM TESTS - C4/C9 COUNTING IN TM PERIOD (MODULE 2ND)

NEXT SCREEN : C4=6, C9=1 >> UPD R9=7, R8=3 (+3105)
EXIT TM MODE ON C9=0 >> UPD R9=7, R8=0

AUTOSYNC ON PREVIOUS SCREEN TEST: R4=H2A R5=#00

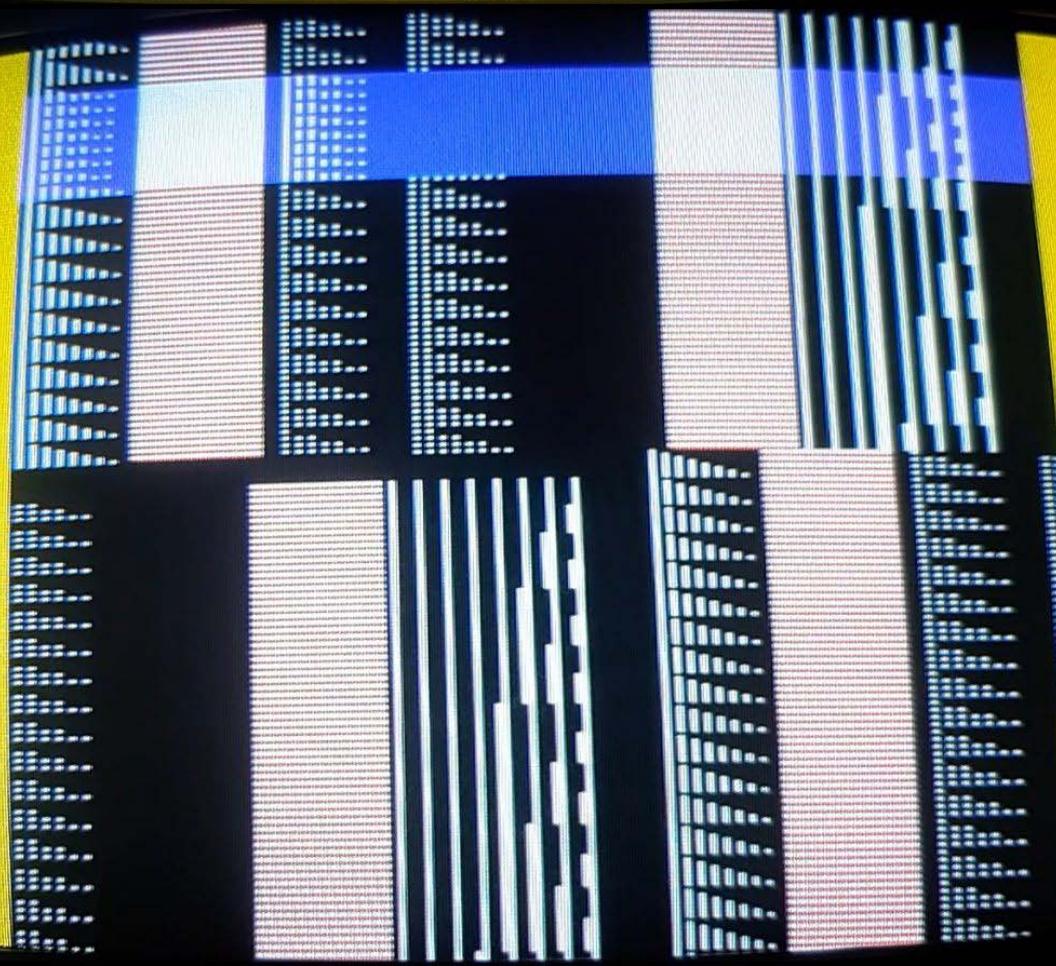


CRTC 1 INTERFACE ON TESTS - C4/C9 COUNTING IN IVM PERIOD (MOVE ZONE)

NEXT SCREEN : C4=5, C9=2 >> UPD R9=7, R8=3 (+3105)

EXIT IVM MODE ON C9=0 >> UPD R9=7, R8=0

AUTOSYNC ON PREVIOUS SCREEN TEST: R4=R29 R5=R06

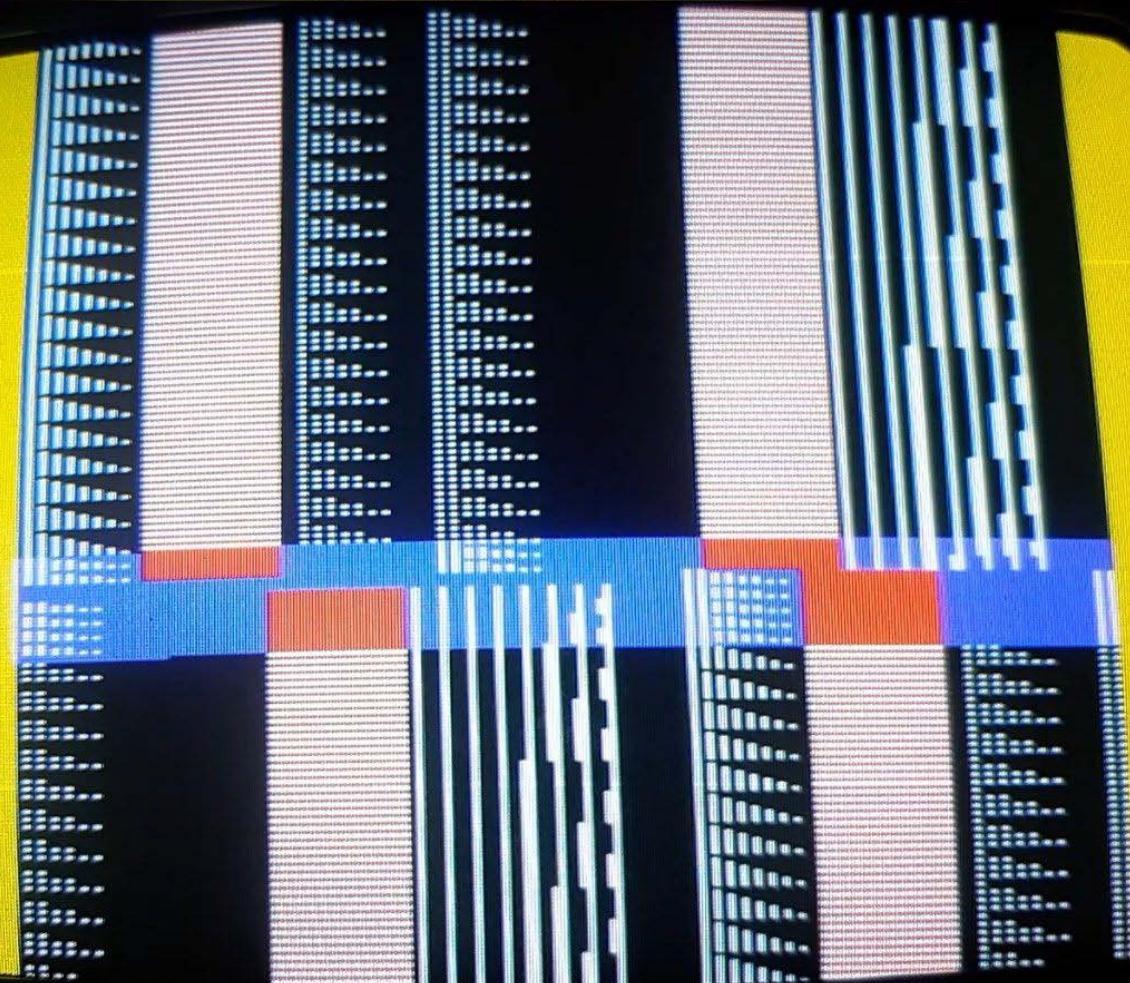


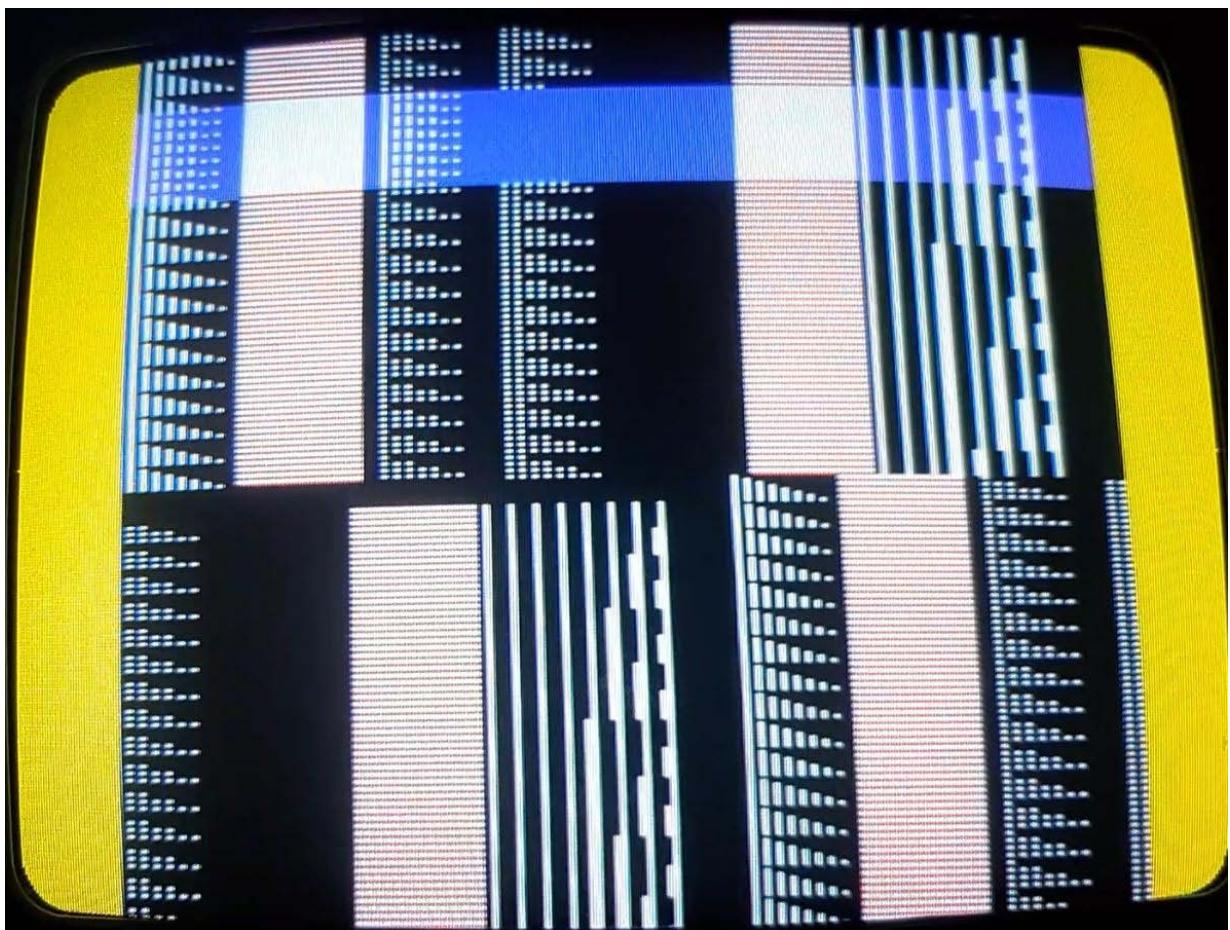
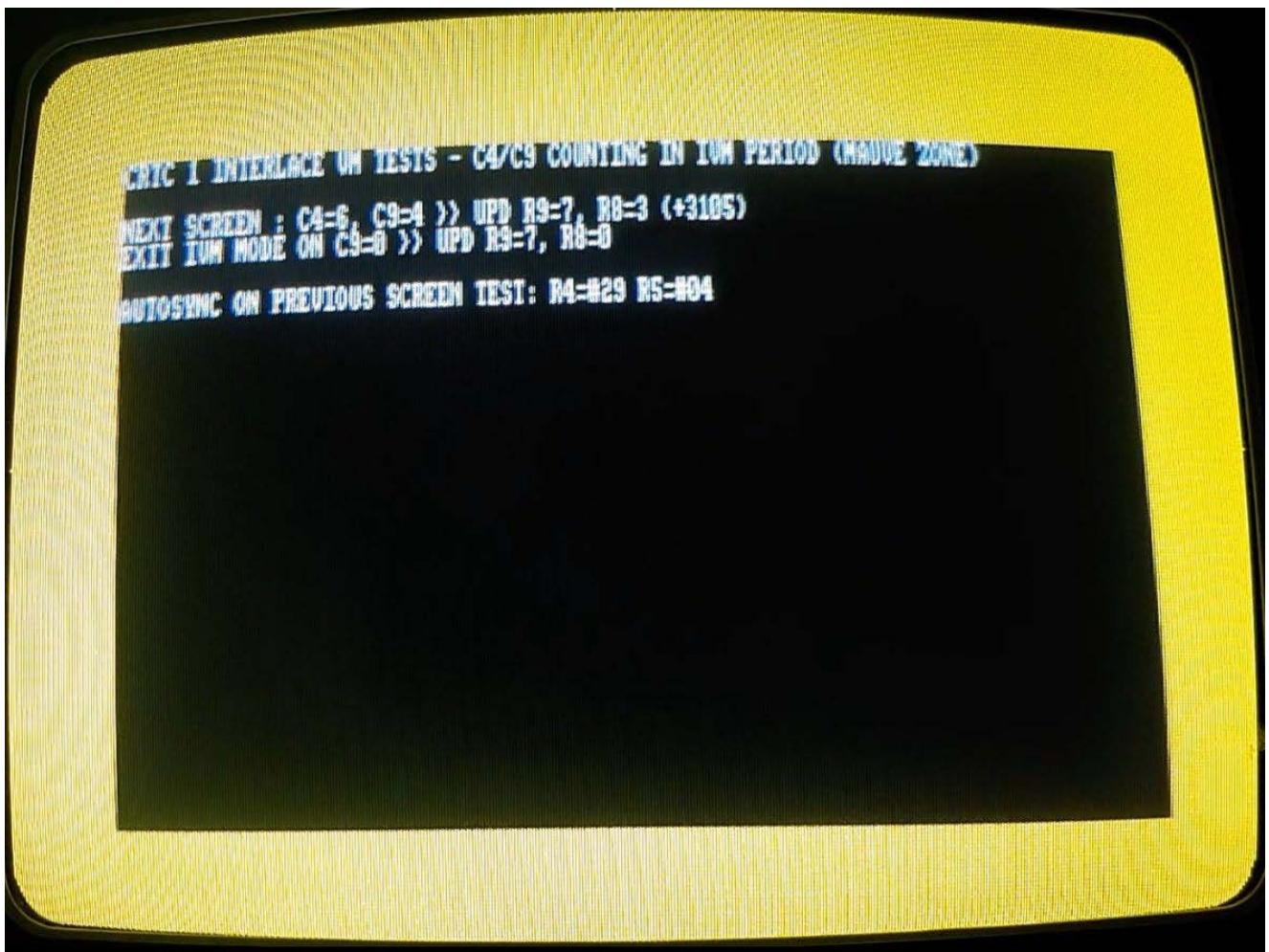
CHIC 1 INTERFACE UV TESTS - C4/C9 COUNTING IN IVM PERIOD (MOVE ZONE)

NEXT SCREEN : C4=6, C9=3 => UPD R9=7, R8=3 (+3105)

EXIT IVM MODE ON C9=0 => UPD R9=7, R8=0

AUTOSYNC ON PREVIOUS SCREEN TEST: R4=#29 R5=#06



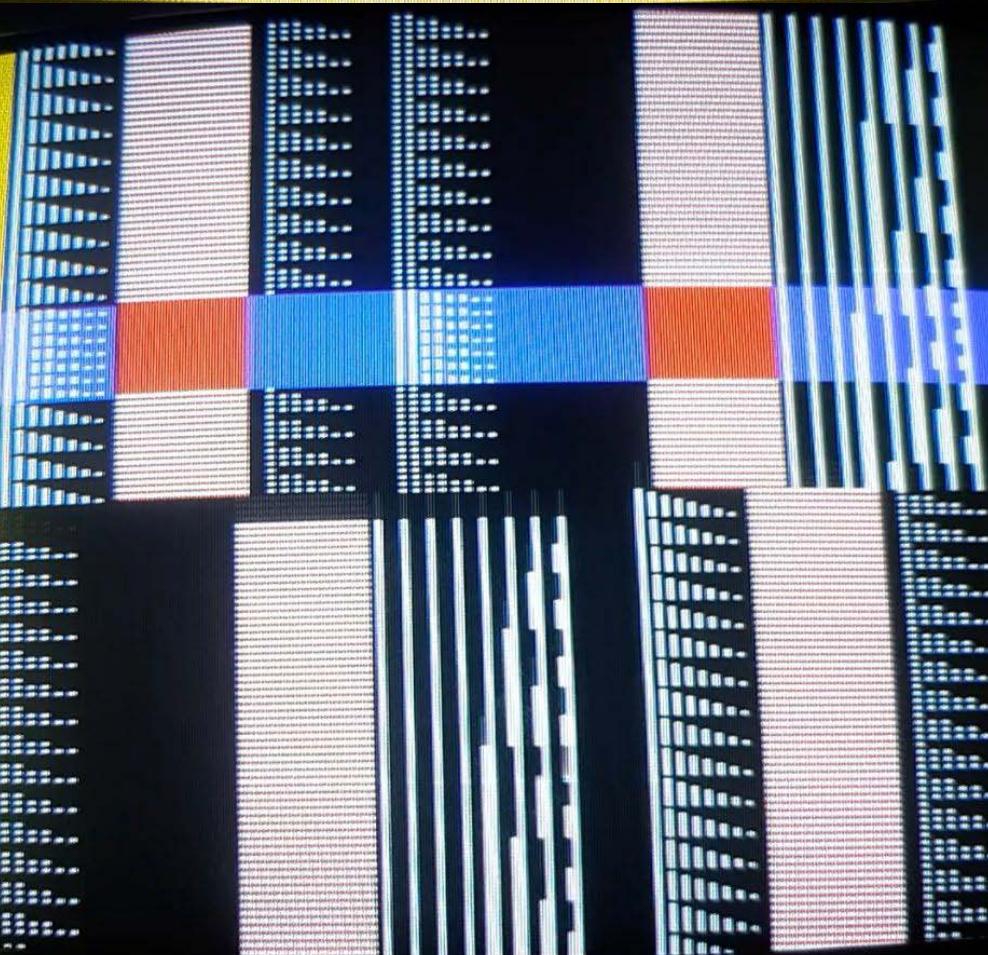


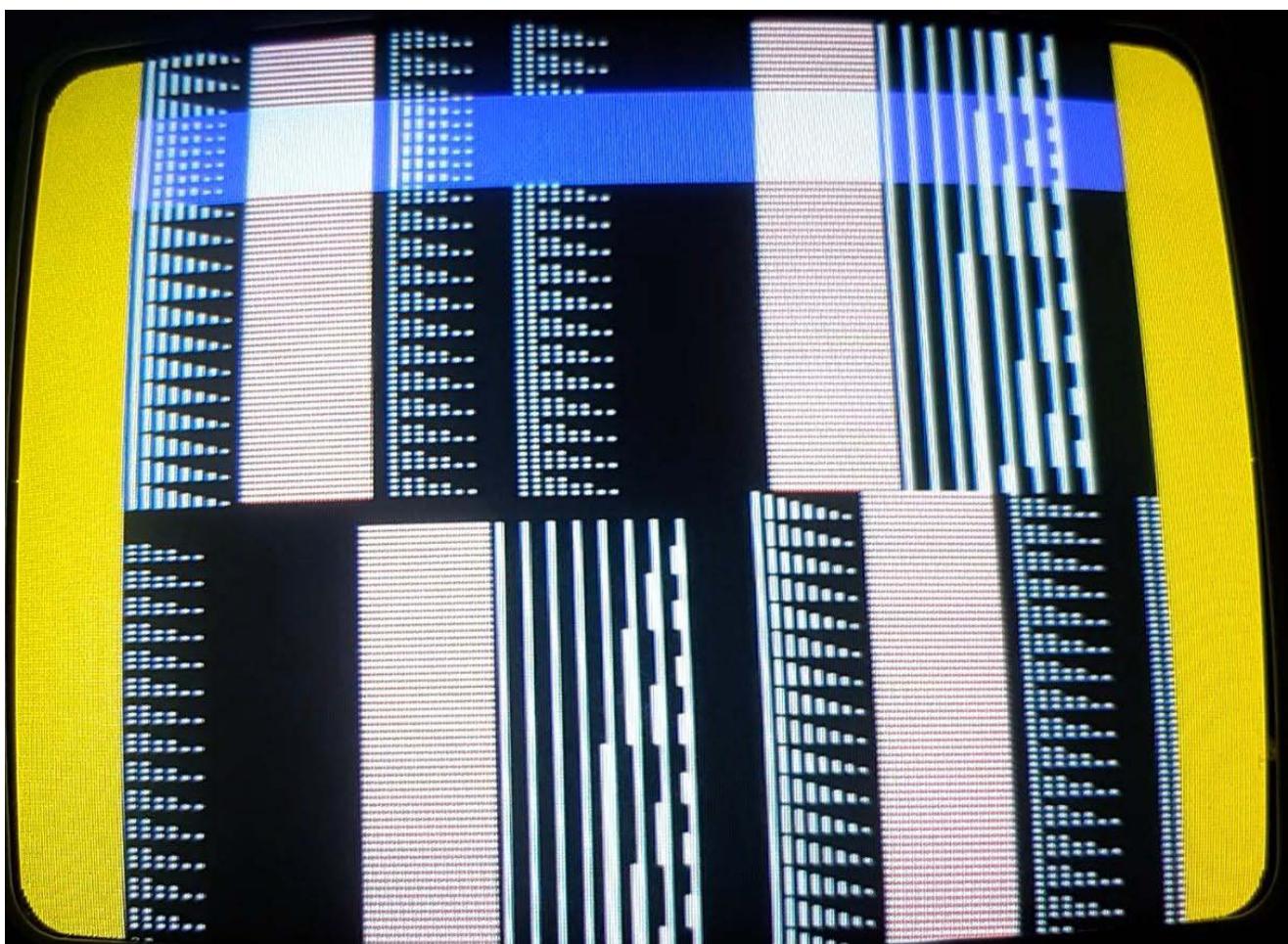
CRIC 1 INTERFACE UN TESTS - C4/C9 COUNTING IN IUM PERIOD (MAINT ZONE)

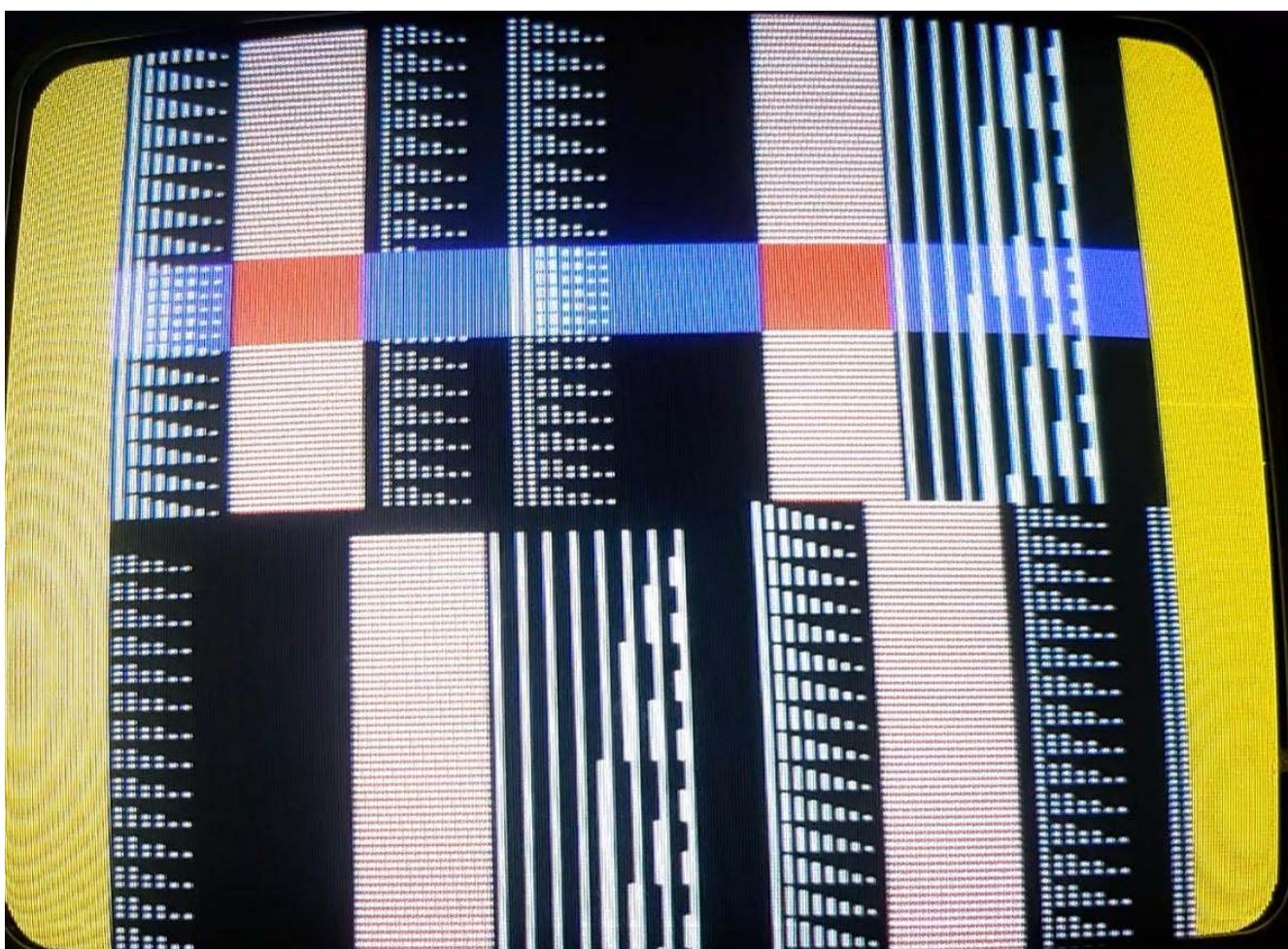
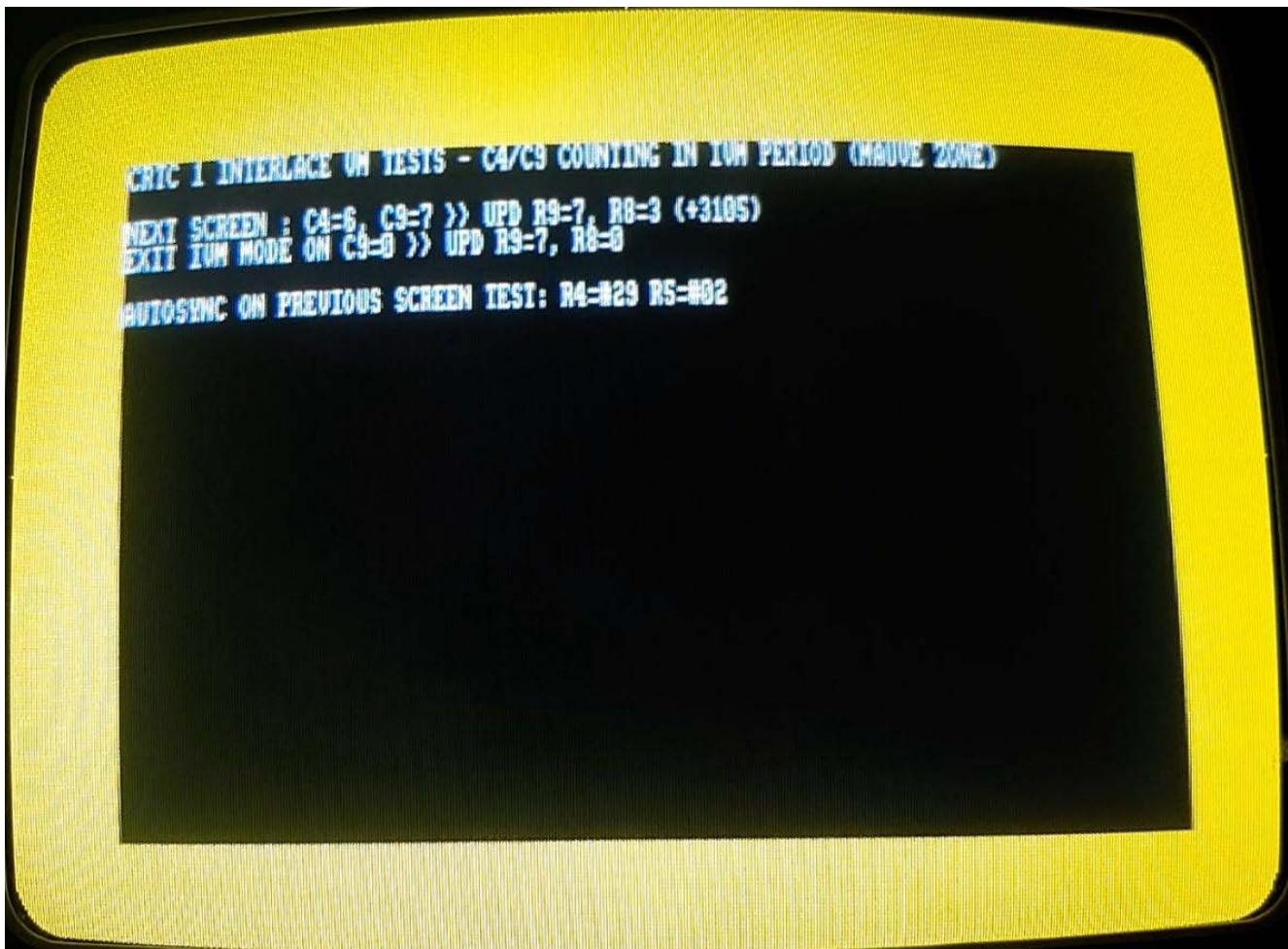
NEXT SCREEN : C4=6, C9=5 >> UPD R9=7, R8=3 (+3105)

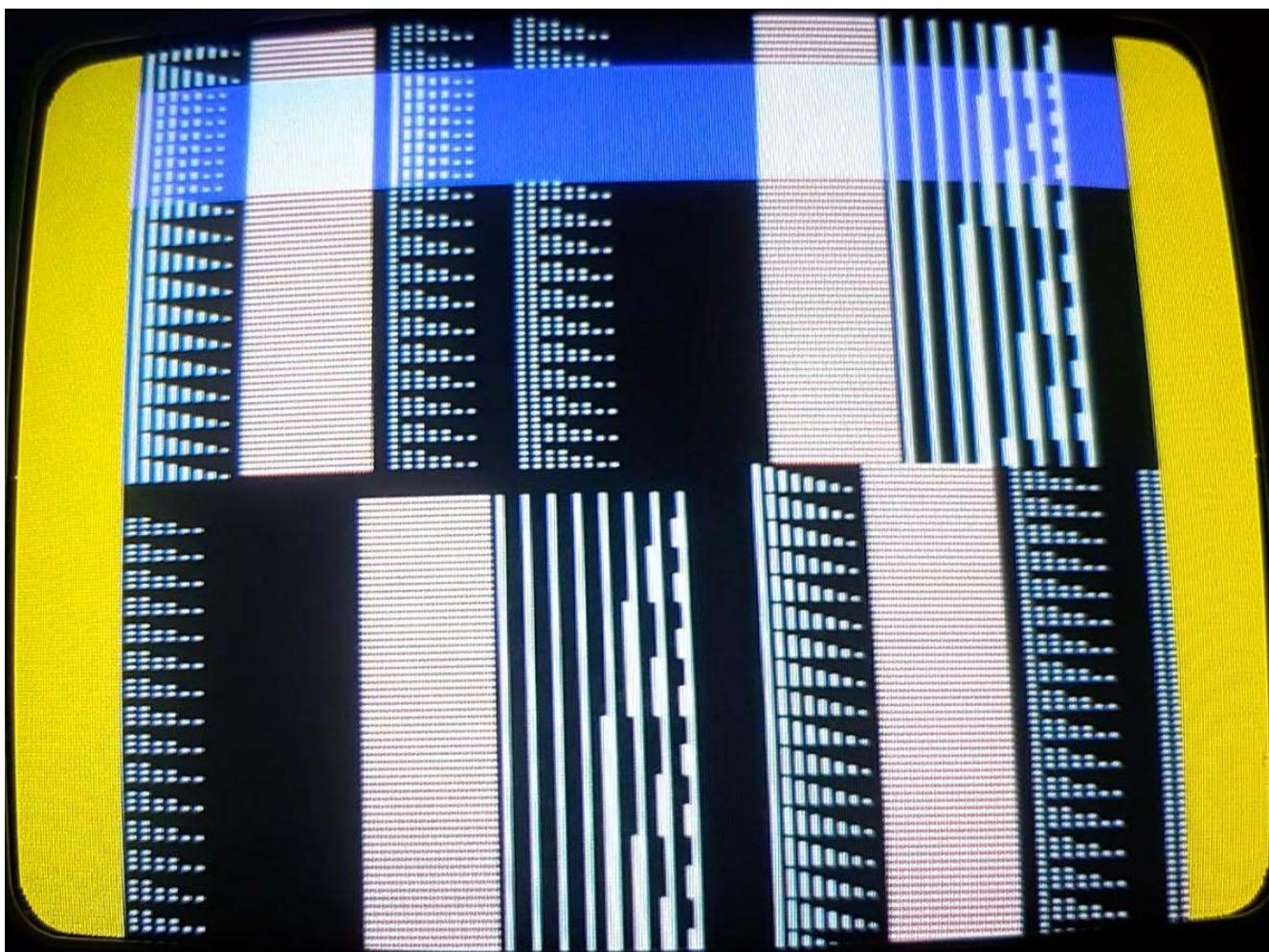
EXIT IUM MODE ON C9=0 >> UPD R9=7, R8=0

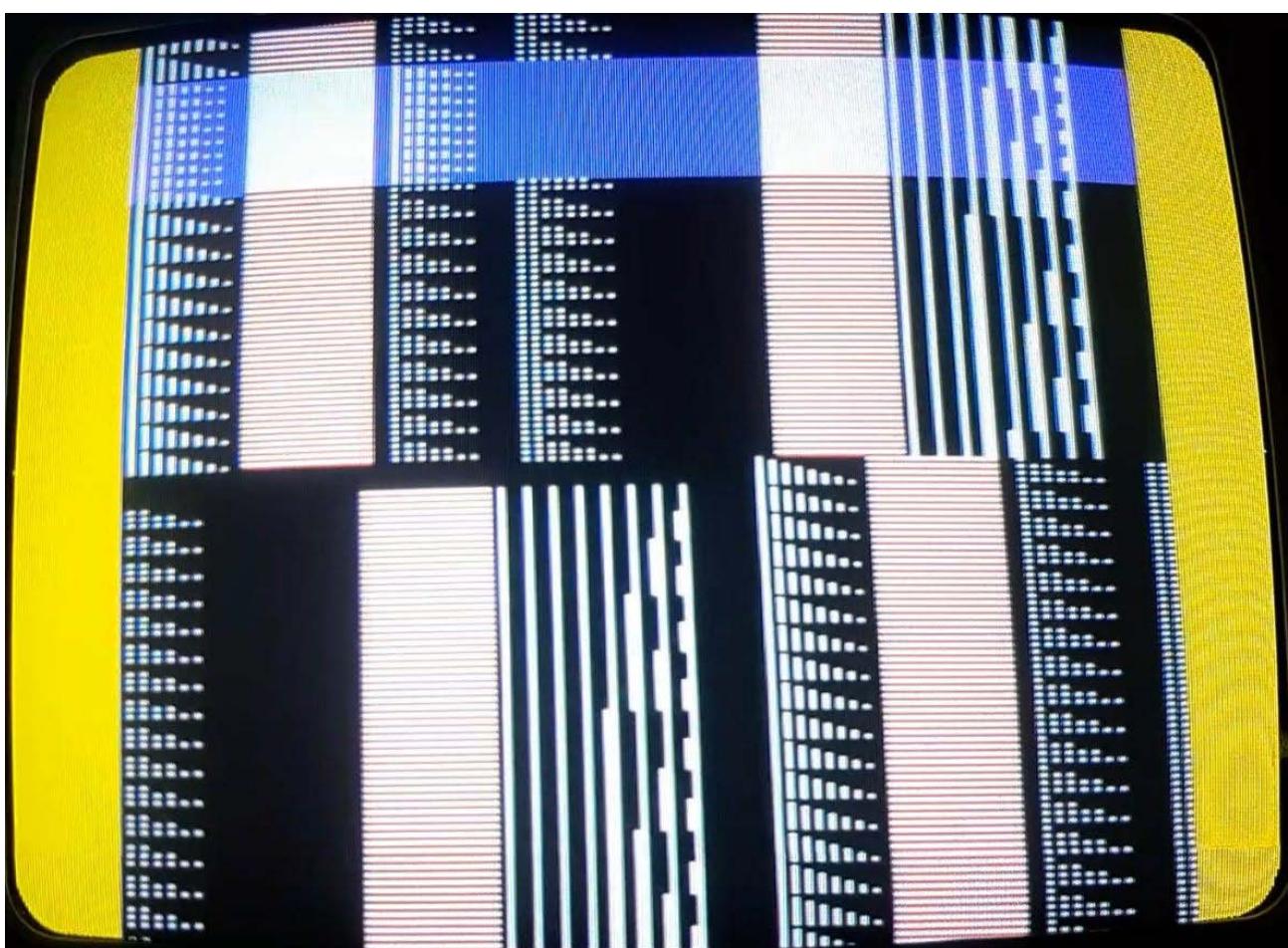
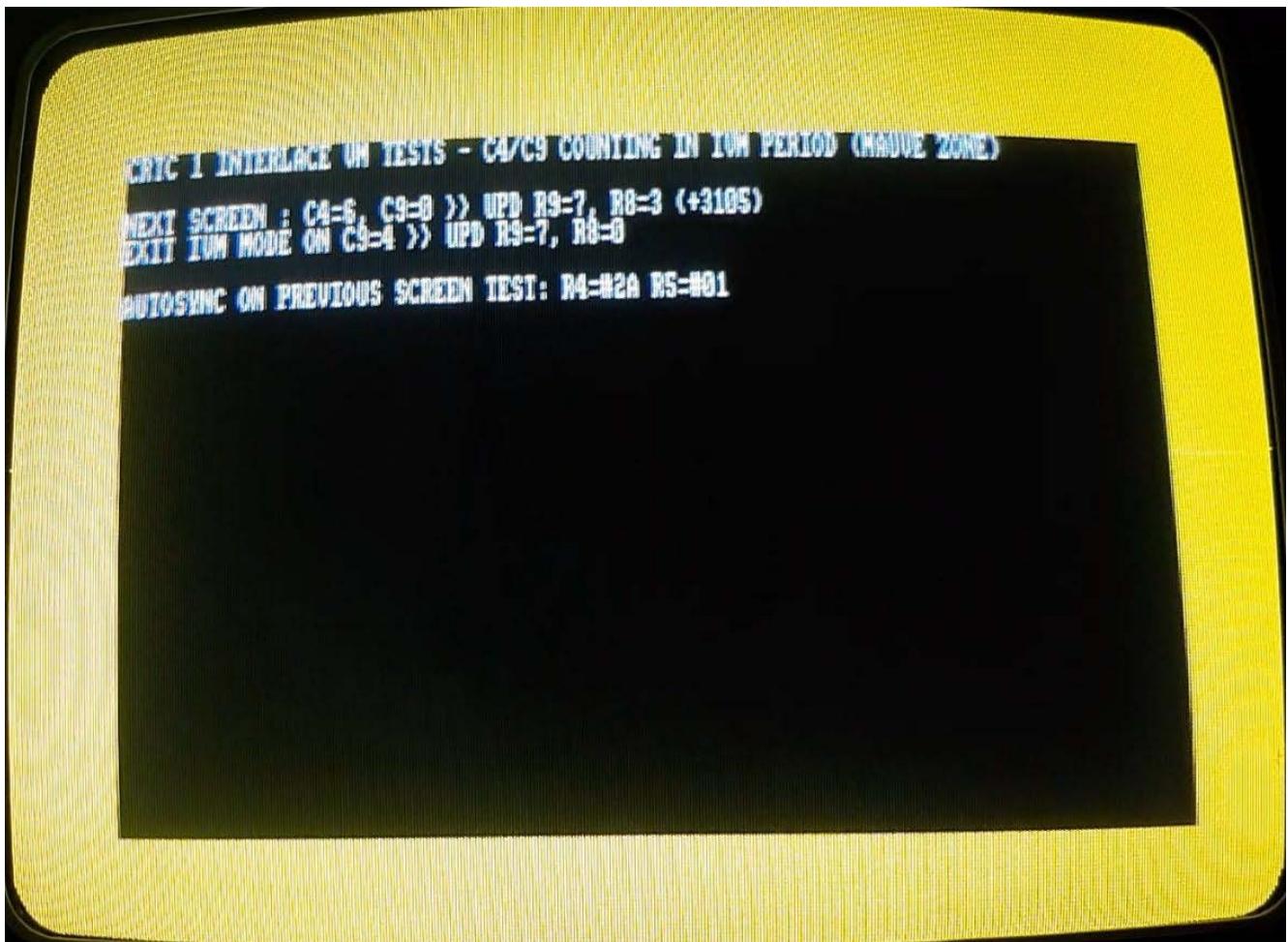
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=#29 R5=#04

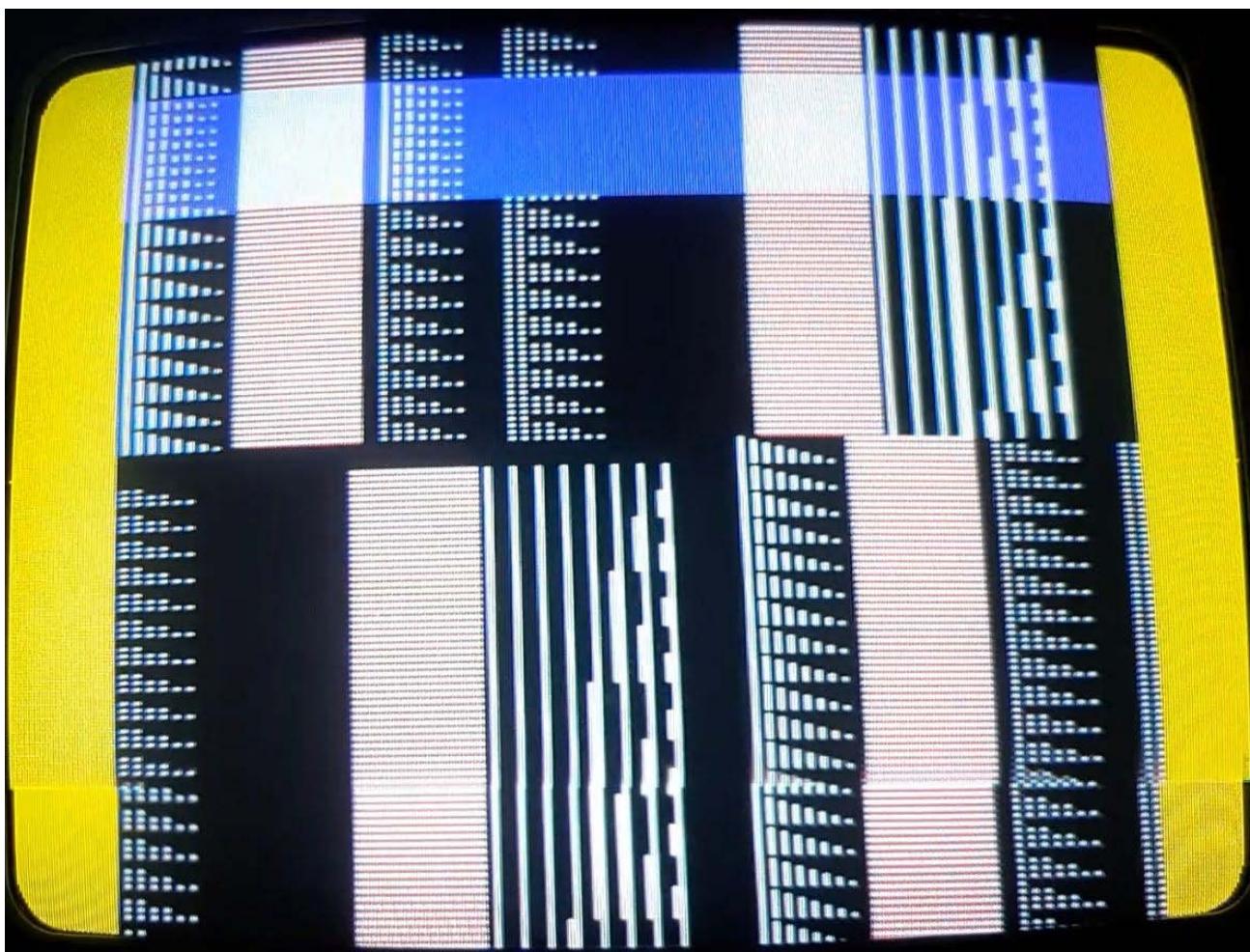
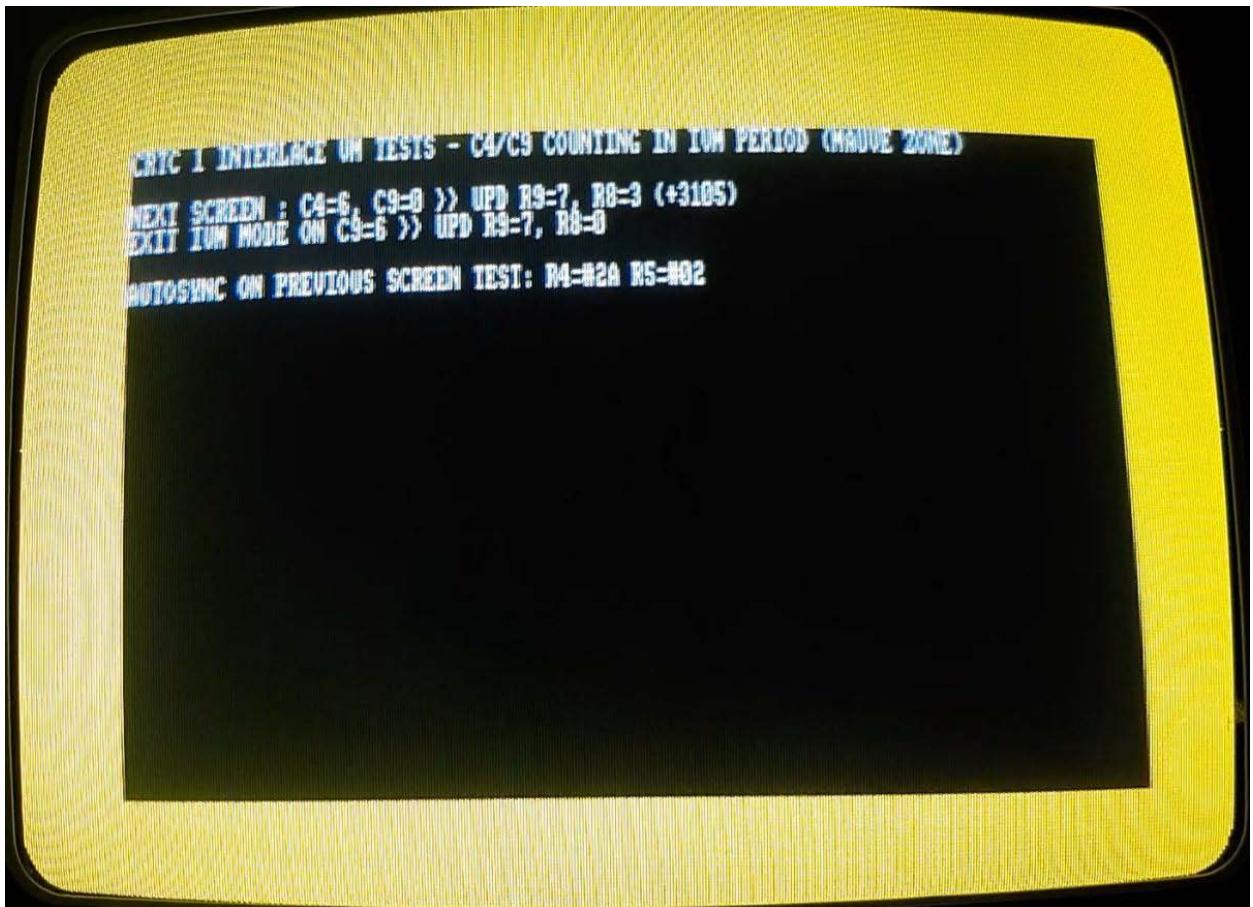












INTERLACE CRTC 2 C9 STRANGER THING

CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM
(1) INTERLACE C4/C9 COUNTERS
(2) INTERLACE CRTC 2 C9 STRANGER THING
(3) FAKE VSYNC ON CRTC 2
(4) CRTC 2 FIND C0 MIN
(5) CRTC 2 RLAL
(6) CRTC 1 BUG OUTI R0

(S) BE00 CHECK (CRTC 1)

(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!

TEST FOR CRTC 2

FAKE VSYNC ON CRTC 2

CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM
(1) INTERLACE C4/C9 COUNTERS
(2) INTERLACE CRTC 2 C9 STRANGER THING
(3) FAKE VSYNC ON CRTC 2
(4) CRTC 2 FIND C0 MIN
(5) CRTC 2 RLAL
(6) CRTC 1 BUG OUTI R0

(S) BE00 CHECK (CRTC 1)

(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!

EMULATING FAKE VSYNC VIA PPI PORT B MIDDLE SCREEN
FAKE VSYNC OK IF VSYNC BLACK BAND

EMULATING FAKE VSYNC VIA PPI PORT B MIDDLE SCREEN
FAKE VSYNC OK IF VSYNC BLACK BAND

LETTING FAKE USING DIA PPI PORT B FROM LCD SCREEN
FAKE USING ON LF USING BLACK BAND

CRTC 1

CRTC 2 FIND C0 MIN

CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM
(1) INTERLACE C4/C9 COUNTERS
(2) INTERLACE CRTC 2 C9 STRANGER THING
(3) FAKE VSYNC ON CRTC 2
(4) CRTC 2 FIND C0 MIN
(5) CRTC 2 RVAL
(6) CRTC 1 BUG OUTI R0

(S) BE00 CHECK (CRTC 1)

(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!

TEST FOR CRTC 2

CRTC 2 - 1 LINE RUPTURE

CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM
(1) INTERLACE C4/C9 COUNTERS
(2) INTERLACE CRTC 2 C9 STRANGER THING
(3) FAKE VSYNC ON CRTC 2
(4) CRTC 2 FIND C0 MIN
(5) CRTC 2 RAL
(6) CRTC 1 BUG OUTI R0

(S) BE00 CHECK (CRTC 1)

(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!

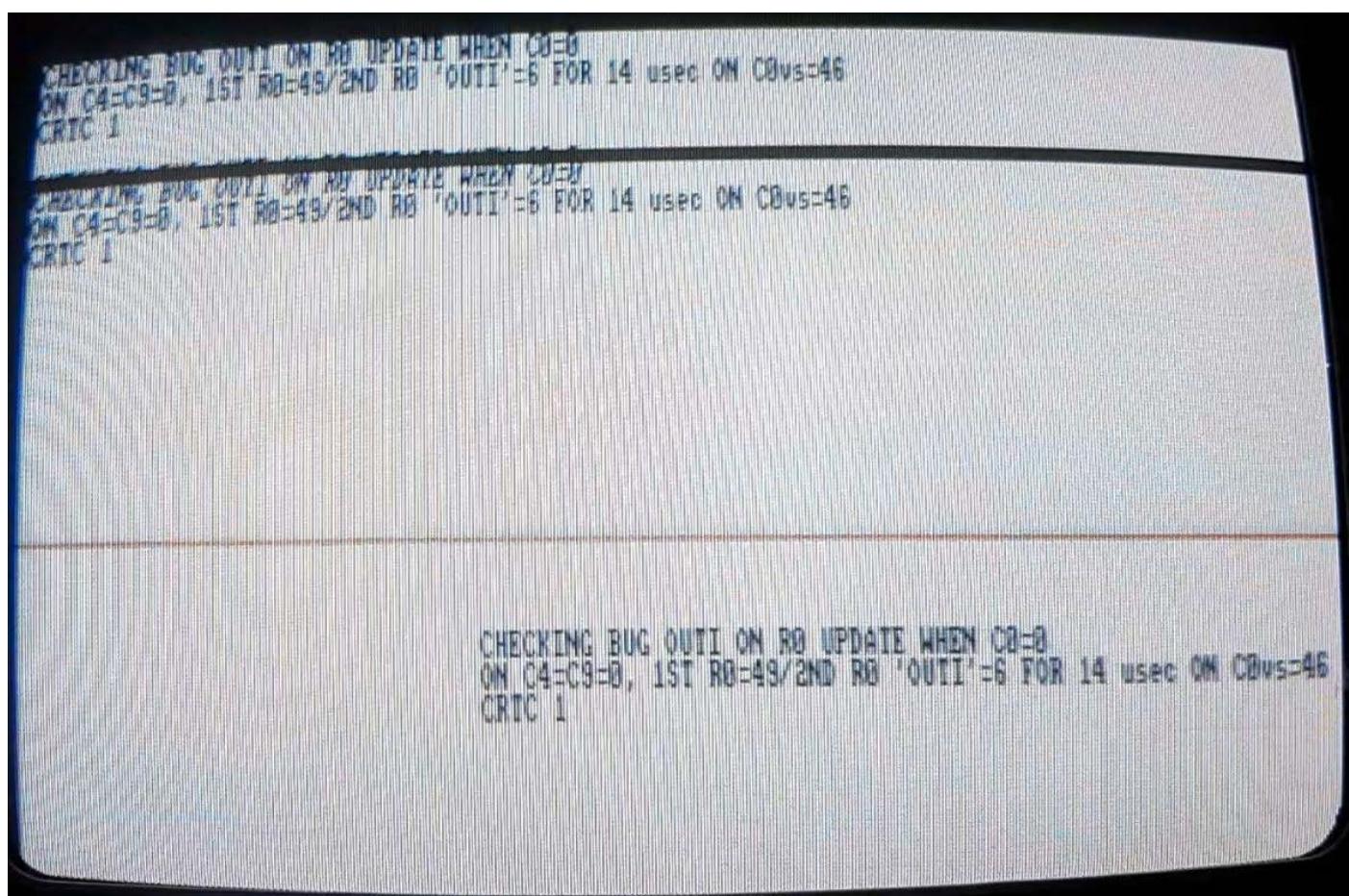
TEST FOR CRTC 2

CRTC 1 - BUG OUTI R0

- CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM
- (1) INTERLACE C4/C9 COUNTERS
- (2) INTERLACE CRTC 2 C9 STRANGER THING
- (3) FAKE VSYNC ON CRTC 2
- (4) CRTC 2 FIND C0 MIN
- (5) CRTC 2 RLAL
- (6) CRTC 1 BUG OUTI R0

(S) BE00 CHECK (CRTC 1)

(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!



CHECKING BUG OUTI ON RD UPDATE WHEN CD=0
ON C4=C9=0, 1ST RD=49/2ND RD 'OUT(C),r8'=6 FOR 14 usec ON CDvs=48
CRTC 1

- CHECKING BUG OUTI ON RD UPDATE WHEN CD=0
ON C4=C9=0, 1ST RD=49/2ND RD 'OUT(C),r8'=6 FOR 14 usec ON CDvs=48
CRTC 1

CHECKING BUG OUTI ON RD UPDATE WHEN CD=0
ON C4=C9=0, 1ST RD=49/2ND RD 'OUT(C),r8'=6 FOR 14 usec ON CDvs=48
CRTC 1

CRTC 1- BE00 CHECK

CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM
(1) INTERLACE C4/C9 COUNTERS
(2) INTERLACE CRTC 2 C9 STRANGER THING
(3) FAKE VSYNC ON CRTC 2
(4) CRTC 2 FIND C0 MIN
(5) CRTC 2 RAL
(6) CRTC 1 BUG OUTI R0

(S) BE00 CHECK (CRTC 1)

(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!

CRTC 1 - BE00 CHECK
FROM C0=#39 BEFORE 1ST LIGNE (C9=C0=C4=0), EVERY 6 USEC (IMI+INC B) :
20,00,00,00,00,00,00,00,00,00,00,00,00,00,00,00
FROM C0=#20 ON VERY LAST LINE BEFORE C4=R6, EVERY 6 USEC (IMI+INC B) :
00,00,00,00,20,20,20,20,20,20,20,20,20,20,20,20
FIRST DETECTION (BIT 5=0) WITH IN A,(C) WHEN C0=#3D
FIRST DETECTION (BIT 5=1) WITH IN A,(C) WHEN C0=#3D
STATUS WHILE R6=0 IN DISPLAY AREA (C4=1,C9=0):#00
STATUS WHILE R6=0 IN DISPLAY AREA (C4=1,C9=1):#00

STATUS BEFORE R31 SEL:#20 AFTER SEL:#20
STATUS 5 US AFTER R31 READ:#20 READ VALUE:#FF
STATUS 5 US AFTER R31 WRITE:#20
STATUS 4 US AFTER STATUS READ:#20
READ R31, LOOKING STATUS UPDATE IN FULL FRAME (0:NO/1 YES):#01