

AMSTRAD CPC / CRTC 2

SHAKER V1.8 OUTPUT

LOGON SYSTEM 2021 / LONGSHOT

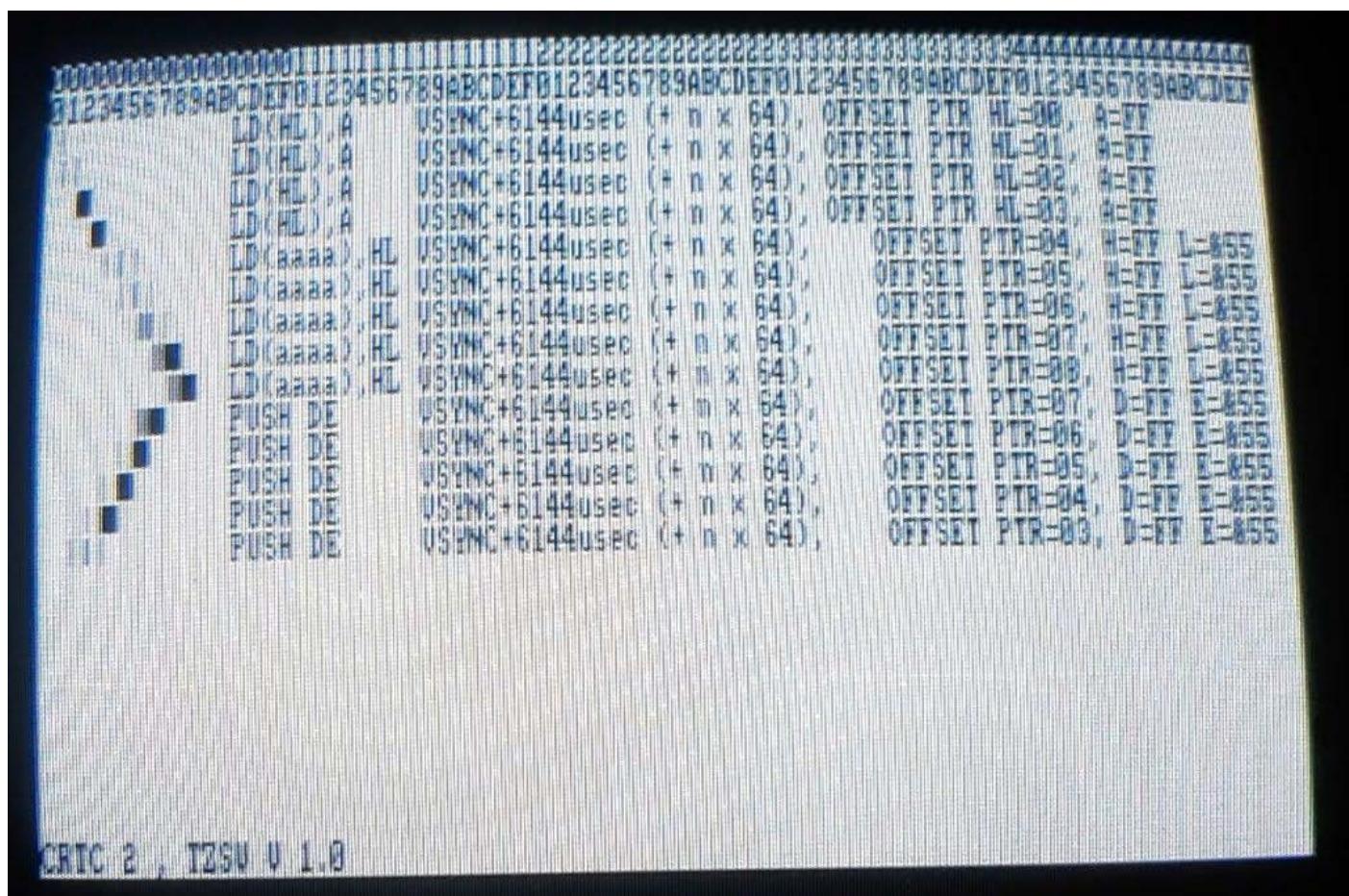
More information about CRTC in Amstrad Cpc Crtc Compendium
("con de chat canadien")

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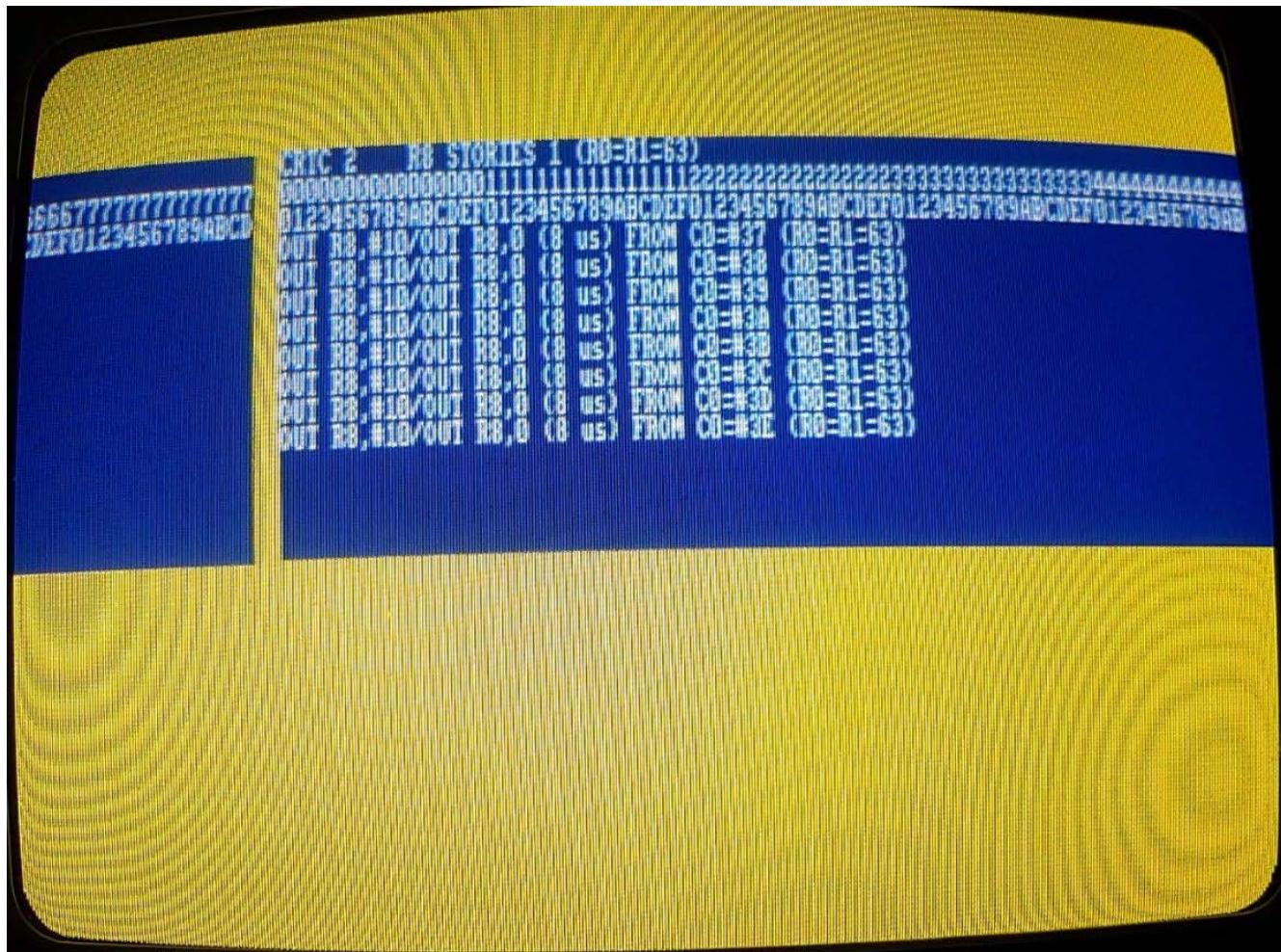
UPDATE VRAM VS CRTC

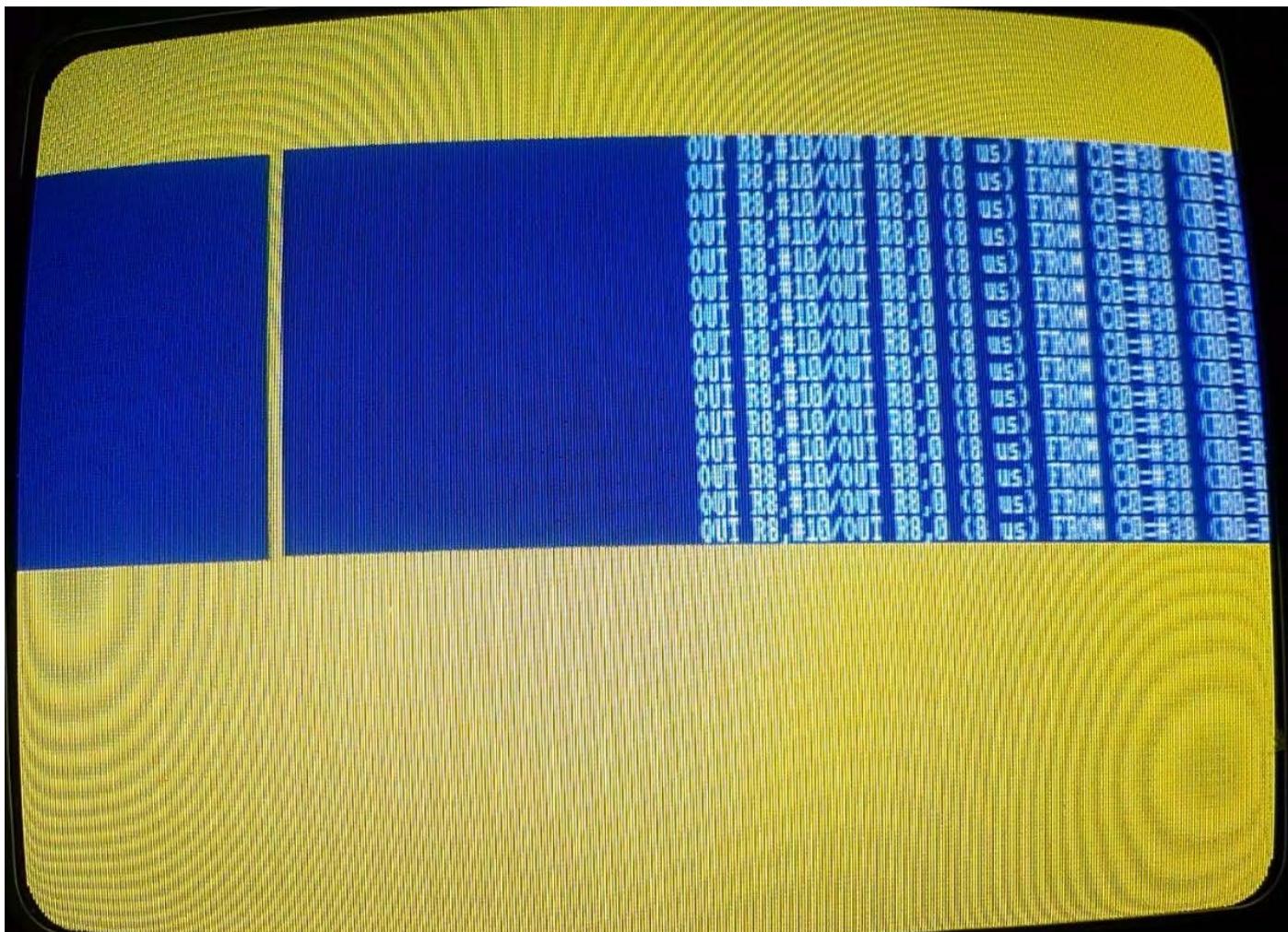
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST) (0) CRTC 2 RUMB
(2) SKEW DISP ON R0 RUPTURE (5 TST) (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC) (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
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(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!



SKEW DISP ON RO RUPTURE

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON RO RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC RO TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
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(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
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!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!





```
OUT R8, #10/OUT R8,0 (8 us) FROM CB-#38 (R8-R)
OUT R8, #10/OUT R8,0 (8 us) FROM CB-#38 (R8-R)
OUT R8, #10/OUT R8,0 (8 us) FROM CB-#38 (R8-R)
OUT R8, #10/OUT R8,0 (8 us) FROM CB-#38 (R8-R)
OUT R8, #10/OUT R8,0 (8 us) FROM CB-#38 (R8-R)
OUT R8, #10/OUT R8,0 (8 us) FROM CB-#38 (R8-R)
OUT R8, #10/OUT R8,0 (8 us) FROM CB-#38 (R8-R)
OUT R8, #10/OUT R8,0 (8 us) FROM CB-#38 (R8-R)
OUT R8, #10/OUT R8,0 (8 us) FROM CB-#38 (R8-R)
OUT R8, #10/OUT R8,0 (8 us) FROM CB-#38 (R8-R)
OUT R8, #10/OUT R8,0 (8 us) FROM CB-#38 (R8-R)
OUT R8, #10/OUT R8,0 (8 us) FROM CB-#38 (R8-R)
OUT R8, #10/OUT R8,0 (8 us) FROM CB-#38 (R8-R)
OUT R8, #10/OUT R8,0 (8 us) FROM CB-#38 (R8-R)
OUT R8, #10/OUT R8,0 (8 us) FROM CB-#38 (R8-R)
```

INTERRUPT DELAY FROM R2

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE URAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
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(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
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(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT < CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```

```
DELAY BETWEEN VSYNC (C0ER2) AND INTERRUPTION (INT)
WHEN R2=0E, INTERRUPT OCCURS #0F USEC AFTER C0=R2 (#FF=NO INT)
WHEN R2=0D, INTERRUPT OCCURS #0E USEC AFTER C0=R2 (#FF=NO INT)
WHEN R2=0C, INTERRUPT OCCURS #0D USEC AFTER C0=R2 (#FF=NO INT)
WHEN R2=0B, INTERRUPT OCCURS #0C USEC AFTER C0=R2 (#FF=NO INT)
WHEN R2=0A, INTERRUPT OCCURS #0B USEC AFTER C0=R2 (#FF=NO INT)
WHEN R2=09, INTERRUPT OCCURS #0A USEC AFTER C0=R2 (#FF=NO INT)
WHEN R2=08, INTERRUPT OCCURS #09 USEC AFTER C0=R2 (#FF=NO INT)
WHEN R2=07, INTERRUPT OCCURS #08 USEC AFTER C0=R2 (#FF=NO INT)
WHEN R2=06, INTERRUPT OCCURS #07 USEC AFTER C0=R2 (#FF=NO INT)
WHEN R2=05, INTERRUPT OCCURS #06 USEC AFTER C0=R2 (#FF=NO INT)
WHEN R2=04, INTERRUPT OCCURS #05 USEC AFTER C0=R2 (#FF=NO INT)
WHEN R2=03, INTERRUPT OCCURS #04 USEC AFTER C0=R2 (#FF=NO INT)
WHEN R2=02, INTERRUPT OCCURS #03 USEC AFTER C0=R2 (#FF=NO INT)
WHEN R2=01, INTERRUPT OCCURS #02 USEC AFTER C0=R2 (#FF=NO INT)
WHEN R2=00, INTERRUPT OCCURS #01 USEC AFTER C0=R2 (#FF=NO INT)

VSYNC DURATION (6=8180 OM CRT 0,3,4)(0=8400 ALL CRT / n=8400 CRT 1,2)
R3 High=6 )) SIDE=80400 USEC
R3 High=0 )) SIDE=80400 USEC

DELAY OF 'CALL TO #38' ON INTERRUPTION IS 05 uSEC (RSTM38=4 uSEC)

CRTC 2
```

DETAILED INFORMATION (SPPMC (00E802) AND INTERRUPTION (IM2))
100 R3=0E, INTERRUPT OCCURS #0F USEC AFTER 00:E82 (#FF=END INT)
101 R3=0D, INTERRUPT OCCURS #0E USEC AFTER 00:E82 (#FF=END INT)
102 R3=0C, INTERRUPT OCCURS #0D USEC AFTER 00:E82 (#FF=END INT)
103 R3=0B, INTERRUPT OCCURS #0C USEC AFTER 00:E82 (#FF=END INT)
104 R3=0A, INTERRUPT OCCURS #0B USEC AFTER 00:E82 (#FF=END INT)
105 R3=09, INTERRUPT OCCURS #0A USEC AFTER 00:E82 (#FF=END INT)
106 R3=08, INTERRUPT OCCURS #09 USEC AFTER 00:E82 (#FF=END INT)
107 R3=07, INTERRUPT OCCURS #08 USEC AFTER 00:E82 (#FF=END INT)
108 R3=06, INTERRUPT OCCURS #07 USEC AFTER 00:E82 (#FF=END INT)
109 R3=05, INTERRUPT OCCURS #06 USEC AFTER 00:E82 (#FF=END INT)
110 R3=04, INTERRUPT OCCURS #05 USEC AFTER 00:E82 (#FF=END INT)
111 R3=03, INTERRUPT OCCURS #04 USEC AFTER 00:E82 (#FF=END INT)
112 R3=02, INTERRUPT OCCURS #03 USEC AFTER 00:E82 (#FF=END INT)
113 R3=01, INTERRUPT OCCURS #02 USEC AFTER 00:E82 (#FF=END INT)
114 R3=00, INTERRUPT OCCURS #01 USEC AFTER 00:E82 (#FF=END INT)

SPPMC DURATION (6=8130 CM CRT 0,3,4)(8=8400 ALL CRT / n=8400 CRT 1,2)

R3 High=0)) SIZE=80400 USEC

R3 High=0)) SIZE=80400 USEC

DELAY OF INTERRUPTION CALL (IM2) IS 07 USEC

CRTC 2

UPDATE CRTC R0 TIMING

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
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(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD_UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```

```
R0=0 / CRTC 10 ON R0 (OUT[0]) [C]
DR: CB=..3F..40..41.. / MO: 00=..3F..00..01..
UPDATE R0=7F, OUT ON HCC=39 :OK
UPDATE R0=7F, OUT ON HCC=38 :OK
UPDATE R0=7F, OUT ON HCC=3B :OK
UPDATE R0=7F, OUT ON HCC=3C :OK
UPDATE R0=7F, OUT ON HCC=3D :OK
UPDATE R0=7F, OUT ON HCC=3E :NO
UPDATE R0=7F, OUT ON HCC=3F :NO
```

OUTI ON CBvs=#3c:01 (01:IO ON 5TH NOP / 00:IO ON 4TH NOP)

CRTC 2

R13 UPDATE IN 4 USEC SCREENS (R0=3)

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
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(3) INTERRUPT DELAY FROM R2 (18 CALC) (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
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(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
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(O) R1 STORIES (7 TST)
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(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT () CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
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Not available on CRTC 2

R13 UPDATE IN 2 USEC SCREENS (R0=1)

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST) (0) CRTC 2 RUMB
(2) SKEW DISP ON R0 RUPTURE (5 TST) (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC) (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
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(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
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(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT () CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
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Not available on CRTC 2

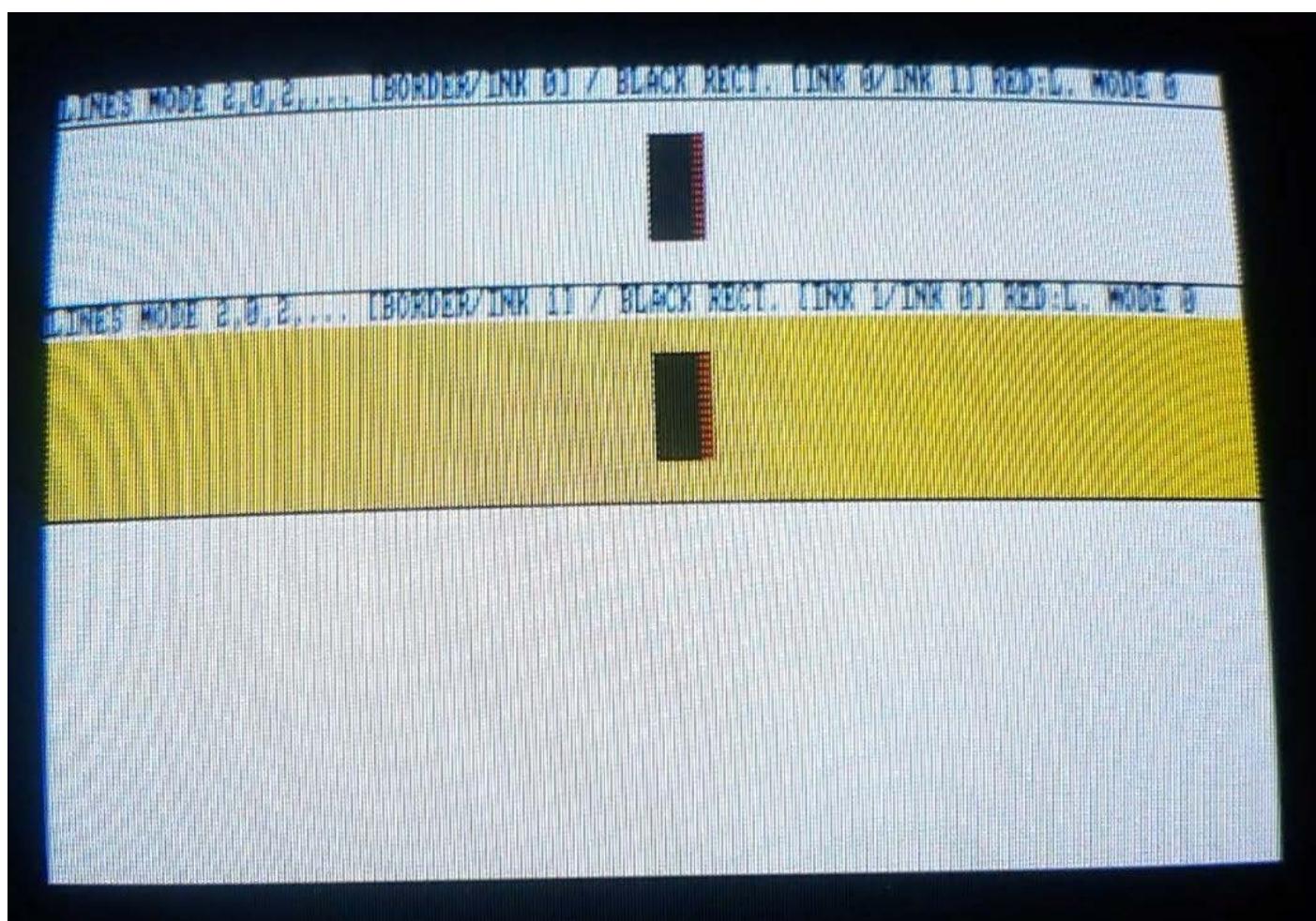
R13 UPDATE IN 1 USEC SCREENS (R0=0)

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(4) UPDATE CRTC R0 TIMING (7 TST)
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Not available on CRTC 2

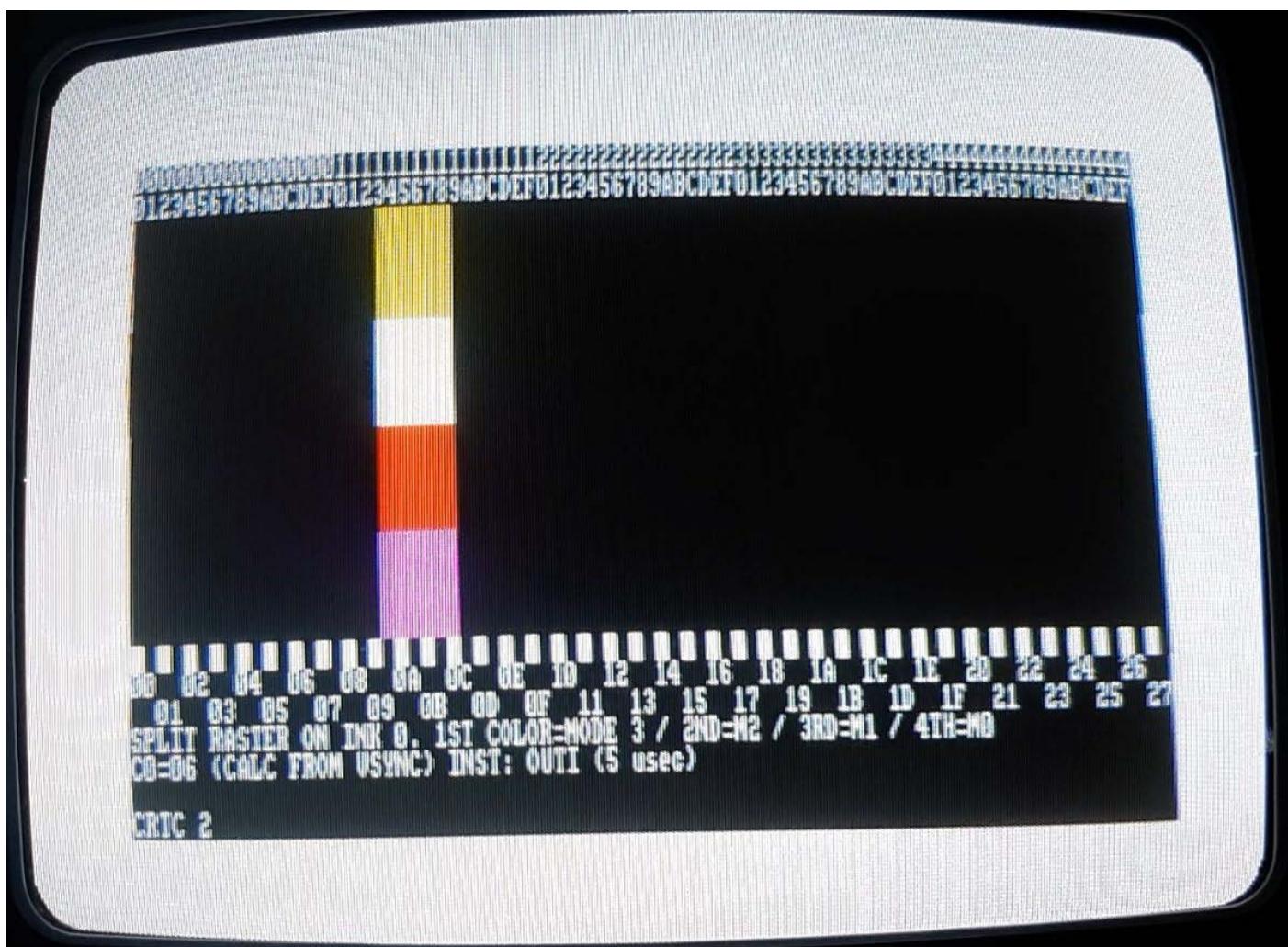
GATE ARRAY PIXELISATION

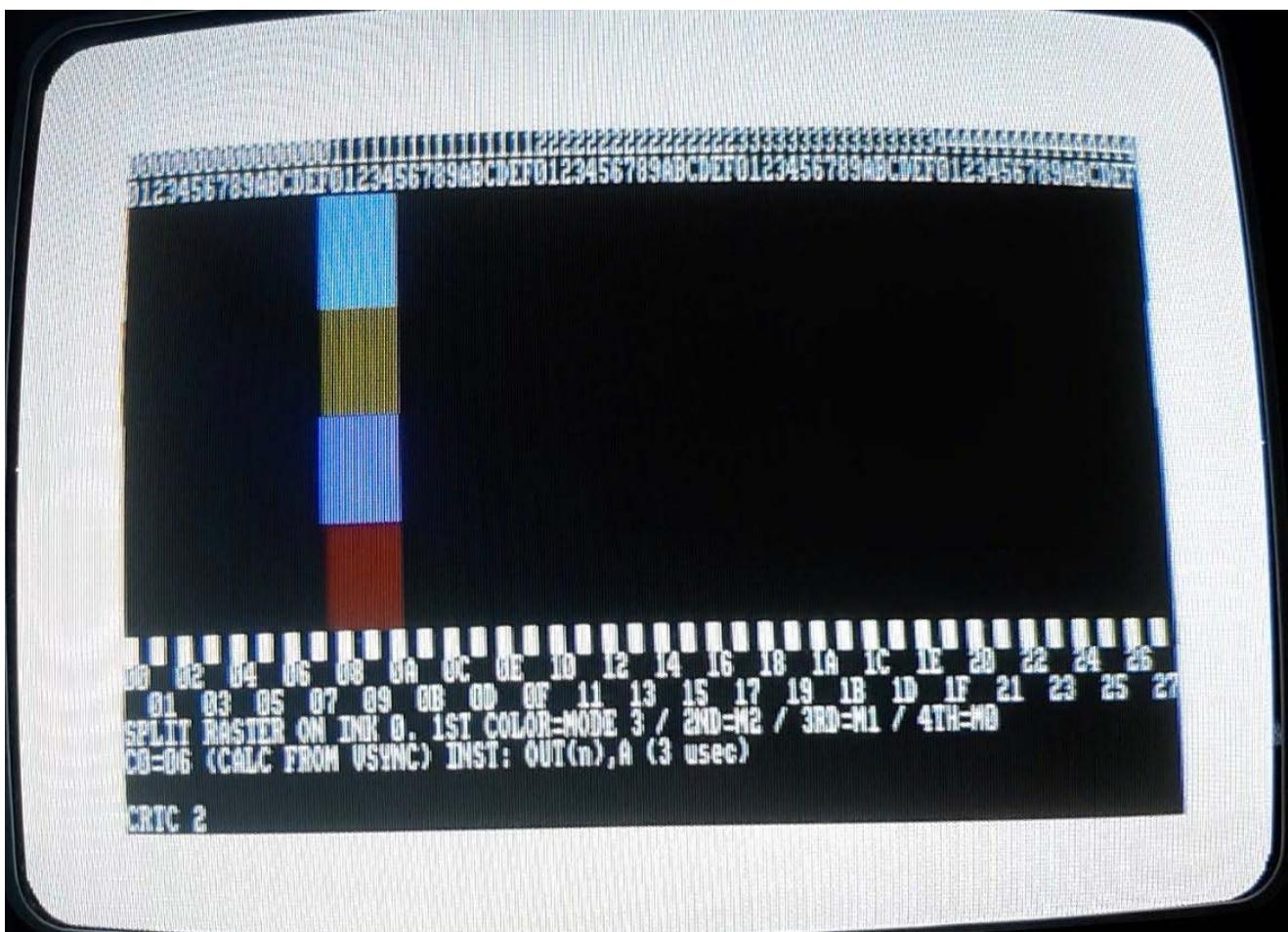
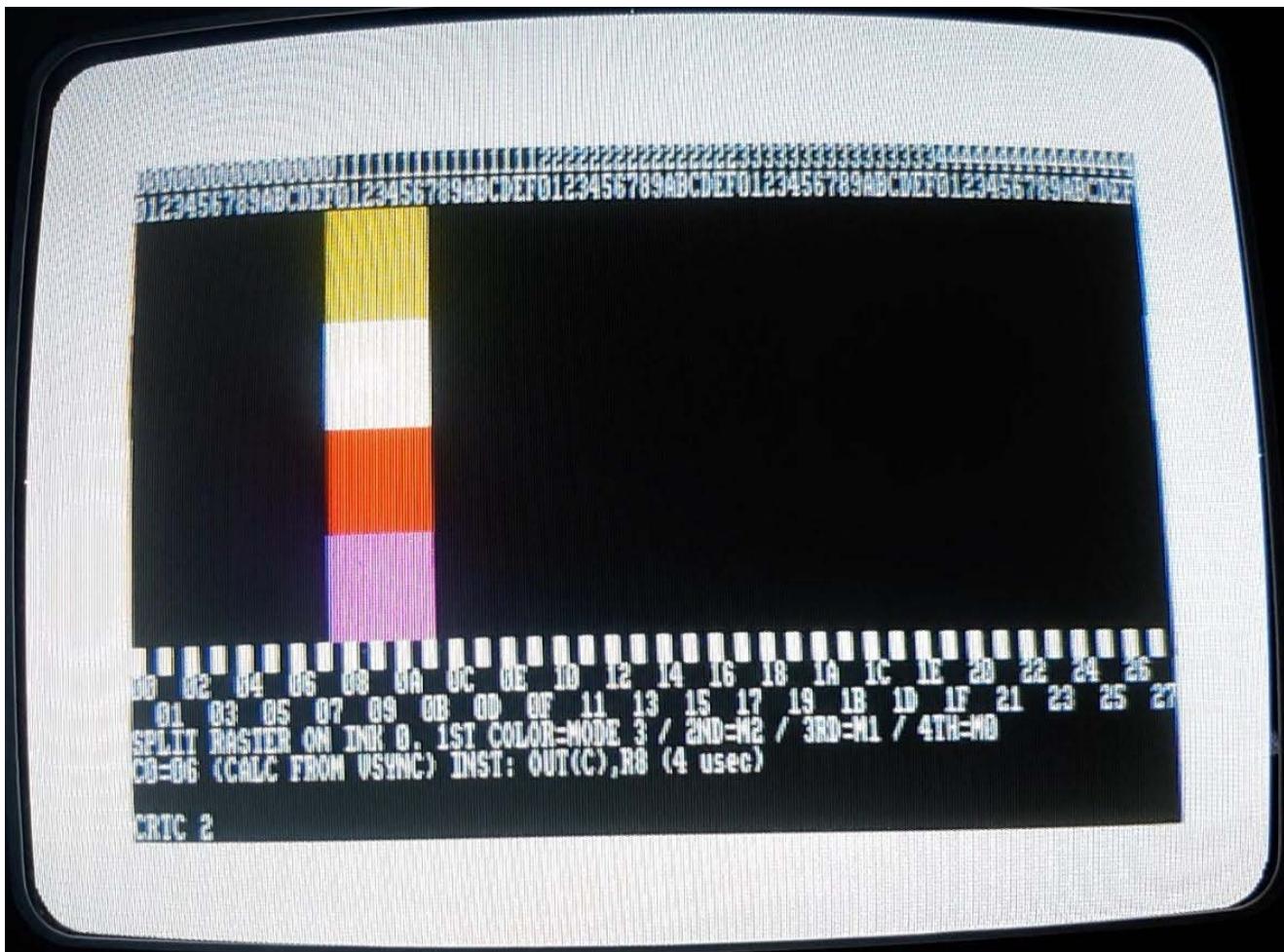
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(COPY) CRTC 2 OFFSET
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GATE ARRAY INKERISATION

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(1) UPDATE VRAM VS CRTC (14 TST) (0) CRTC 2 RUMB
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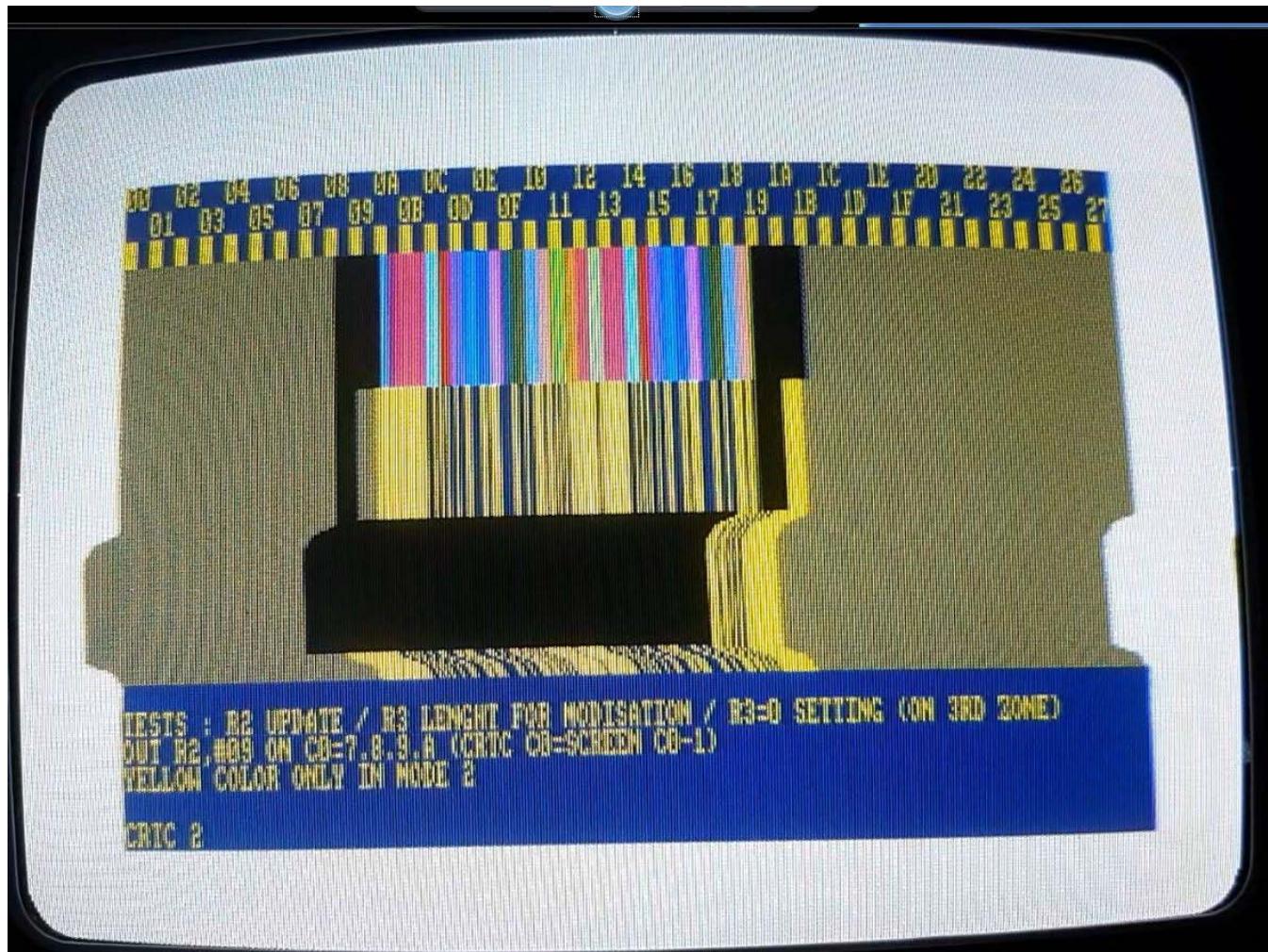
GATE ARRAY MODERISATION

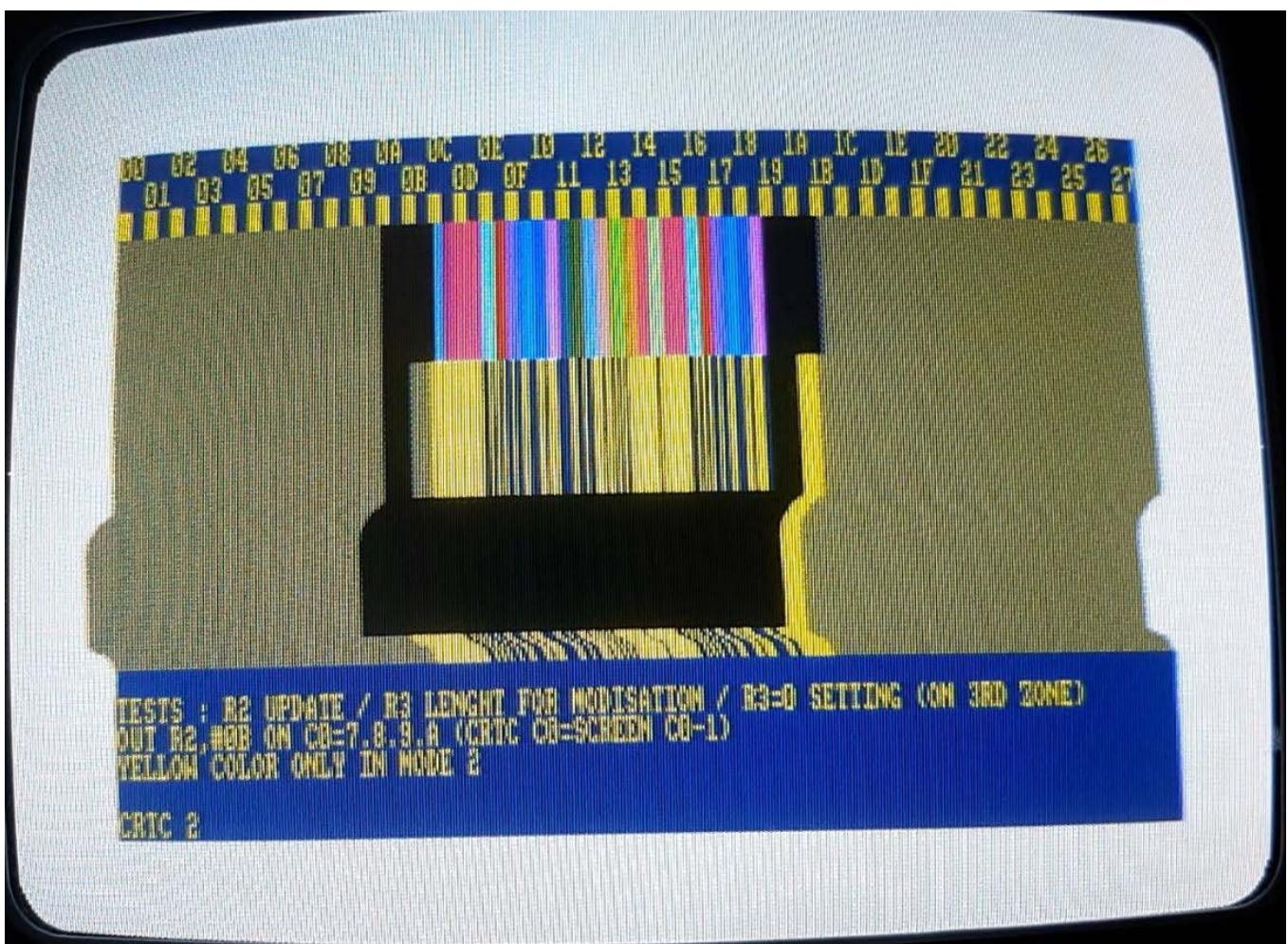
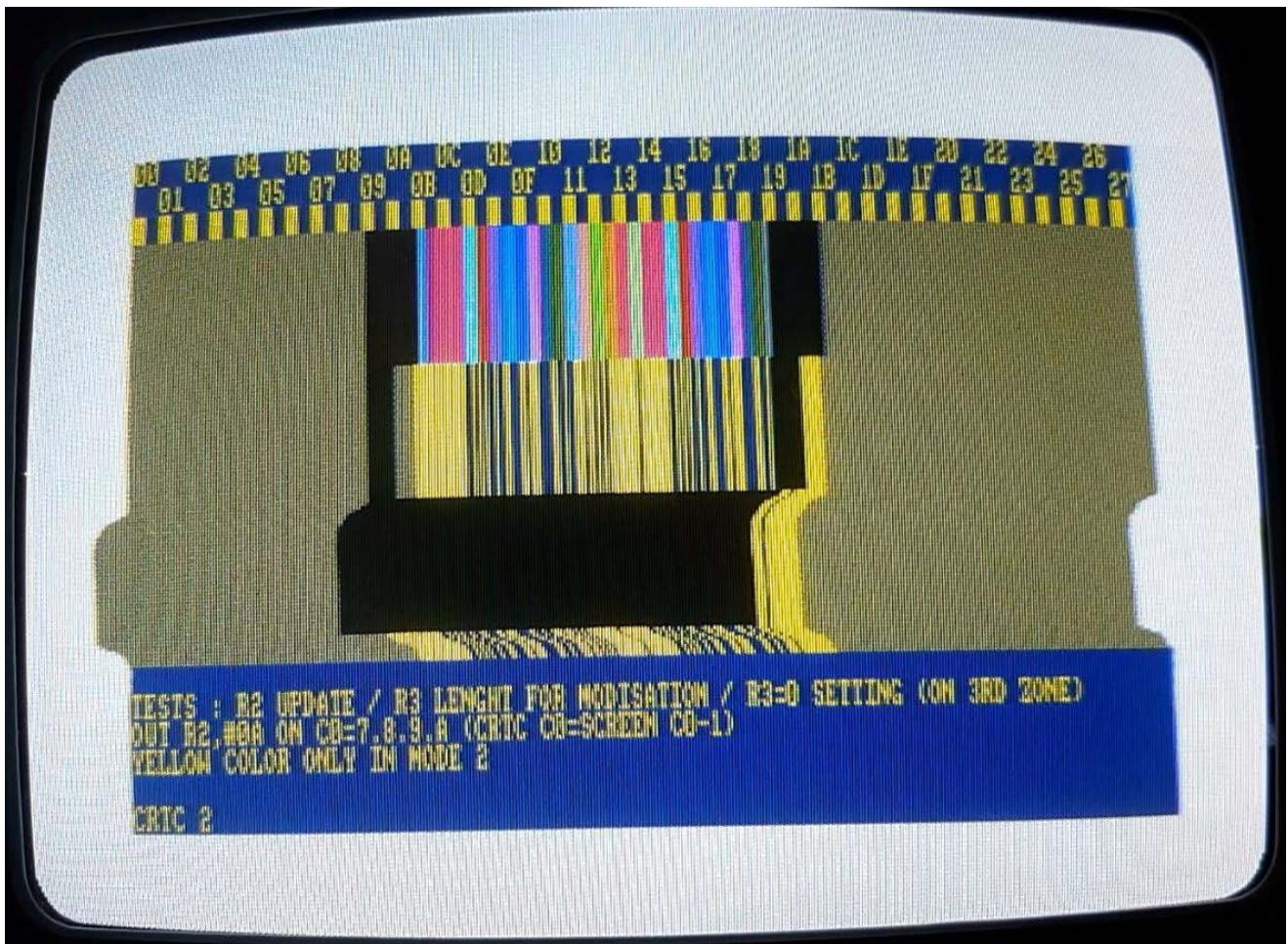
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(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!



HSYNC DELAY ON MODE UPDATE, R2 UPDATE/R3 LENGTH 2 to 0

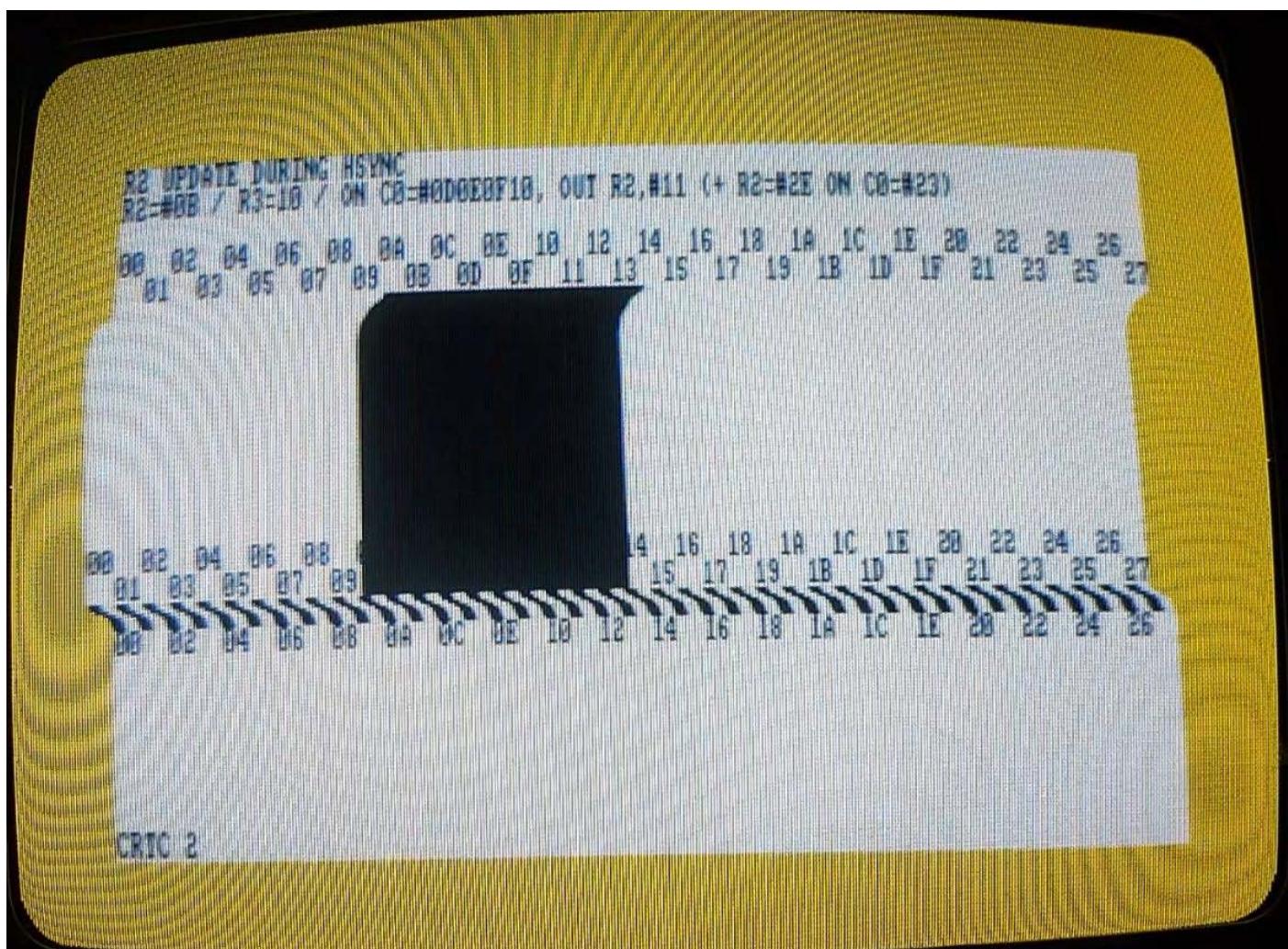
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD_UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!





R2 UPDATE DURING & AFTER HSYNC

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST) (0) CRTC 2 RUMB
(2) SKEW DISP ON R0 RUPTURE (5 TST) (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC) (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!



R2 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON CD=#0D0E0F10, OUT R2,#12 (+ R2=#2E ON CD=#23)

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

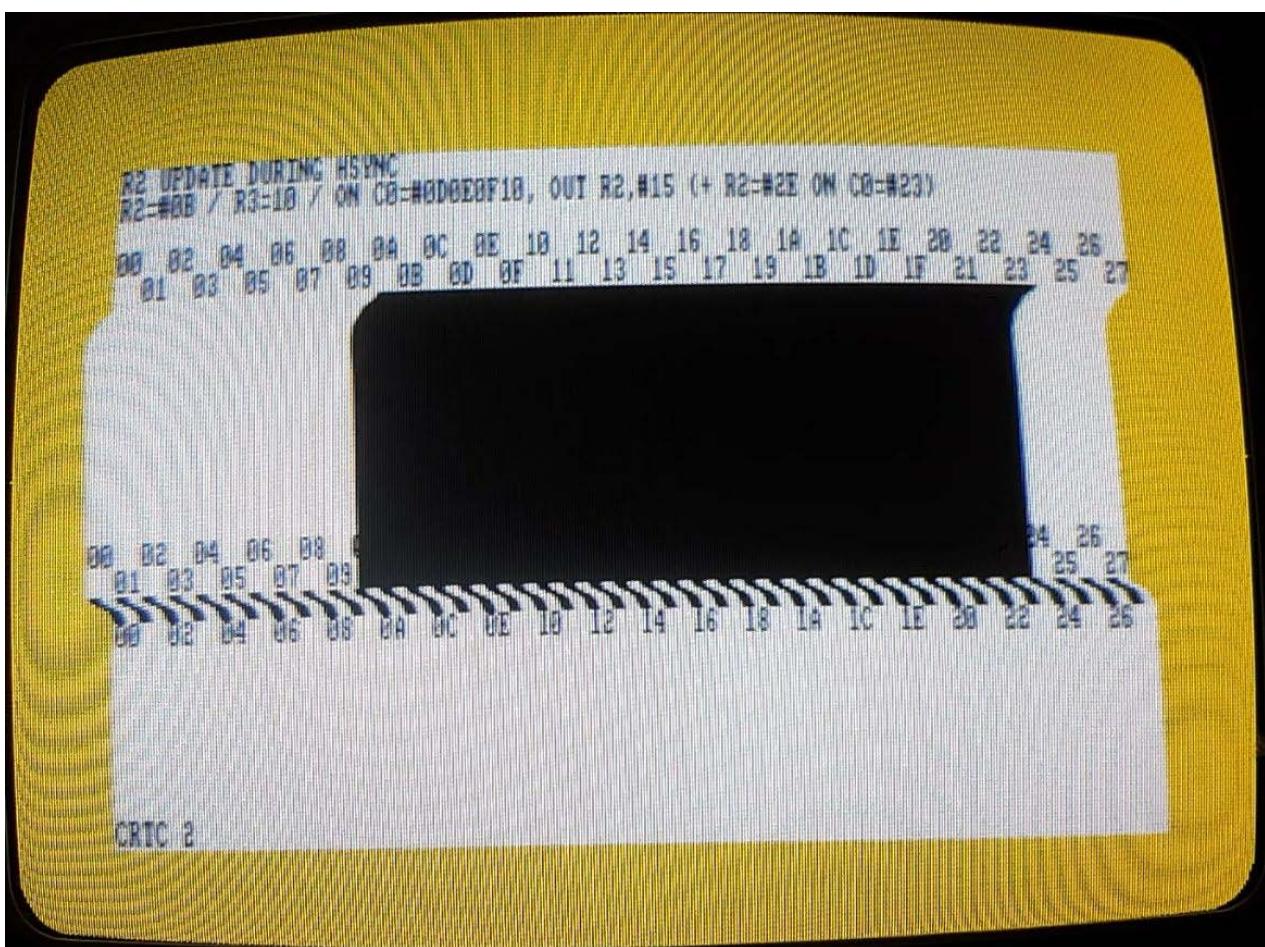
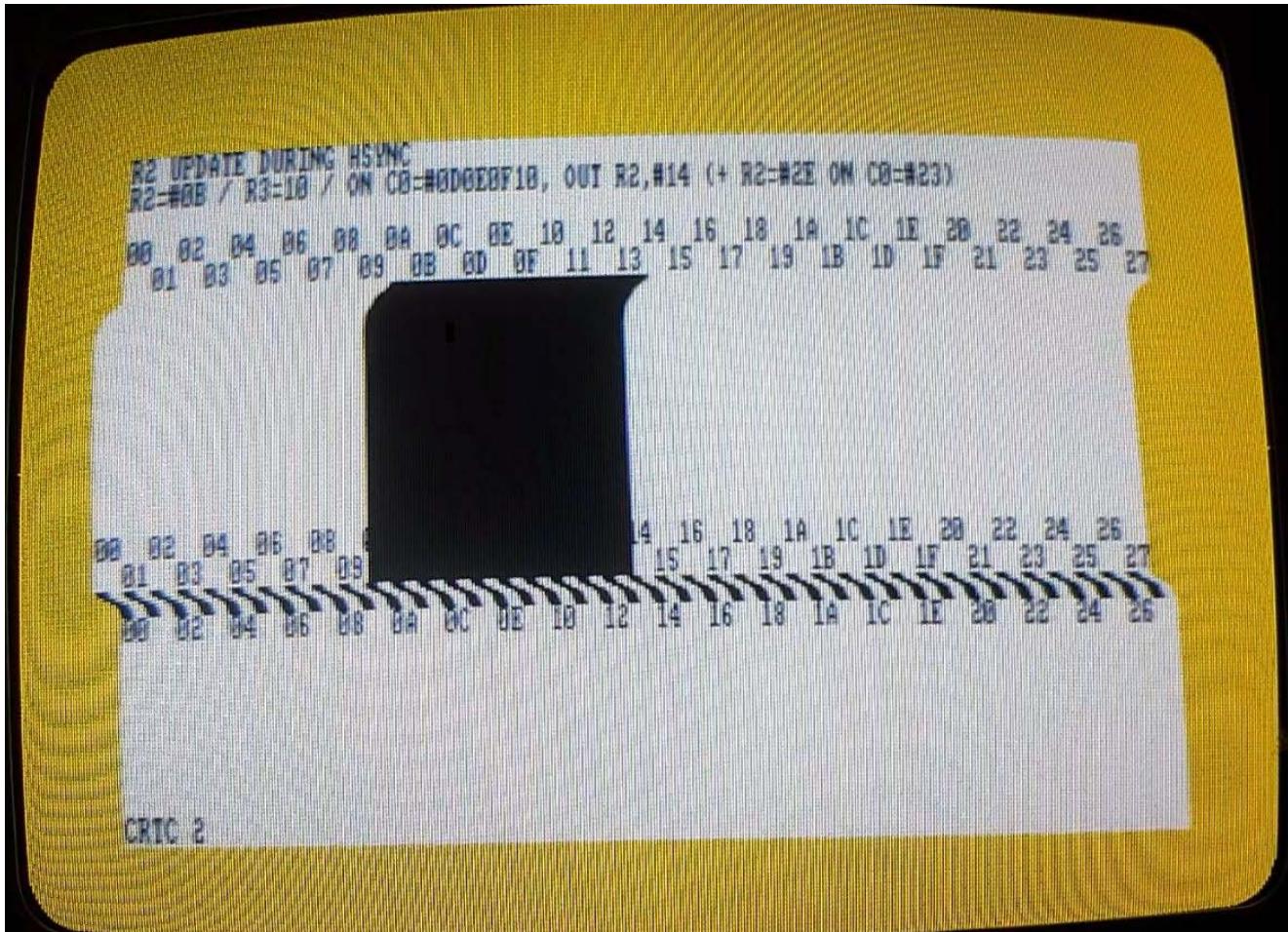
CRTC 2

R2 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON CD=#0D0E0F10, OUT R2,#13 (+ R2=#2E ON CD=#23)

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

CRTC 2



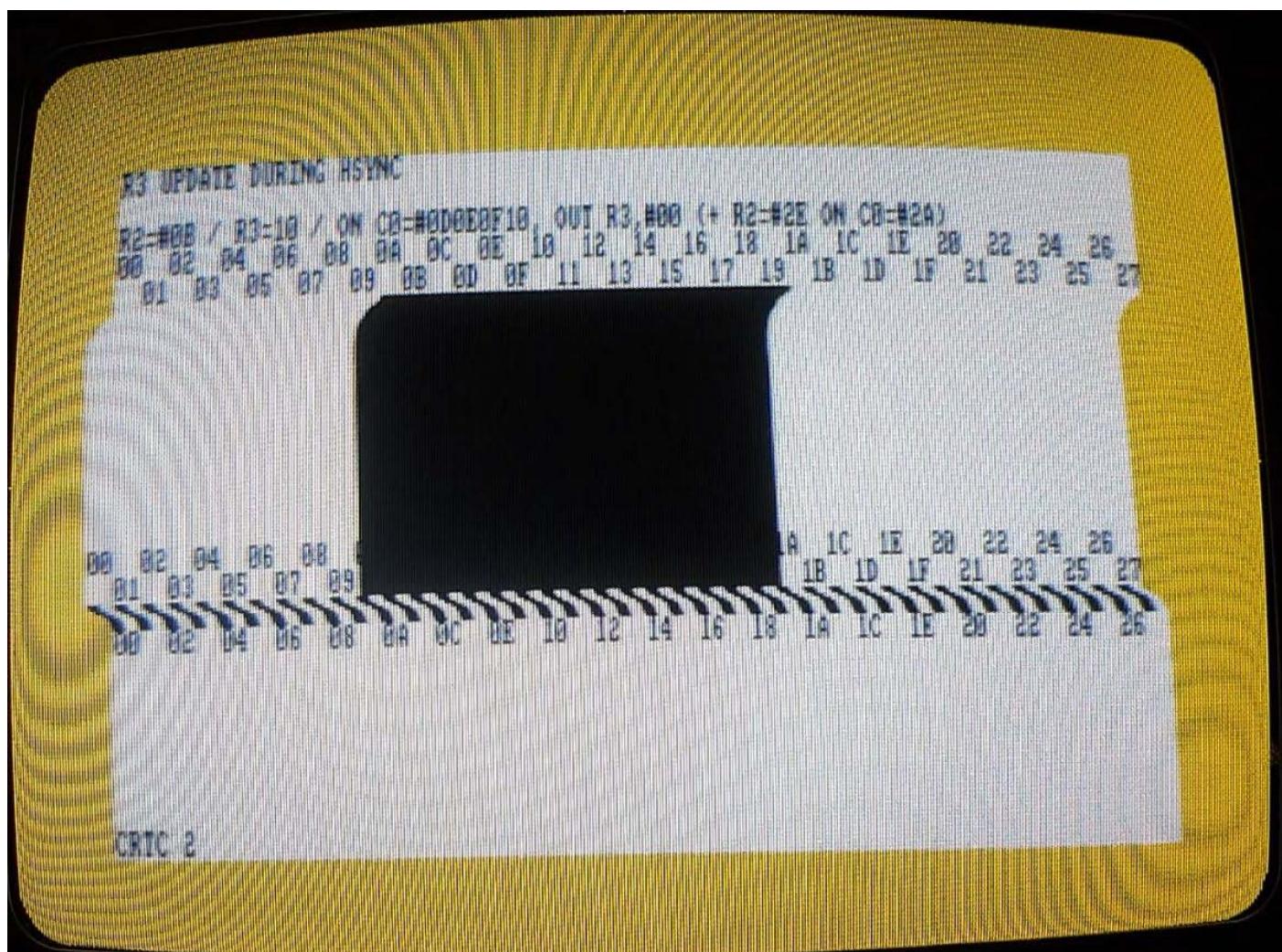
R2 UPDATE DURING HSYNC
R2=#9B / R3=10 / OM CB=#0D0E0F10, OUT R2,#16 (+ R2=#2E OM CB=#23)

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
91 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

HTC 6

R3 UPDATE DURING HSYNC

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD_UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```



R3 UPDATE DURING HSYNC

R2=#0B / R3=10 / ON C0=#0D0E0F10, OUT R3,#01 (+ R2=#2E ON C0=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

CRTC 2

R3 UPDATE DURING HSYNC

R2=#0B / R3=10 / ON C0=#0D0E0F10, OUT R3,#02 (+ R2=#2E ON C0=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

CRTC 2

R3 UPDATE DURING HSYNC

R2=#0B / R3=10 / OUT 0B=#0D0E0F10, OUT R3:#03 (+ R2=#2E OUT 0B=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

CRTC 2

R3 UPDATE DURING HSYNC

R2=#0B / R3=10 / OUT 0B=#0D0E0F10, OUT R3:#04 (+ R2=#2E OUT 0B=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

CRTC 2

R3 UPDATE DURING HSEMC

R2=#0B / R3=10 / ON CD=#0D0E0F10 OUT R3:#05 (+ R2:#2E ON CD:#2A)
00 02 04 06 08 0A 0C BE 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27



00 02 04 06 08 0A 0C BE 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C BE 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

CRTC 2

R3 UPDATE DURING HSEMC

R2=#0B / R3=10 / ON CD=#0D0E0F10 OUT R3:#06 (+ R2:#2E ON CD:#2A)
00 02 04 06 08 0A 0C BE 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27



00 02 04 06 08 0A 0C BE 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C BE 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

CRTC 2

R3 UPDATE DURING HSYNC

R2=#88 / R3=10 / ON CR=#0D0E0F1B OUT R3,#07 (+ R2=#2E ON CR=#2A)

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

CRTC 2

R4 & R9 CHECKING

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```

RESULT OF CRT-R4 & R9 CHECK

```
PROV R9=7 )) UPD R3=1 WHEN C9=3))C9=0 (OK FOR CRT 3+4 ONLY):xH0x
PROV R9=7 R4=38 )) UPD R4=1 WHEN C4=1 & (C9=7 )) C4=0 :OK
PROV R9=7 R4=38 )) UPD R4=0 WHEN C4=1 & (C9=7 )) C4=2 (0wf) :OK
PROV R9=7 R4=38 )) UPD R9=0 WHEN C4=1 & C9=0 (UPD FROM C0vsin) (00=Upd 0k)
((00/00/30=00/3E=00/3F=00/00=01/01=01/02=01/03=01/04=01/05=01
((00/00/30=00/3E=00/3F=00/00=01/01=01/02=01/03=01/04=01/05=01
PROV R9=7 R4=38 )) UPD R4=1 WHEN C4=1 & C9=7 (UPD FROM C0vsin) (01=C4 0wf)
((21=00/20=00/1E=00/3F=00/00=01/01=01/02=01/03=01/04=01/05=01
PROV R9=7 R4=1 )) UPD R9=1 WHEN (C4=1,C9=7) LASTLINE FROM C0=23 R2=3E(01:C9=8)
01 01 01 01 01 01 01 01 01 01 01 01 01 01 01 01 01 01 01 01
PROV R9=7 R4=1 )) UPD R4=3 WHEN C4=1 & C9=7 (LAST LINE):01 (00:04wf 01:04=0)
PROV R9=7 R4=1 )) UPD R4=0 WHEN C4=1 & C9=7 (UPD FROM C0vsin)(01:C4=0 00:04 wf)
))3C=01/30=01/3E=01/3F=01/00=01/01=01/02=01/03=01/04=01/05=01
```

CRTC 2

VSYNC CONDITIONS

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD, UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!

VSYNC MANAGEMENT DURING R3

R3 APPLIED ON ALL VALUES OF C4
R2=50, R3=12, R0=63 : V1:#5E, V2:#5F
R2=50, R3=13, R0=63 : V1:#5E, V2:#5F
R2=50, R3=14, R0=63 : V1:#5E, V2:#5F
R2=50, R3=15, R0=63 : V1:#5E, V2:#5F

R3 APPLIED ON ALL VALUES OF C4, EXCEPTED WHEN C4=R7 (C9=0) (THEN R3=12)

R2=50, R3=12, R0=63 : V1:#5E, V2:#5F
R2=50, R3=13, R0=63 : V1:#5E, V2:#5F
R2=50, R3=14, R0=63 : V1:#5E, V2:#5F
R2=50, R3=15, R0=63 : V1:#5E, V2:#5E

R2=50, R3=15, R0=63 : V1:#5E, V2:#5E ON PREVIOUS LINE

VSYNC CONDITIONS IN HSYNC (R2=#2E/R3=14)
D) UPD R7=04 ON C9=0,C0v=#35 PPI.B ON C9=0,C0v=#3A:#5E
D) UPD R7=04 ON C9=0,C0v=#35 PPI.B ON C9=0,C0v=#3E:#5E
D) UPD R7=04 ON C9=0,C0v=#35 PPI.B ON C9=1,C0v=#3A:#5E
D) UPD R7=04 ON C9=0,C0v=#35 PPI.B ON C9=1,C0v=#3E:#5E

PPI.STATUS 5us BEFORE R7=04 :#5E
PPI.STATUS 5us AFTER UPD R7(=04 (R7=04 BEFORE) (VSYNC CANCEL))(C9=0) :#5E
PPI.ST C0=46 15 LINES AFTER R7=04 ON C0vs10=#1E:5F,5F,5F,5E,5E

CRTC 2

PPI1 IN51MC ST: EACH bus FROM UPD R1=04,10 ON COVs= #11 (04=1,09=0)
 PPI1 OUT R7,1 ON COVs= #11 (04=1,09=0) IN HSYNC (COInst=R2=46), THEN
 PPI1 OUT R7,1 ON COVs= #11 (04=1,09=0, COInst=10,18: PPI.B=#5E
 PPI1 OUT R7,1 ON COVs= #11 (04=1,09=0, COInst=5 : PPI.B=#5E
 PPI1 OUT R7,1 ON COVs= #11 (04=1,09=0, COInst=34: PPI.B=#5E
 PPI1 OUT R7,3 ON COVs= #11 (04=1,09=0)
 PPI1 OUT R7,3 ON COVs= #11 (04=1,09=0)
 PPI1 OUT R7,3 ON COVs= #11 (04=1,09=0)

R1 STORIES

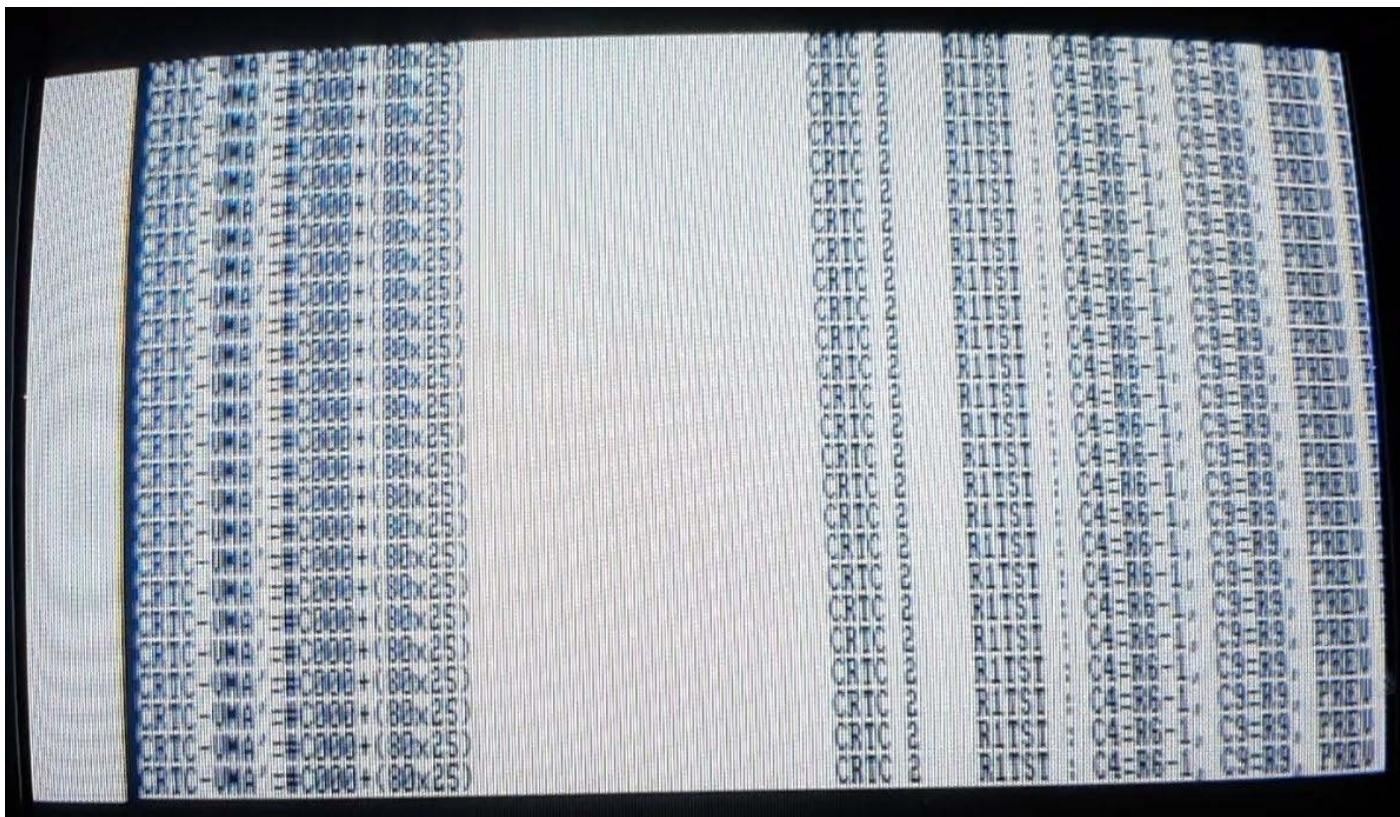
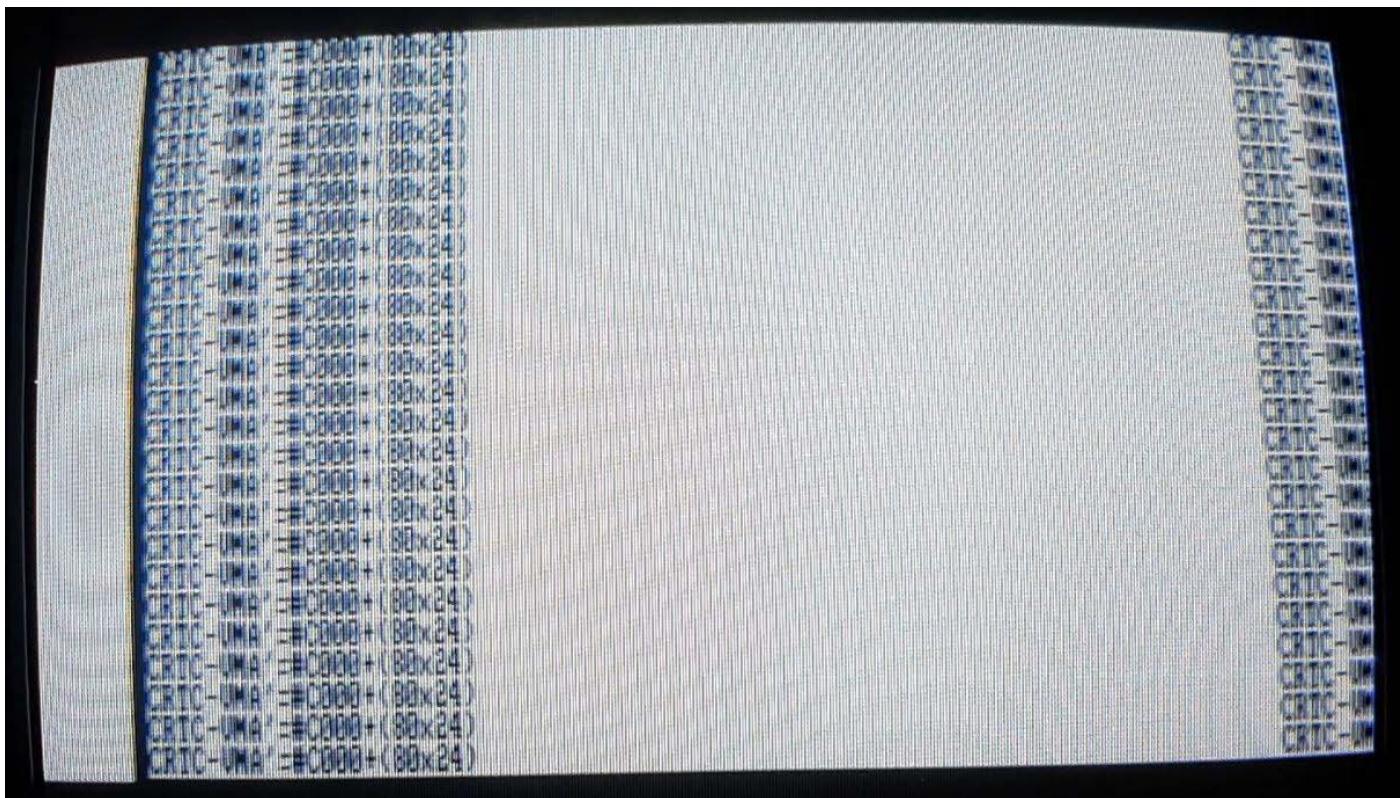
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
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(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD_UPD R2,LGTH R3 (2.1.0)(3 TST)
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(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!

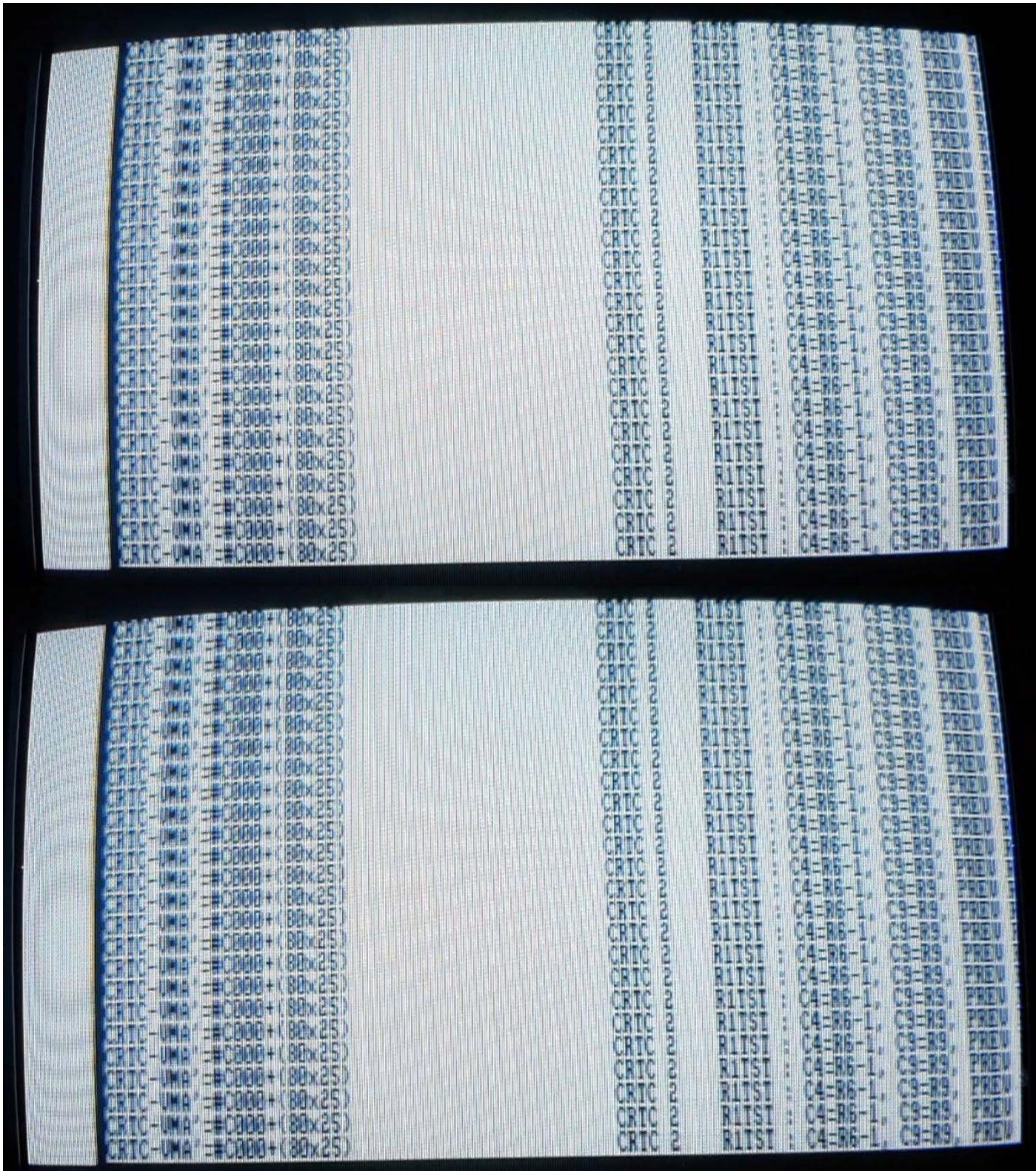


CRIC 2 : RI STORIES
STORY 2 : RI > R0 WHEN C9=R9 & C9<R9
PROCESS : UPDATE RI ON 16 LINES (64 x 7, 48 (C9=7))+(48 x 7, 96(C9=7))
R0 R2 R4 R6 R8 R9 DC BE 10 12 14 16 18 1A 1C 1E 20 22 24 26
R1 R3 R5 R7 R9 R8 R0 R7 11 13 15 17 19 1B 1D 1F 21 23 25 27

(1.1) AT #0000+(5x20)
(1.2) AT #0000+(6x20))
(1.3) AT #0000+(5x20))
(1.4) AT #0000+(7x20))

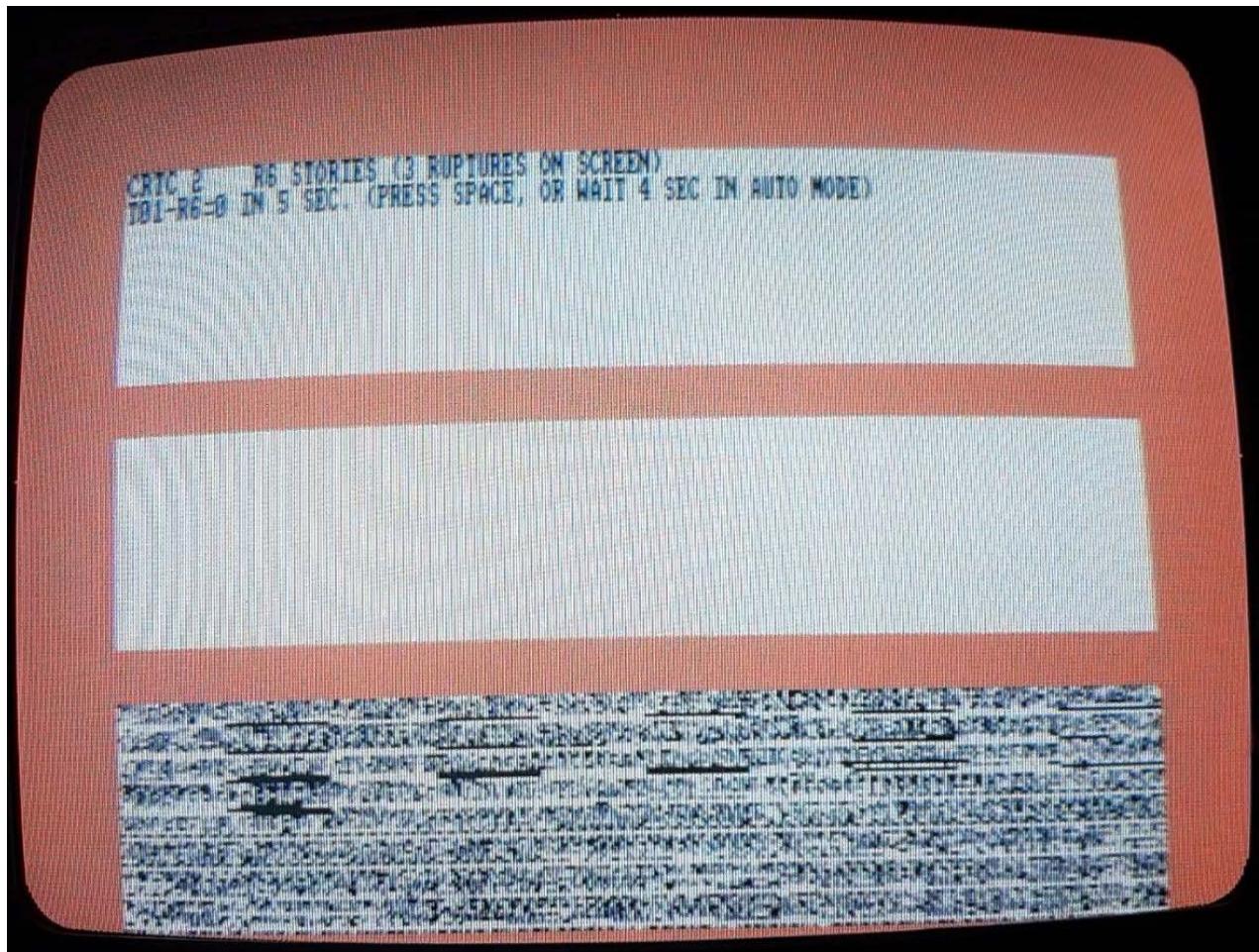
CRIC 2 : RI STORIES
STORY 3 : RI=0 EFFECT (EACH LINE : 4 x OUT RI 8/OUT RI, 48)
PROCESS : UPDATE RI=0 FOR 4x8 Lines FROM CB=3C, CB=3D, CB=3E, CB=3F
R0 R2 R4 R6 R8 R9 DC BE 10 12 14 16 18 1A 1C 1E 20 22 24 26
R1 R3 R5 R7 R9 R8 R0 R7 11 13 15 17 19 1B 1D 1F 21 23 25 27





R6 STORIES

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST) (0) CRTC 2 RUMB
(2) SKEW DISP ON R0 RUPTURE (5 TST) (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC) (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!

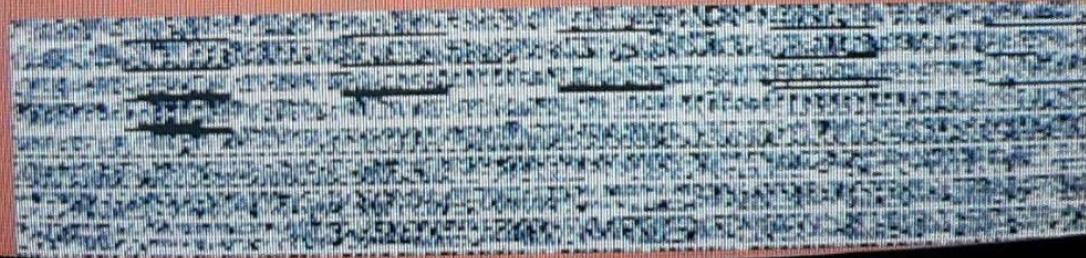
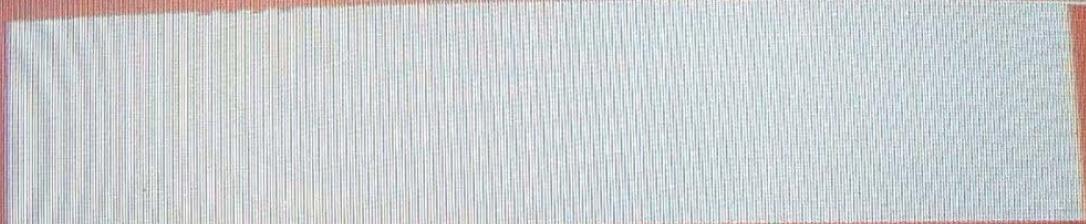


CRTC 2 R6 STORIES (3 RUPTURES ON SCREEN)
DB2-58 L. PATCHWORK R6=D/8 FROM VERY 1ST LINE OF MIDDLE SCREEN RUPT (C4=8,C9=8)

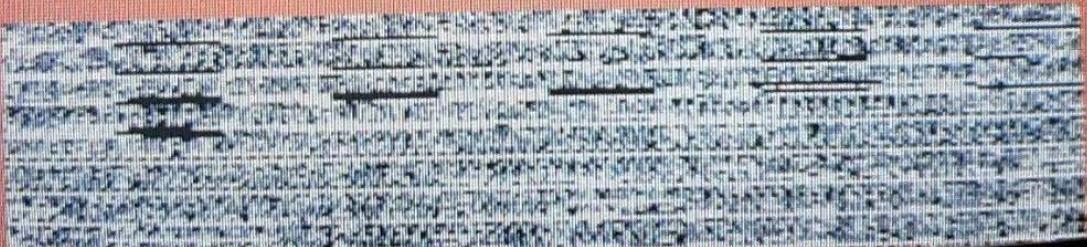
CRTC 2 R6 STORIES (3 RUPTURES ON SCREEN)
T03-50 L. PATCHWORK R6=0/8 FROM 2ND LINE OF MIDDLE SCREEN RUPTURE (C4=0,C9=1)



CRTC 2 R6 STORIES (3 RUPTURES ON SCREEN)
T04-1ST LINE IN DISPLAY AREA : SEQUENCE R6=0/R6=8/ WHEN R1>R0



CRTC 2 R6 STORIES (3 RUPTURES ON SCREEN)
TDS-SB L. FROM 2ND LINE IN DISP AREA : PATCHWORK R6=8/R6=8 WHEN R1>R0



CRTC 2 R6 STORIES - AGAIN -
TDS-SB L. C4=8/C9=0 PATCHWORK R6=8/25 IN DISP AREA FOR 64 LINES

XX/C 2 RD STORIES - AGAIN-
T05B-ON C4=9/C9=1 PATCHWORK RS=9/25 IN DISP AREA FOR 64 LINES

XX/C 2 RD STORIES - AGAIN-
T05C-ON C4=9/C9=1 PATCHWORK RS=8/25 IN DISP AREA FOR 64 LINES

CRTC 2 R6 STORIES -LAST LINE-
R6=0/FF FROM C8=2 ON C4=R4, C9=0..7, PREVIOUS R6=R4+1

..7, PREVIOUS R6=R4+1

CRTC 2 R6 STORIES -LAST LINE-
R6=0/FF FROM C8=2 ON C4=R4, C9=0

CRTC 2 R6 STORIES -LAST LINE-
R6=0/FF FROM C8=2 IN U.ADJ ZONE (RS=16) (C4=fnc(CRTC)) PREVIOUS R6=R4+3

(RS=16) (C4=fnc(CRTC)) PREVIOUS R6=R4+3

CRTC 2 R6 STORIES -LAST LINE-
R6=0/FF FROM C8=2 IN U.ADJ ZONE

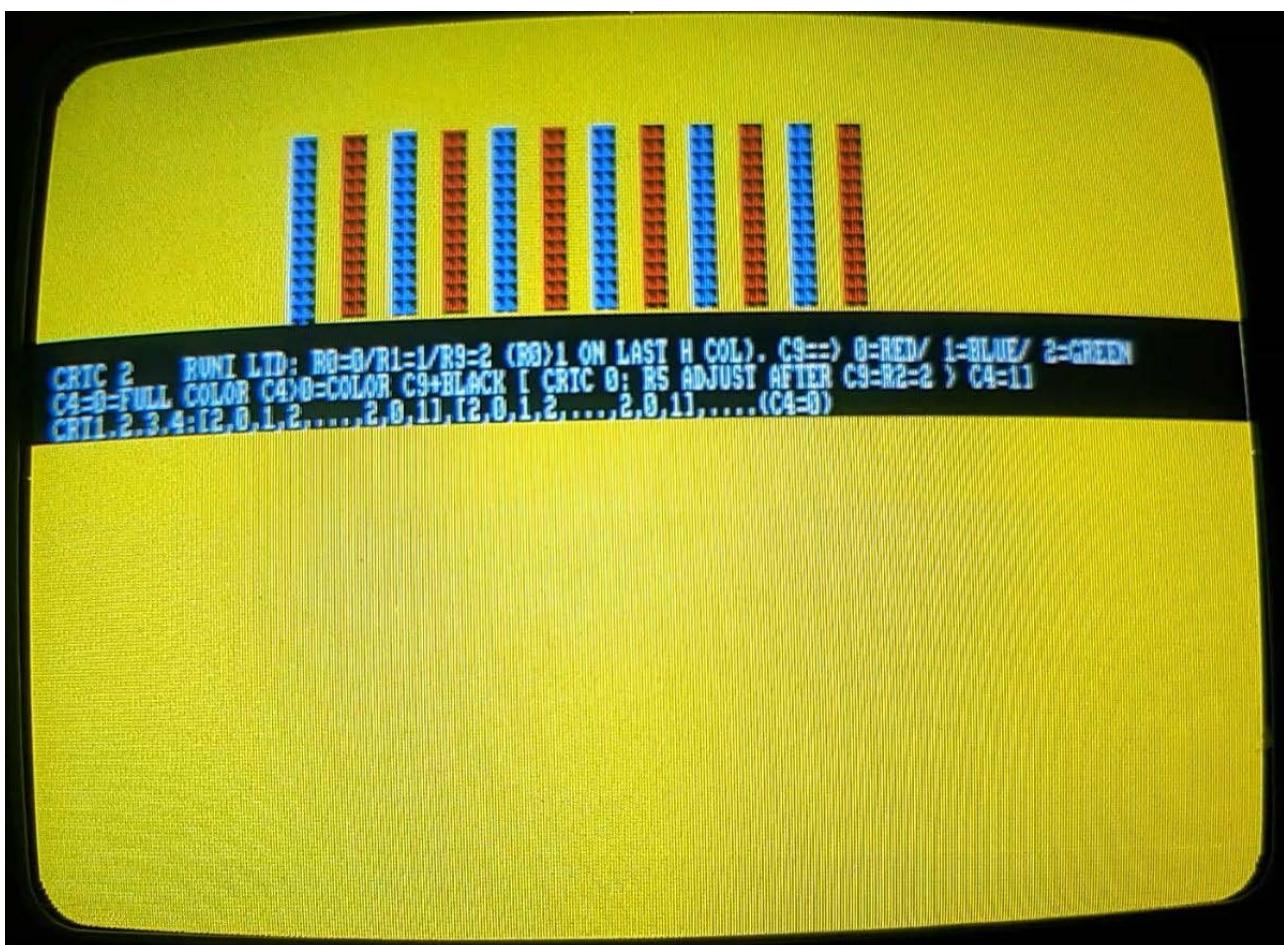
CRTC 2 R6 STORIES -LAST LINE-
R6=R4+1/FF FROM CR=2 IN V. ADJ ZONE (RS=16) (C4=fnc(CRTC)) PREVIOUS R6=R4+3

CRTC 2 R6 STORIES -LAST LINE-
R6=R4+1/FF FROM CR=2 IN V. ADJ ZONE (RS=16) (C4=fnc(CRTC)) PREVIOUS R6=R4+3

RVNI (NON INVISIBLE VERTICAL RUPTURE)

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST) (0) CRTC 2 RUMB
(2) SKEW DISP ON R0 RUPTURE (5 TST) (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC) (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!





ANALYZER / FORCED STABILISATION ON R0=0

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD_UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!



R5 SCANNER (for CRTC 1)

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```

Only for CRTC 1

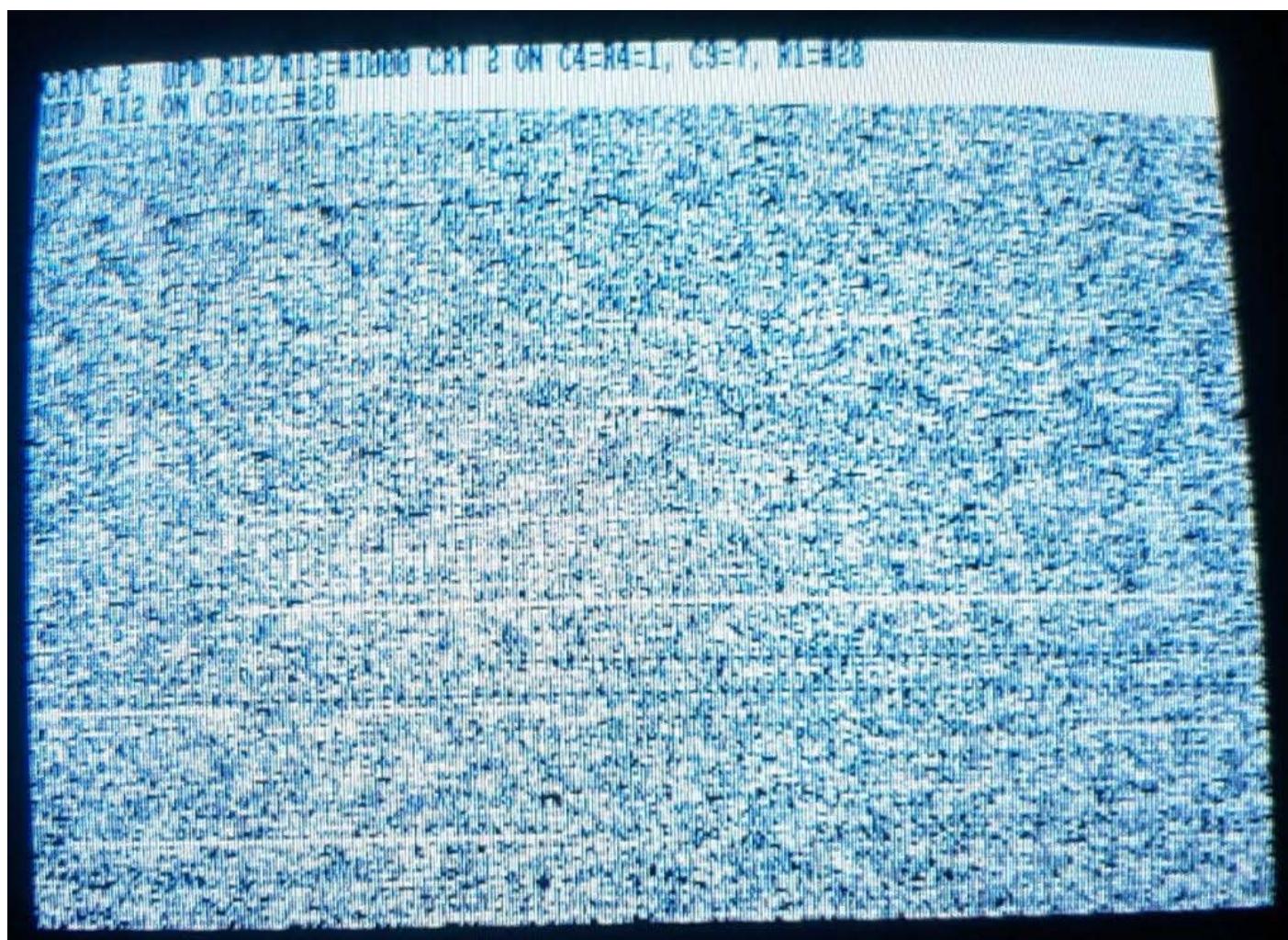
R5 STORIES / INTERACTIVE TEST

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT () CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```

Only for CRTC 1

OFFSET UPDATE

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD_UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!

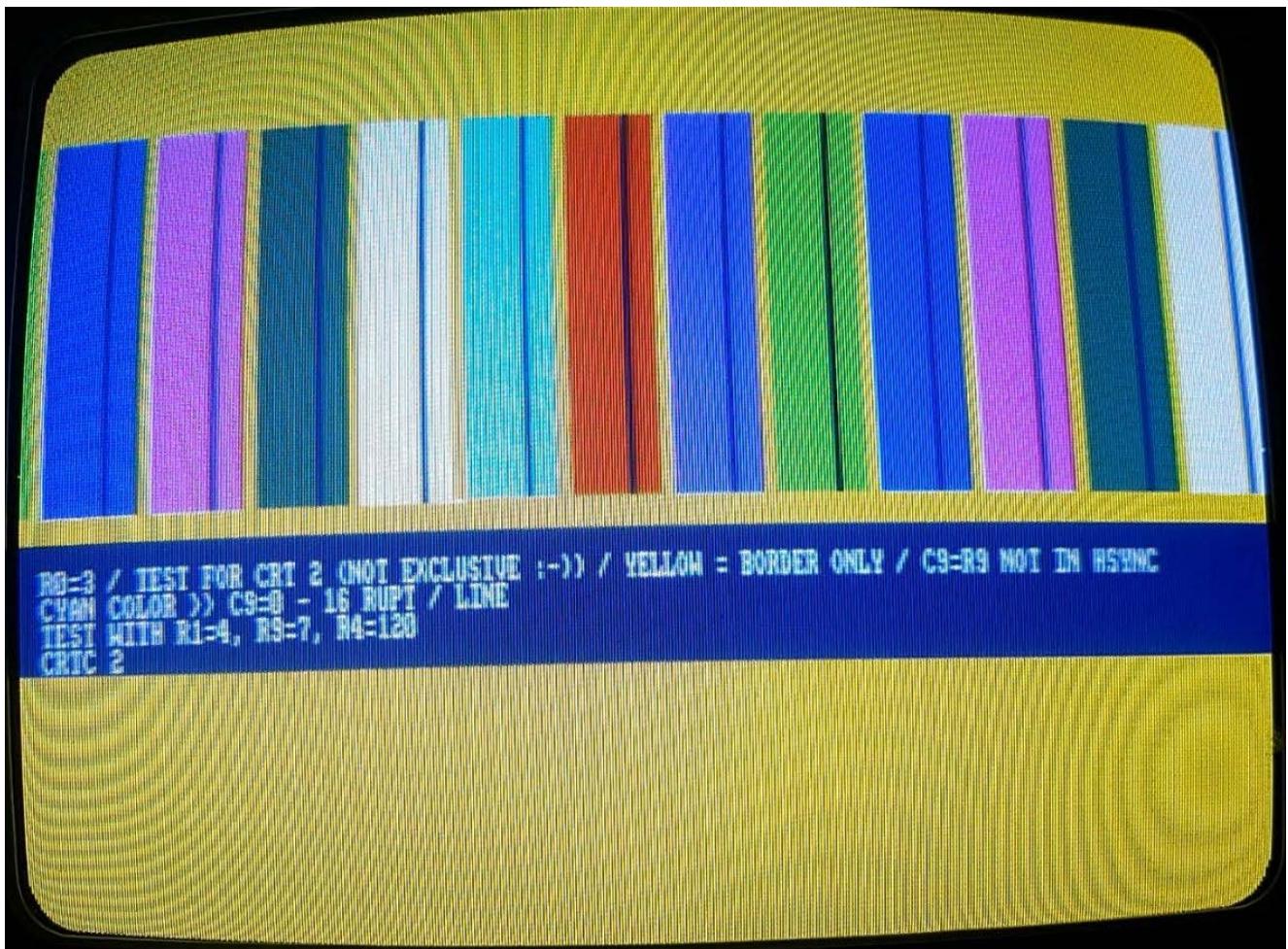


CR1C 2 UPD R12/R13=#1000 CRT 2 ON C4=R4=1, C9=7, R1=#28
UPD R12 ON C0V0C=#29
CRTC 2 UPD R12/R13=#1000 CRT 2 ON C4=R4=1, C9=7, R1=#28
UPD R12 ON C0V0C=#29

« RVMB »

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT () CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!





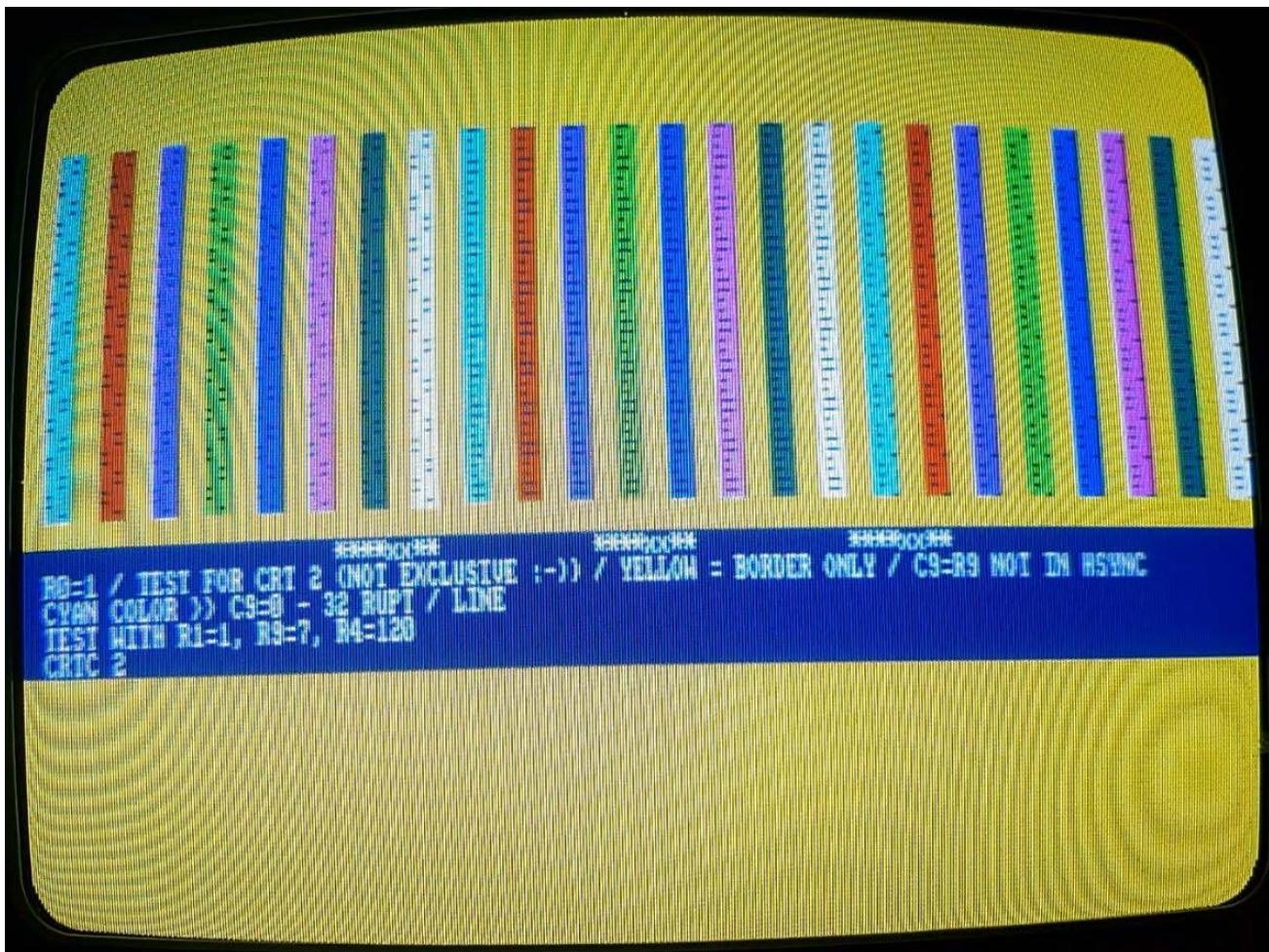




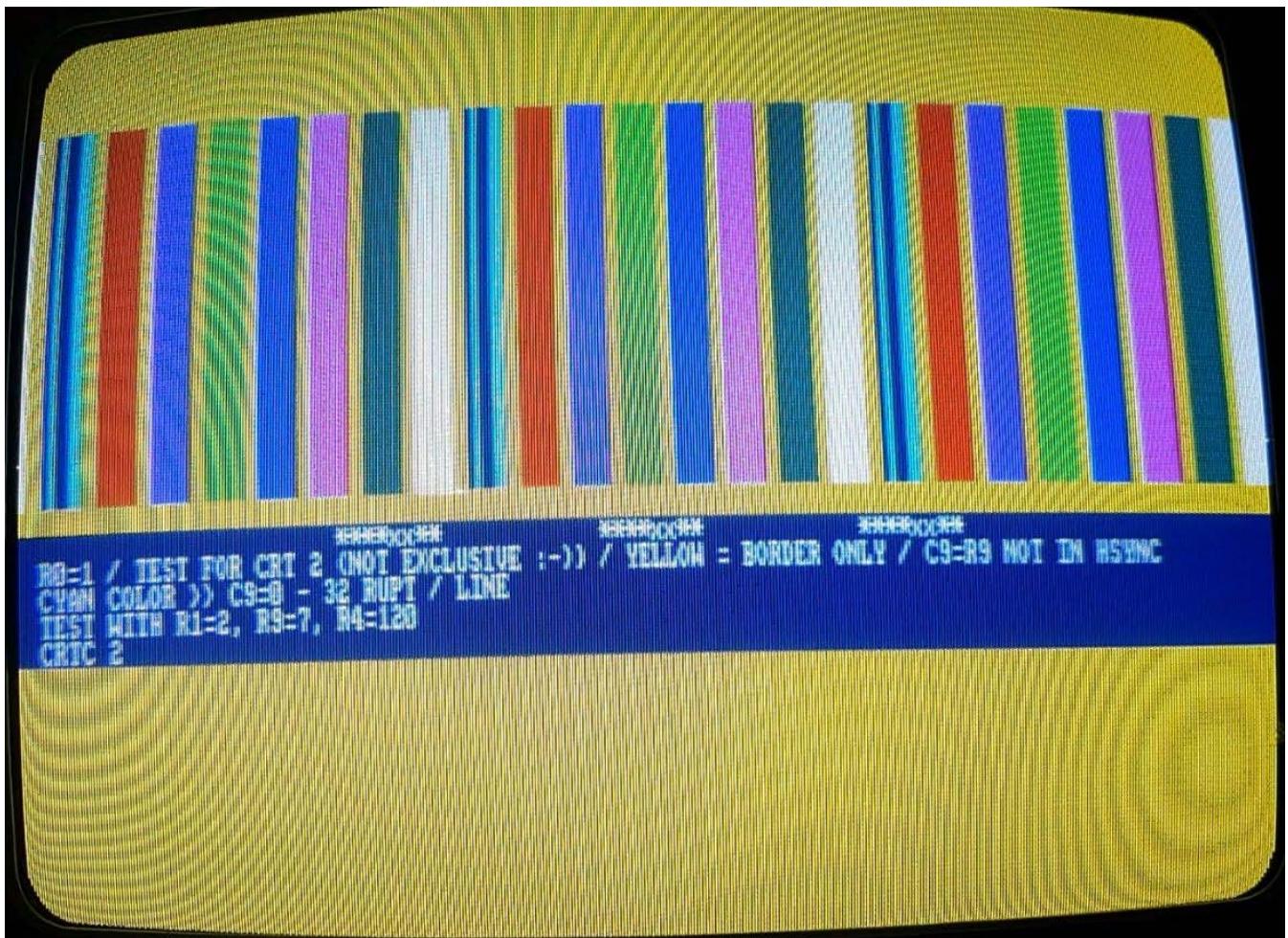






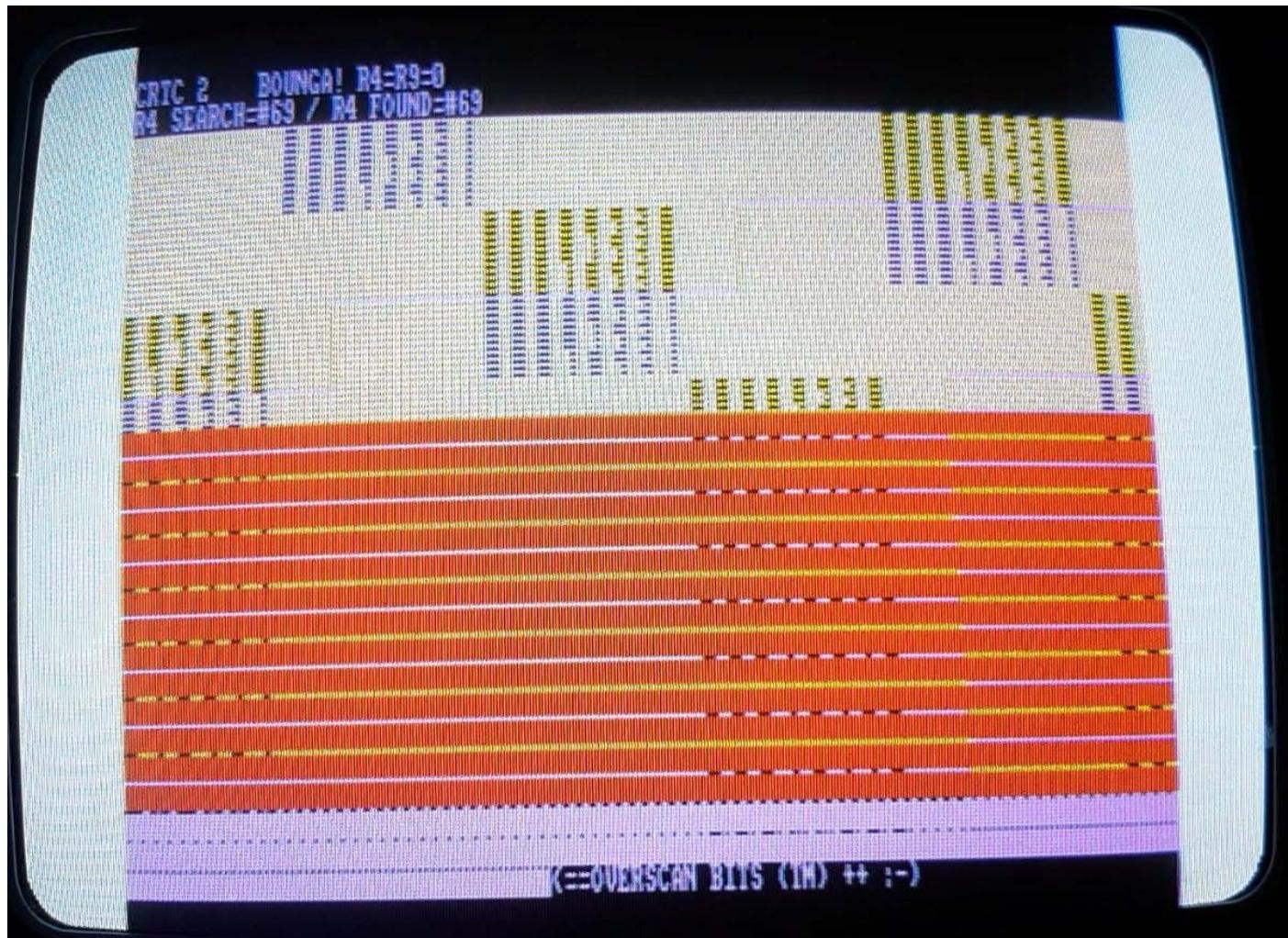






BOUNGA : CRTC 2 R4=R9=0 FORCED

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```



INTERLACE VM

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE URAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```

```
CRTC 2 INTERLACE VIDEO MODE
CRTC WITH R6=19:
R8-3 ON LINE 0 : FRAME SIZE=#4E40 usec (R9=7)(R7=0)
R8-3 ON LINE 1 : FRAME SIZE=#4E40 usec (R9=7)(R7=0)
R8-3 ON LINE 2 : FRAME SIZE=#4E40 usec (R9=7)(R7=0)
R8-3 ON LINE 3 : FRAME SIZE=#4E40 usec (R9=7)(R7=0)
R8-3 ON LINE 4 : FRAME SIZE=#4E40 usec (R9=7)(R7=0)
R8-3 ON RASTER LINE 2 / R8=0 ON LINE 43 / FRAME SIZE=#4000 usec (R9=7)(R7=0)

CRTC WITH R6=17:
R8-3 ON LINE 0 : FRAME SIZE=#4E30 usec (R9=7)(R7=0)
R8-3 ON LINE 1 : FRAME SIZE=#4E30 usec (R9=7)(R7=0)
R8-3 ON LINE 2 : FRAME SIZE=#4E40 usec (R9=7)(R7=0)
R8-3 ON LINE 3 : FRAME SIZE=#4E20 usec (R9=7)(R7=0)
R8-3 ON LINE 4 : FRAME SIZE=#4E40 usec (R9=7)(R7=0)
R8-3 ON RASTER LINE 2 / R8=0 ON LINE 43 / FRAME SIZE=#4000 usec (R9=7)(R7=0)

R8-13 BEFORE RS
CRTC WITH R6=19:
R8-3 ON LINE 0 : FRAME SIZE=#3020 usec (R9=7)(R7=0)
R8-3 ON LINE 1 : FRAME SIZE=#3020 usec (R9=7)(R7=0)
R8-3 ON LINE 2 : FRAME SIZE=#3020 usec (R9=7)(R7=0)
R8-3 ON LINE 3 : FRAME SIZE=#3020 usec (R9=7)(R7=0)
R8-3 ON LINE 4 : FRAME SIZE=#3020 usec (R9=7)(R7=0)
R8-3 ON RASTER LINE 2 / R8=0 ON LINE 43 / FRAME SIZE=#3000 usec (R9=7)(R7=0)
```

CHC 2 INTERFACE VIDEO MODE

R8 UPDATE DELAY + 0 FRAME DELAY
R8=3 ON CB8=0, CB=#30 : FRAME SIZE=#4E40 usec (R9=7)
R8=3 ON CB8=0, CB=#31 : FRAME SIZE=#4E40 usec (R9=7)
R8=3 ON CB8=0, CB=#32 : FRAME SIZE=#4E40 usec (R9=7)
R8=3 ON CB8=0, CB=#33 : FRAME SIZE=#4E20 usec (R9=7)
R8=3 ON CB8=1, CB=#30 : FRAME SIZE=#4E20 usec (R9=7)
R8 UPDATE DELAY + 0 FRAME DELAY
R8=3 ON CB8=0, CB=#30 : FRAME SIZE=#4E40 usec (R9=7)
R8=3 ON CB8=0, CB=#31 : FRAME SIZE=#4E40 usec (R9=7)
R8=3 ON CB8=0, CB=#32 : FRAME SIZE=#4E40 usec (R9=7)
R8=3 ON CB8=0, CB=#33 : FRAME SIZE=#4E20 usec (R9=7)
R8=3 ON CB8=1, CB=#30 : FRAME SIZE=#4E20 usec (R9=7)
R8 UPDATE DELAY + 1 FRAME DELAY
R8=3 ON CB8=0, CB=#30 : FRAME SIZE=#4E60 usec (R9=7)
R8=3 ON CB8=0, CB=#31 : FRAME SIZE=#4E60 usec (R9=7)
R8=3 ON CB8=0, CB=#32 : FRAME SIZE=#4E60 usec (R9=7)
R8=3 ON CB8=0, CB=#33 : FRAME SIZE=#4E40 usec (R9=7)
R8=3 ON CB8=1, CB=#30 : FRAME SIZE=#4E40 usec (R9=7)

DELAY FOR EVEN-ODD FRAME (E/O R6=50/50, 7F/50, 50/7F, 7F/7F)

R8=3 ON LINE 0 : FRAME SIZE=#9060 usec (R9=7)(R7=0)
R8=3 ON LINE 0 : FRAME SIZE=#9040 usec (R9=7)(R7=0)
R8=3 ON LINE 0 : FRAME SIZE=#9080 usec (R9=7)(R7=0)
R8=3 ON LINE 0 : FRAME SIZE=#9080 usec (R9=7)(R7=0)

INTERLACE C4/C9 COUNTERS

CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM
(1) INTERLACE C4/C9 COUNTERS
(2) INTERLACE CRTC 2 C9 STRANGER THING
(3) FAKE VSYNC ON CRTC 2
(4) CRTC 2 FIND C0 MIN
(5) CRTC 2 RLAL
(6) CRTC 1 BUG OUTI R0

(S) BE00 CHECK (CRTC 1)

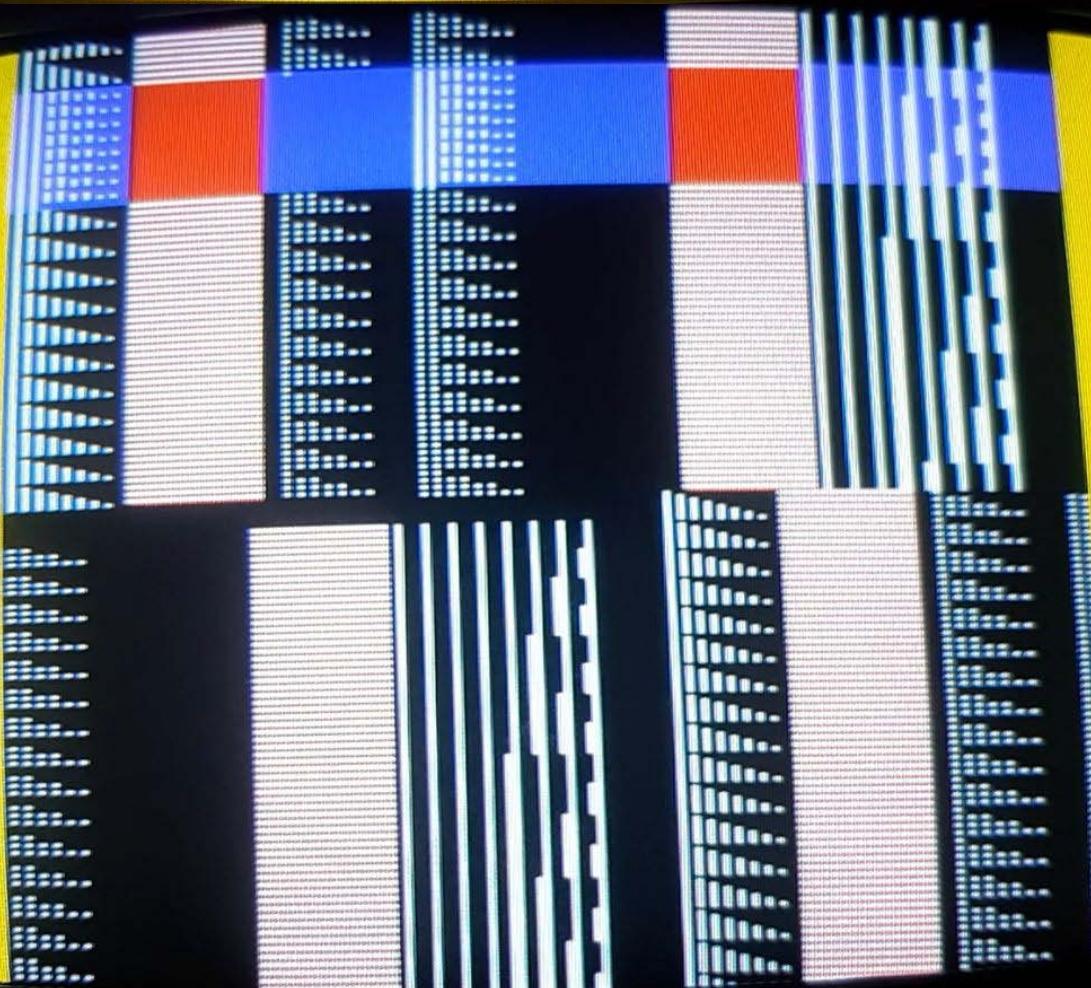
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!

CNIC 2 INTERFACE TM TESTS - C4/C9 COUNTING IN TM PERIOD (MOVE 200)

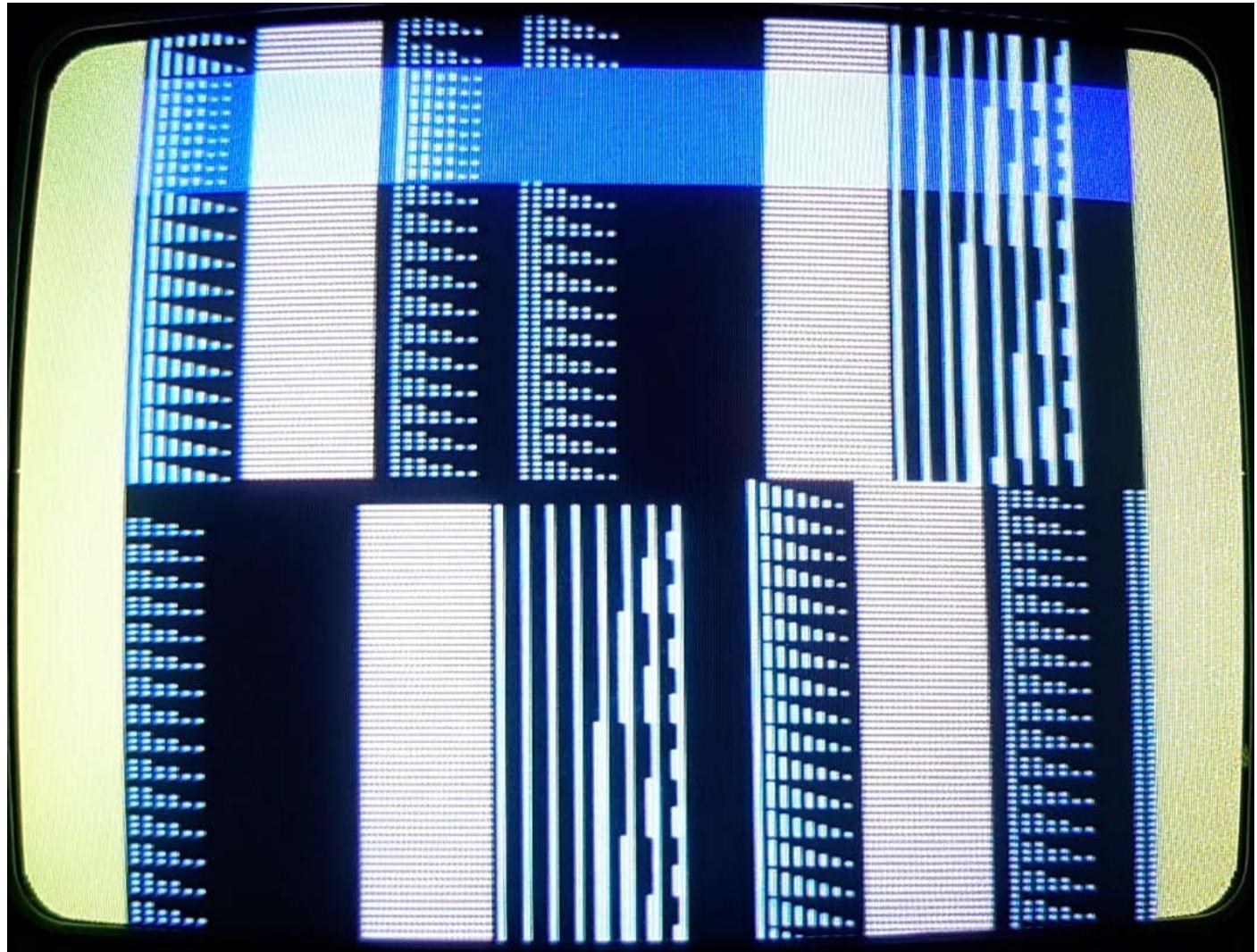
NEXT SCREEN : C4=6, C9=0 >> UPD R9=7, R8=3 (+3105)

EXIT TM MODE ON C9=0 >> UPD R9=7, R8=0

AUTOSYNC ON PREVIOUS SCREEN TEST: R4=0xx RS=0xx



Or this

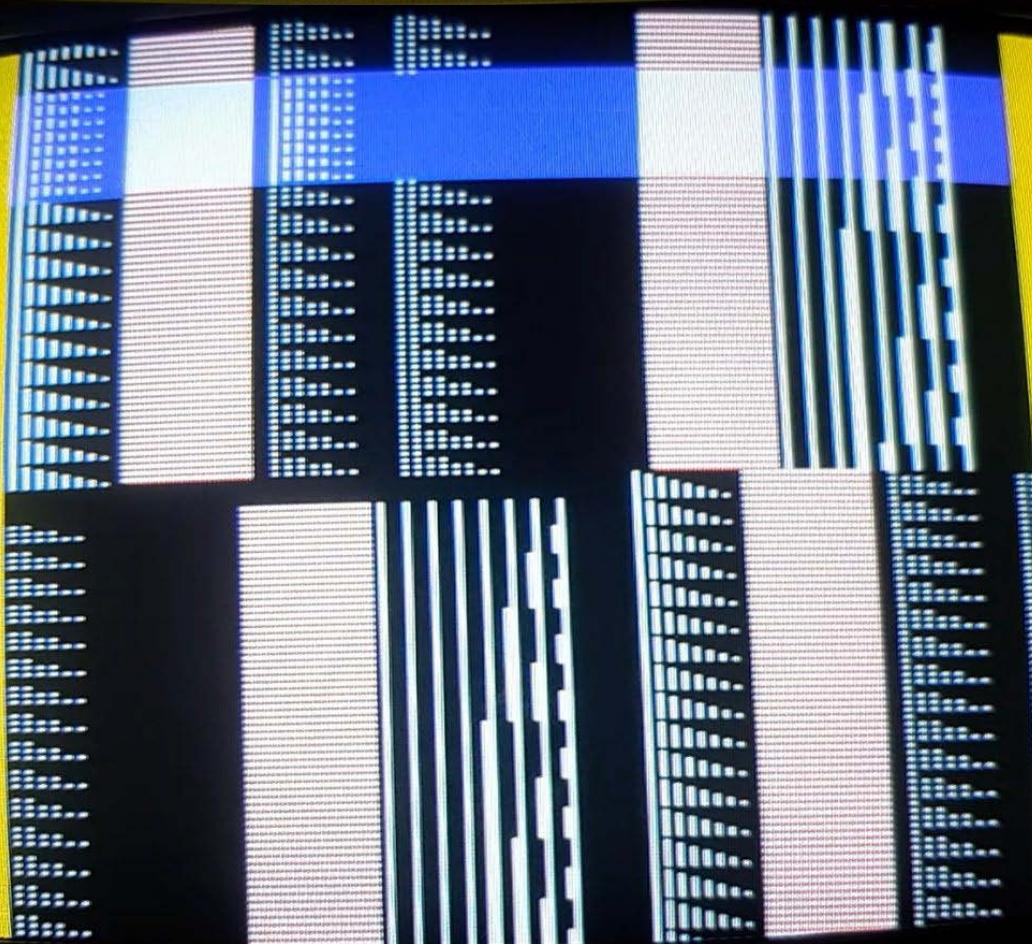


CNIC 2 INTERFACE VM TESTS - C4/C9 COUNTING IN IVM PERIOD (MAXIVE 2003)

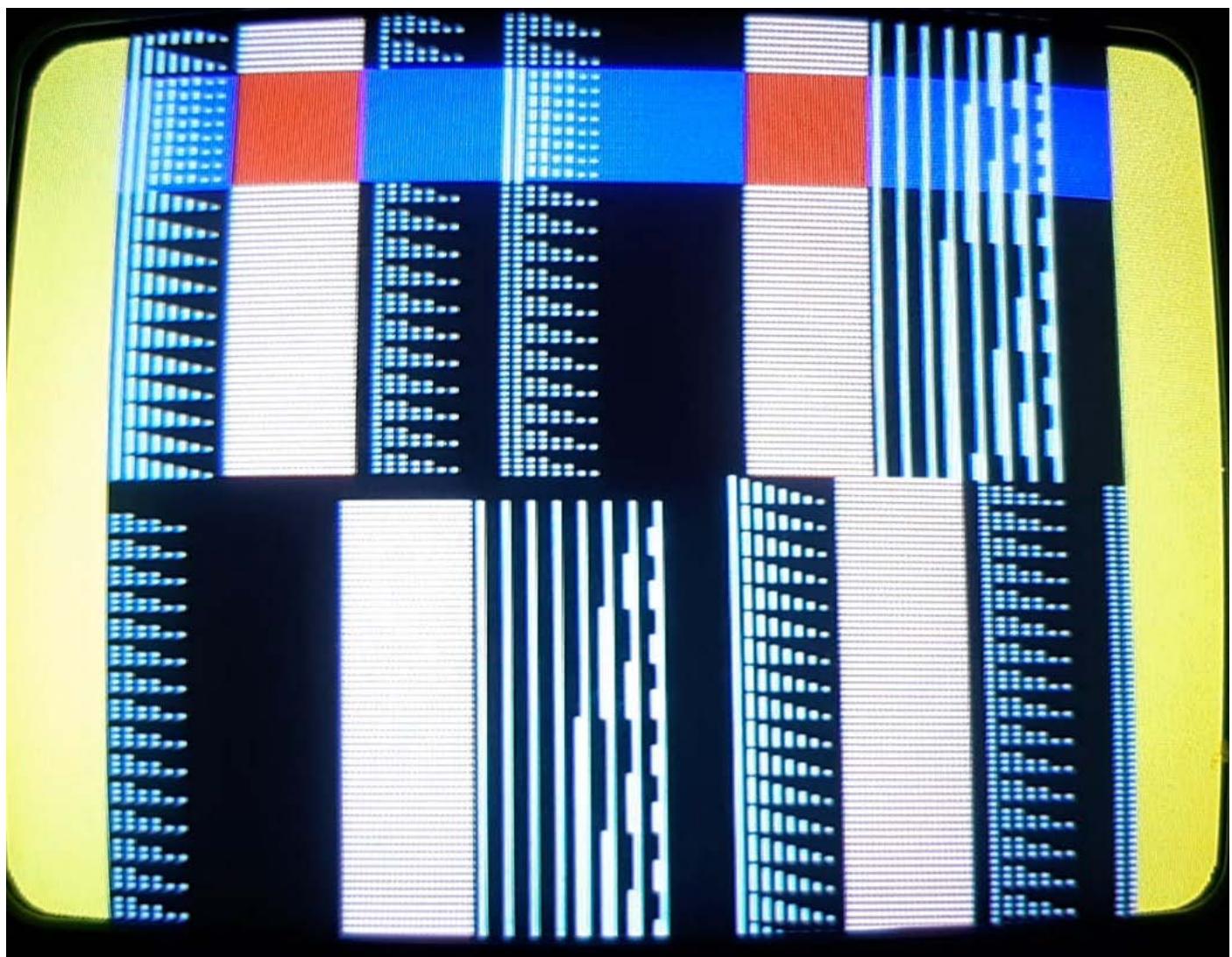
NEXT SCREEN : C4=6, C9=1 => UPD RS=7, RB=3 (+3105)

EXIT IVM MODE ON C9=0 => UPD RS=7, RB=0

AUTOSHINC ON PREVIOUS SCREEN TEST: R4=126 RS=100



Or this

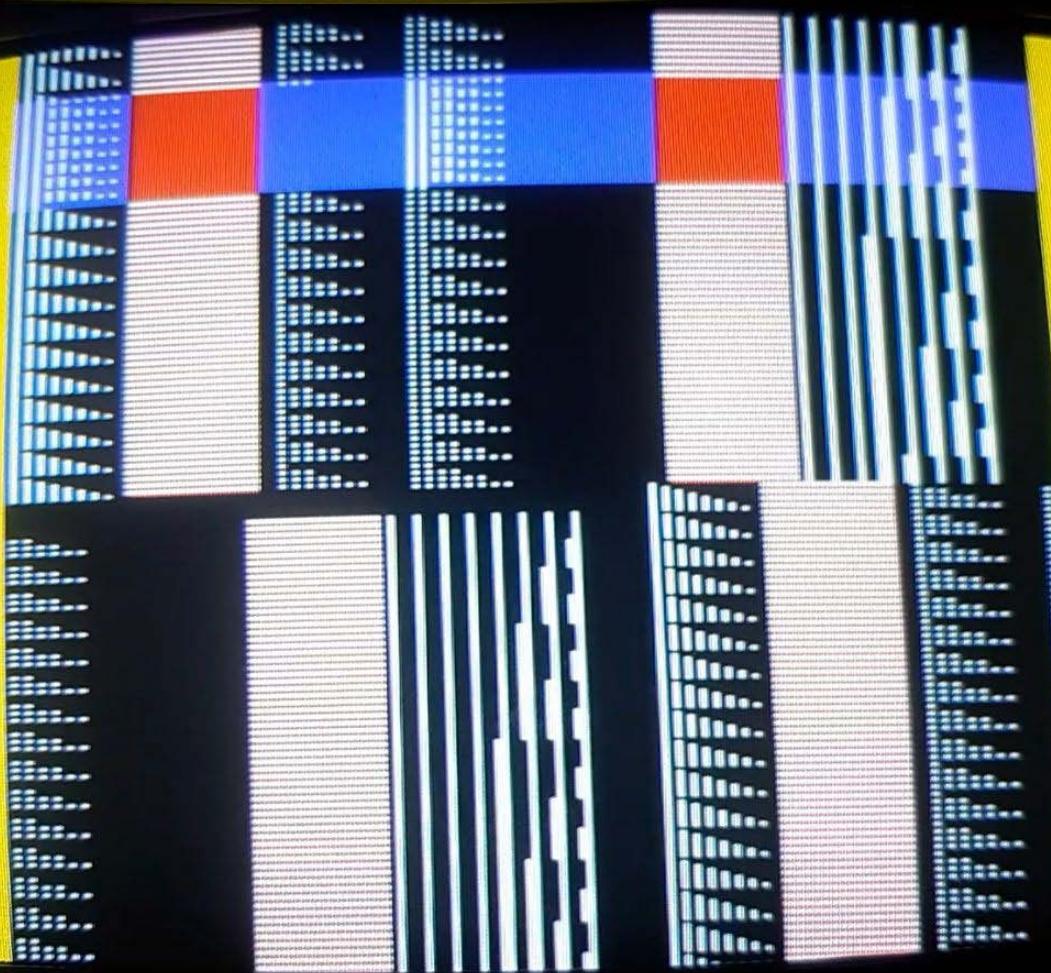


CRIC 2 INTERFACE ON TESTS - C4/C9 COUNTING IN IVM PERIOD (MESSAGE 2003)

NEXT SCREEN : C4=6, C9=2 >> UPD R9=7, R8=3 (+3105)

EXIT IVM MODE ON C9=0 >> UPD R9=7, R8=0

AUTOSYNC ON PREVIOUS SCREEN TEST: R4=126 R5=100

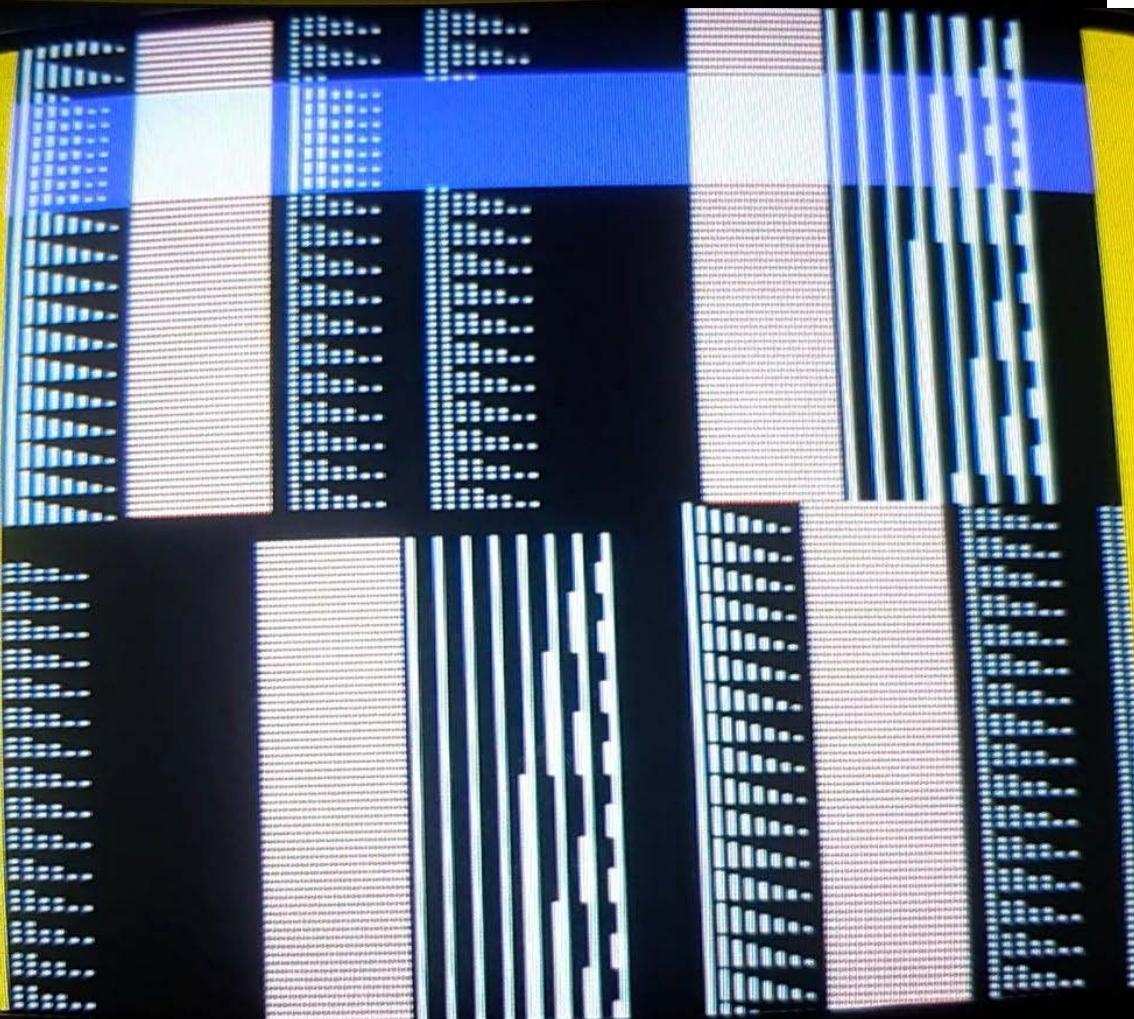


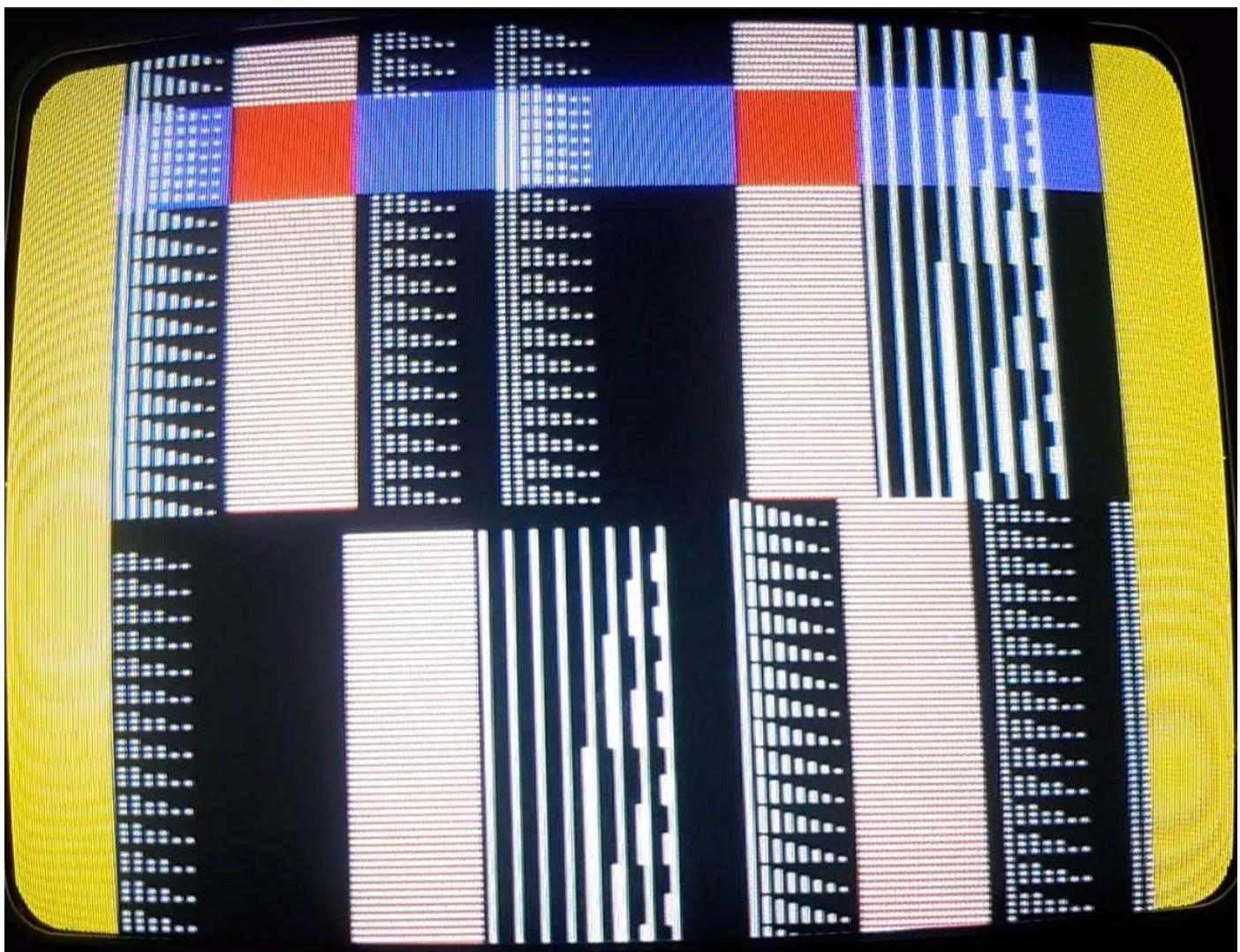
CRTC 2 INTERFACE IVM TESTS - C4/C5 COUNTING IN IVM PERIOD (MAX 2000)

NEXT SCREEN : C4=6, C5=3 >> UPD R9=7, R8=3 (+3105)

EXIT IVM MODE ON C4=0 >> UPD R9=7, R8=0

AUTOSYNC ON PREVIOUS SCREEN TEST: R4=026 R5=400



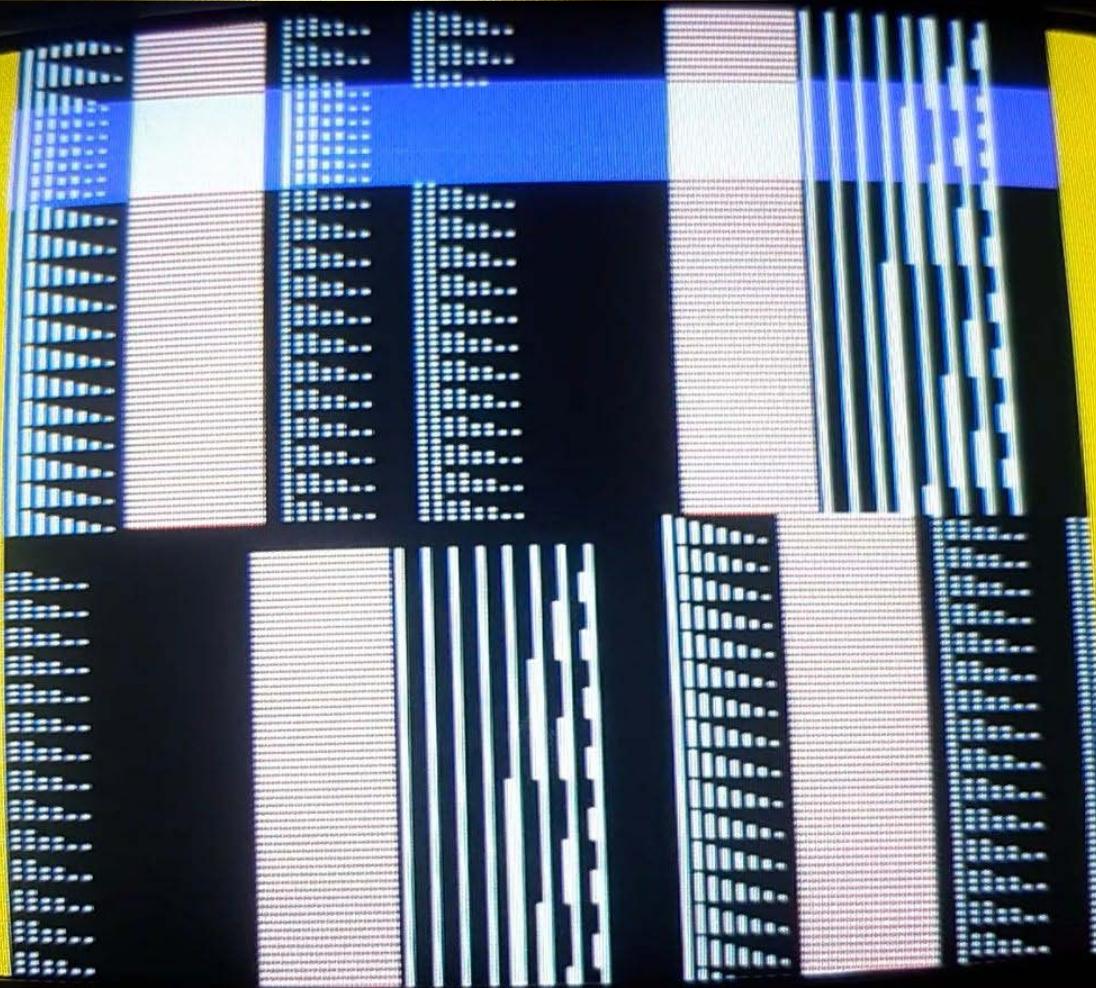


CRTC 2 INTERFACE VM TESTS - C4/C9 COUNTING IN IVM PERIOD (MOVE 200)

NEXT SCREEN : C4=6, C9=5 >> UPD R9=7, R8=3 (+3105)

EXIT IVM MODE ON C9=0 >> UPD R9=7, R8=0

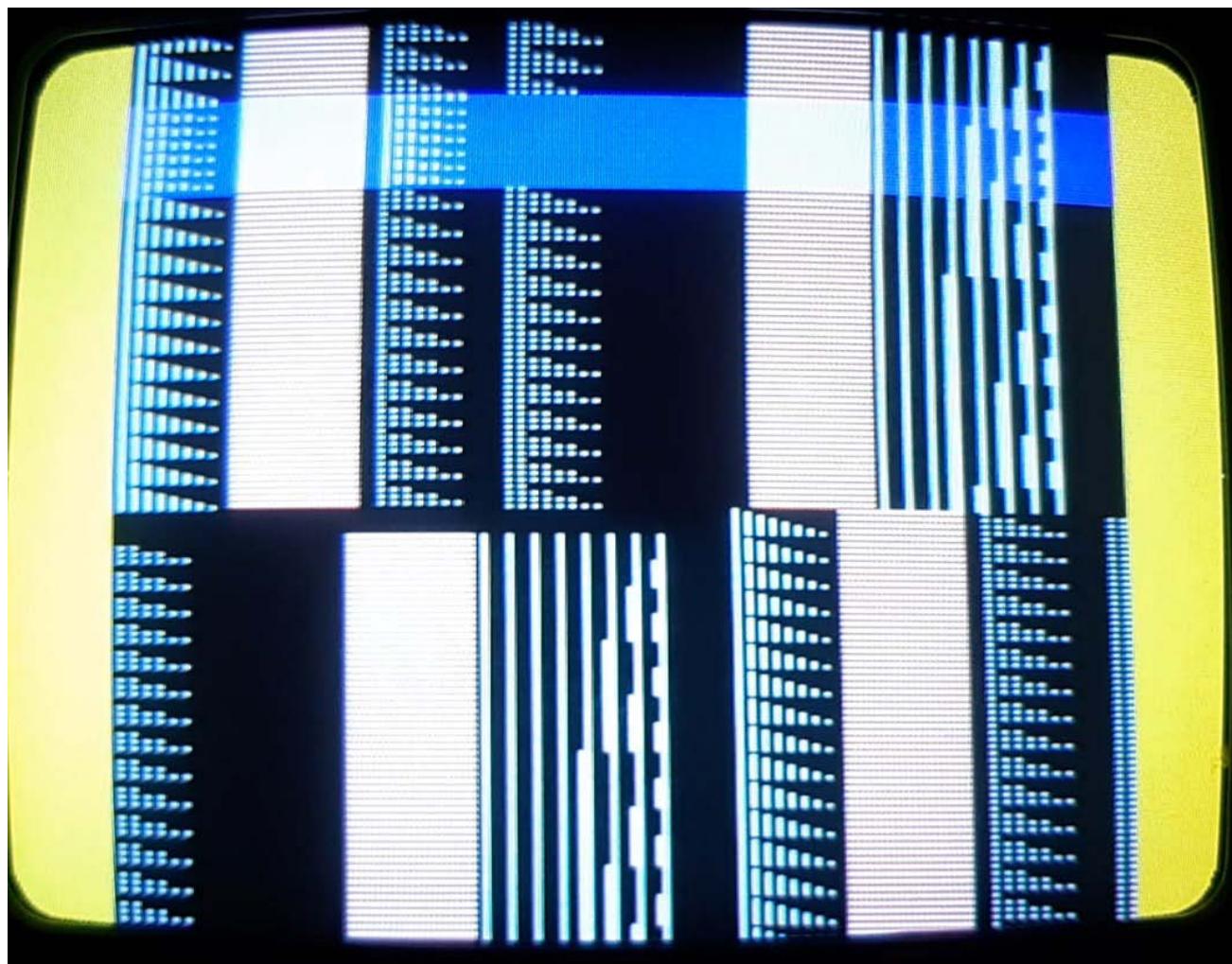
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=126 R5=100



CRIC 2 INTERFACE UV TESTS - C4/C9 COUNTING IN IVM PERIOD (CHAUVIE ZONE)

NEXT SCREEN : C4=6, C9=6 >> UPD R9=7, R8=3 (+3105)
EXIT IVM MODE ON C9=0 >> UPD R9=7, R8=0

AUTOSYNC ON PREVIOUS SCREEN TEST: R4=R26 RS=R00

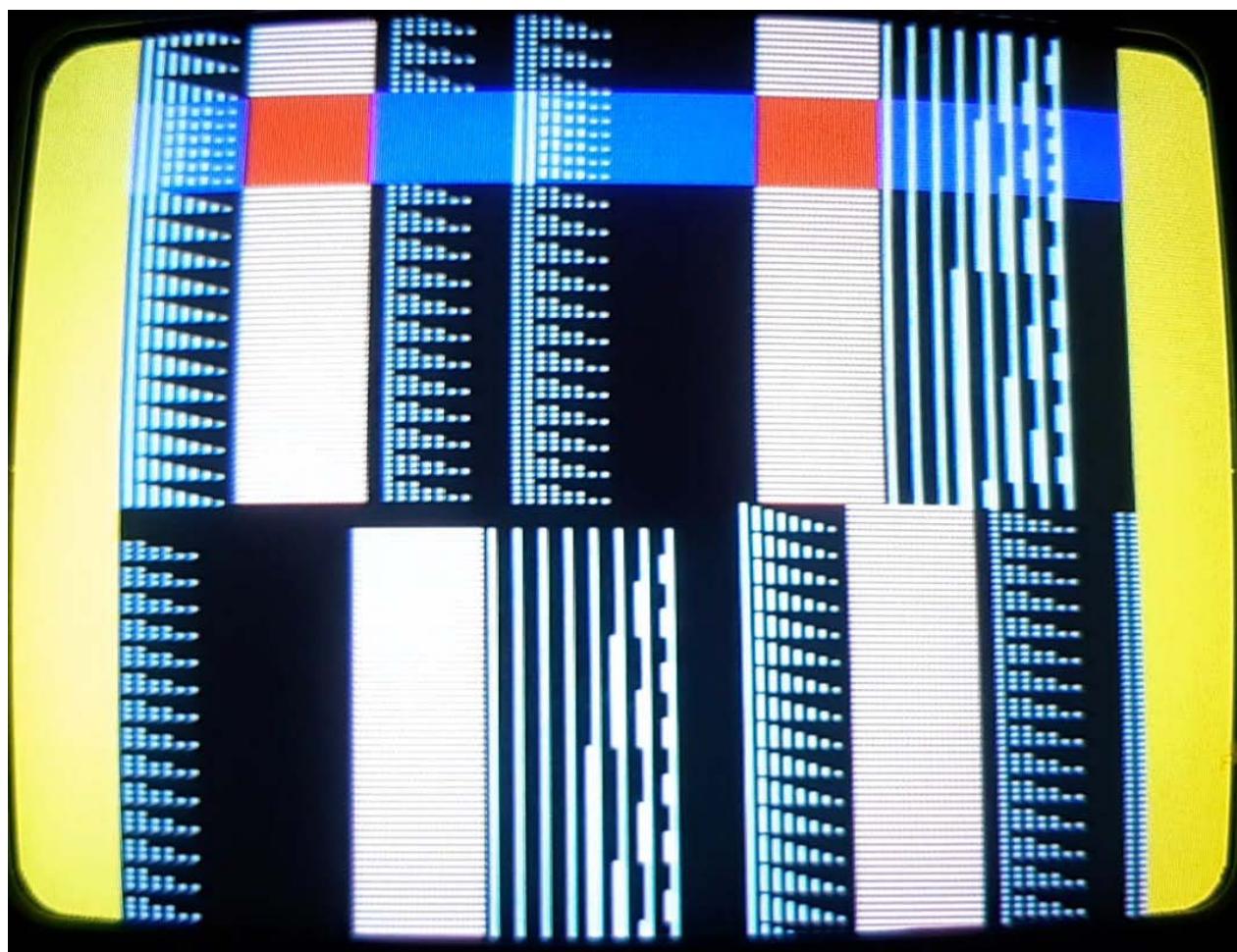


CBIC 2 INTERFACE INN TESTS - C9/C9 COUNTING IN IOW PERIOD (GROUVE ZONE)

NEXT SCREEN : C4=6, C9=7)) UPD R9=7, R8=3 (+3105)

EXIT INN MODE ON C9=0)) UPD R9=7, R8=0

AUTOSYNC ON PREVIOUS SCREEN TEST: R4=R26 R5=R00



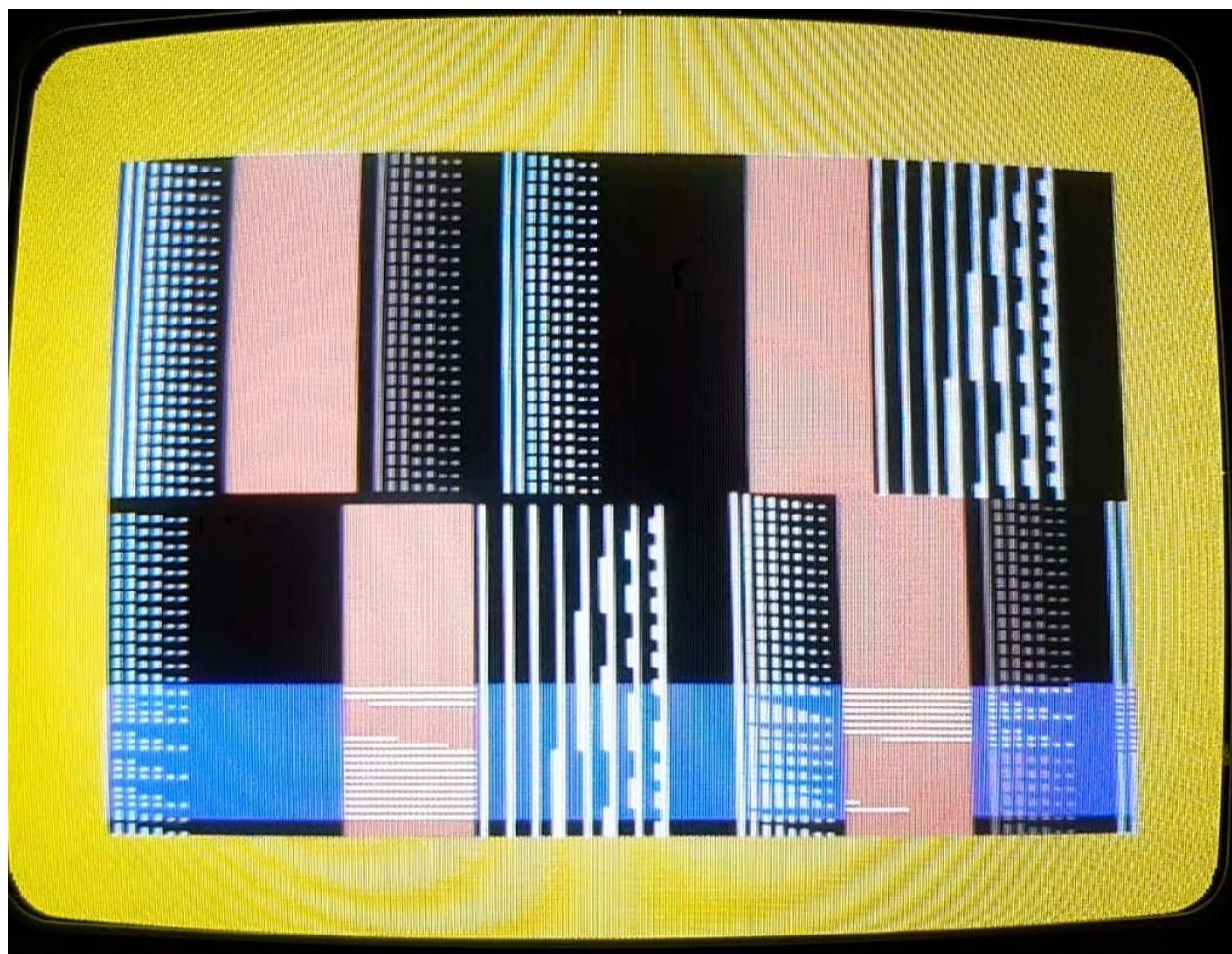
INTERLACE CRTC 2 C9 STRANGER THING

CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT, LOGON SYSTEM

- (1) INTERLACE C4/C9 COUNTERS
- (2) INTERLACE CRTC 2 C9 STRANGER THING
- (3) FAKE VSYNC ON CRTC 2
- (4) CRTC 2 FIND C0 MIN
- (5) CRTC 2 RLAL
- (6) CRTC 1 BUG OUTI R0

(S) BE00 CHECK (CRTC 1)

(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!



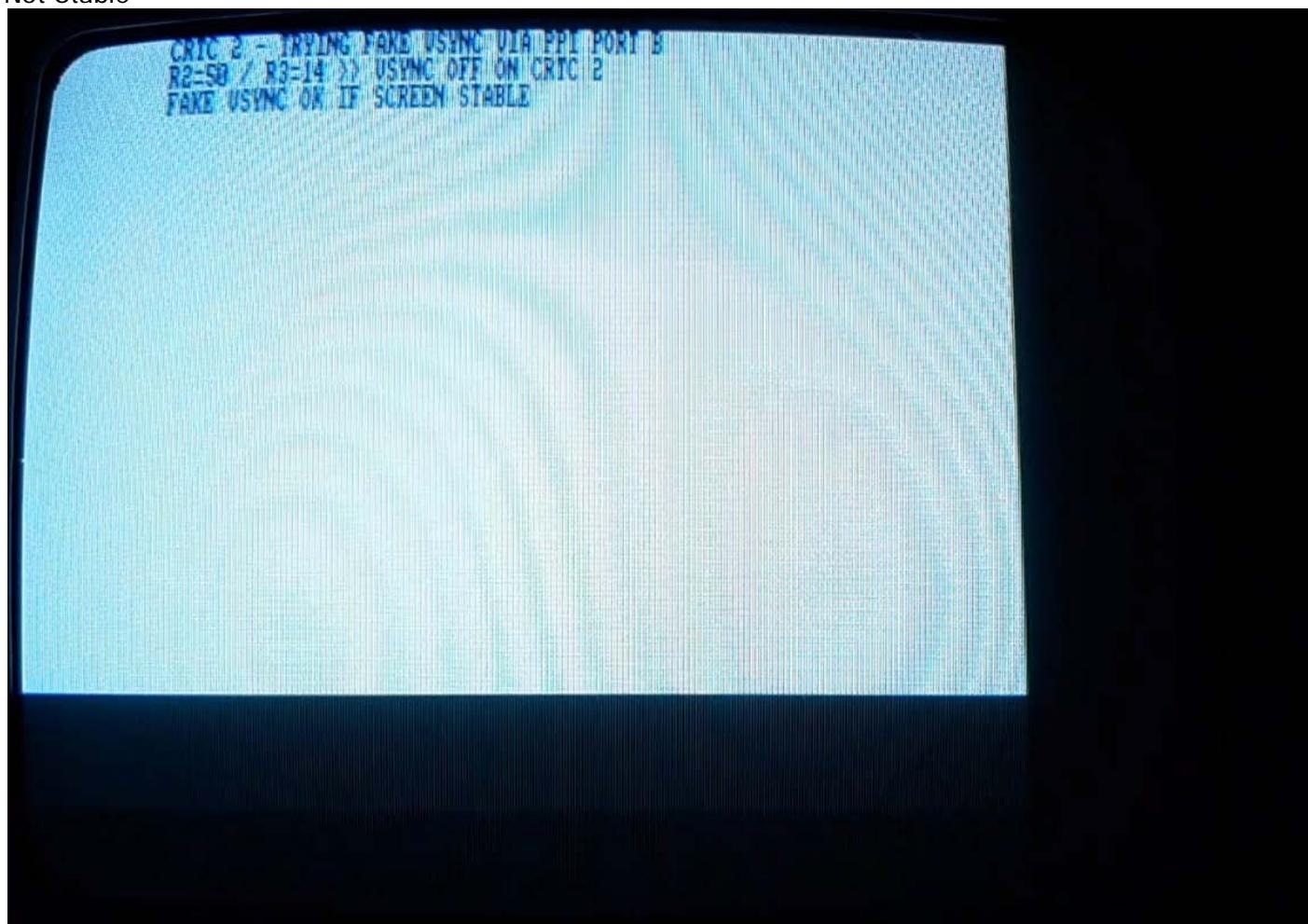
FAKE VSYNC ON CRTC 2

CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM
(1) INTERLACE C4/C9 COUNTERS
(2) INTERLACE CRTC 2 C9 STRANGER THING
(3) FAKE VSYNC ON CRTC 2
(4) CRTC 2 FIND C0 MIN
(5) CRTC 2 RLAL
(6) CRTC 1 BUG OUTI R0

(S) BE00 CHECK (CRTC 1)

(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!

Not Stable



IRIPPING FAKE USYNC DLA PPI PORT 3 MIDDLE SCREEN
FAKE USYNC OK IF USYNC BLACK BAND

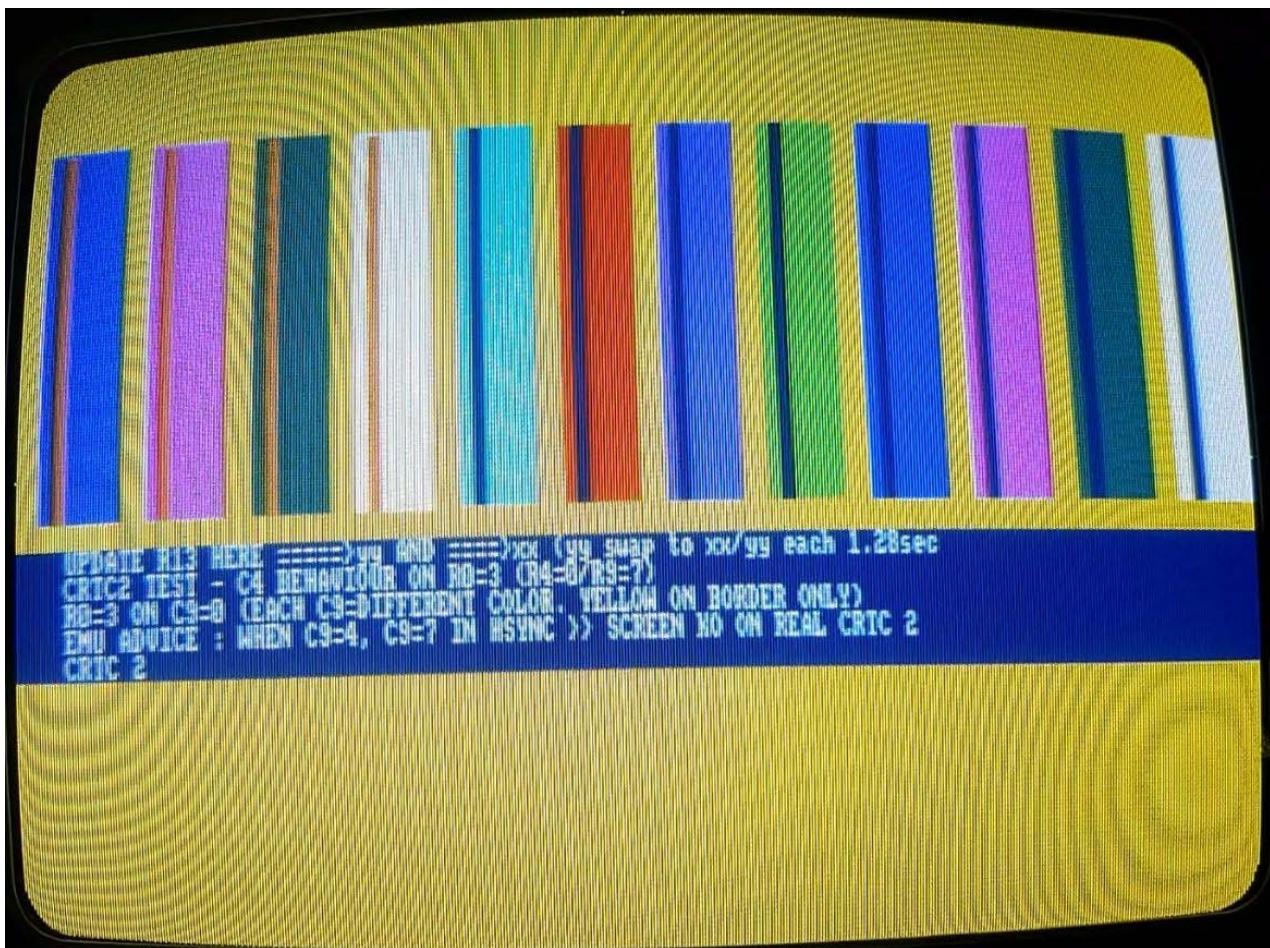
CRTC 2

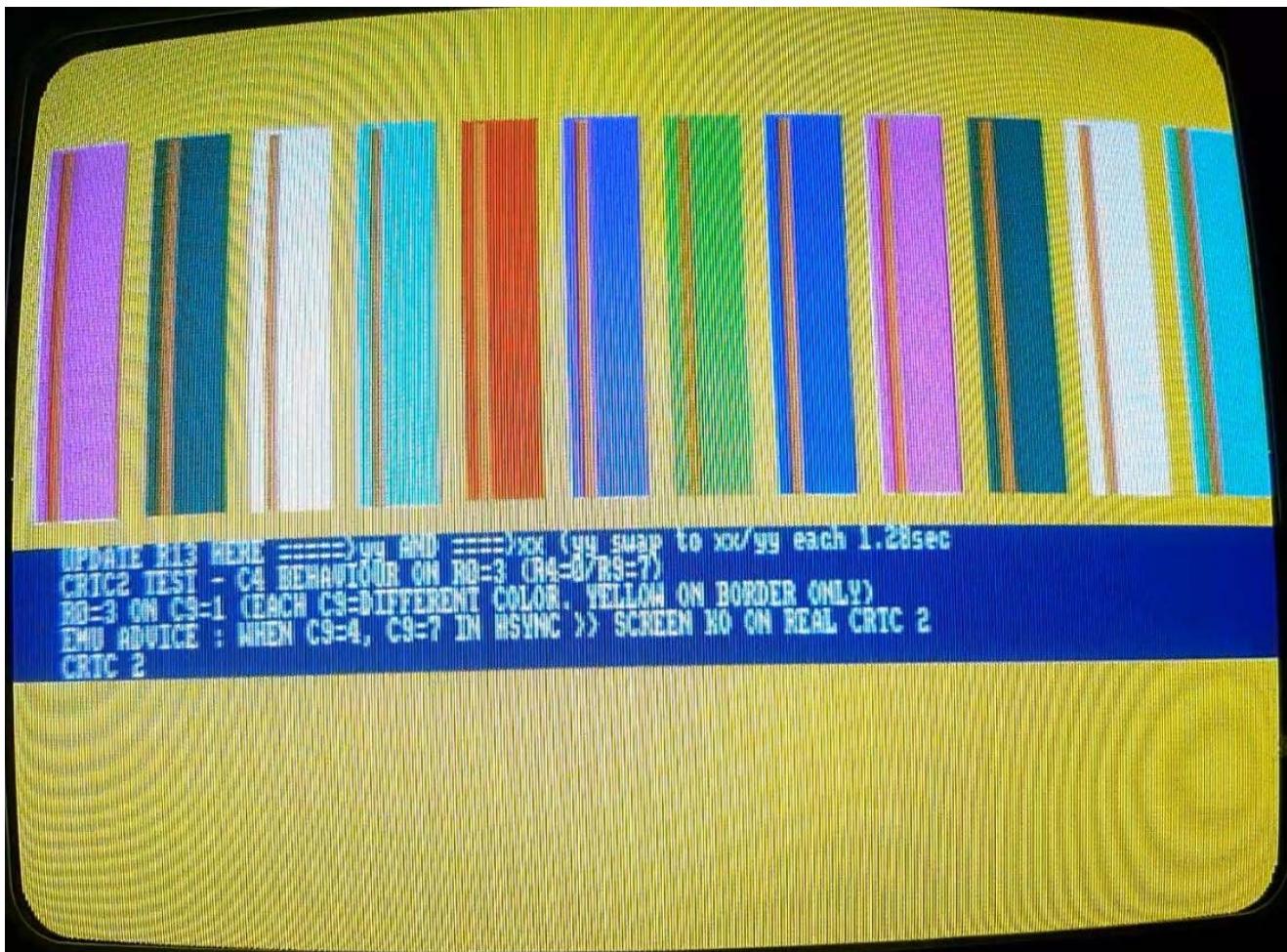
CRTC 2 FIND C0 MIN

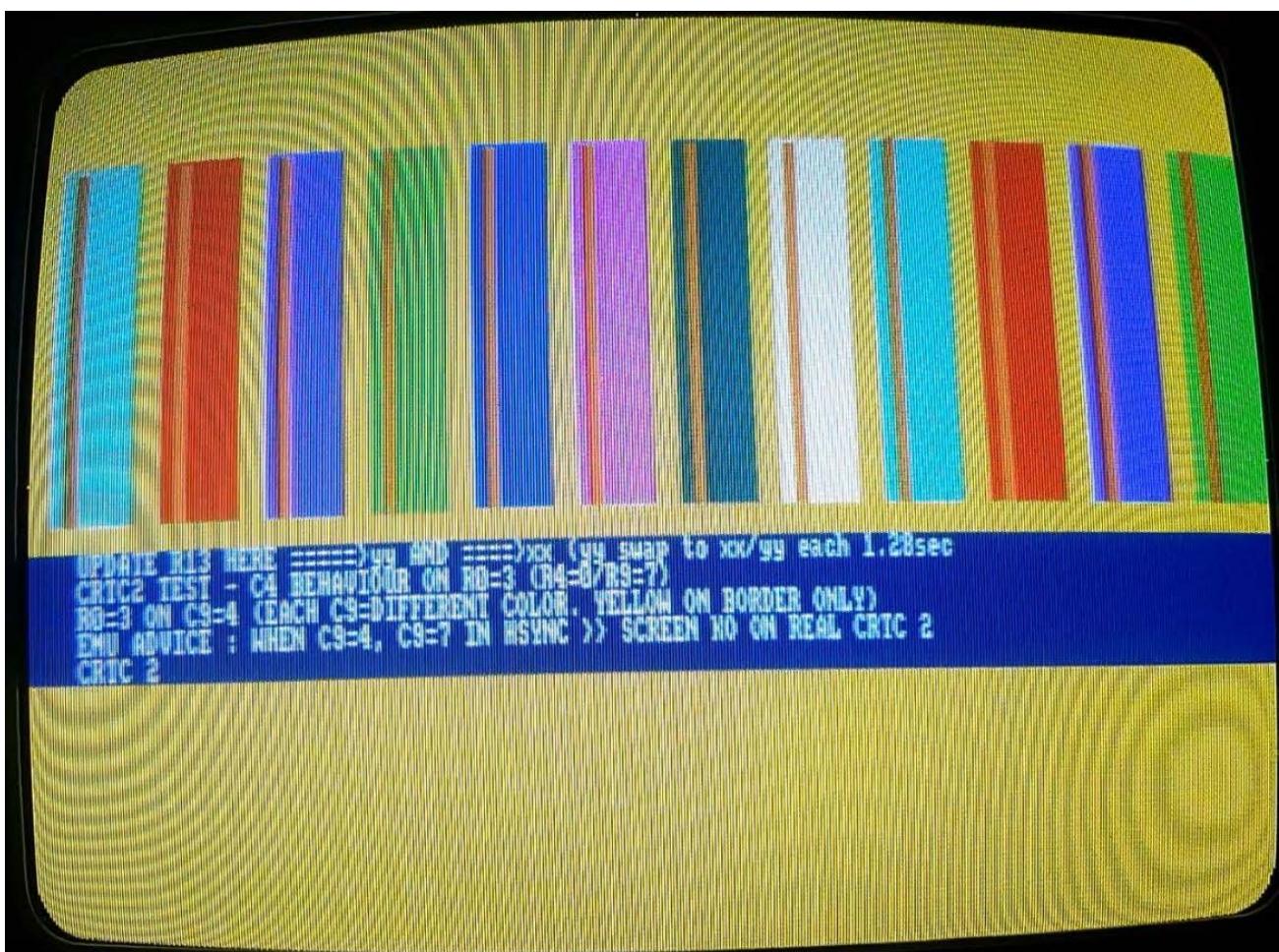
CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM
(1) INTERLACE C4/C9 COUNTERS
(2) INTERLACE CRTC 2 C9 STRANGER THING
(3) FAKE VSYNC ON CRTC 2
(4) CRTC 2 FIND C0 MIN
(5) CRTC 2 RVAL
(6) CRTC 1 BUG OUTI R0

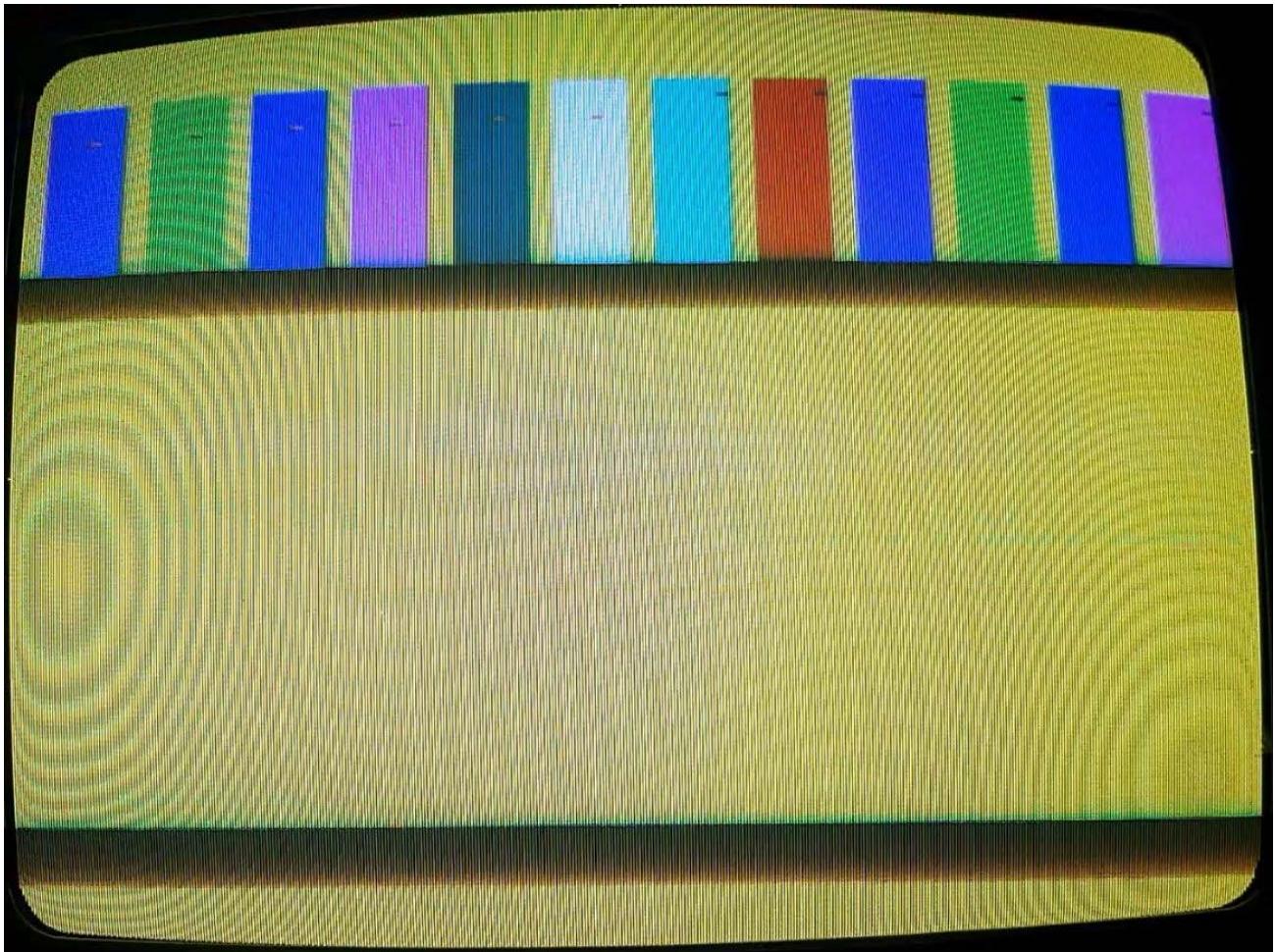
(S) BE00 CHECK (CRTC 1)

(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!

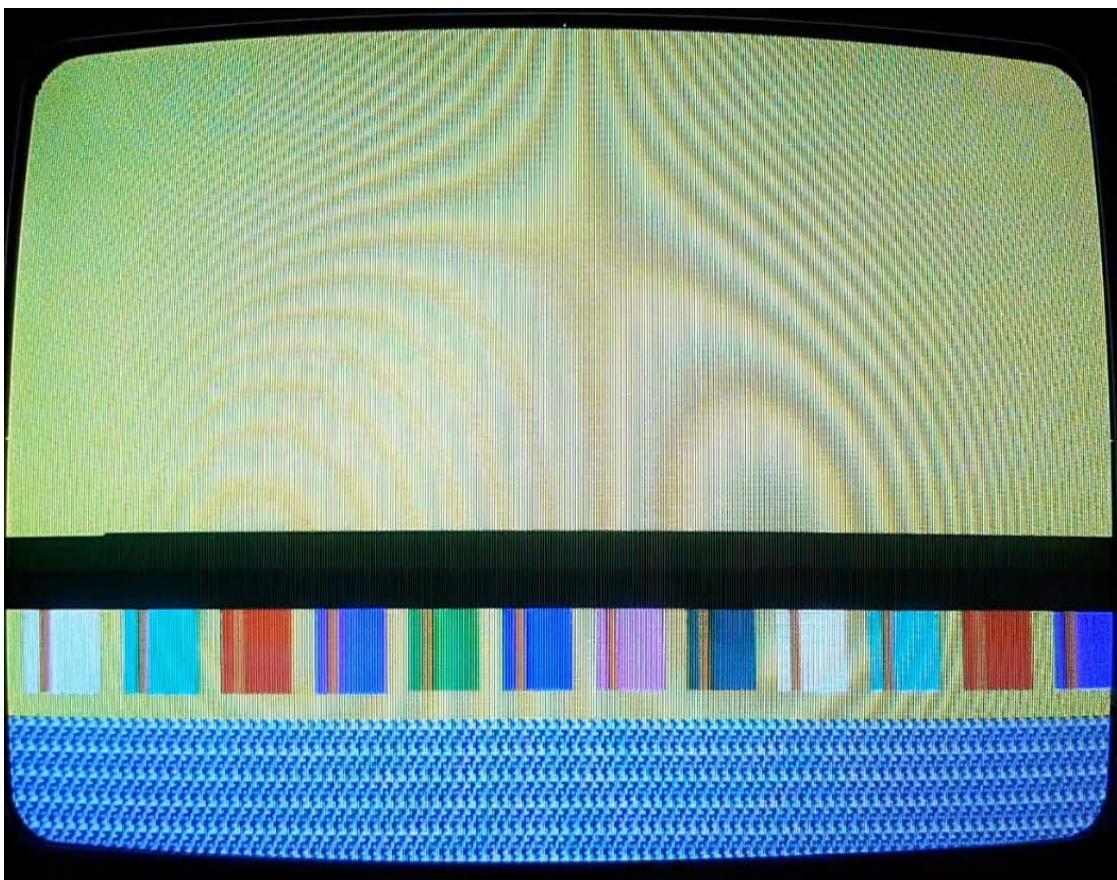








Screen KO (compare to CRTC 1 for stable screen)



(compare to CRTC 1 for stable screen)

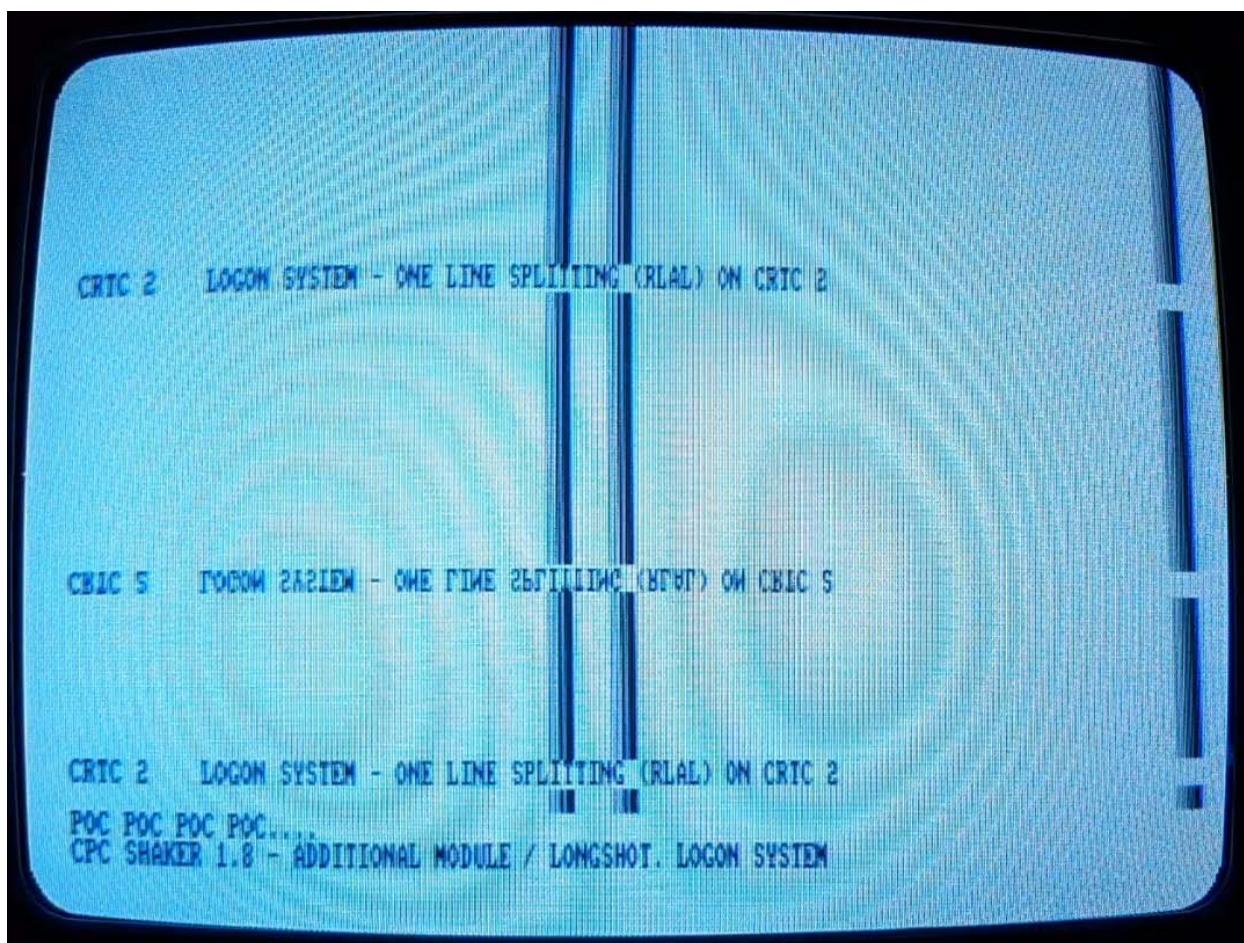
Screen KO

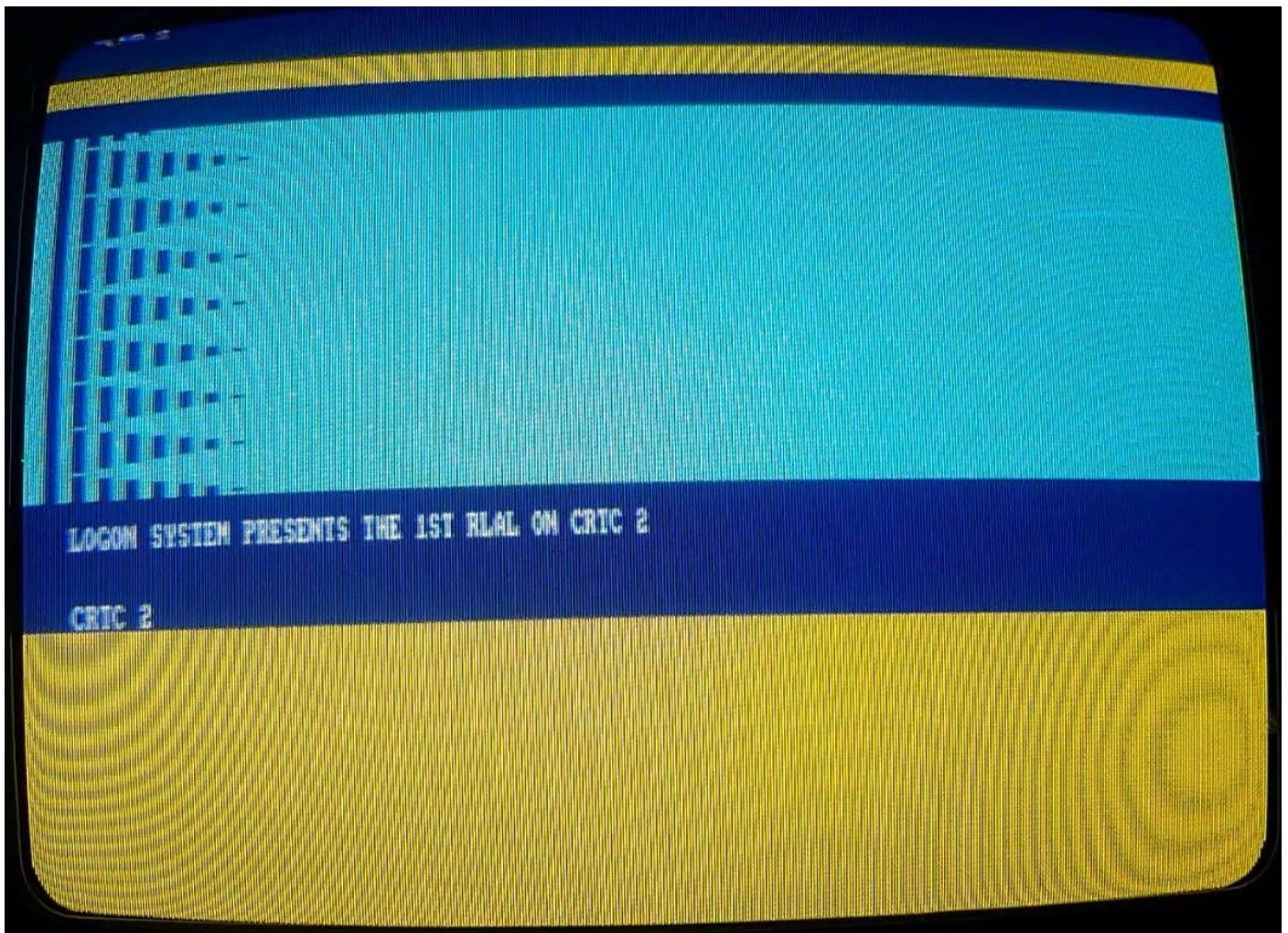
CRTC 2 - 1 LINE RUPTURE

CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM
(1) INTERLACE C4/C9 COUNTERS
(2) INTERLACE CRTC 2 C9 STRANGER THING
(3) FAKE VSYNC ON CRTC 2
(4) CRTC 2 FIND C0 MIN
(5) CRTC 2 RLAL
(6) CRTC 1 BUG OUTI R0

(S) BE00 CHECK (CRTC 1)

(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!





CRTC 1 – BUG OUTI R0

CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM
(1) INTERLACE C4/C9 COUNTERS
(2) INTERLACE CRTC 2 C9 STRANGER THING
(3) FAKE VSYNC ON CRTC 2
(4) CRTC 2 FIND C0 MIN
(5) CRTC 2 RLAL
(6) CRTC 1 BUG OUTI R0

(S) BE00 CHECK (CRTC 1)

(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!

Only for CRTC 1

CRTC 1- BE00 CHECK

CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM
(1) INTERLACE C4/C9 COUNTERS
(2) INTERLACE CRTC 2 C9 STRANGER THING
(3) FAKE VSYNC ON CRTC 2
(4) CRTC 2 FIND C0 MIN
(5) CRTC 2 RLAL
(6) CRTC 1 BUG OUTI R0

(S) BE00 CHECK (CRTC 1)

(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!

Only for CRTC 1