Individual Project II

Signal Integrity Engineering

**PCI Express 4.0 Interconnect Cross-Talk Characterization & Optimization with ANSYS HFSS and Designer**

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Abstract:

The goal of this project was to construct an interconnect with two traces: an active transmit line and a “quiet”, victim transmit line. We were to analyze cross-talk performance and alter the structure in an effort to reduce cross-talk. We built three designs in total: one original, un-optimized design, and two designs that were our effort to reduce cross-talk. We were able to greatly minimize cross-talk, however we found that there seems to be a trade-off with signal integrity, as our signal integrity lowered when our cross-talk lowered.

Group Work:

I worked with Nahlah Condict and Dharini Parthasarathy. The HFSS designs and tests were created as a group. Together, we discussed ideas for reducing cross-talk and what would be best for our project. Individually, we ran the tests on designer to find values for NEXT and FEXT. We each contributed evenly and fairly.

Mary Floren contributed 33%:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

Nahlah Condict contributed 33%:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

Dharini Parthasarathy contributed 33%:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

Problem Overview:

Cross-talk occurs when two channels are in range of each other and they affect each other’s signals or electric fields. This is unwanted, as this altercation can cause signal loss, errors in calculations or noise in a line. Cross-talk is caused by capacitance and inductance between the lines.

The objective of this project was to reduce cross-talk. Since cross-talk is formed by capacitance and inductance between the lines, it is important to address this issue and try to reduce the capacitance and inductance.

The formula for capacitance is:

where is the capacitance value of the dielectric, A is the area of the surfaces facing each other, and d is the distance between the lines. To reduce capacitance, the area of the surfaces facing each other on the lines can be lessened. It will also help reduce inductance to reduce the time the two transmission lines are running in parallel. Another way to minimize capacitance is to increase d, the distance between the lines so the lines are as far away form each other as possible.

Another way to reduce cross-talk is to place grounded wires in-between the aggressor and victim lines. This blocks the signal interference between the two lines.

In our project, we were to have a 10000mil by 100mil motherboard, with two layers of FR4 as the dielectric. The layers of the dielectric were to total 20 mil together, however the specific heights could be altered. Two copper signal traces, each of at least 10 mil width, and 8 separate square power pads of width and length of 50x50 mil were to be placed in this schematic.

We first constructed a standard schematic to have a base-line of cross-talk values so we could see what makes cross-talk improve and what makes it worsen. Then we created two designs using our knowledge of how to reduce capacitance and inductance to optimize cross-talk between the two copper traces.

First Design

The first design consisted of both traces placed at the very top of the highest dielectric. The eight power pads were evenly spaced out in between the two traces. We knew that giving space between the components helps reduce capacitance so we placed everything far apart on the plane. Both traces are on 10mil width and are only 2mil from their respective edge of the schematic. Figure 1 shows the schematic of the first design.

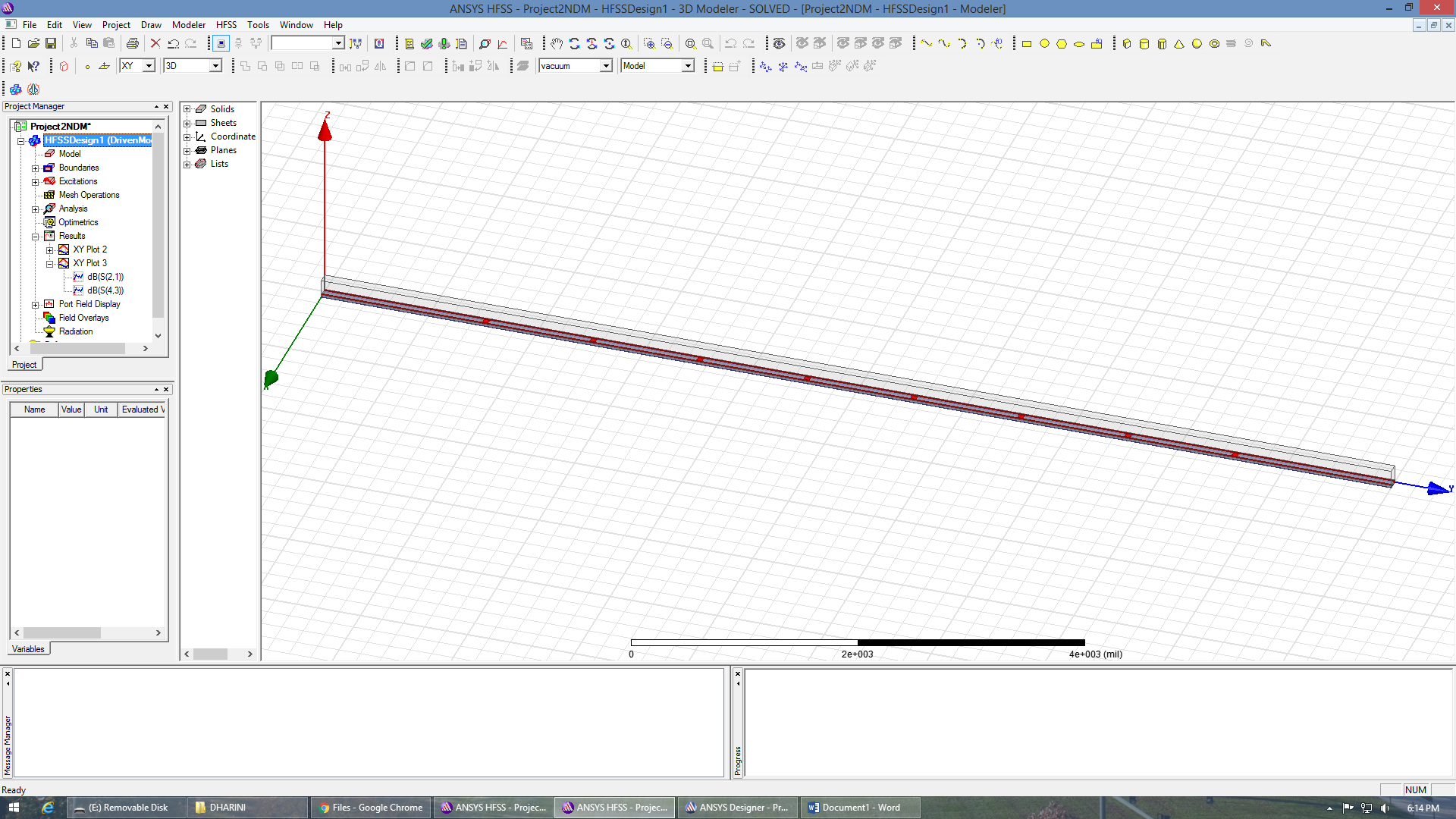


Figure 1: HFSS Design of the first schematic.

We did not encounter many challenges in designing this first model. The calculations of the component placements were not difficult to complete because of the symmetry of the design. Since everything is on the same plane, the z-component remained constant.

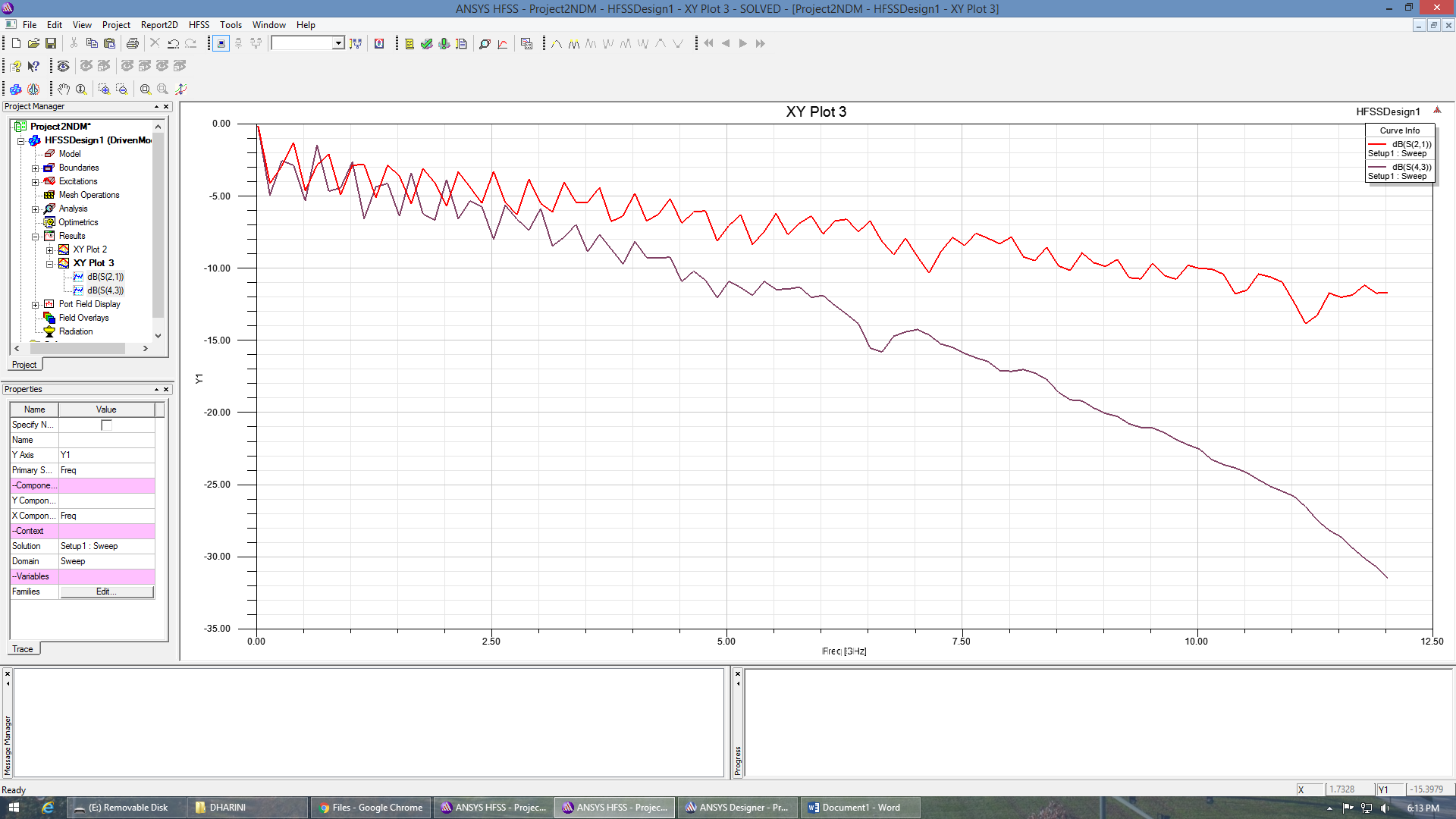


Figure 2: First schematic’s plot of the signals through the wire, S21 and S43.

In our schematic, Port 1 is the input end of a trace while Port 2 is the corresponding output of that trace. Port 3 is the input of the other trace while Port 4 is the corresponding output of that trace. Therefore, by plotting S21 and S43, we can observe the signal on the trace.

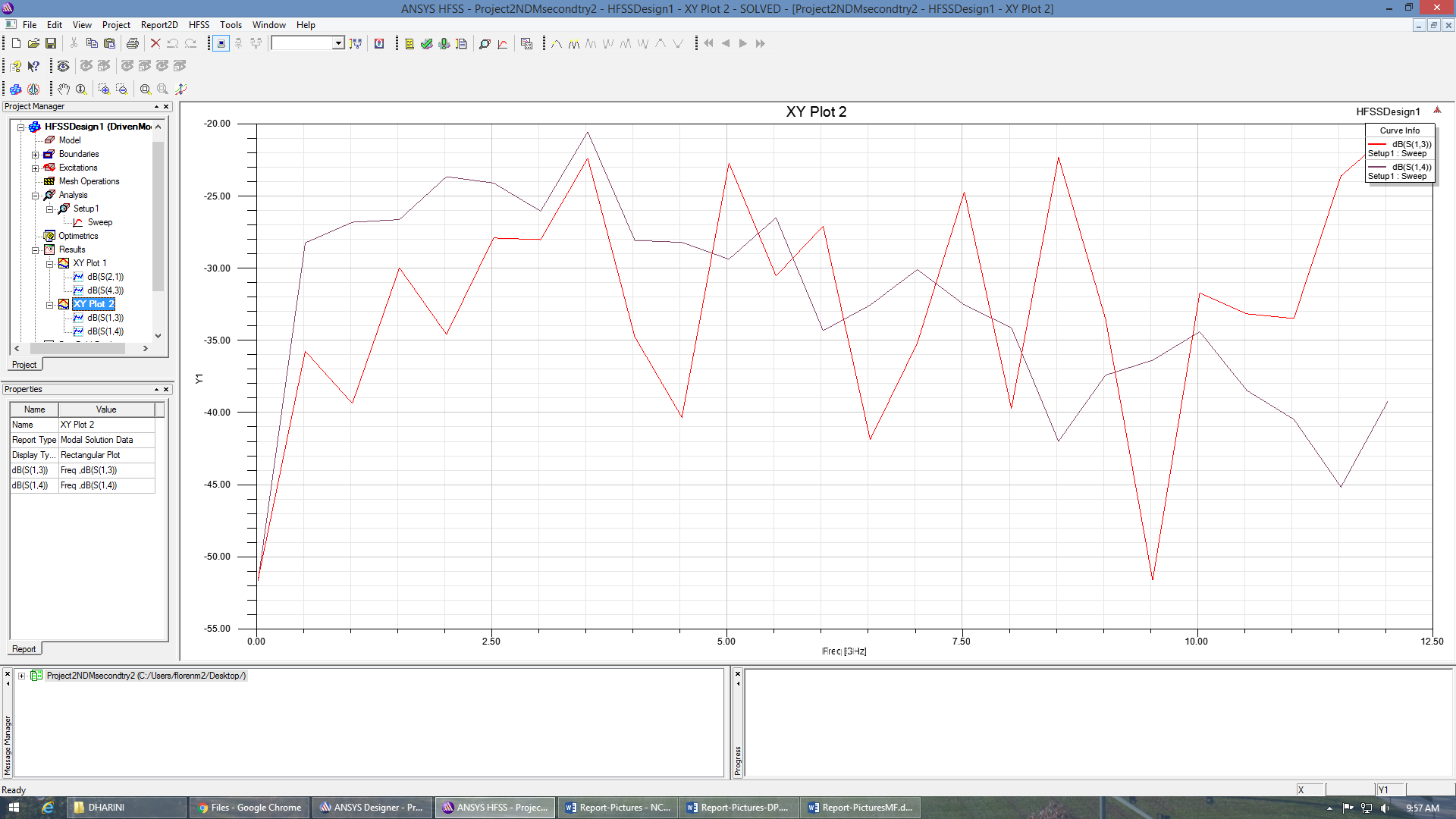


Figure 3: The plot of S13 and S14.

Figure 3 displays the relationship between the input and output signal, determining the quality of the signal integrity, or how well the original signal is maintained.

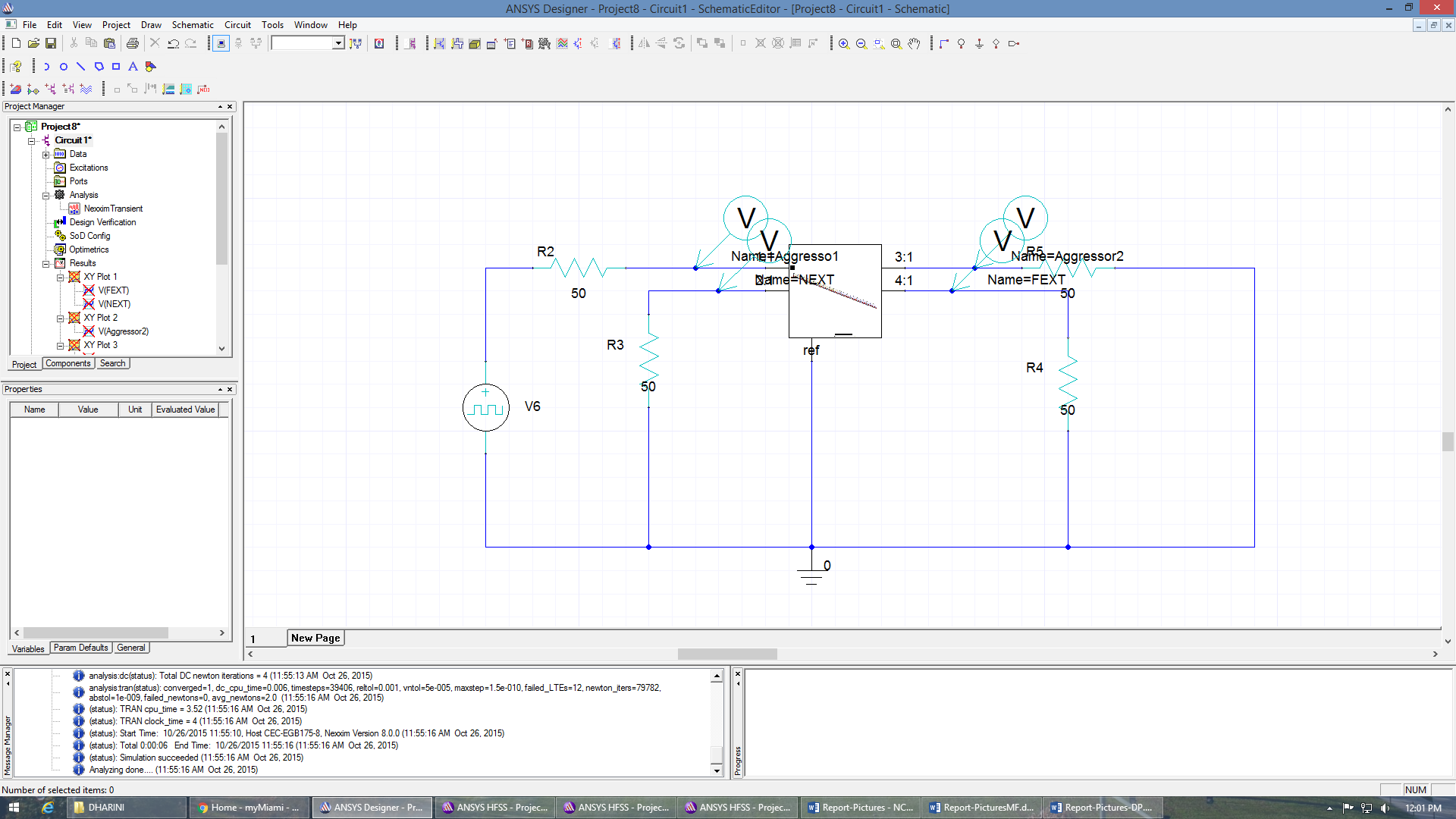


Figure 4: The designer circuit for the simulation of the first schematic.



Figure 5: The input signal of the aggressor trace.

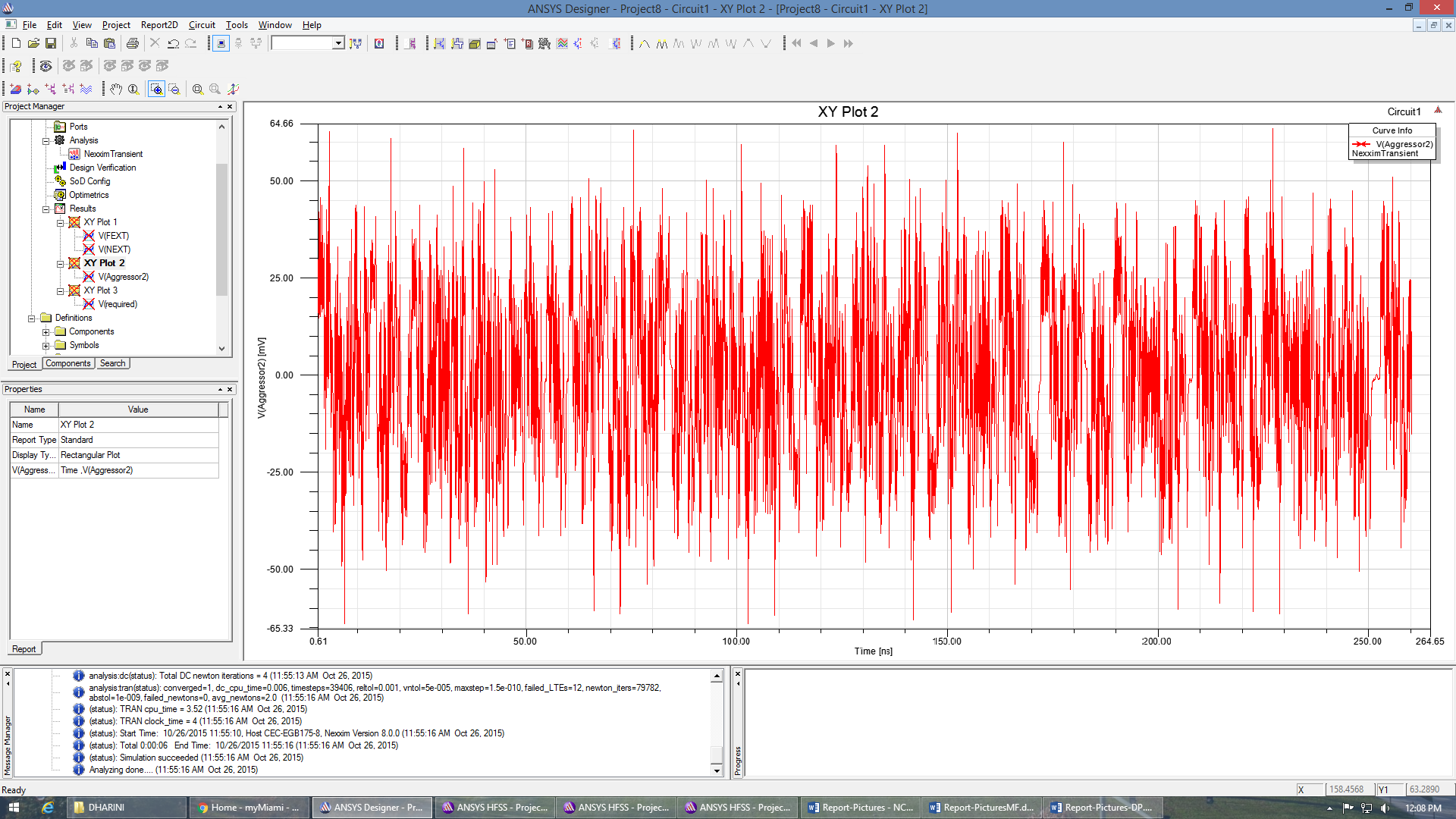


Figure 6: The input signal of the aggressor trace.

Figure 5 and 6 display the signal through the aggressor. It can be seen that a square wave is put into the aggressor and, though it is still a clear signal when it exits, it is altered through the process.

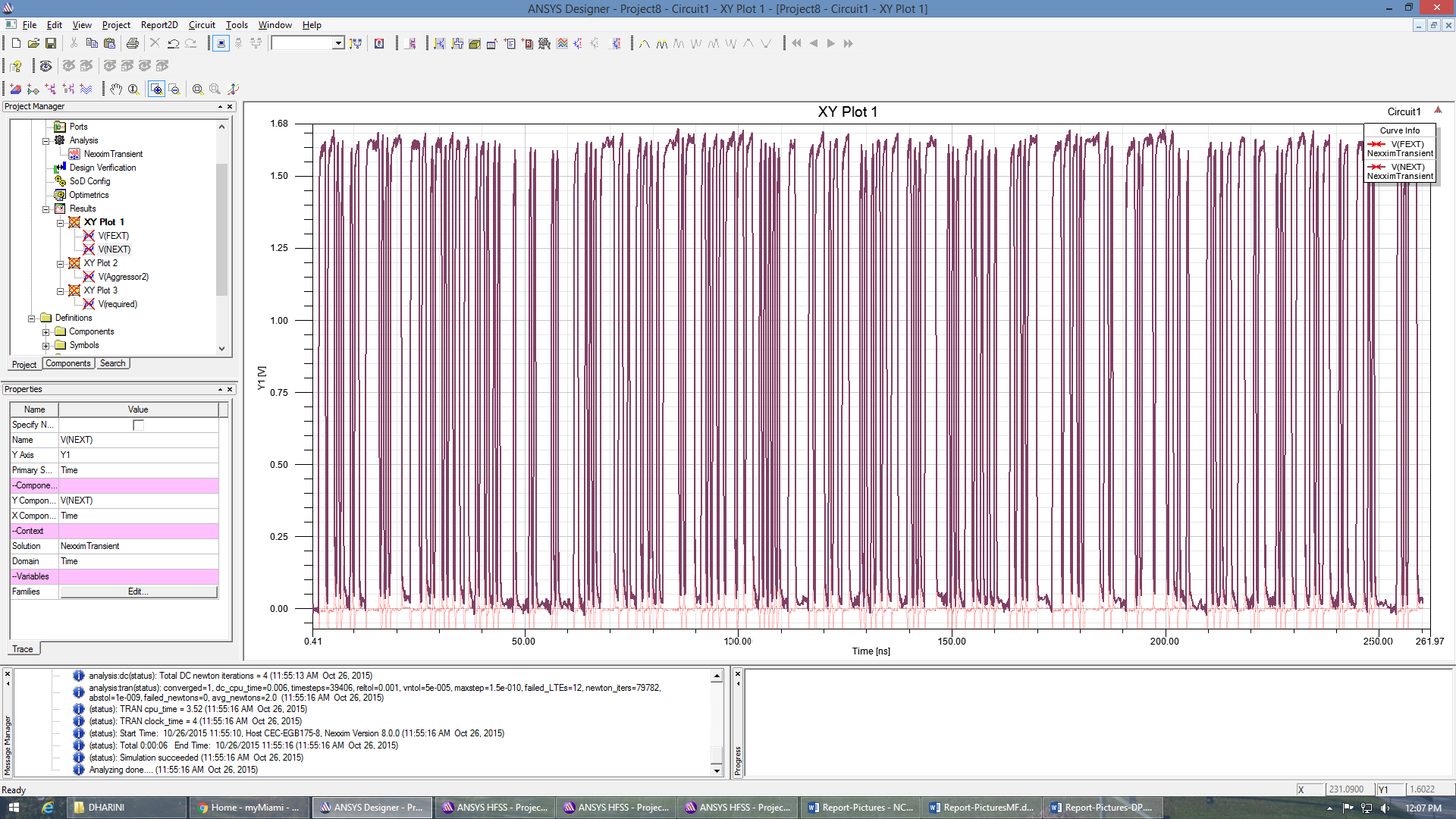


Figure 7: The NEXT values of the first schematic.

The NEXT, or Next End Cross-talk, values can be seen in Figure 7. They are around 1.65 V, which is pretty average in terms of cross-talk optimization.

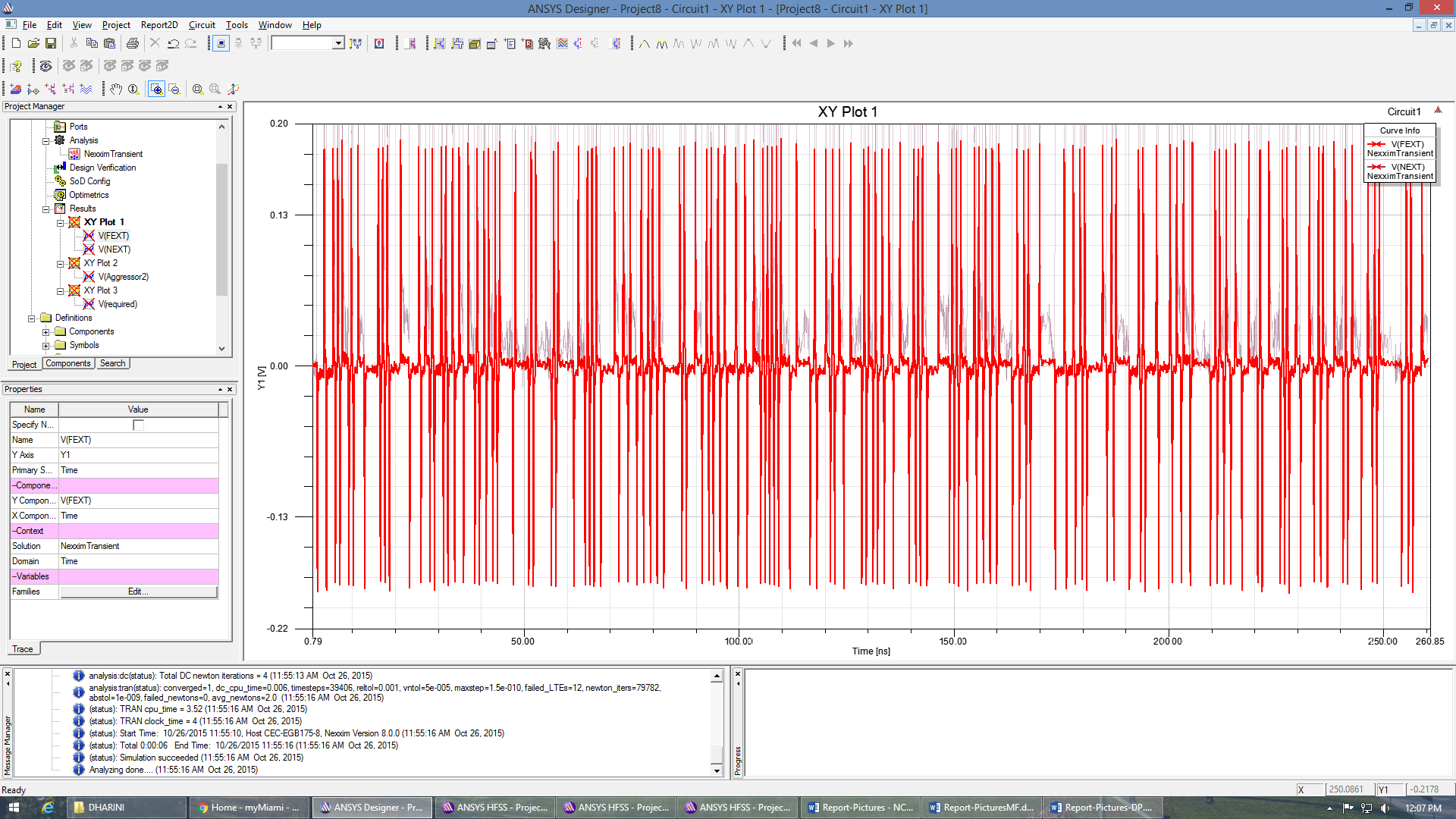


Figure 8: FEXT values of the first schematic.

The FEXT, or Far End Cross-talk, values are displayed in Figure 8. They hover around .18 V.

Our chosen strategy was somewhat successful. It helped to space the components along the board, however, keeping everything at the same dielectric set us up for a lot of excess cross-talk. We learned that we should take advantage of the opportunity to use two levels of dielectric. We also realized that the traces should not be running perfectly parallel to each other for the entire segment: this set us up for a larger value or inductance and capacitance. We used the HFSS plot of S21 and S43 to ensure the signal was successfully making it through the line and observed the plot of S13 and S14 to analyze the signal integrity of the line. The signal integrity was not very good.

Second Design:

With the second design, we wanted to improve our NEXT and FEXT values. We recognized that it might be detrimental to house both traces on the same level of dielectric. Therefore, we took advantage of having two dielectrics and performed calculations to separate the traces. The traces started on different dielectrics and switched dielectric levels twice throughout the design. Specifically, the first trace began in the middle level of the design, on top of the bottom dielectric, moved through a via to be at the top of the second dielectric, then through another via was moved back down to the first dielectric. The second trace did the opposite: it began on the top dielectric, moved through a via to the bottom dielectric, and was moved back to the top dielectric. Both traces switched their respective dielectrics at the exact same spot on the y-axis so they would have very little time that they were parallel on the same dielectric.

The intent of this method was to reduce the amount of time the traces were on the same dielectric. We wanted to switch them throughout the design because we knew that parallel lines are susceptible to cross-talk, the theory was that moving the lines a little bit would help reduce cross-talk.

We placed the power pads on the top layer. They were placed evenly throughout the middle section, we far as possible from the trace that was also o the top section at that point. This was to increase distance between the trace and power pads, reducing the capacitance between the two. We also placed a transmission line on the top layer in between the power pads and the trace. This transmission line was connected through a via to a second transmission line that was placed in the middle of the lower dielectric and extended the entire y-length of the motherboard. This second transmission was connected to ground by using a via. Therefore, there was a grounded shield between the power pads and the trace, and as well as around the trace on the bottom layer.

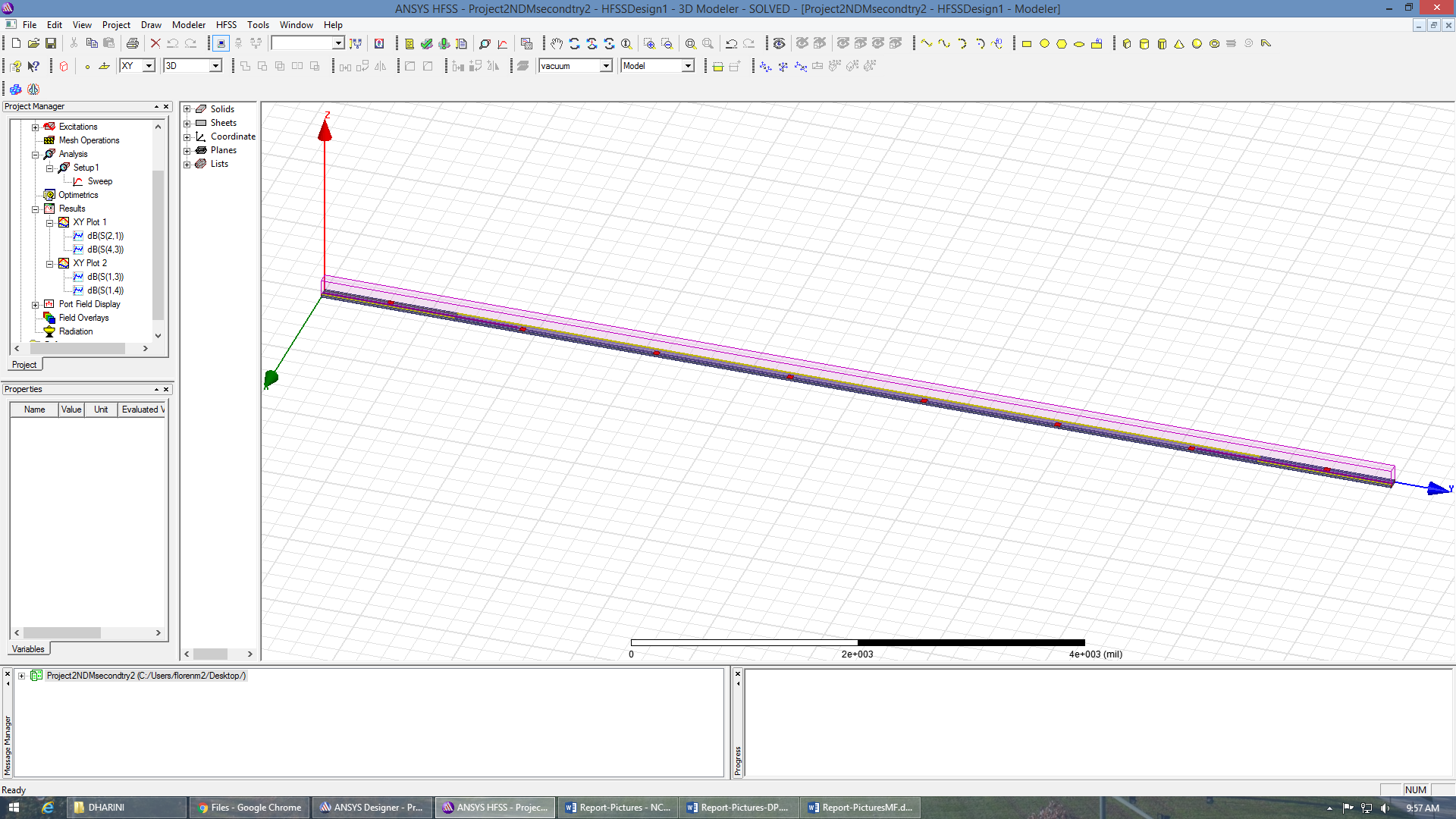


Figure 9: The HFSS schematic of the second design.

The complications in this design stemmed from the calculations of the vias. It was important to keep all of the traces perfectly lined up. We had to expand the width of the traces to 12mil because the diameter of each via was 10mil. We wanted to give 1mil of trace edge around the vias. Another complication with the vias was the height calculation. Each dielectric is of height 10mil so we made all of the vias have a height of 10mil. However, for the vias connecting trace on the middle layer to traces on the top layer, we realized that we had to account for the height of the bottom trace, which was 2mil. Therefore, instead of having vias of height 10mil between the middle and top layer, we had to make them 8mil because they all started 2mil above the bottom of the top dielectric. Once these calculations were accounted for, the schematic was ready for testing.

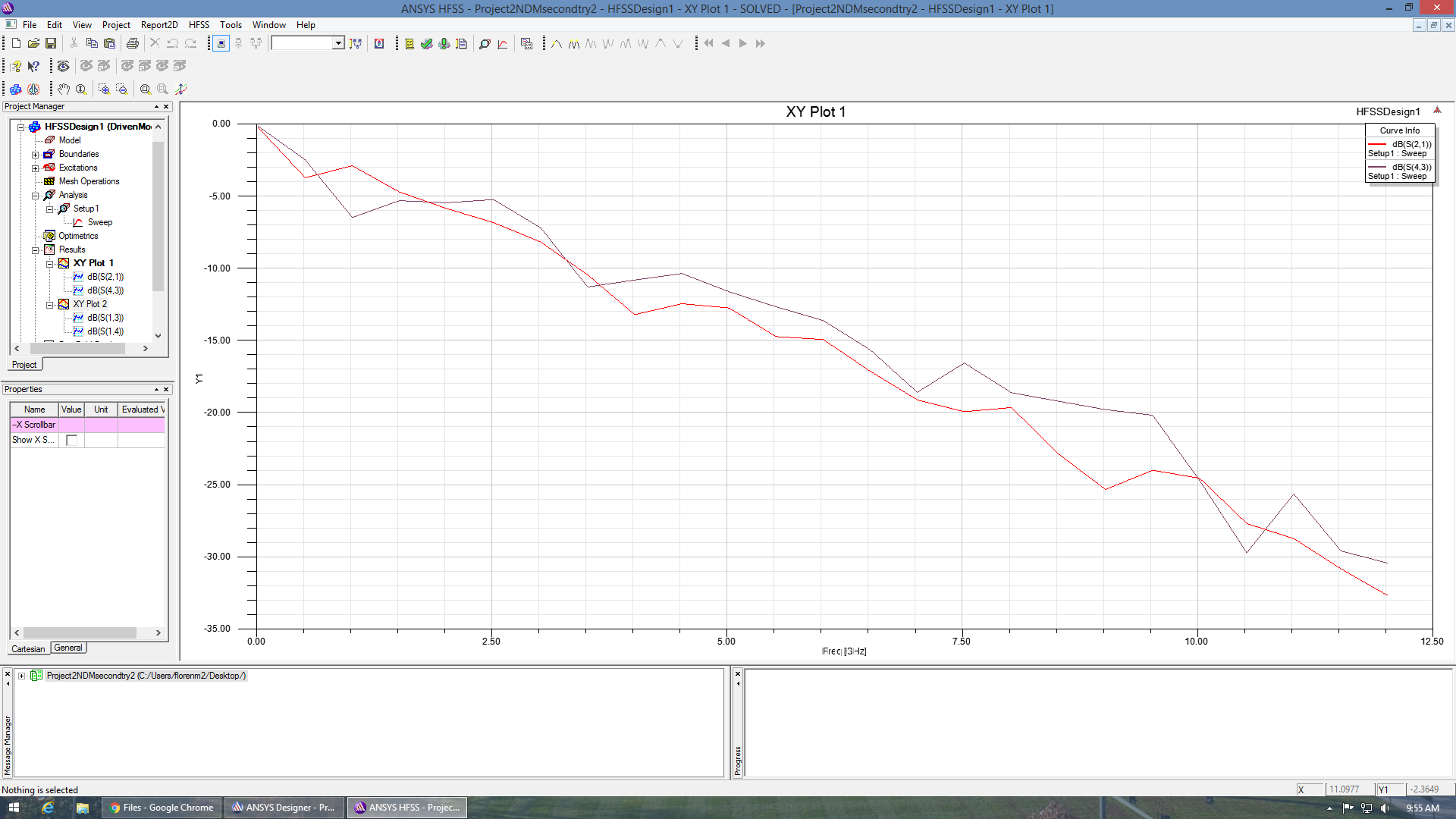


Figure 10: The graph of S21 and S43.

Once again in this schematic, Port 1 is the input end of a trace and Port 2 is the output of that same trace. Port 3 is the input of the second trace and Port 4 is the output of the second trace. We plotted S21 and S43, to observe the signal.

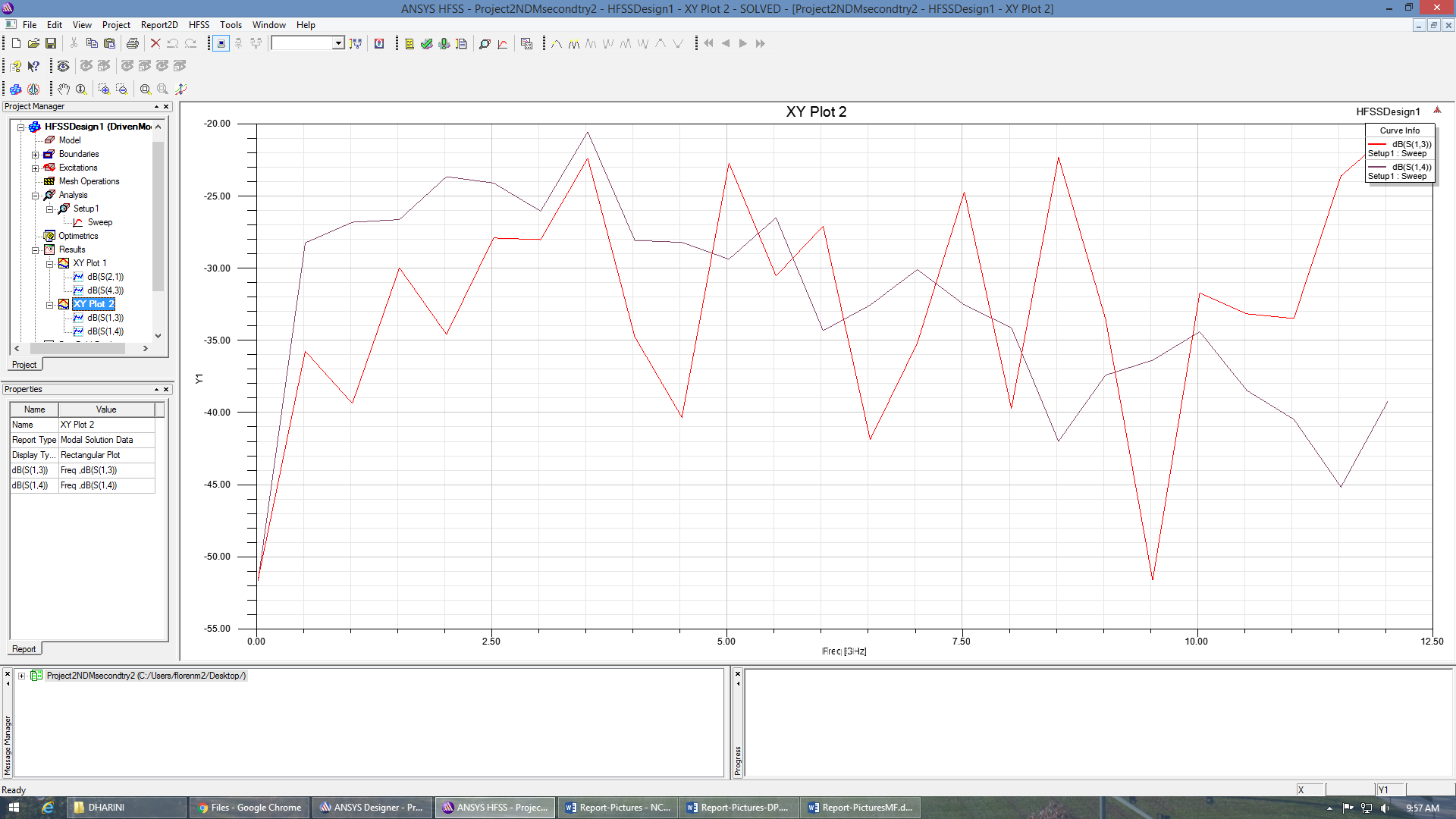


Figure 11: The graph of S13 and S14.

Figure 11 shows the level of signal integrity maintained.

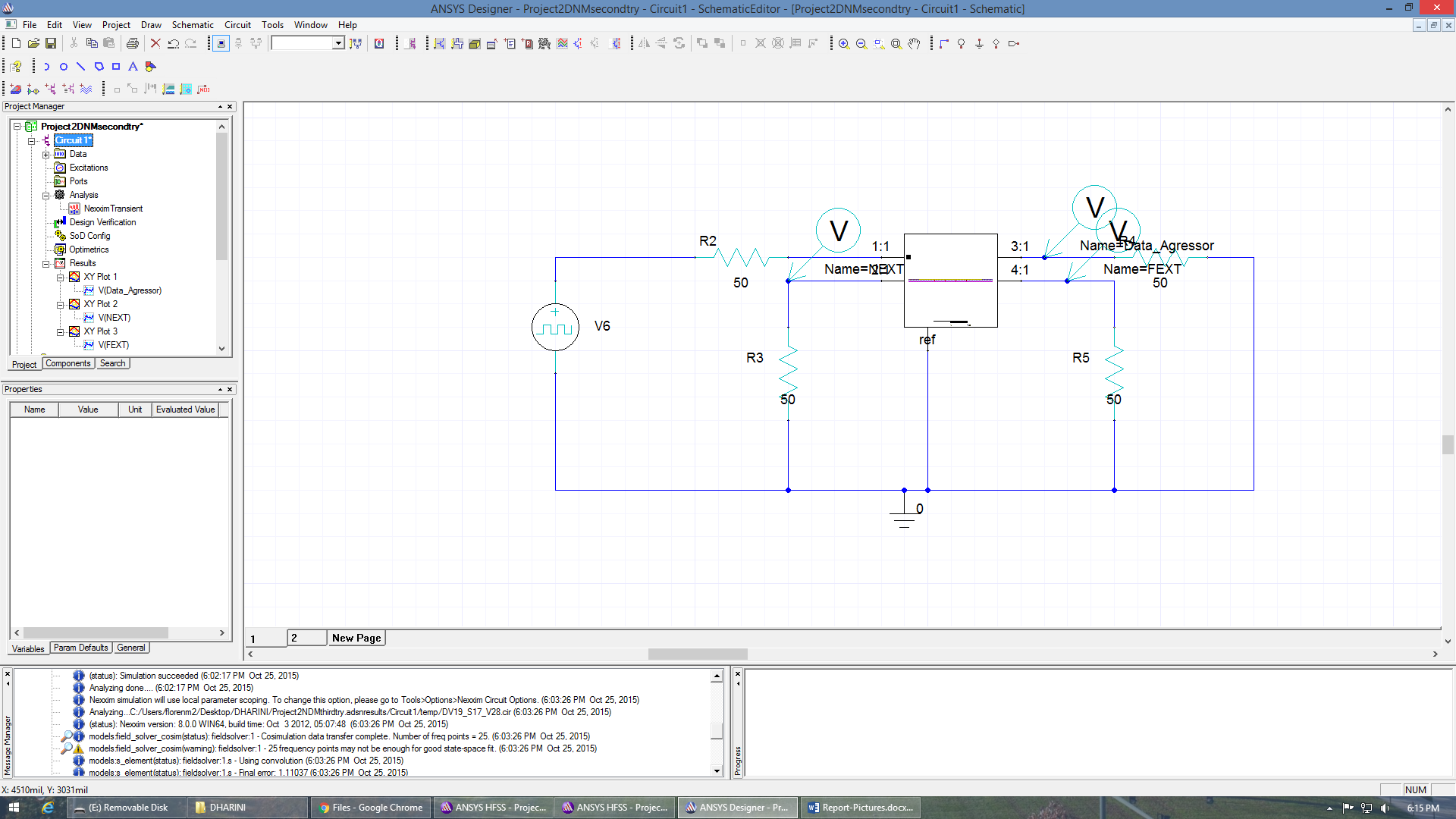


Figure 12: The Designer circuit of the second schematic.

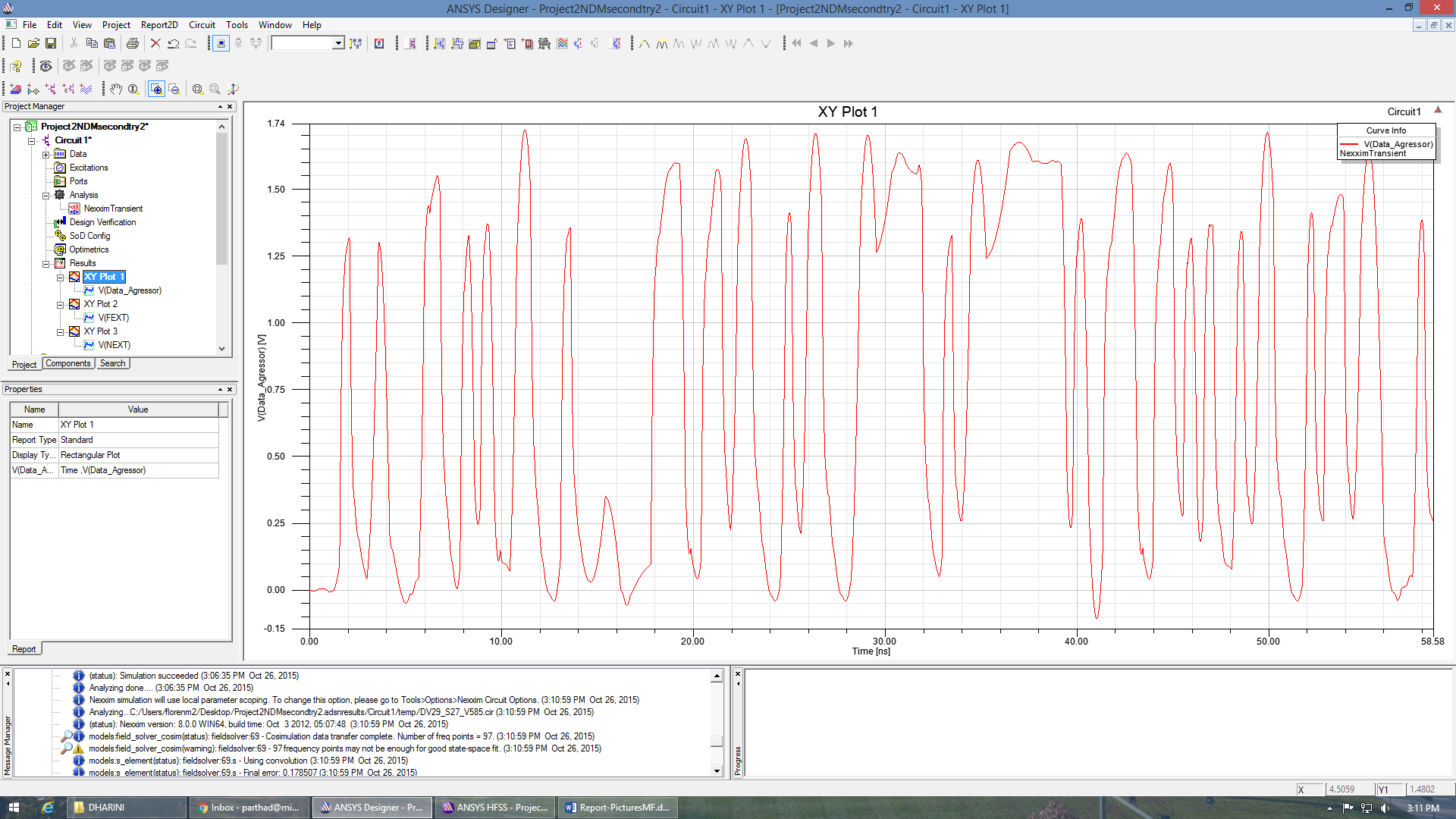


Figure 13: Input signal of the aggressor.

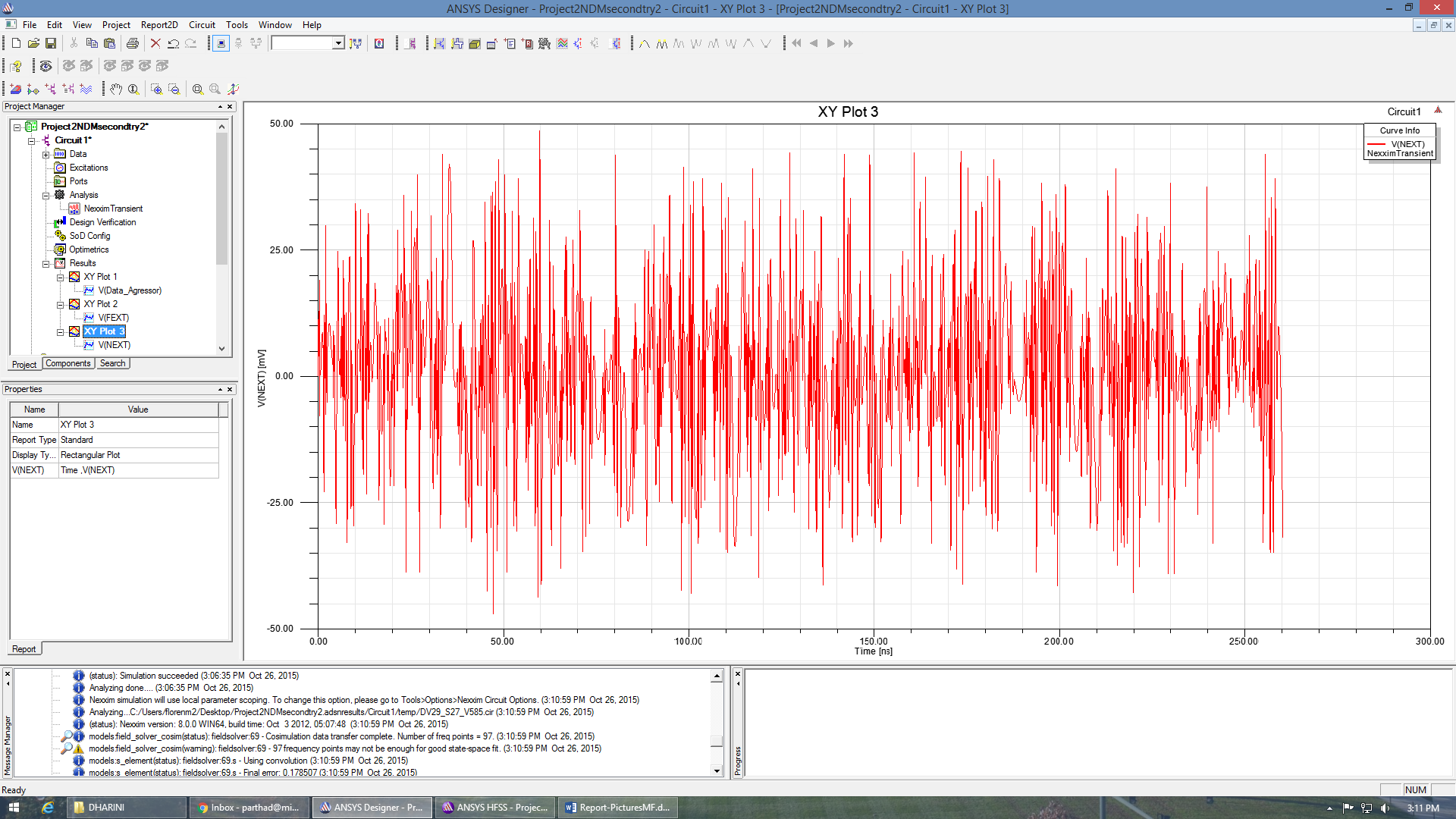


Figure 14: Output of the aggressor.

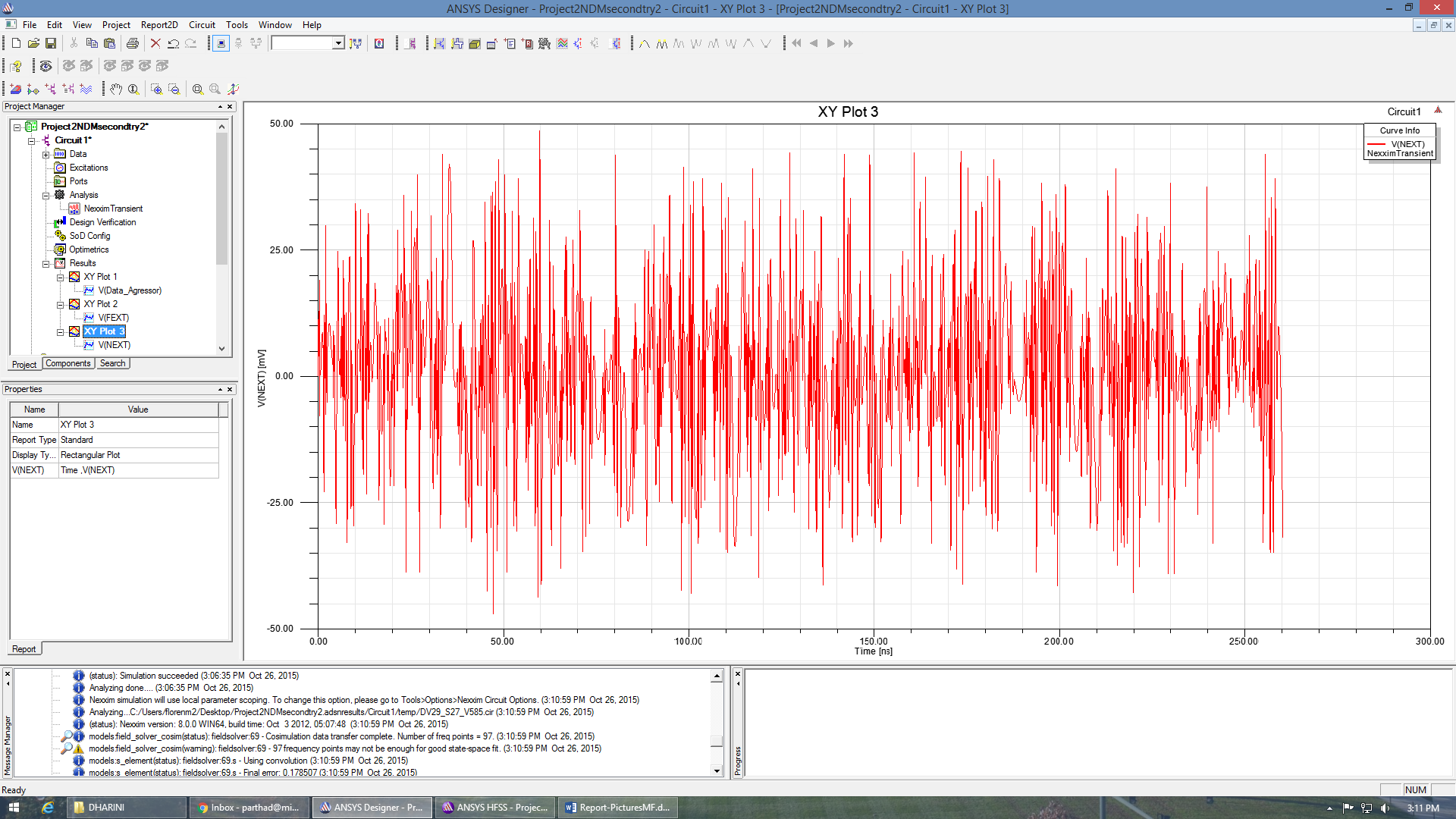


Figure 15: The plot of the NEXT values for the second schematic.

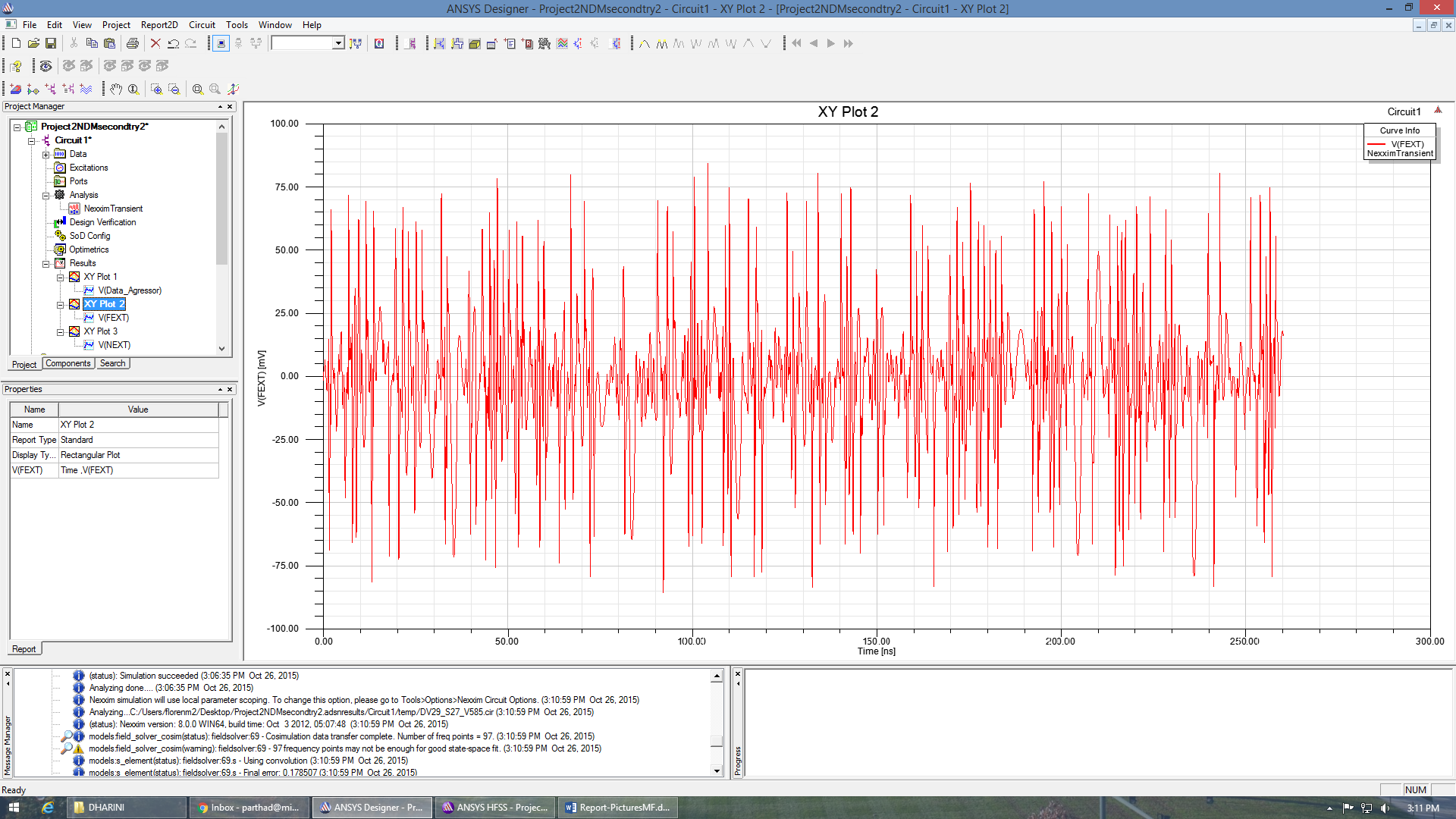


Figure 16: The plot of the FEXT values for the second schematic.

The value of the NEXT and FEXT values greatly decreased from the first test. Here, the values of NEXT are around 45 mV and the values of FEXT are around 75 mV.

We were successful in reducing cross-talk in the second simulation. Our idea to separate the traces on different dielectrics proved to lower cross-talk. Also, incorporating a shield connected to ground adequately helped reduce the communication between the two traces. However, we recognized that having a shield so close to the aggressor line may interrupt the original signal. We also noticed that having the signal go through vias may reduce signal integrity because or reflection loss where the turns occur. Our next goal was to reduce cross-talk even further while improving signal integrity.

Third Design

For our third design, we continued to take advantage of having two dielectrics. However, we did not switch the traces between the two: in order to minimize reflection loss due to bends in the line, we kept both traces perfectly straight. The aggressor was placed on the very top dielectric, in order to keep it far enough from ground that the original signal through the aggressor would not be hindered. Then the victim trace was placed on the middle level with a trace shield next to it that was connected to ground. The power pads were placed closely, each with only 1mil space between the other, on the top level and were blocked by a trace shield that was connected to ground. This grouping was on the side away from the aggressor in attempt to be as far as possible form it.



Figure 17: The HFSS design of the third try.

The calculations were fairly straight-forward and we had no major complications in designing this schematic.

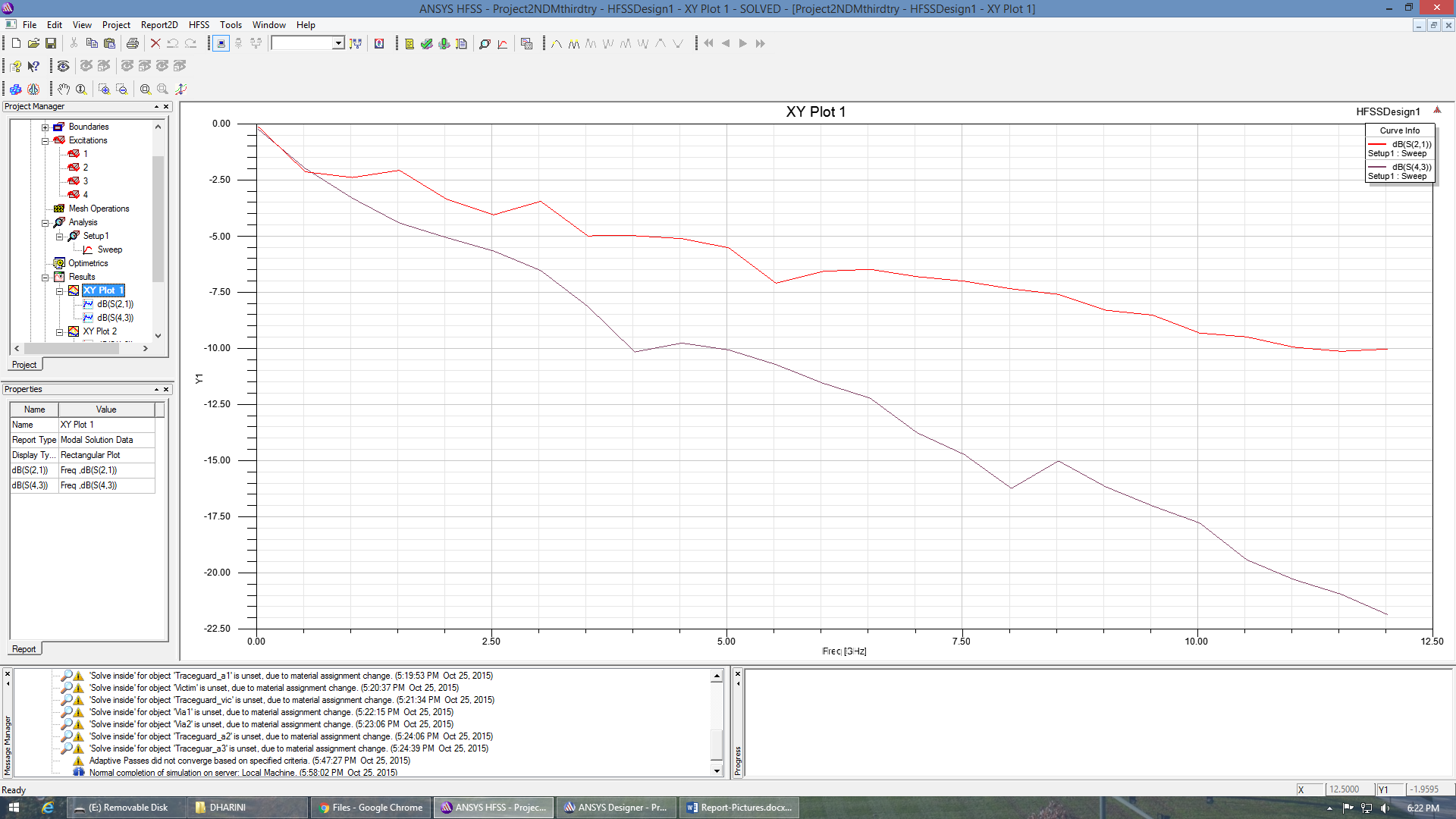


Figure 18: The plot of S21 and S43.

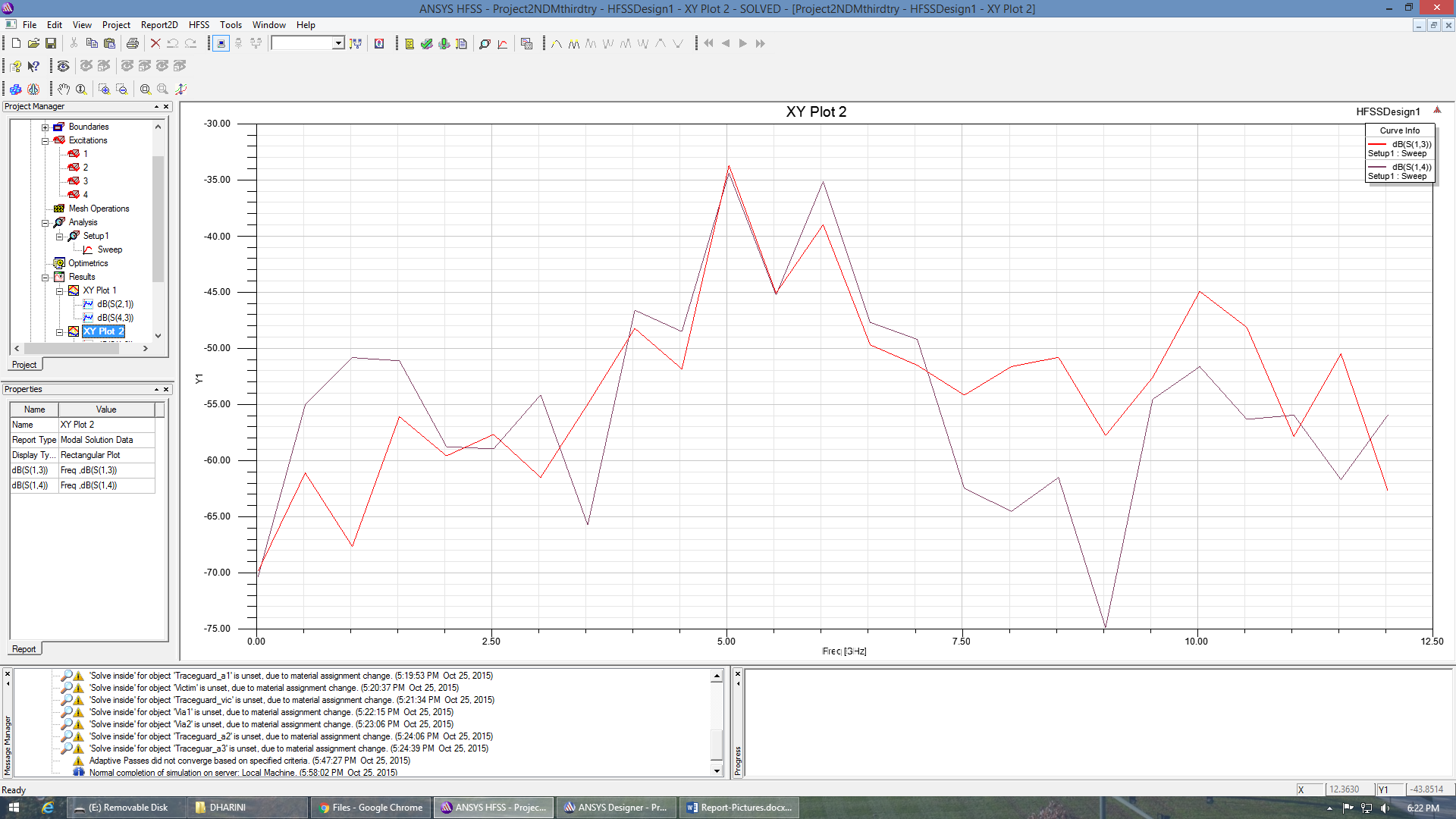


Figure 19: The plot of S13 and S14.

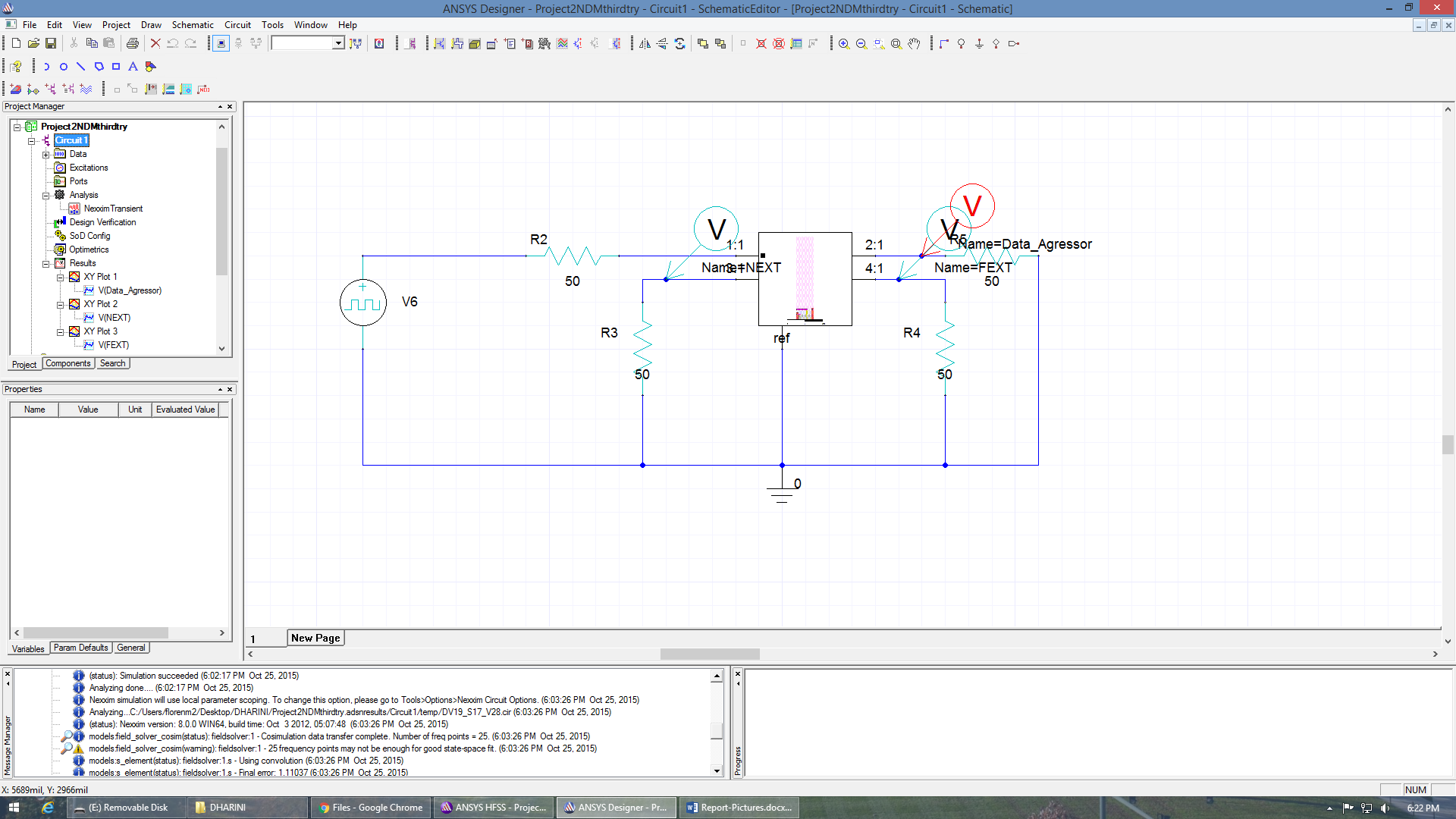


Figure 20: The designer schematic of the circuit for the third test.

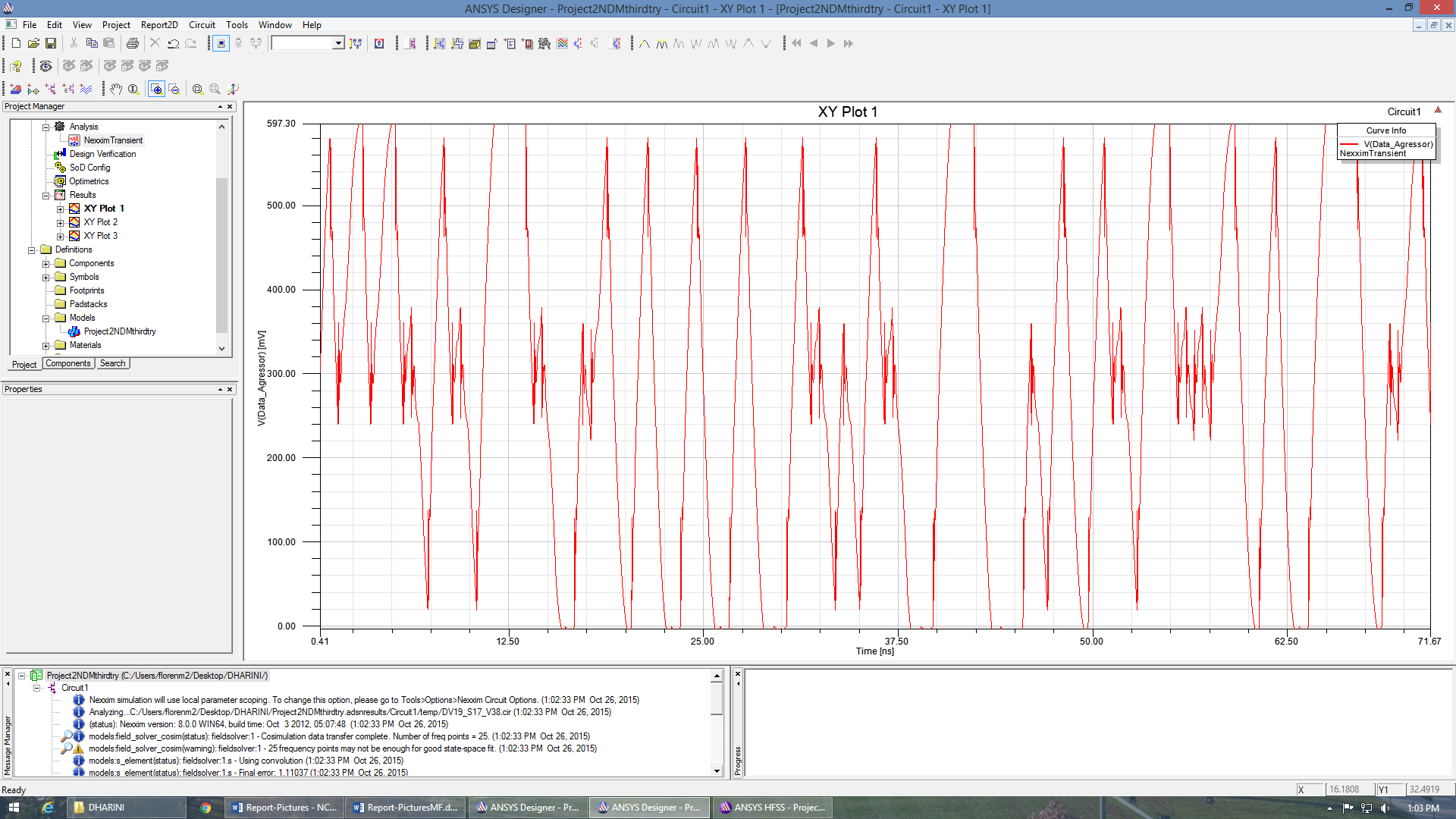


Figure 21: The output signal of the aggressor.

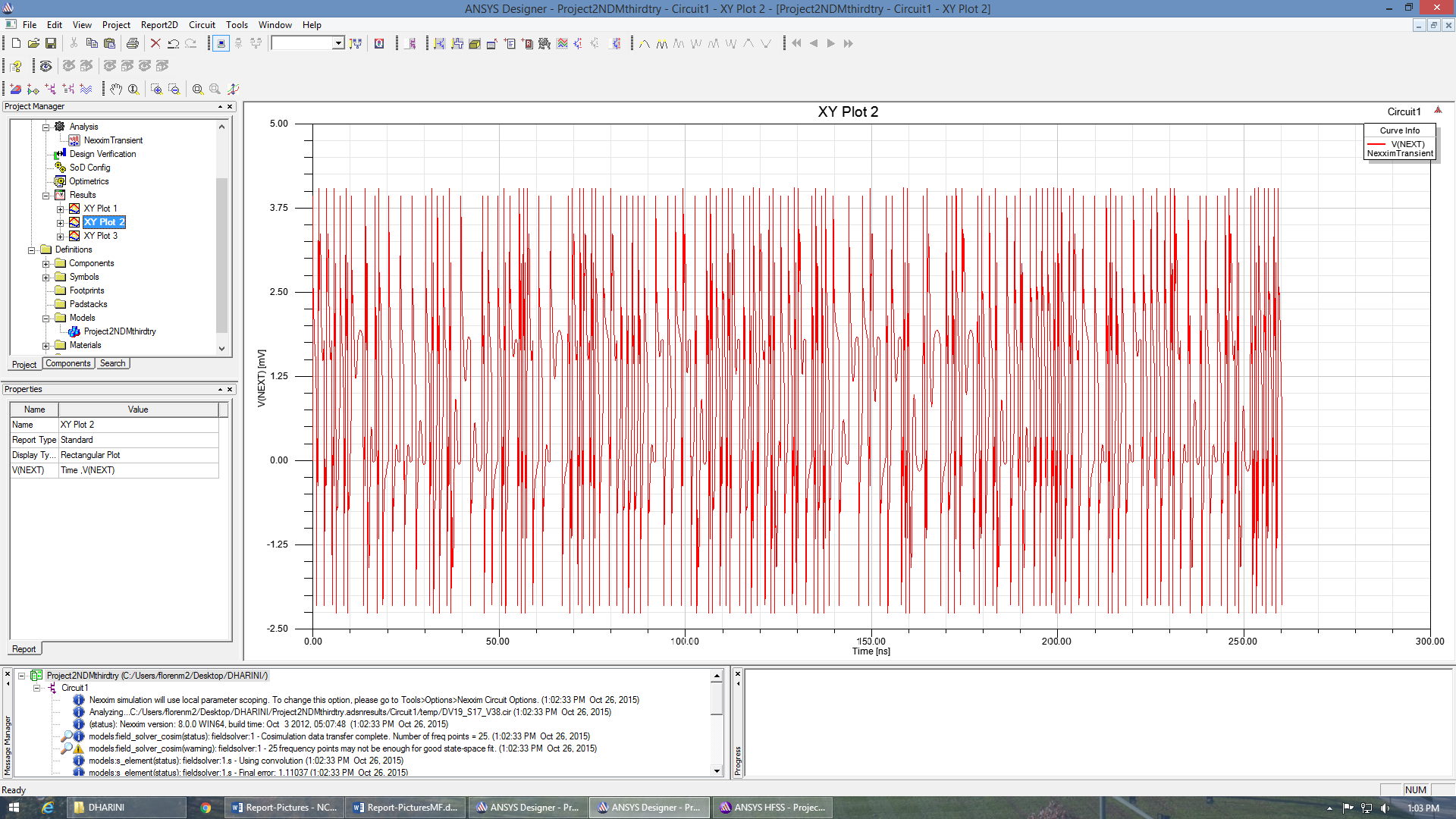


Figure 22: The NEXT values of the third schematic.

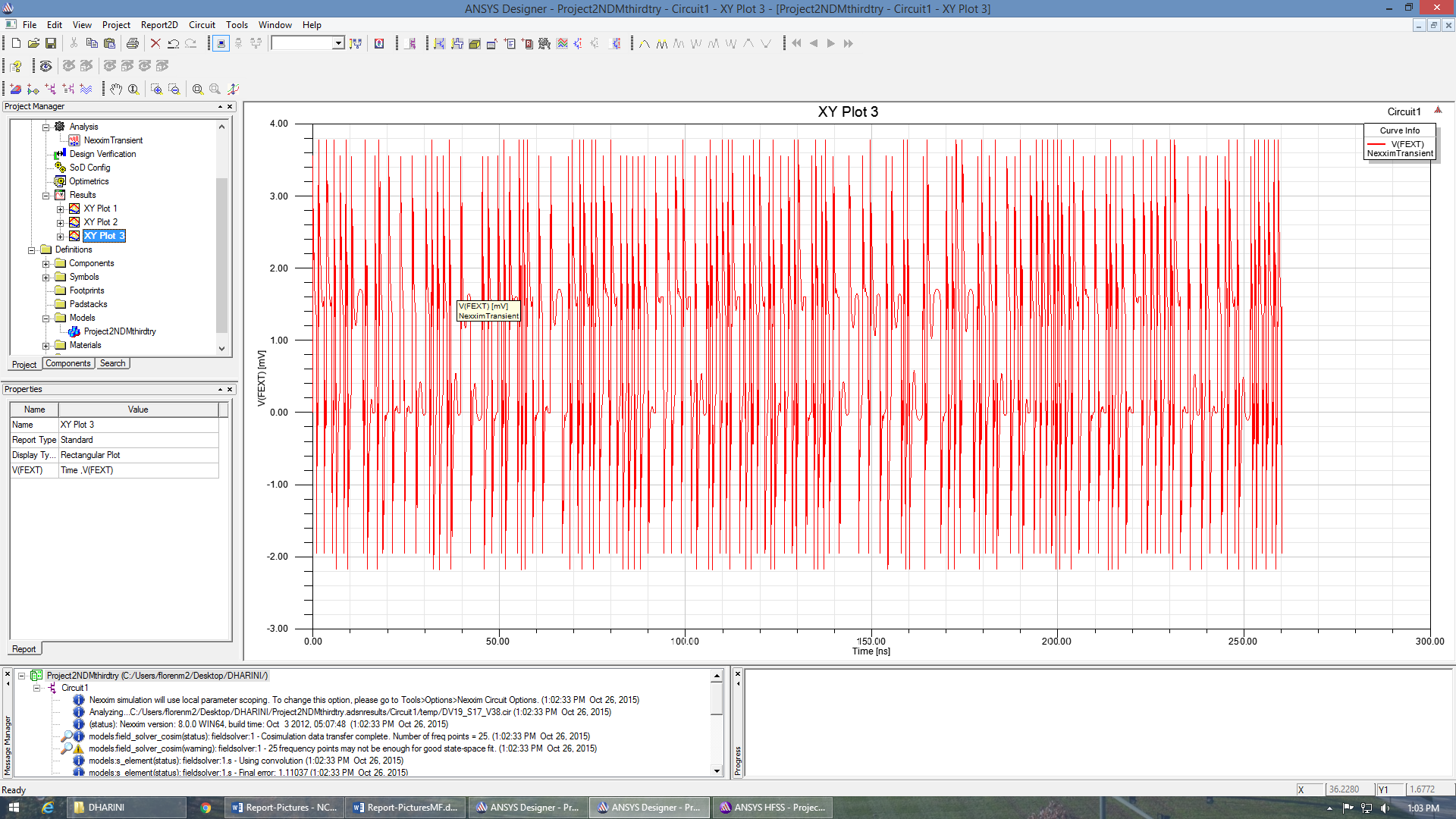


Figure 23: The FEXT values of the third schematic.

The cross-talk was greatly reduced in this test. The values of NEXT are about 4.0 mV while the values for FEXT are between 3.6 and 3.8 mV. This is a significant drop in cross-talk. The schematic is better with signal integrity as well, as in Figure 21 it can be seen that the output signal of the aggressor remains shape more-so than in the previous tests. This can be attributed to the fact that the aggressor and victim were completely separated and had no bends in either trace, so reflection loss due to bending of the line was not an issue. Also, placing the power pads all together and blocked by a guard greatly diminished their affect on the trace.

Summary

In this project, I learned how to reduce cross-talk between traces. Key ways to do this include separating the traces so they are as far apart as possible, providing a grounded trace in-between the aggressor and victim, and minimizing the amount that the traces are parallel to each other. Also, it helps to segregate and block the power pads so they cannot interfere with the traces. One more thing I learned is that often times, to reduce cross-talk means to also reduce the integrity of the signal.

Our schematic could have been improved in a number of ways. First and foremost, the bottom dielectric could have been made smaller and the aggressor could have been placed on the bottom while the victim would be on the top dielectric. This would increase distance between the traces and would ensure that the aggressor is close enough to ground that some of the signal could be muted. This would provide for poor signal integrity, however, as the aggressor would be close enough to ground that the signal could be partially lost.

In out third try, we also could have placed the grouping of power pads on the lower lever of dielectric. This way they would be even farther from the aggressor trace and close to ground.

Our group worked very well together. We all spent a lot of time in the lab and I feel each member did his or her fair share. The only improvement I would make is during our brainstorming process. We immediately crafted a design on HFSS and I think that if we took more time to think through the path of the signal, we could have saved time by creating the third design sooner.

Conclusion

The goal of the project was to reduce cross-talk between two traces and this was successfully achieved. I learned how to reduce cross-talk and that, when designing a circuit to minimize cross-talk, it is necessary to keep in mind that signal integrity may be lost. This project added a lot of value to my education because I have a deeper understanding of how components on a circuit impact each other. Instead of simply reading about it, I was able to observe what happens and think through the process of a circuit. This is a form of learning that is indispensible when mastering a concept. I recommend that future groups be required to make more than two schematics. I learned the most from creating two optimized schematics. It helped me see what worked and what didn’t I think that if students have to create several designs, they will learn even more about the topic.