S7CAS – APP1

# FORMATION À LA PRATIQUE PROCÉDURALE #2

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# PROBLÈME #1

***Déterminer les TENSIONS d'alimentation et le DÉCOUPLAGE nécessaires pour alimenter correctement (UG394.pdf)***

a. *le cœur du FPGA*

b. *les entrées / sorties et circuits associées (banques I/O) ;*

c. *les circuits auxiliaires.*

*Table 2-1:* **Spartan-6 FPGA Voltage Supplies**

| Supply Input | Description | Devices | Nominal Supply Voltage |
|---|---|---|---|
| $V_{CCINT}$ | Internal core supply voltage. Supplies all internal logic functions, such as CLBs, block RAM, and DSP blocks. Input to the power-on reset (POR) circuit. Powers input signals for most standards at 1.2V, 1.5V, and 1.8V. | All | 1.2V; 1.0V (-1L) in lower-power Spartan-6 LX devices |
| $V_{CCAUX}$ | Auxiliary supply voltage. Supplies clock management tiles (CMTs), some I/O resources, some dedicated configuration pins, and JTAG interface. Powers input signals for most standards at 2.5V and 3.3V. Input to the POR circuit. | All | 2.5V; 3.3V optional |
| $V_{CCO\_0}$ | Supplies the output buffers in I/O bank 0, the bank along the top edge of the FPGA. | All | Selectable: 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V |
| $V_{CCO\_1}$ | Supplies the output buffers in I/O bank 1, the bank along the right edge of the FPGA. During configuration in byte-wide peripheral interface (BPI) Parallel Flash Mode, connects to the same voltage as the Flash PROM. | All | Selectable: 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V |
| $V_{CCO\_2}$ | Supplies the output buffers in I/O bank 2, the bank along the bottom edge of the FPGA. Connects to the same voltage as the FPGA configuration source. Input to the POR circuit. | All | Selectable: 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V |
| $V_{CCO\_3}$ | Supplies the output buffers in I/O bank 3, the bank along the left edge of the FPGA. | All | Selectable: 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V |

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*Table 2-1:* **Spartan-6 FPGA Voltage Supplies *(Cont'd)***

| Supply Input | Description | Devices | Nominal Supply Voltage |
|---|---|---|---|
| $V_{CCO\_4}$ | Supplies the output buffers in I/O bank 4, the bank along the top of the left edge of the FPGA in 6-bank devices. | LX75/T, LX100/T, and the LX150/T in FG(G)676 and FG(G)900 | Selectable: 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V |
| $V_{CCO\_5}$ | Supplies the output buffers in I/O bank 5, the bank along the top of the right edge of the FPGA in 6-bank devices. | LX75/T, LX100/T, and the LX150/T in FG(G)676 and FG(G)900 | Selectable: 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V |
| $V_{REF}$ | Input threshold voltage pins when HSTL/SSTL standards are used in the bank, otherwise user I/Os. When used as a reference voltage within a bank, all $V_{REF}$ pins within that bank must be connected. | All | Varies |
| MGTAVCC | Power-supply pin for the transceiver mixed-signal circuitry. | LXT | 1.2V |
| MGTAVCCPLL0/1 | Power-supply pin for the transceiver PLL | LXT | 1.2V |
| MGTAVTTX/RX | Power-supply pin for the transceiver TX and RX circuitry. | LXT | 1.2V |
| MGTAVTTRCAL | Power-supply pin for the transceiver resistor calibration circuit. | LXT | 1.2V |
| $V_{BATT}$ | Decryptor key memory backup supply. When key is not used, tie this pin to $V_{CC}$ or GND, or it can be left floating. | LX75/T, LX100/T, LX150/T | 3.3V |
| $V_{FS}$ | Decryptor key EFUSE power supply pin for programming. When key is not being programmed, tie this pin to $V_{CC}$ or GND, or it can be left floating. | LX75/T, LX100/T, LX150/T | 3.3V |

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## $V_{CCAUX}$

$V_{CCAUX}$ powers the auxiliary logic, including configuration logic and some internal and I/O resources. The Spartan-6 FPGA's $V_{CCAUX}$ is either 2.5V or 3.3V. These two voltages provide greater flexibility and allow $V_{CCAUX}$ to be set to the same level as an existing $V_{CCO}$ rail, to minimize the number of power rails. Reducing $V_{CCAUX}$ to 2.5V can reduce the power consumption on the $V_{CCAUX}$ rail by 40%.

During configuration, if $V_{CCO\_2}$ is 1.8V, $V_{CCAUX}$ must be 2.5V. If $V_{CCO\_2}$ is 2.5V or 3.3V, $V_{CCAUX}$ can be either 2.5V or 3.3V. See UG380, *Spartan-6 FPGA Configuration User Guide*.

The -1L speed grade devices require $V_{CCAUX}$ = 2.5V when using the LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, RSDS_25, RSDS_33, PPDS_25, and PPDS_33 I/O standards on inputs. See DS162, *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics*.

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*Table 2-1:* **Required PCB Capacitor Quantities per Device(1)(3) *(Continued)***

| Package | Device (XC6S) | $V_{CCINT}$ in µF | | | $V_{CCAUX}$ in µF | | | $V_{CCO}$ Bank 0 in µF | | | $V_{CCO}$ Bank 1 in µF | | | $V_{CCO}$ Bank 2 in µF | | | $V_{CCO}$ Bank 3 in µF | | | $V_{CCO}$ Bank 4 in µF | | | $V_{CCO}$ Bank 5 in µF | | | Total (2) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 100 | 4.7 | 0.47 | 100 | 4.7 | 0.47 | 100 | 4.7 | 0.47 | 100 | 4.7 | 0.47 | 100 | 4.7 | 0.47 | 100 | 4.7 | 0.47 | 100 | 4.7 | 0.47 | 100 | 4.7 | 0.47 | |
| FG(G)484 | LX75 | 1 | 2 | 3 | 1 | 2 | 4 | 1 | 1 | 2 | 1 | 1 | 3 | 1 | 1 | 4 | 1 | 1 | 3 | | | | | | | 33 |
| FG(G)484 | LX75T | 1 | 2 | 3 | 1 | 2 | 4 | 1 | 1 | 2 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 3 | | | | | | | 32 |
| FG(G)484 | LX100 | 1 | 2 | 4 | 1 | 2 | 4 | 1 | 1 | 2 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 3 | | | | | | | 33 |
| FG(G)484 | LX100T | 1 | 2 | 4 | 1 | 2 | 4 | 1 | 1 | 2 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 3 | | | | | | | 33 |
| FG(G)484 | LX150 | 2 | 3 | 6 | 1 | 2 | 4 | 1 | 1 | 2 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 3 | | | | | | | 37 |
| FG(G)484 | LX150T | 2 | 3 | 6 | 1 | 2 | 4 | 1 | 1 | 2 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 3 | | | | | | | 37 |
| FG(G)676 | LX45 | 1 | 1 | 2 | 1 | 2 | 5 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 4 | | | | | | | 33 |
| FG(G)676 | LX75 | 1 | 2 | 3 | 2 | 3 | 6 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 2 | 1 | 1 | 2 | 45 |
| FG(G)676 | LX75T | 1 | 2 | 3 | 1 | 2 | 5 | 1 | 1 | 3 | 1 | 1 | 2 | 1 | 1 | 3 | 1 | 1 | 2 | 1 | 1 | 2 | 1 | 1 | 2 | 40 |
| FG(G)676 | LX100 | 1 | 2 | 4 | 2 | 3 | 6 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 2 | 1 | 1 | 2 | 46 |
| FG(G)676 | LX100T | 1 | 2 | 4 | 1 | 2 | 5 | 1 | 1 | 3 | 1 | 1 | 2 | 1 | 1 | 3 | 1 | 1 | 2 | 1 | 1 | 2 | 1 | 1 | 2 | 41 |
| FG(G)676 | LX150 | 2 | 3 | 6 | 2 | 3 | 6 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 2 | 1 | 1 | 2 | 50 |
| FG(G)676 | LX150T | 2 | 3 | 6 | 1 | 2 | 5 | 1 | 1 | 3 | 1 | 1 | 2 | 1 | 1 | 3 | 1 | 1 | 2 | 1 | 1 | 2 | 1 | 1 | 2 | 45 |
| FG(G)900 | LX100T | 1 | 2 | 4 | 2 | 3 | 6 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 3 | 1 | 1 | 4 | 1 | 1 | 2 | 1 | 1 | 2 | 47 |
| FG(G)900 | LX150 | 2 | 3 | 6 | 2 | 4 | 7 | 1 | 1 | 5 | 1 | 1 | 3 | 1 | 1 | 5 | 1 | 1 | 4 | 1 | 1 | 2 | 1 | 1 | 2 | 57 |
| FG(G)900 | LX150T | 2 | 3 | 6 | 2 | 3 | 7 | 1 | 1 | 4 | 1 | 1 | 3 | 1 | 1 | 4 | 1 | 1 | 4 | 1 | 1 | 2 | 1 | 1 | 2 | 54 |

**Notes:**

1. PCB Capacitor specifications are listed in Table 2-2.
2. Total includes all capacitors for all supplies, accounting for the number of I/O banks in the device.
3. These guidelines do not include some of the 100 µF capacitors of previous versions and the total capacitance requirement can include an increase in the quantity of 4.7 µF capacitors. Both versions of these guideline are valid, and either can be used. The quantities listed here should produce a lower BOM cost.

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# Capacitor Specifications

The electrical characteristics of the capacitors in Table 2-1 are described in this section. Characteristics of the PCB bulk and high-frequency capacitors are specified in Table 2-2, followed by guidelines on acceptable substitutions. The equivalent series resistance (ESR) ranges specified for these capacitors can be over-ridden. However, this requires analysis of the resulting power distribution system impedance to ensure that no resonant impedance spikes result.

*Table 2-2:* **PCB Capacitor Specifications**

| Ideal Value | Value Range(1) | Body Size(2) | Type | ESL Maximum | ESR Range(3) | Voltage Rating(4) | Suggested Part Number |
|---|---|---|---|---|---|---|---|
| 100 µF | C > 100 µF | 1210 | 2-Terminal Ceramic X7R or X5R | 5 nH | 10 mΩ < ESR < 60 mΩ | 6.3V | GRM32ER60J107ME20L |
| 4.7 µF | C > 4.7 µF | 0805 | 2-Terminal Ceramic X7R or X5R | 2 nH | 10 mΩ < ESR < 60 mΩ | 6.3V | |
| 0.47 µF | C > 0.47 µF | 0204 or 0402 | 2-Terminal Ceramic X7R or X5R | 1.5 nH | 10 mΩ < ESR < 60 mΩ | 6.3V | |

**PCB Capacitor Substitution Rules:**

1. Values can be larger than specified.
2. Body size can be smaller than specified.
3. ESR must be within the specified range.
4. Voltage rating can be higher than specified.

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# Ou placer les condensateur de découplage sur le PCB?

# PCB Capacitor Placement and Mounting Techniques

Placement and mounting restrictions presented in this section are unique to each capacitor type listed in the Capacitor Specifications section.

## PCB Bulk Capacitors

Bulk capacitors can be large and difficult to place very close to the FPGA. Fortunately, this is not a problem because the low-frequency energy covered by bulk capacitors is not as sensitive to capacitor location. Bulk capacitors can be placed almost anywhere on the PCB, but the best placement is as close as possible to the FPGA. Capacitor mounting should follow normal PCB layout practices, tending toward short and wide shapes connecting to power planes with multiple vias.

## 0805 Ceramic Capacitor

The 4.7 µF 0805 capacitor covers the middle frequency range. Placement has some impact on its performance. The capacitor should be placed as close as possible to the FPGA. Any placement within two inches of the device's outer edge is acceptable.

The capacitor mounting (solder lands, traces, and vias) should be optimized for low inductance. Vias should be butted directly against the pads. Vias can be located at the ends of the pads (see Figure 2-1B), but are more optimally located at the sides of the pads (see Figure 2-1C). Via placement at the sides of the pads decreases the mounting's overall parasitic inductance by increasing the mutual inductive coupling of one via to the other. Dual vias can be placed on both sides of the pads (see Figure 2-1D) for even lower parasitic inductance, but with diminishing returns.

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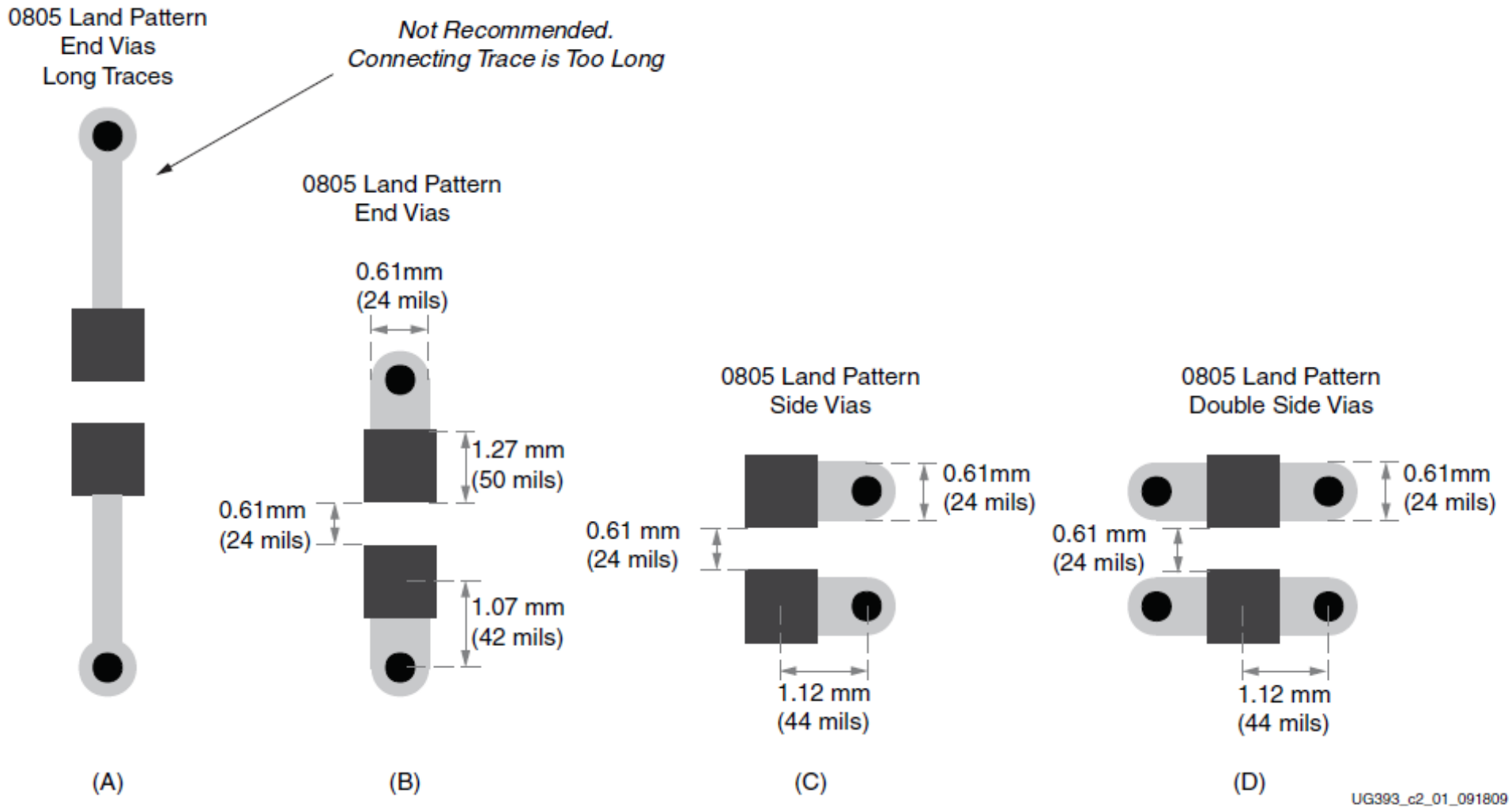


*Figure 2-1:* **Example 0805 Capacitor Land and Mounting Geometries**

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## 0402 Ceramic Capacitor

The 0.47 µF 0402 capacitor covers the high-middle frequency range. Placement and mounting are *critical* for these capacitors.

The capacitor should be mounted as close to the FPGA as possible (achieves the least parasitic inductance possible).

For PCBs with a total thickness of < 1.575 mm (62 mils), the best placement location is on the PCB *backside*, within the device footprint (in the empty cross with an absence of vias). $V_{CC}$ and GND vias corresponding to the supply of interest should be identified in the via array. Where space is available, 0402 mounting pads should be added and connected to these vias.

For PCBs with a total thickness > 1.575 mm (62 mils), the best placement location could be on the PCB top surface. The depth of the $V_{CC}$ plane of interest in the PCB stackup is the key factor: if the $V_{CC}$ plane is in the PCB stackup's top half, capacitor placement on the top PCB surface is optimal; if the $V_{CC}$ plane is in the PCB stackup's bottom half, capacitor placement on the bottom PCB surface is optimal.

Any 0402 capacitors placed outside the device footprint (whether on the top or bottom surface) should be within 0.5 inch of the device's outer edge.

The capacitor mounting (solder lands, traces, and vias) must be optimized for low inductance. Vias should be butted against the pads with no trace length in-between. These vias should be at the sides of the pads if at all possible (see Figure 2-2C). Via placement at the sides of the pads decreases the mounting's parasitic inductance by increasing the mutual inductive coupling of one via to the other. Dual vias can be placed on both sides of the pads (see Figure 2-2D) for even lower parasitic inductance, but with diminishing returns.

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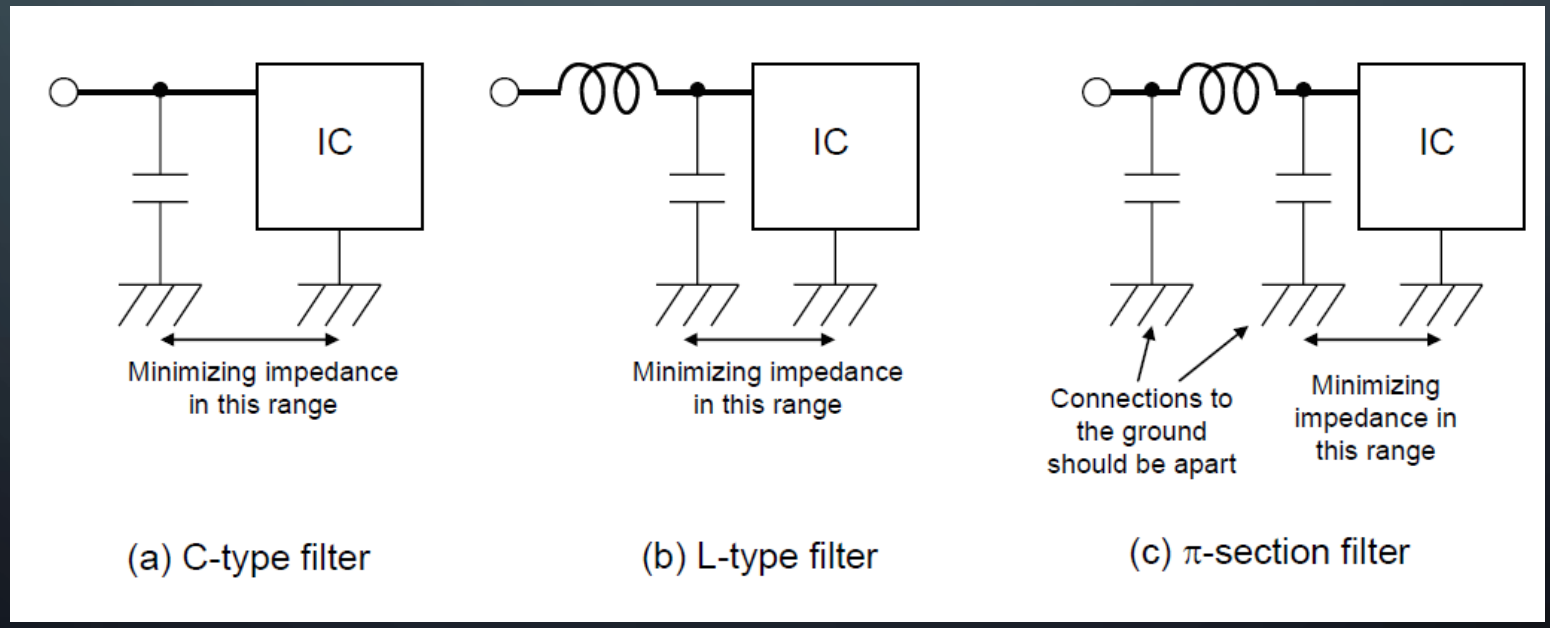
# PROBLÈME #5

***Soit les filtres suivants tirés composés de capacités et d'une ferrite.***

a) *Expliquez le rôle de ces filtres dans un circuit de découplage d'alimentation.*



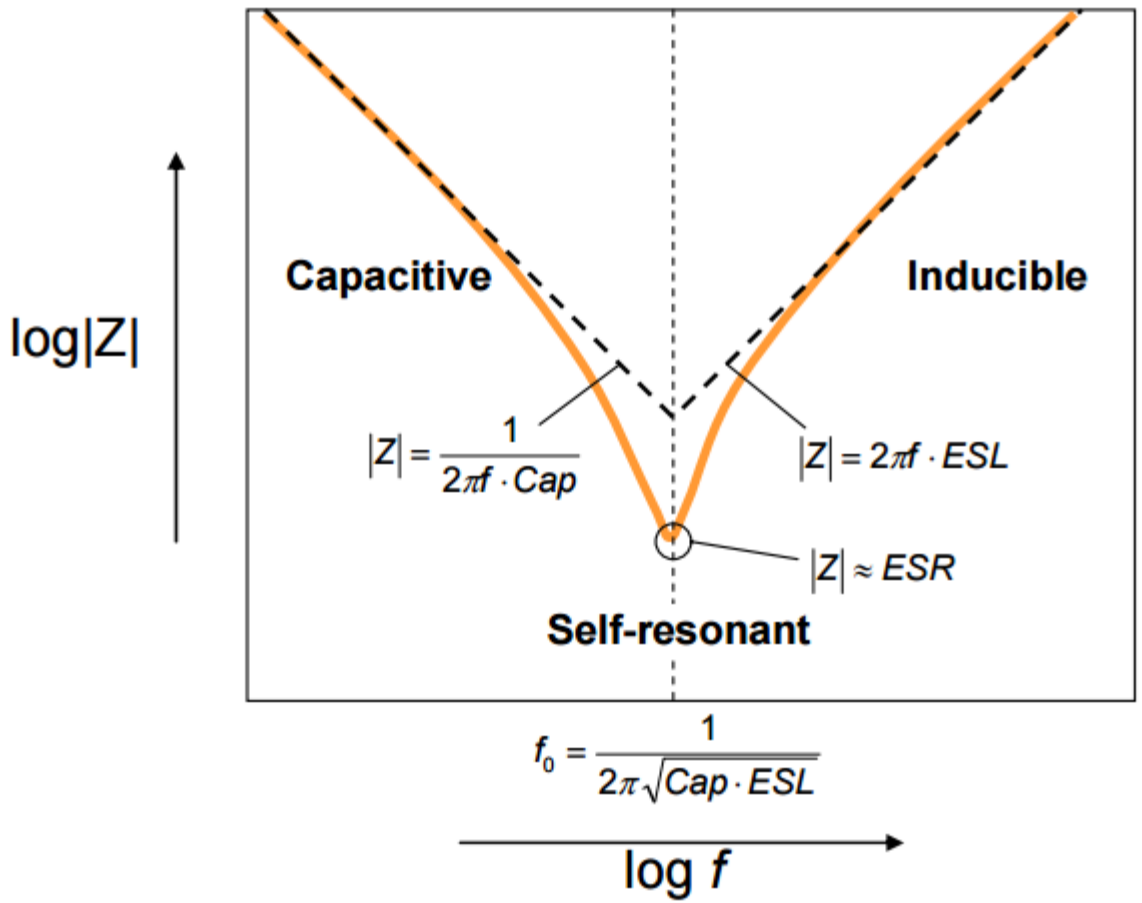
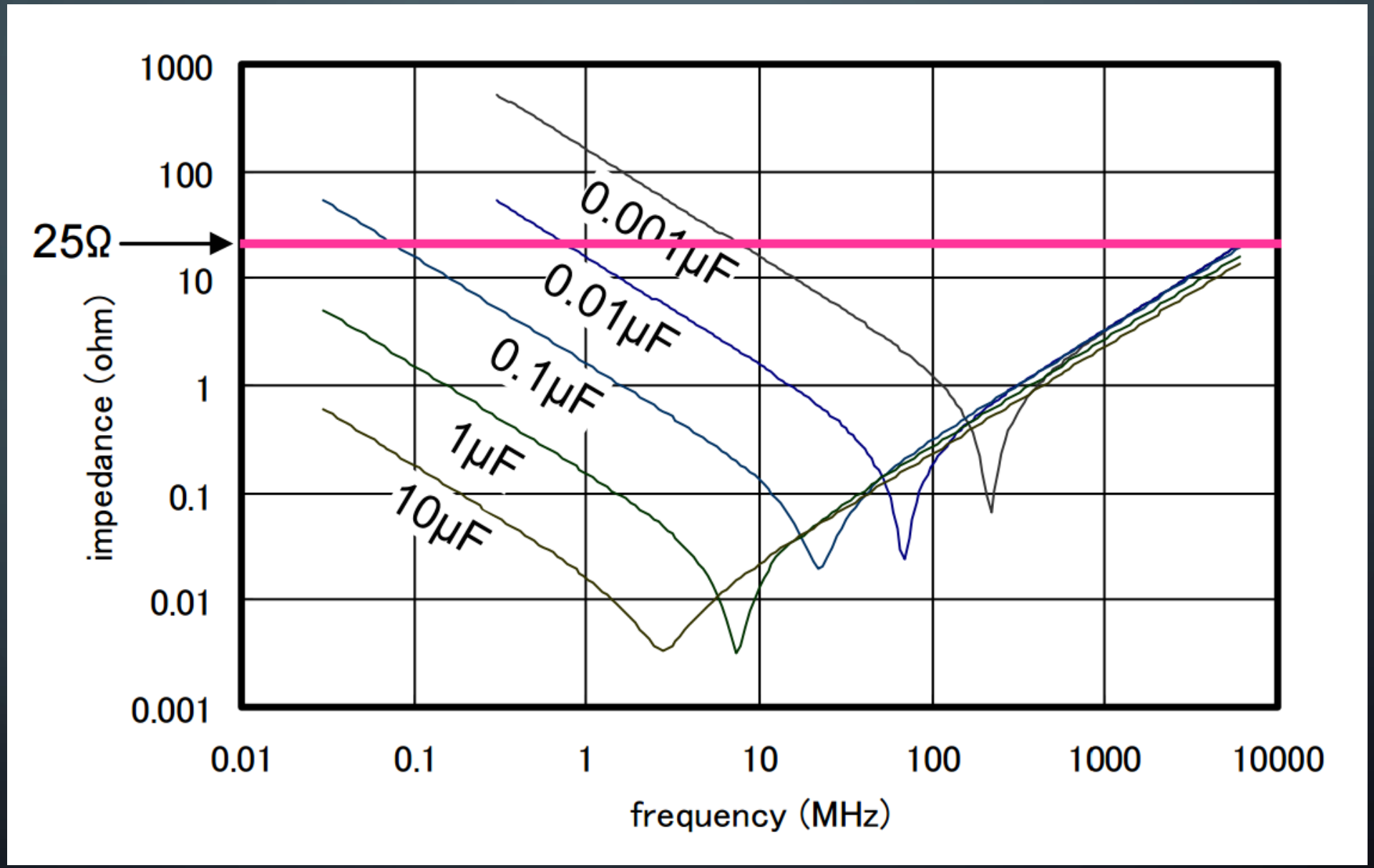
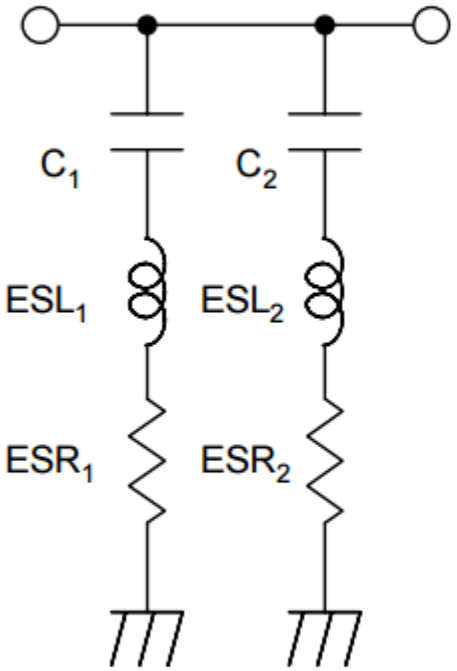



Figure 3-2 Frequency characteristics of the capacitor

C39e_DecouplageMurata : p. 12




C39e_DecouplageMurata : p. 13



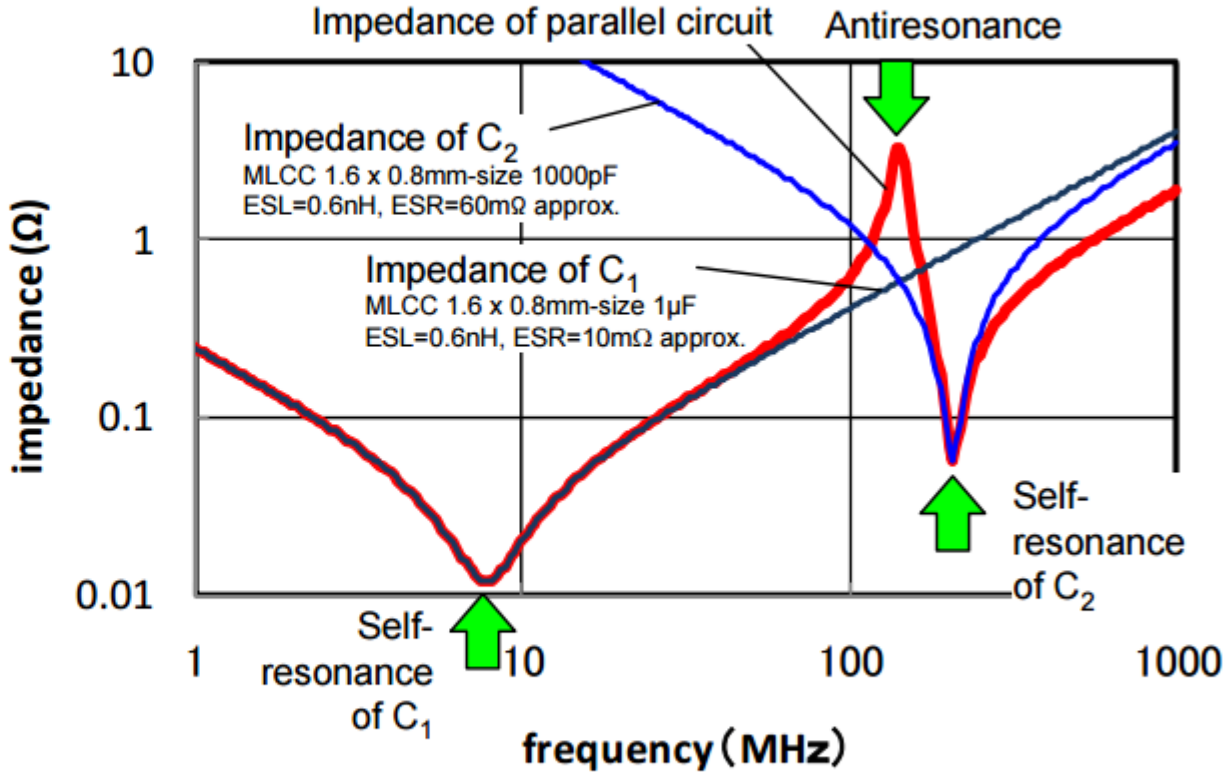




Figure 3-12 Parallel resonance of the capacitor (calculated values)

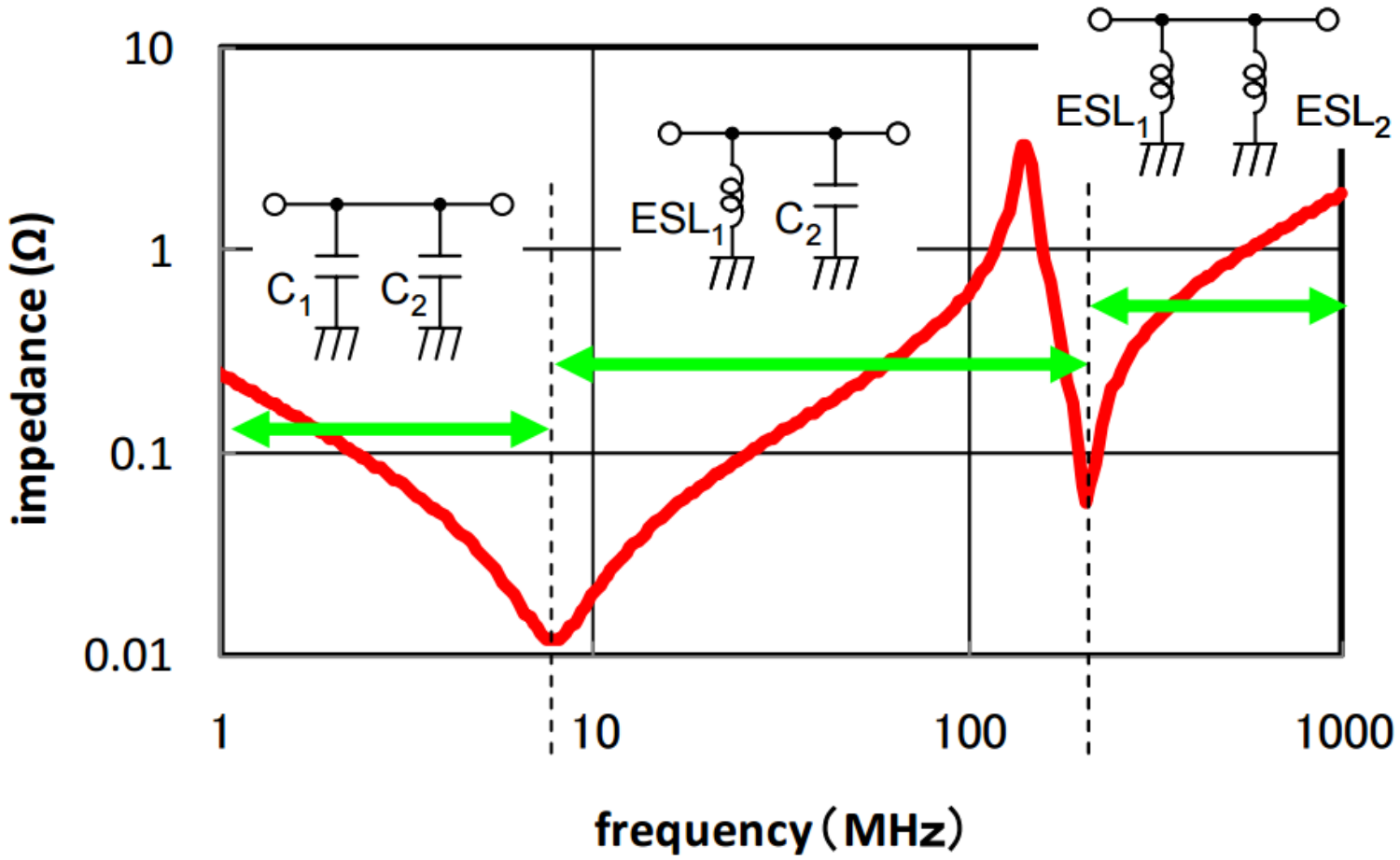



Figure 3-13 Mechanism of the capacitor's parallel resonance

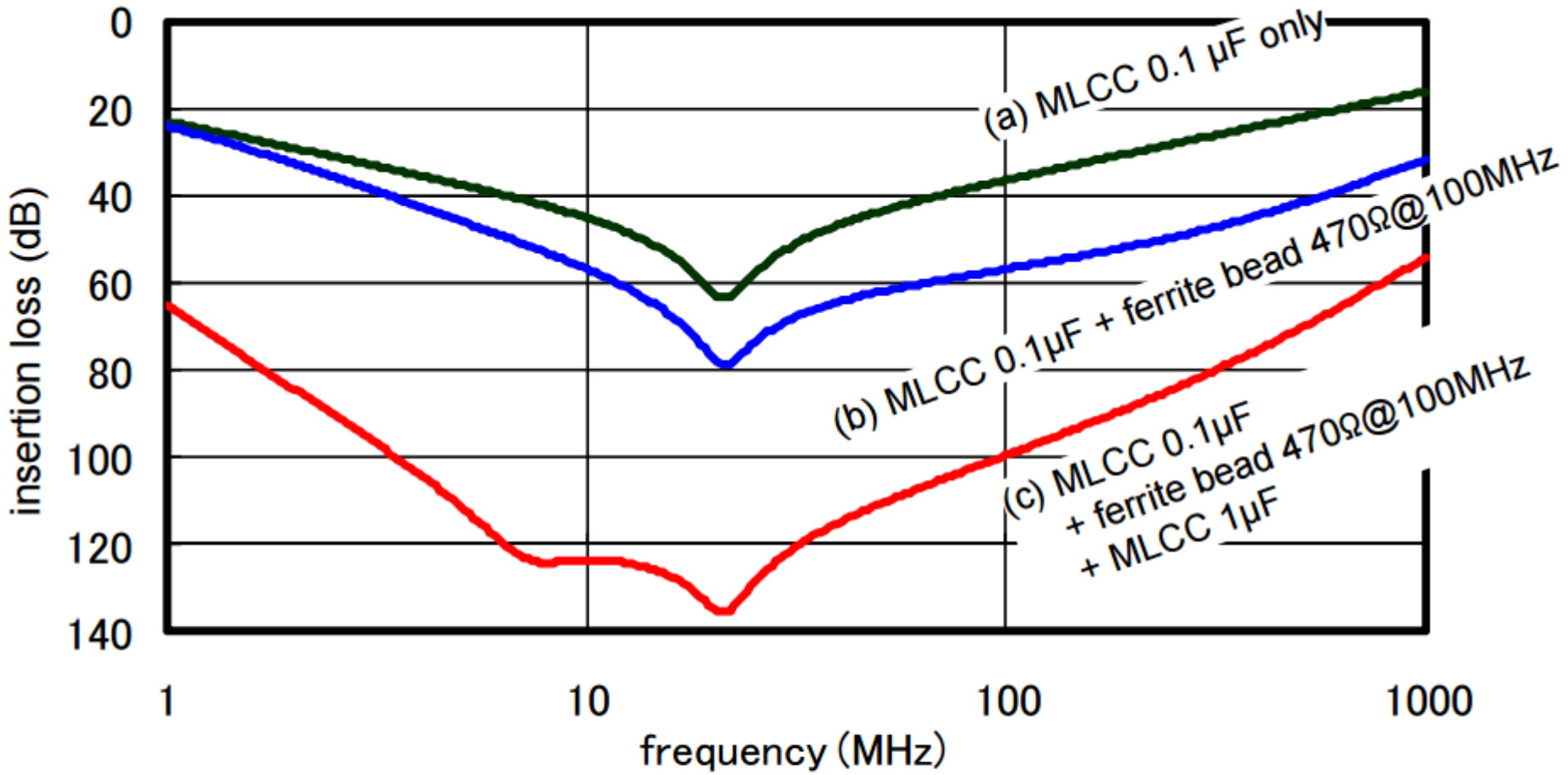
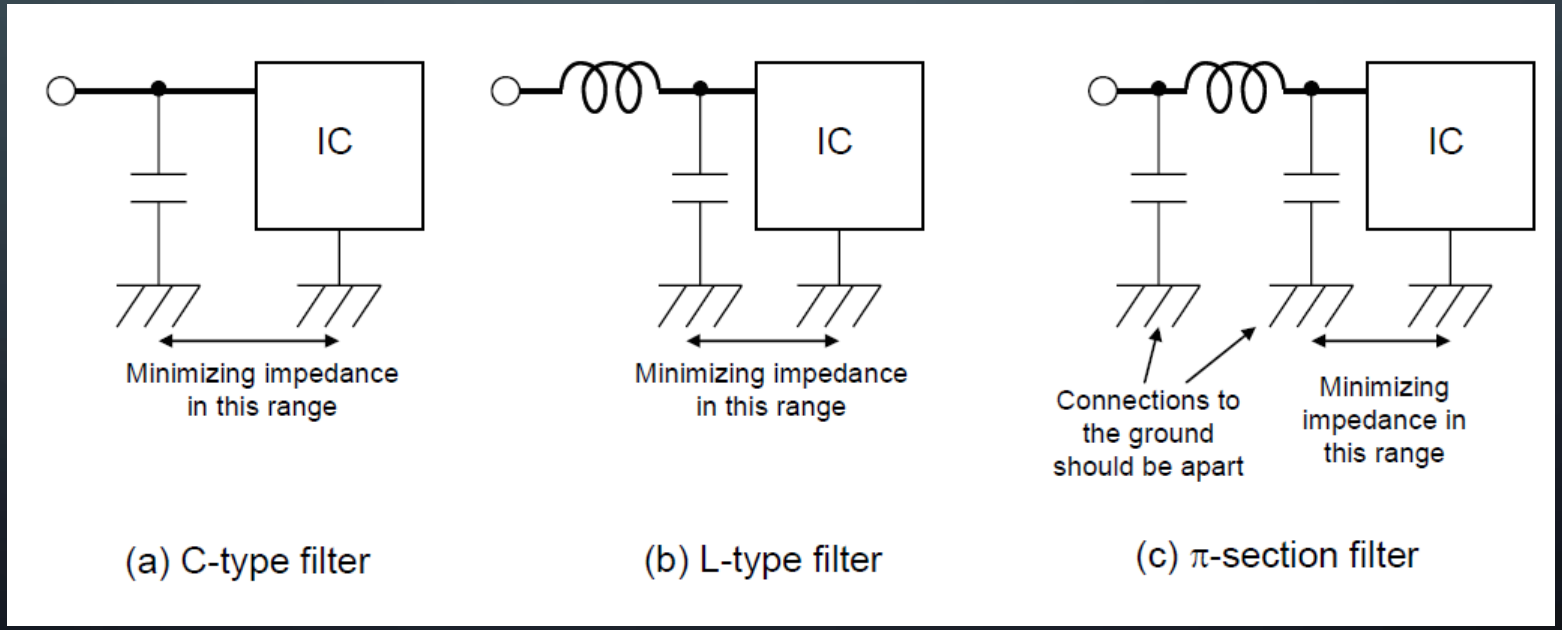


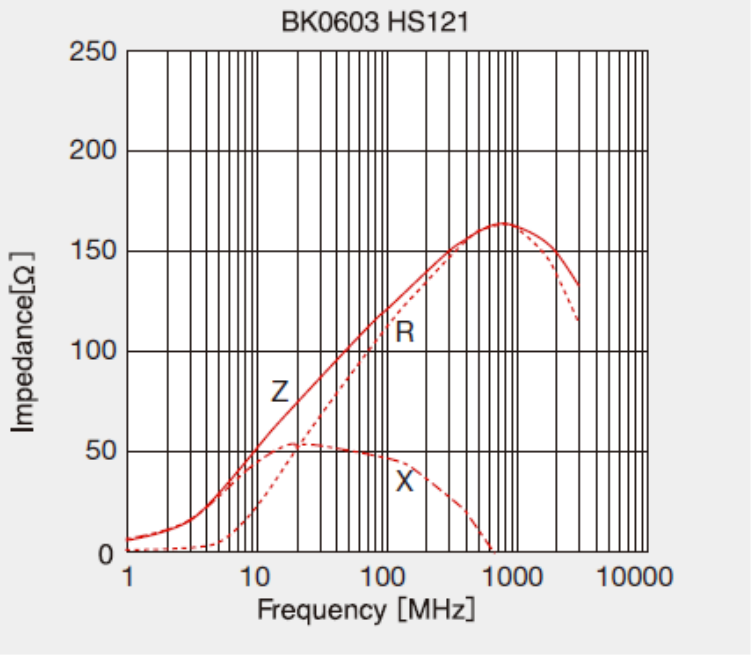

Figure 2-10 An example of insertion loss fluctuation when an inductor is combined (calculated values)

# PROBLÈME #5

***Soit les filtres suivants composés de capacités et d'une ferrite.***

b) Quel est l'effet des ferrites sur l'impédance de l'alimentation ? Est-ce désirable ?




BK0603 HS121
Impedance[Ω]
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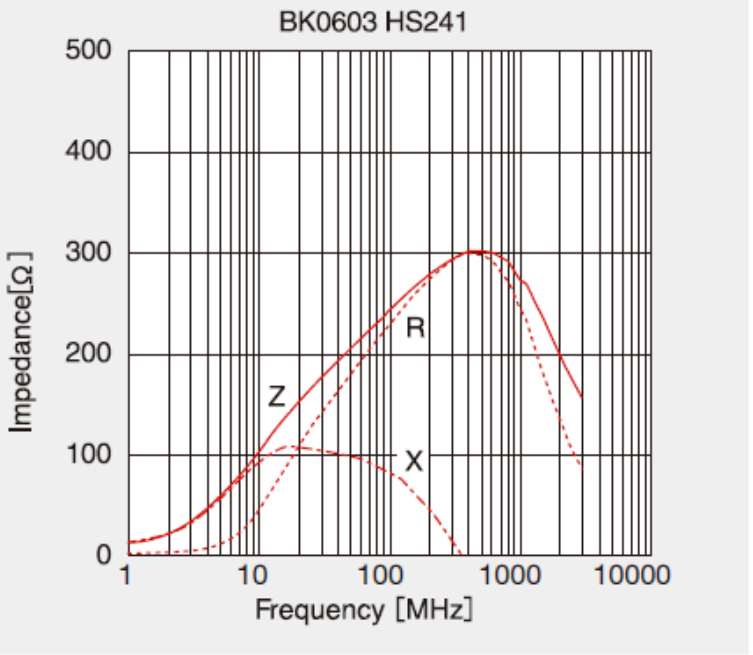
200
150
100
50
0
Z
R
X
1
10
100
1000
10000
Frequency [MHz]


BK0603 HS241
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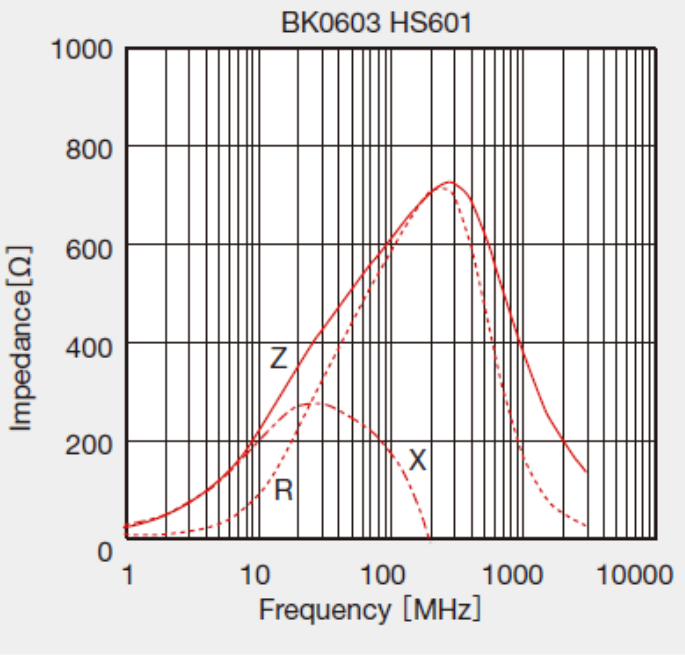
200
100
0
Z
R
X
1
10
100
1000
10000
Frequency [MHz]


BK0603 HS601
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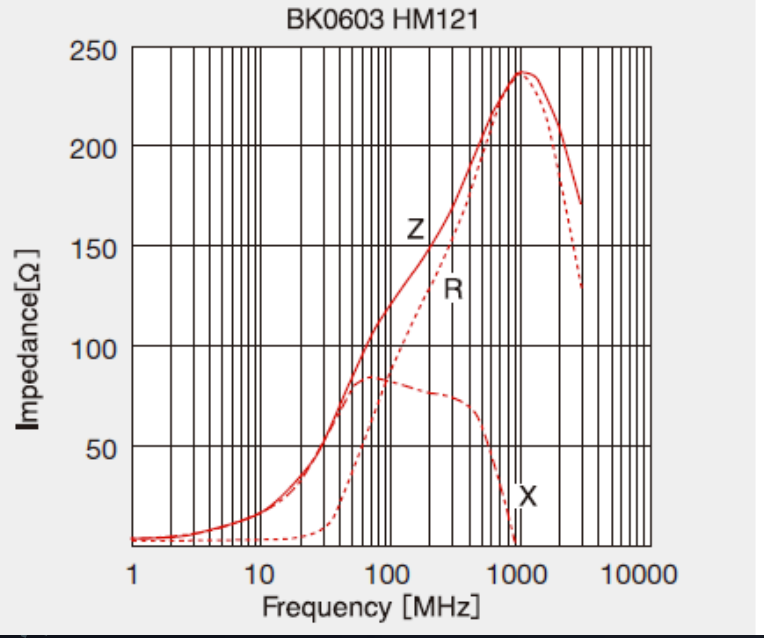
R
X
1
10
100
1000
10000
Frequency [MHz]


BK0603 HM121
Impedance[Ω]
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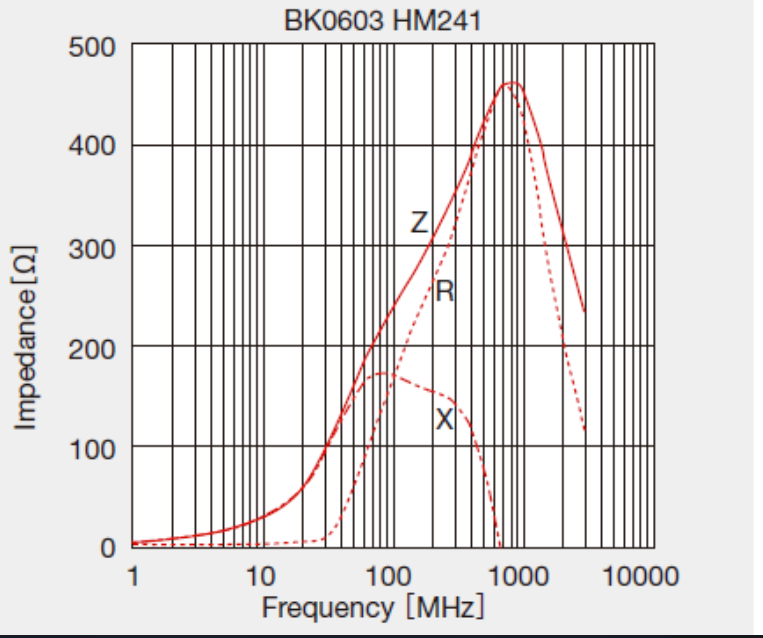
200
150
100
50
Z
R
X
1
10
100
1000
10000
Frequency [MHz]


BK0603 HM241
Impedance[Ω]
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400
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200
100
0
Z
R
X
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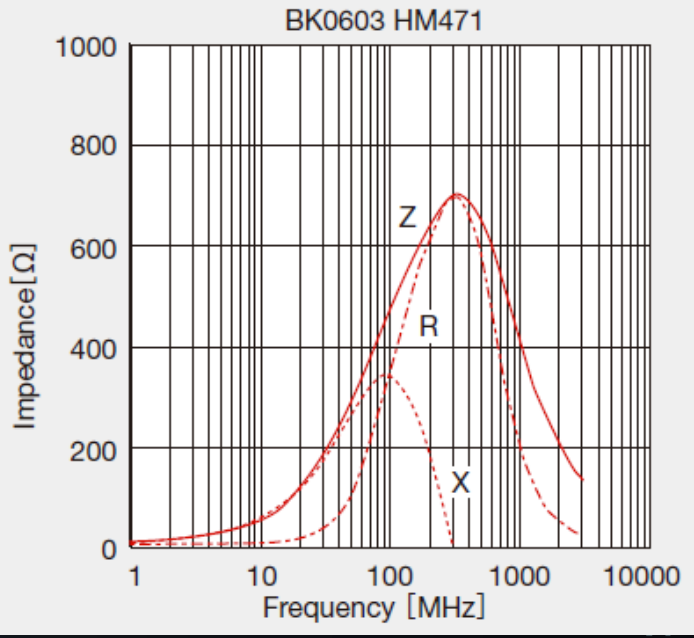
10000
Frequency [MHz]


BK0603 HM471
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400
200
0
Z
R
X
1
10
100
1000
10000
Frequency [MHz]

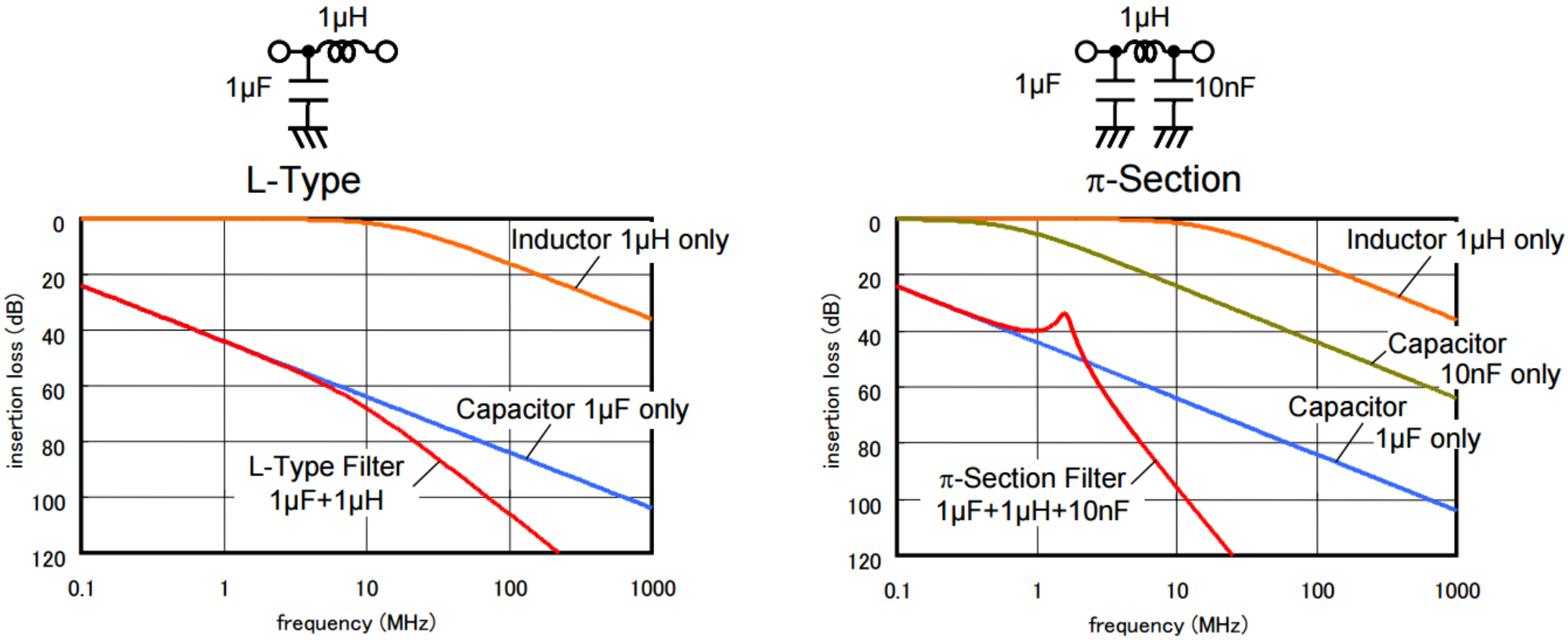
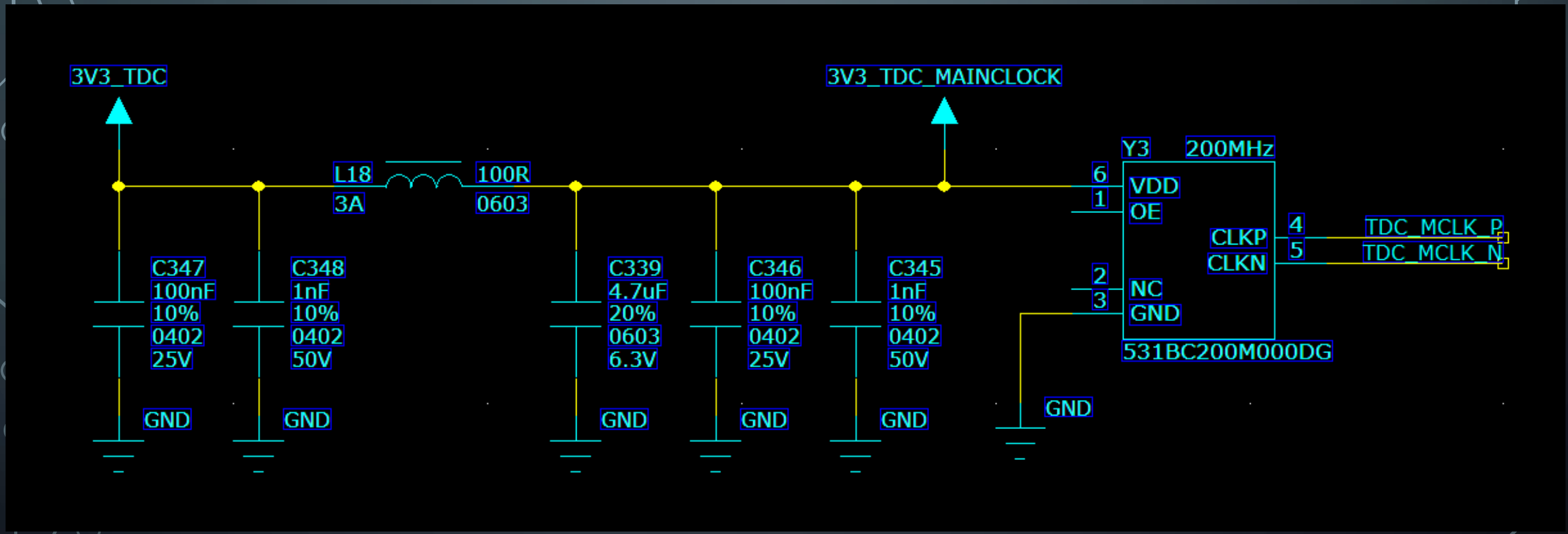



Figure 5-12 Examples of insertion loss characteristics of L-type and π-section filters (calculated values)

# PROBLÈME #5

***Soit les filtres suivants composés de capacités et d'une ferrite.***

c) Quand doit-on mettre une ferrite ?


3V3_TDC
3V3_TDC_MAINCLOCK
L18
3A
100R
0603
C347
100nF
10%
0402
25V
C348
1nF
10%
0402
50V
C339
4.7uF
20%
0603
6.3V
C346
100nF
10%
0402
25V
C345
1nF
10%
0402
50V
GND
GND
GND
GND
GND
GND
Y3
200MHz
6
VDD
1
OE
2
NC
3
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CLKN
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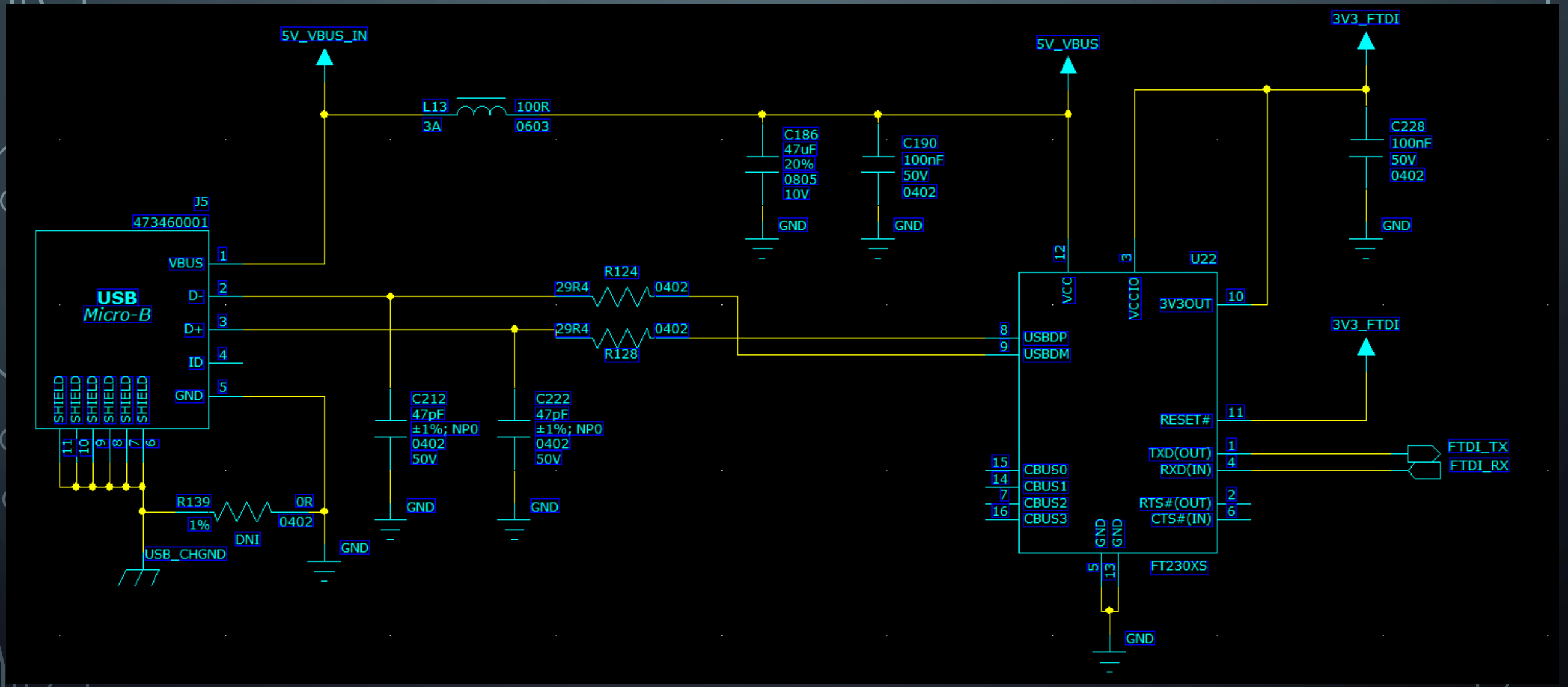
5
TDC_MCLK_P
TDC_MCLK_N
531BC200M000DG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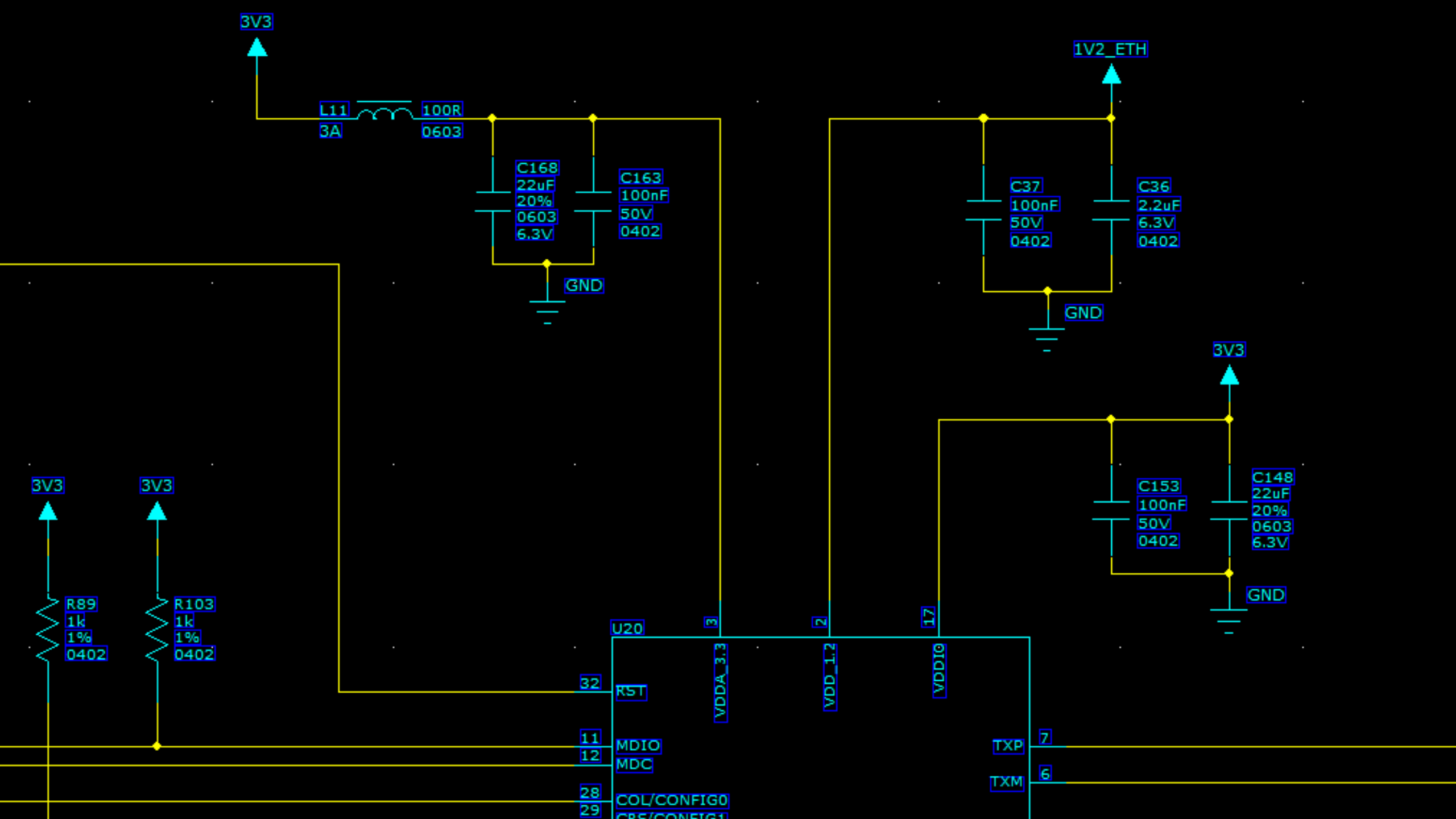
3A
100R
0603
C186
47uF
20%
0805
10V
GND
C190
100nF
50V
0402
GND
5V_VBUS
3V3_FTDI
C228
100nF
50V
0402
GND
J5
473460001
USB
Micro-B
VBUS
D-
D+
ID
GND
SHIELD
SHIELD
SHIELD
SHIELD
SHIELD
SHIELD
R124
29R4
0402
29R4
0402
R128
C212
47pF
±1%; NP0
0402
50V
GND
C222
47pF
±1%; NP0
0402
50V
GND
R139
1%
0R
0402
DNI
USB_CHGND
GND
U22
VCC
VCCIO
3V3OUT
USBDP
USBDM
RESET#
TXD(OUT)
RXD(IN)
RTS#(OUT)
CTS#(IN)
CBUS0
CBUS1
CBUS2
CBUS3
GND
GND
FT230XS
GND
3V3_FTDI
FTDI_TX
FTDI_RX


3V3
L11
3A
100R
0603
C168
22uF
20%
0603
6.3V
C163
100nF
50V
0402
GND
1V2_ETH
C37
100nF
50V
0402
C36
2.2uF
6.3V
0402
GND
3V3
C153
100nF
50V
0402
C148
22uF
20%
0603
6.3V
GND
3V3
3V3
R89
1k
1%
0402
R103
1k
1%
0402
U20
3
2
17
VDDA_3.3
VDD_1.2
VDDIO
32
RST
11
MDIO
12
MDC
28
COL/CONFIG0
29
7
TXP
6
TXM