

S7CAS-PLEIADES-CARTE-MERE_P20

S7_APP1

P20: couf1001-norc2802

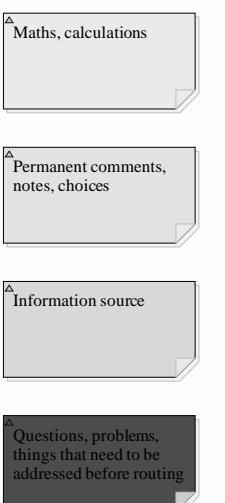
Revision 1.00

Date: 24-01-12

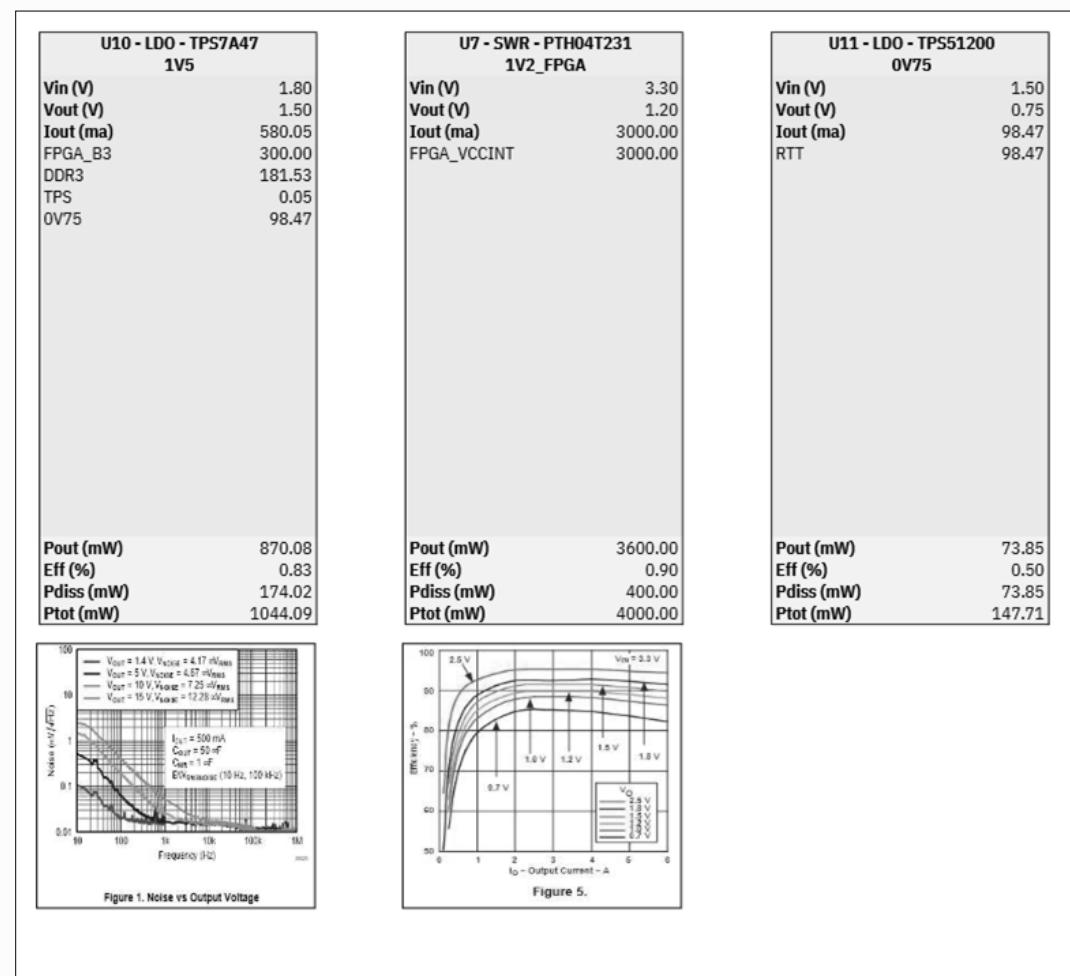
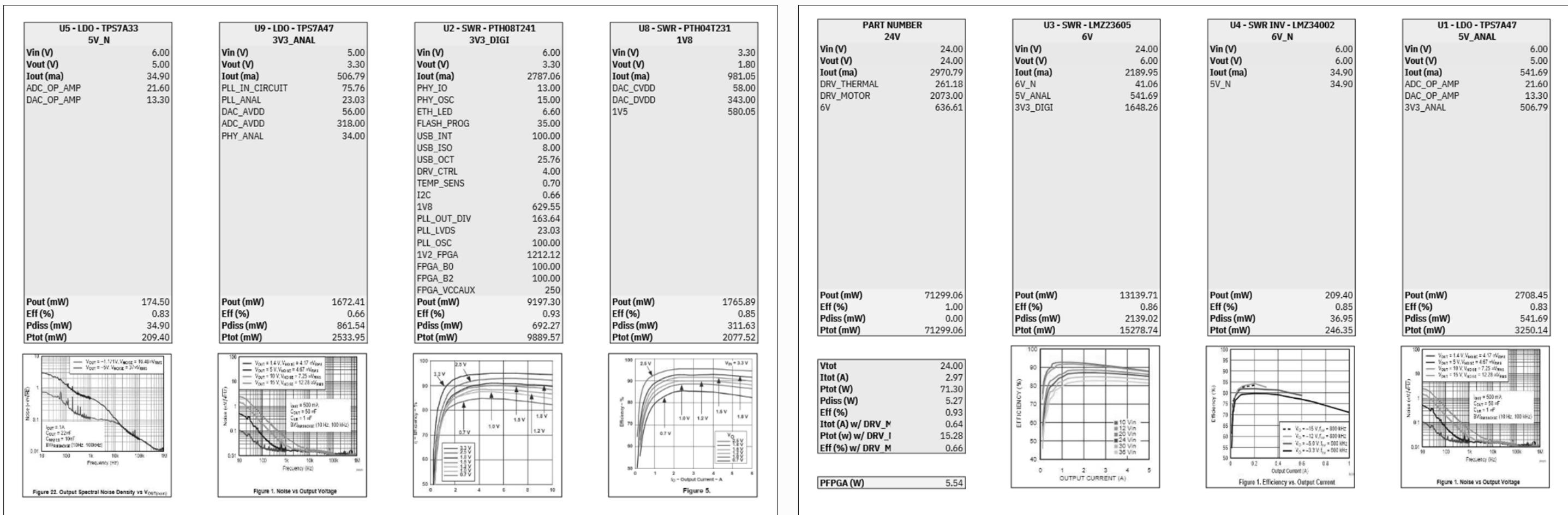
Revision history	

Package size conversion	
Metric	Imperial
1005	0402
1608	0603
2012	0805
3216	1206
3225	1210
6432	2512

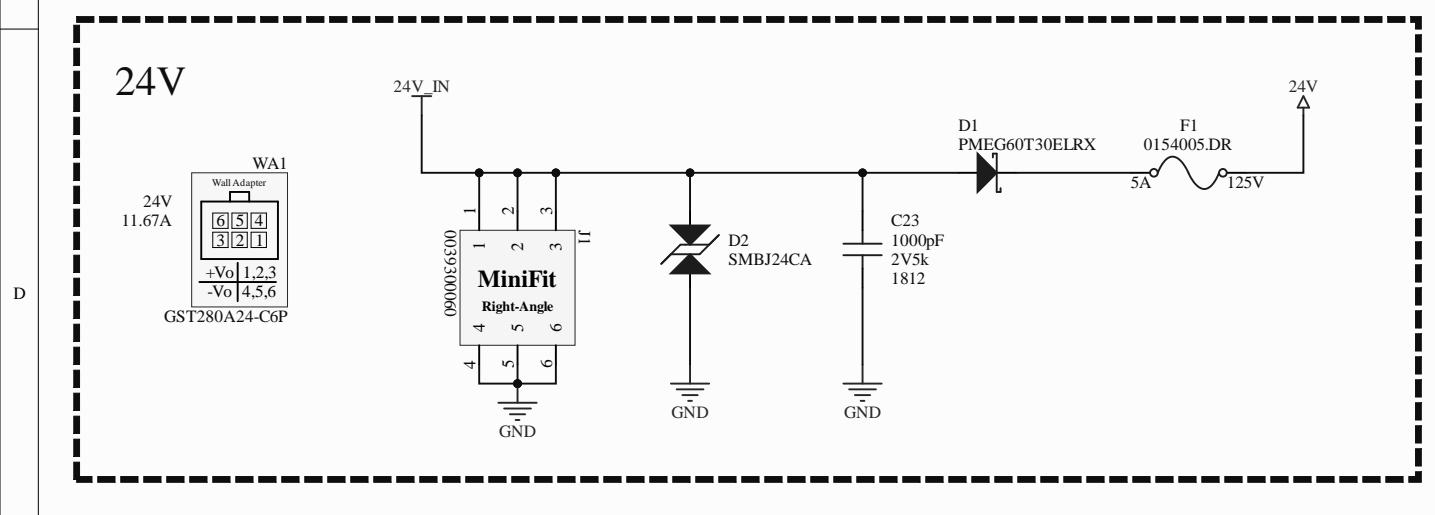
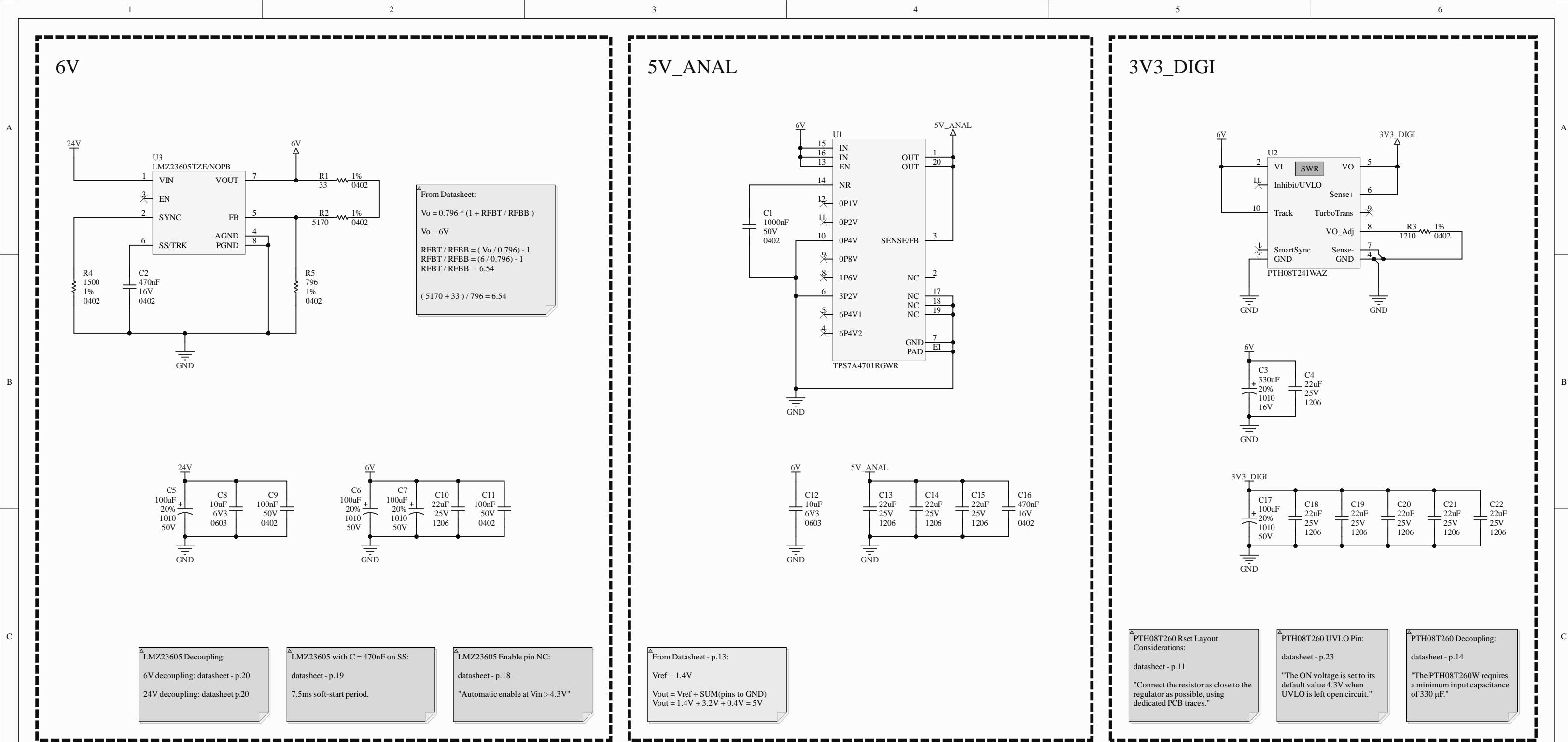
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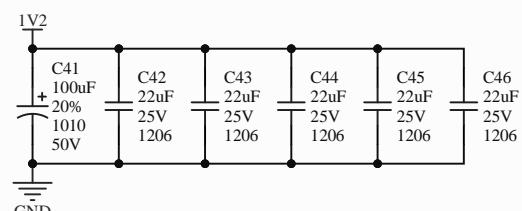
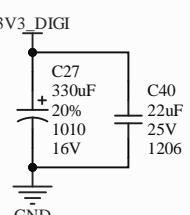
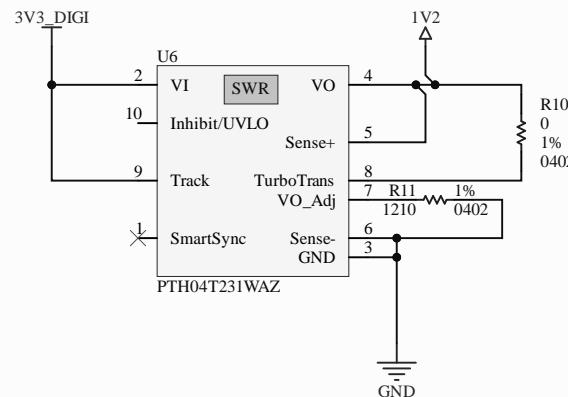
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S7CAS-PLEIADES-CARTE-MERE_P20		
Global Project		
S7_APP1		
Size	Group	Revision
11x17	P20: couf1001-norc2802	1.00
Date	Sheet	
24-01-12	1 of 20	
Filename		Designers
S7CAS-PLEIADES-CARTE-MERE_P20_Title.SchDoc		Florent Cournoyer Charles Normandeau



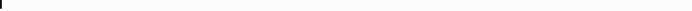
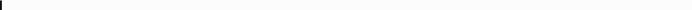
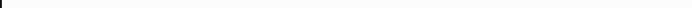
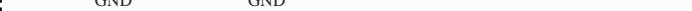
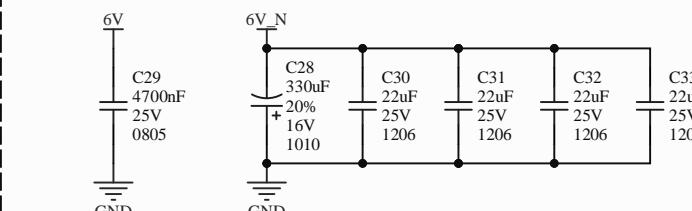
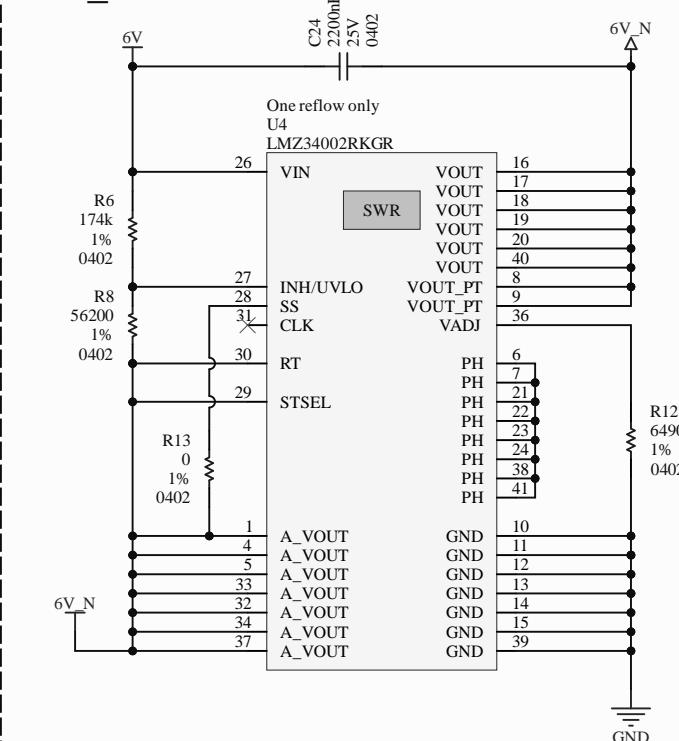
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Project Title	S7CAS-PLEIADES-CARTE-MERE_P20		
Global Project	S7_APP1		
Size	Group	Revision	
11x17		1.00	
Date	24-01-12	Sheet	2 of 20
Filename	S7CAS-PLEIADES-CARTE-MERE_P20_Power-Tree-Analysis.SchDoc		
Designers	Florent Cournoyer Charles Normandeau		



1V2



6V_N



Sheet Name

Power Tree 2/3

Project Title

S7CAS-PLEIADES-CARTE-MERE_P20

Global Project

S7_APP1

Size

11x17

Group

P20: couf1001-norc2802

Revision

1.00

Date

24-01-12

Sheet

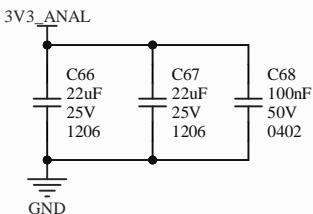
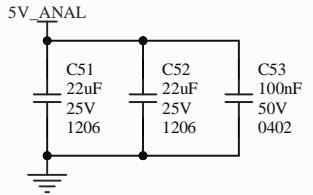
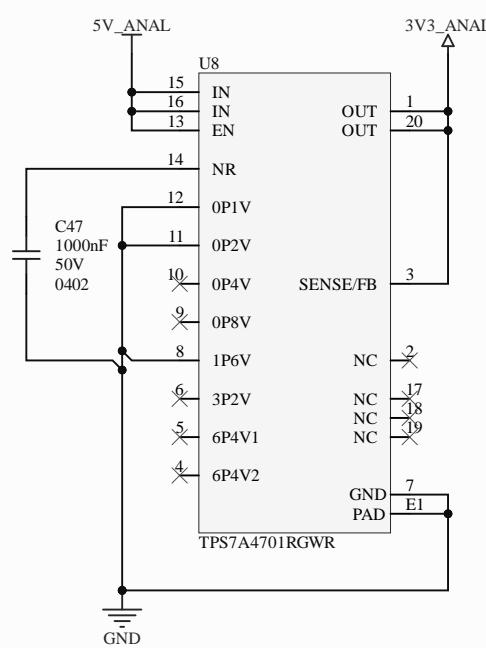
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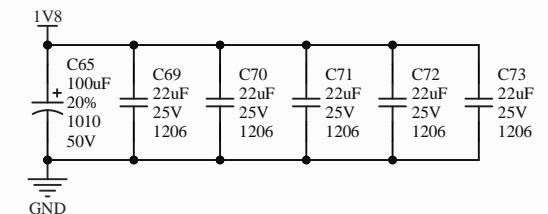
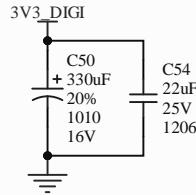
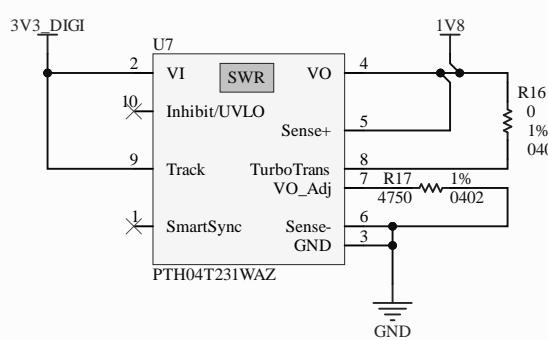
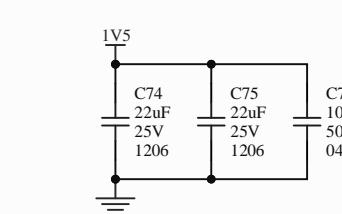
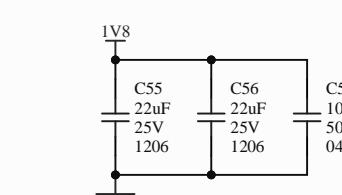
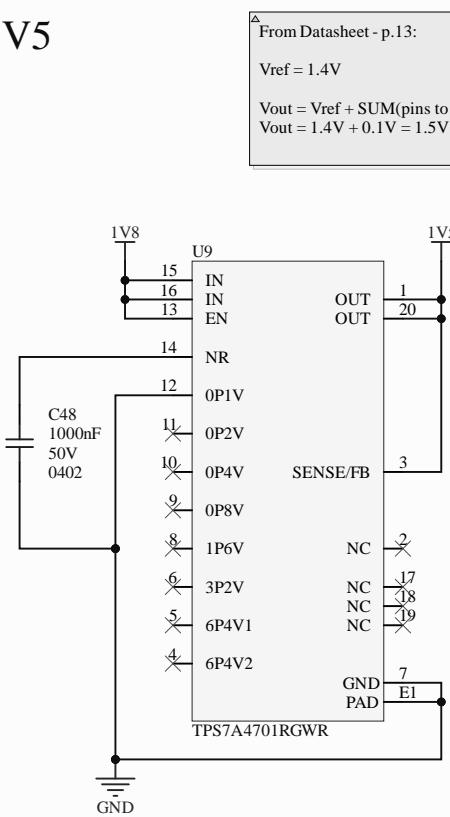
S7CAS-PLEIADES-CARTE-MERE_P20_Power-Tree-2.SchDoc

Designers

Florent Cournoyer
Charles Normandeau

3V3_ANAL

WHAT TO DO WITH
SENSE

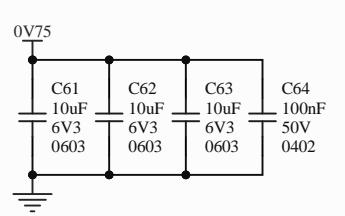
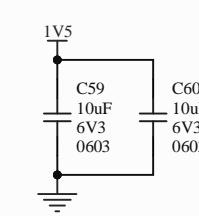
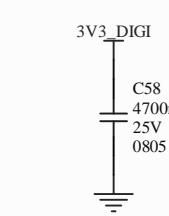
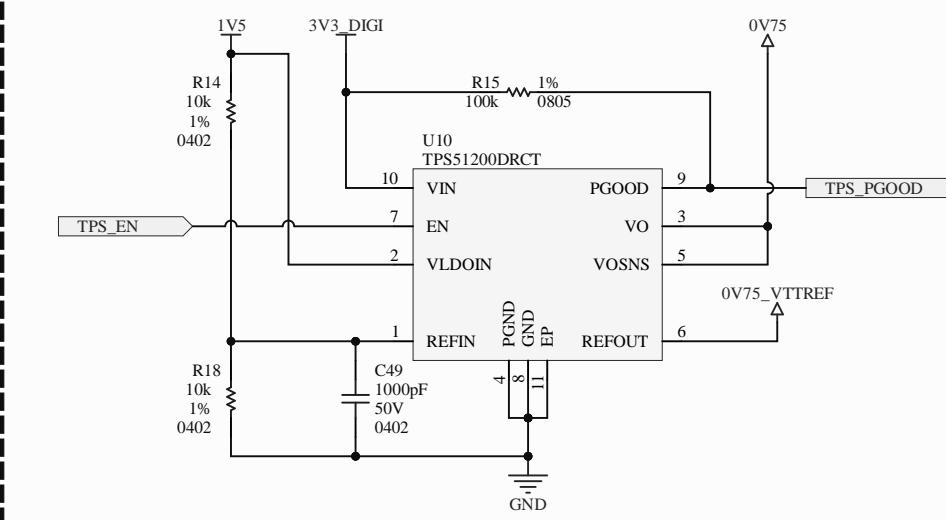
1V8**1V5**

From Datasheet - p.13:

Vref = 1.4V

$$\text{Vout} = \text{Vref} + \text{SUM}(\text{pins to GND})$$

$$\text{Vout} = 1.4V + 0.1V = 1.5V$$

0V75

TPS5 BOM:
datasheet - p.17

BOM is only for 3.3V which is why we choose 3.3V over 2.5V

TPS5 Pin EN:
desing note - LINK BELOW
"Chip enable can use random FPGA IO."

Sheet Name

Power Tree 3/3

Project Title

S7CAS-PLEIADES-CARTE-MERE_P20

Global Project

S7_APP1

Size

11x17

Group

P20: couf1001-norc2802

Revision

1.00

Date

24-01-12

Sheet

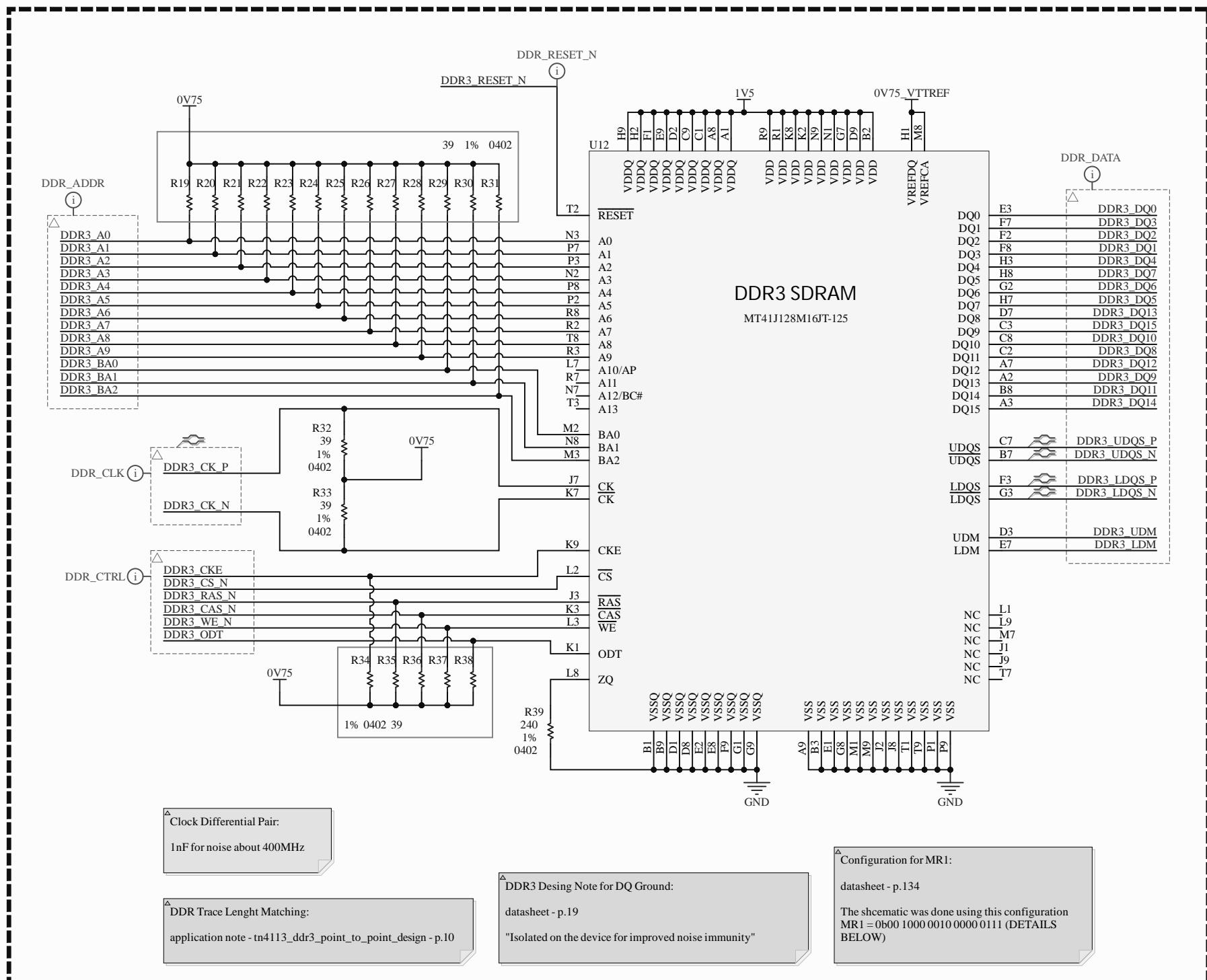
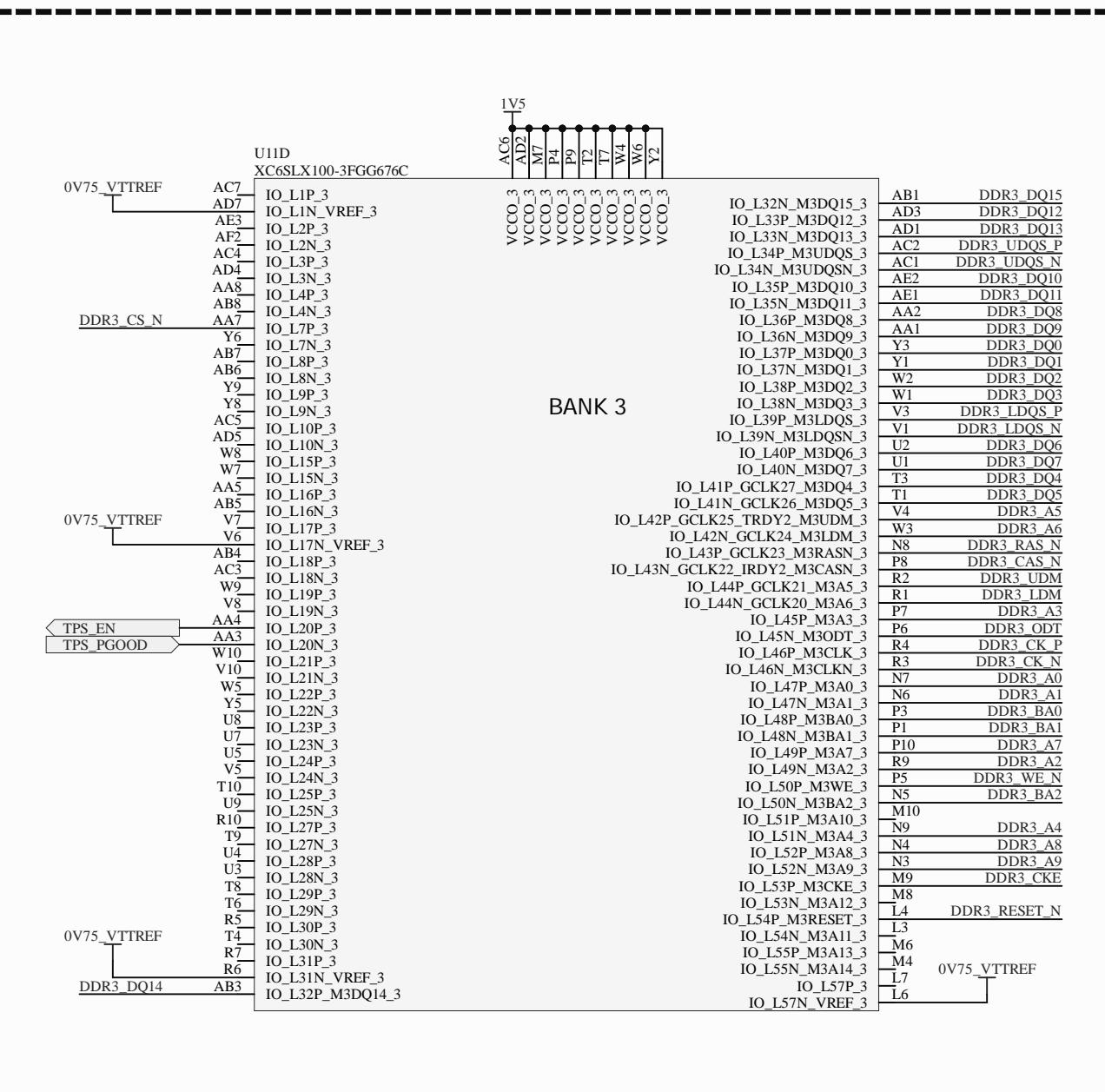
5 of 20

Filename

S7CAS-PLEIADES-CARTE-MERE_P20_Power-Tree-3.SchDoc

Designers

Florent Cournoyer
Charles Normandeau



TOTAL POWER

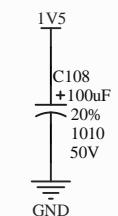
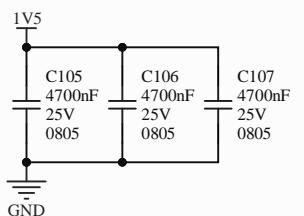
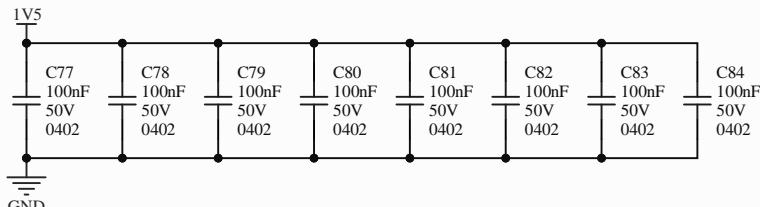
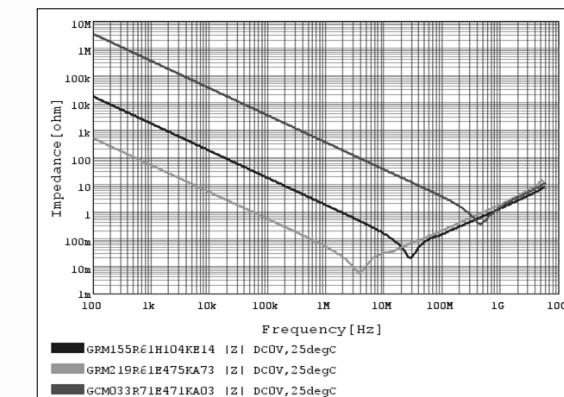
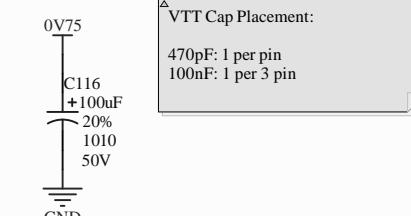
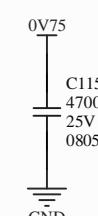
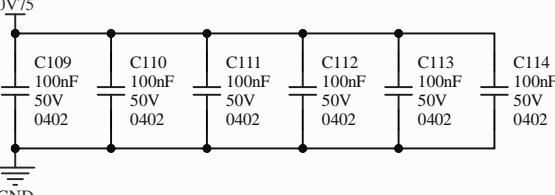
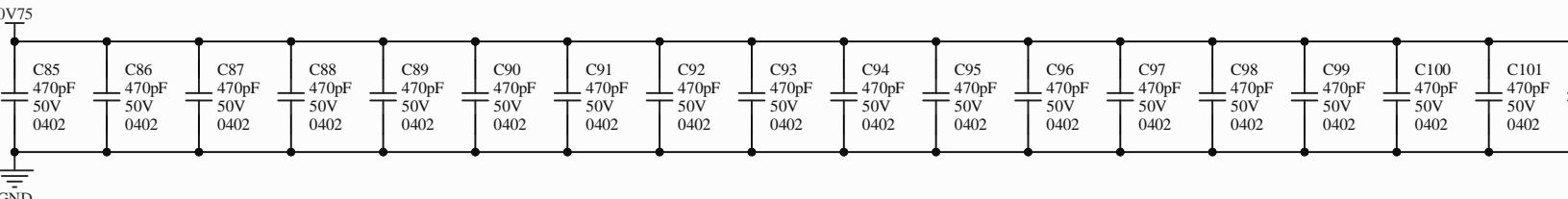
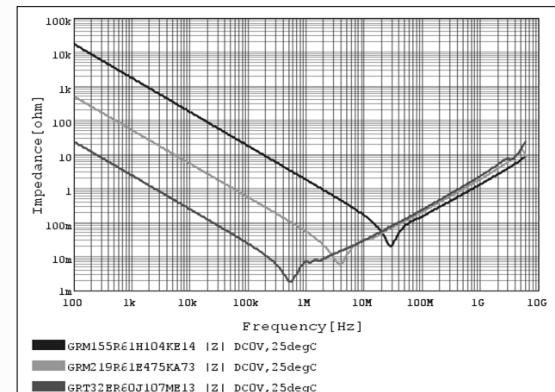
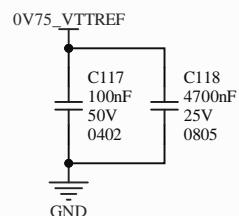
R_TT: $P = NB \cdot (V \cdot V / R) = 18 \cdot (0.4 \cdot 0.4 / 39) = 73.85 \text{ mW}$

FPGA_B3: $P = V \cdot I = 1.5 \cdot 0.3 = 450.00 \text{ mW}$

DDR3: $P = 272.30 \text{ mW}$

TOTAL: $P = 824.95 \text{ mW}$

Sheet Name	DDR3		
Project Title	S7CAS-PLEIADES-CARTE-MERE_P20		
Global Project	<i>S7_APP1</i>		
Size 11x17	Group P20: couf1001-norc2802	Revision 1.00	
Date 24-01-12	Sheet 6	of 20	
Filename S7CAS-PLEIADES-CARTE-MERE_P20_DDR3-FPGA-Bank-3.SchDoc	Designers Florent Cournoyer Charles Normandeau		

1V5_VDD**0V75****0V75_VTTREF**

Sheet Name

DDR3 Decoupling

Project Title

Global Project

Size 11x17

Group P20: couf1001-norc2802

Revision 1.00

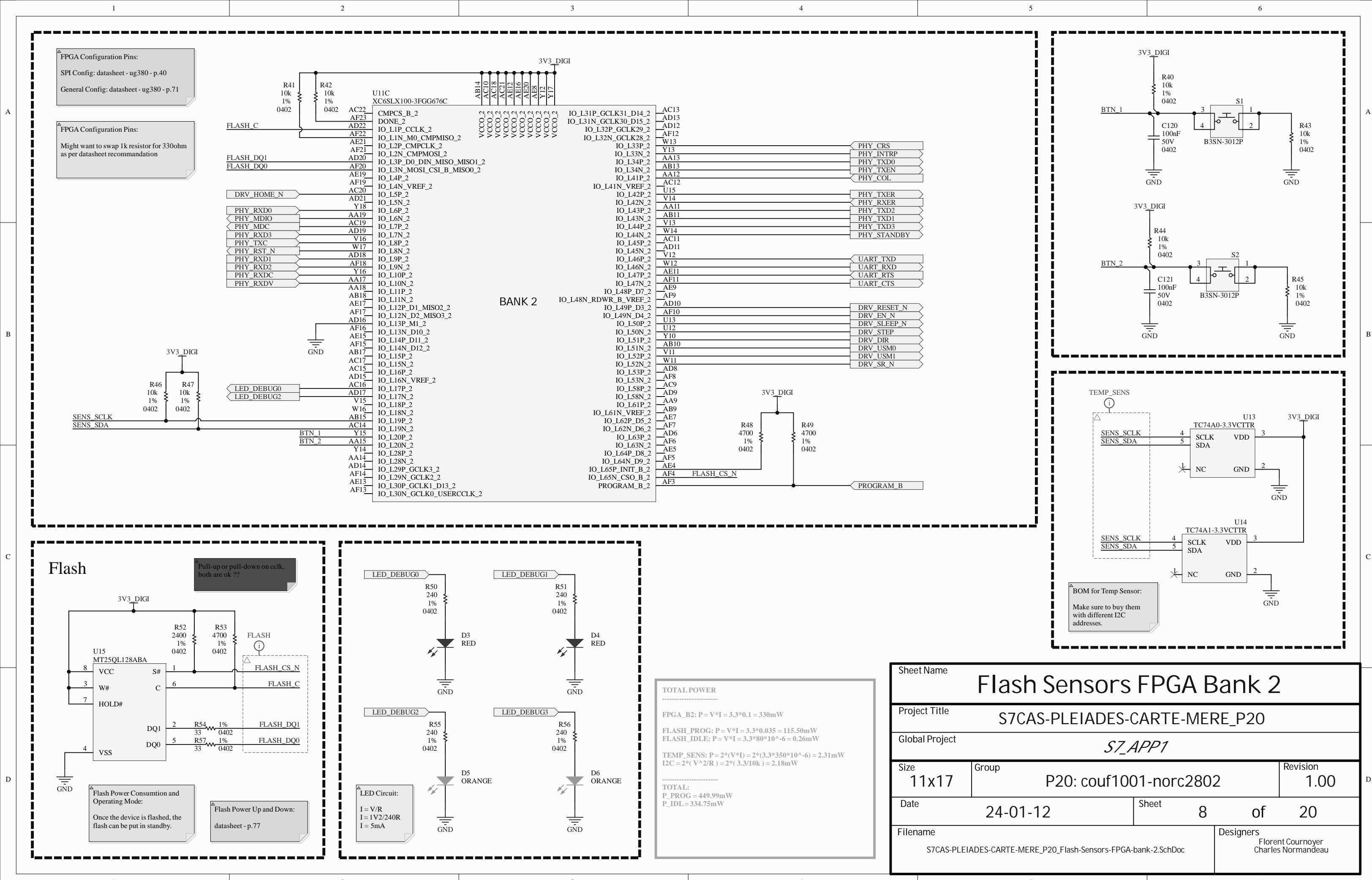
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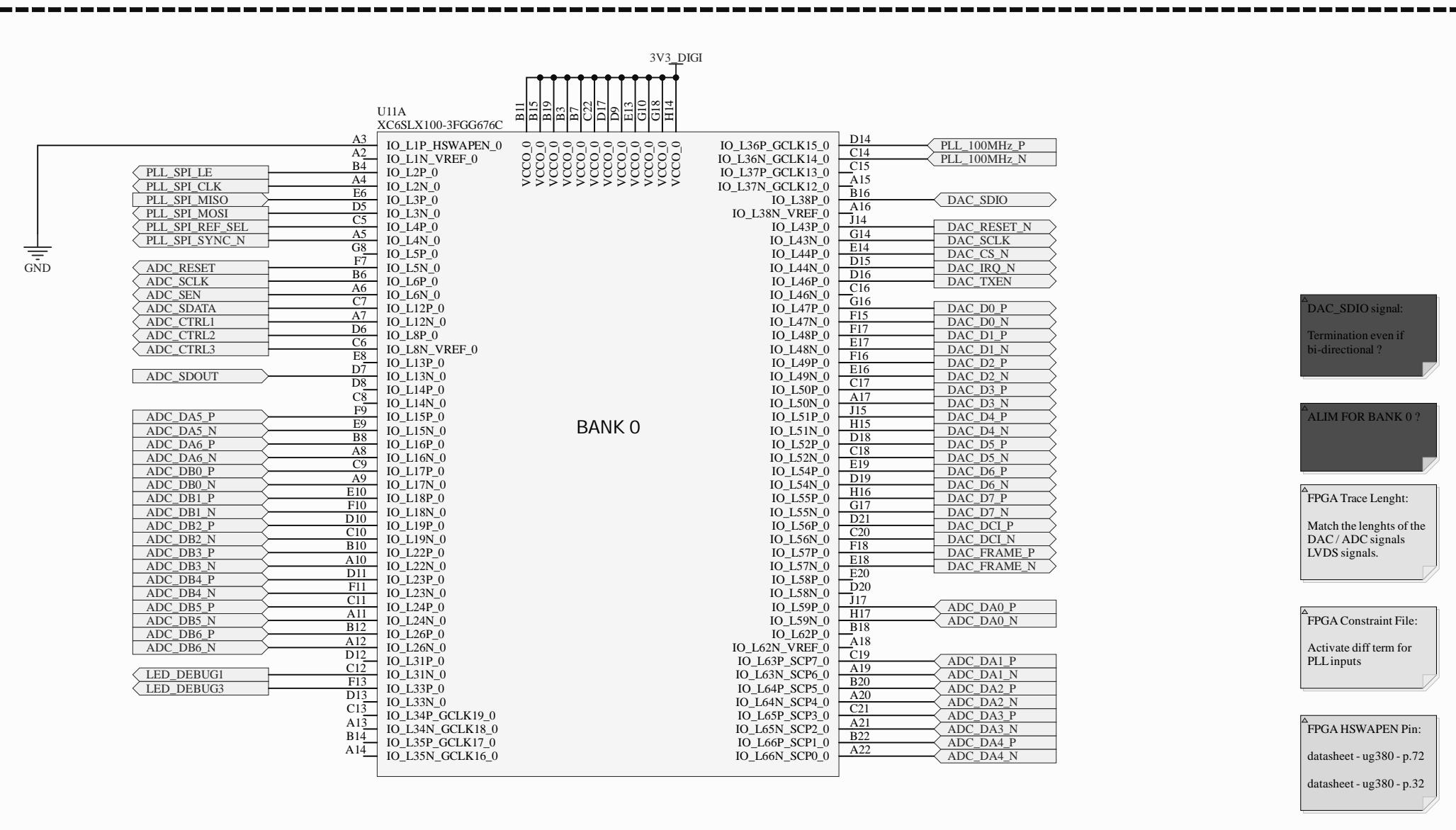
Sheet 7 of 20

Filename

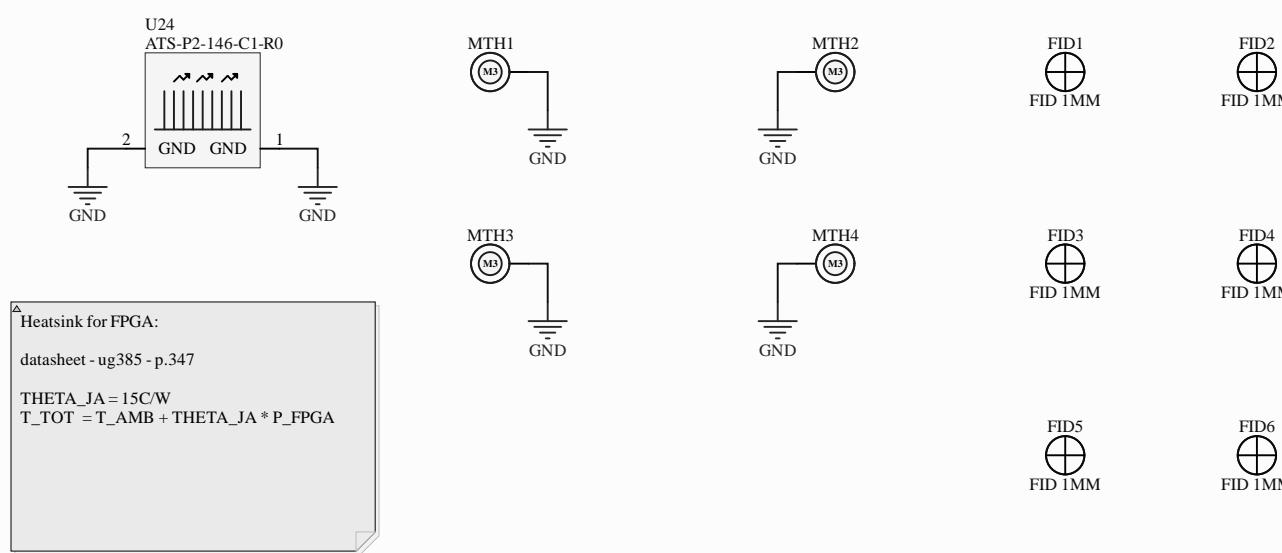
S7CAS-PLEIADES-CARTE-MERE_P20_DDR3-Decoupling.SchDoc

Designers Florent Cournoyer
Charles Normandeau





Mechanical

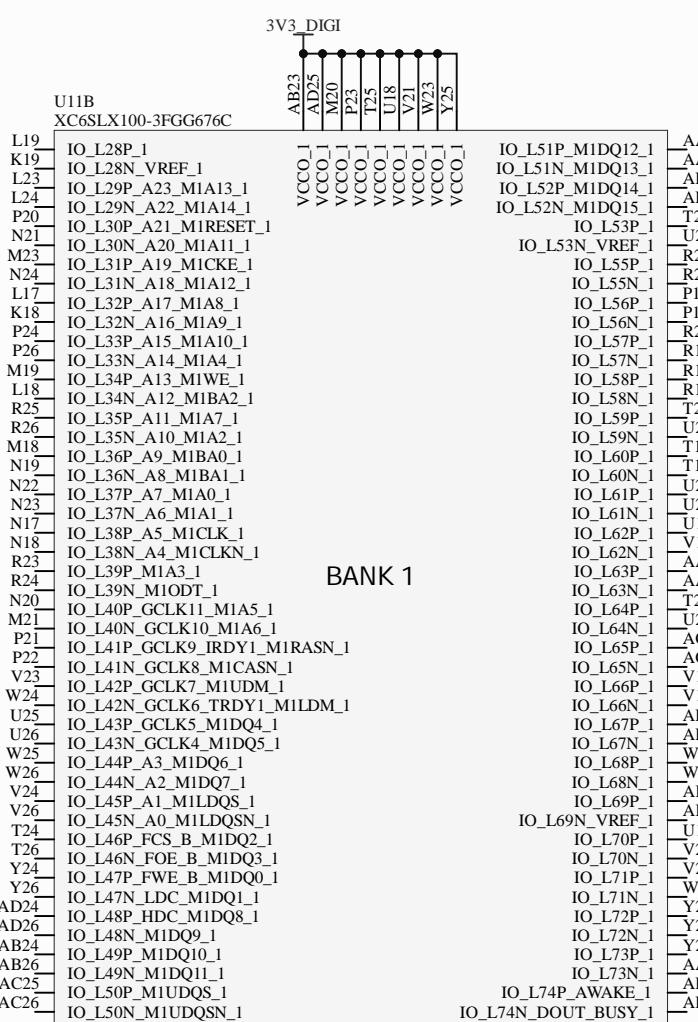


Heatsink for FPGA:
datasheet - ug385 - p.347

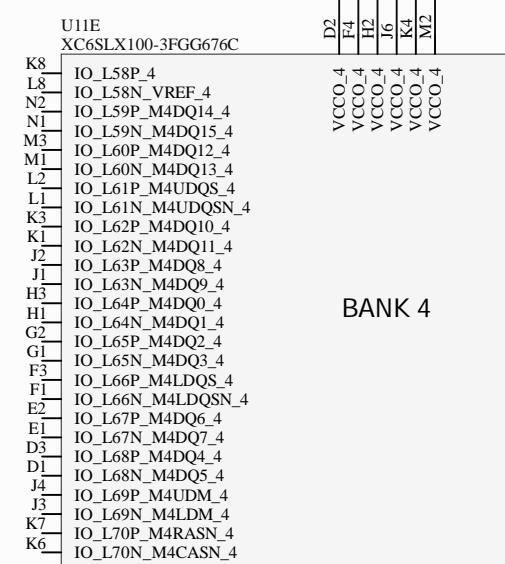
THETA_JA = 15C/W

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Project Title	S7CAS-PLEIADES-CARTE-MERE_P20		
Global Project	<i>S7APP1</i>		
Size 11x17	Group P20: couf1001-norc2802	Revision 1.00	
Date 24-01-12	Sheet 9	of 20	
Filename S7CAS-PLEIADES-CARTE-MERE_P20_Mechanical-FPGA-Bank-0.SchDoc	Designers Florent Cournoyer Charles Normandeau		

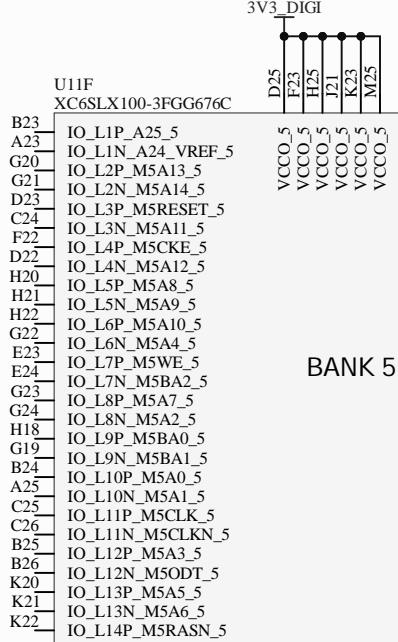
A



BANK 1

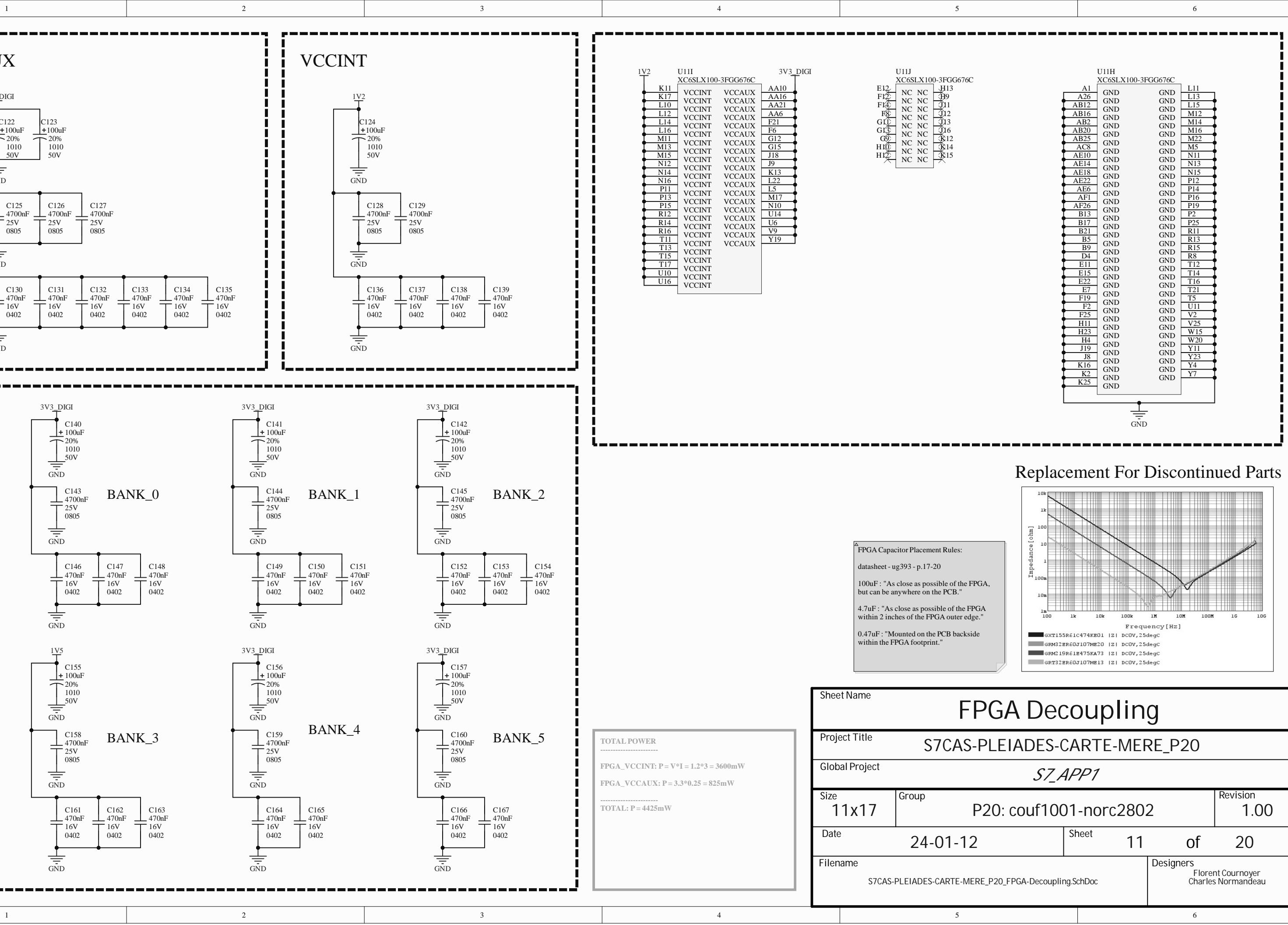


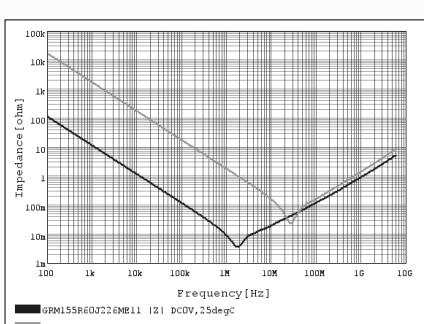
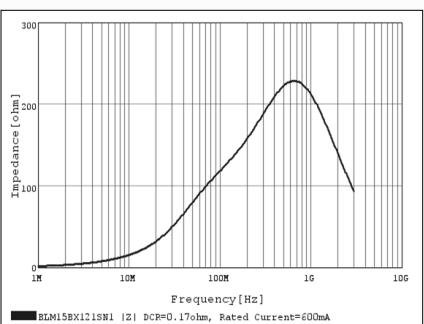
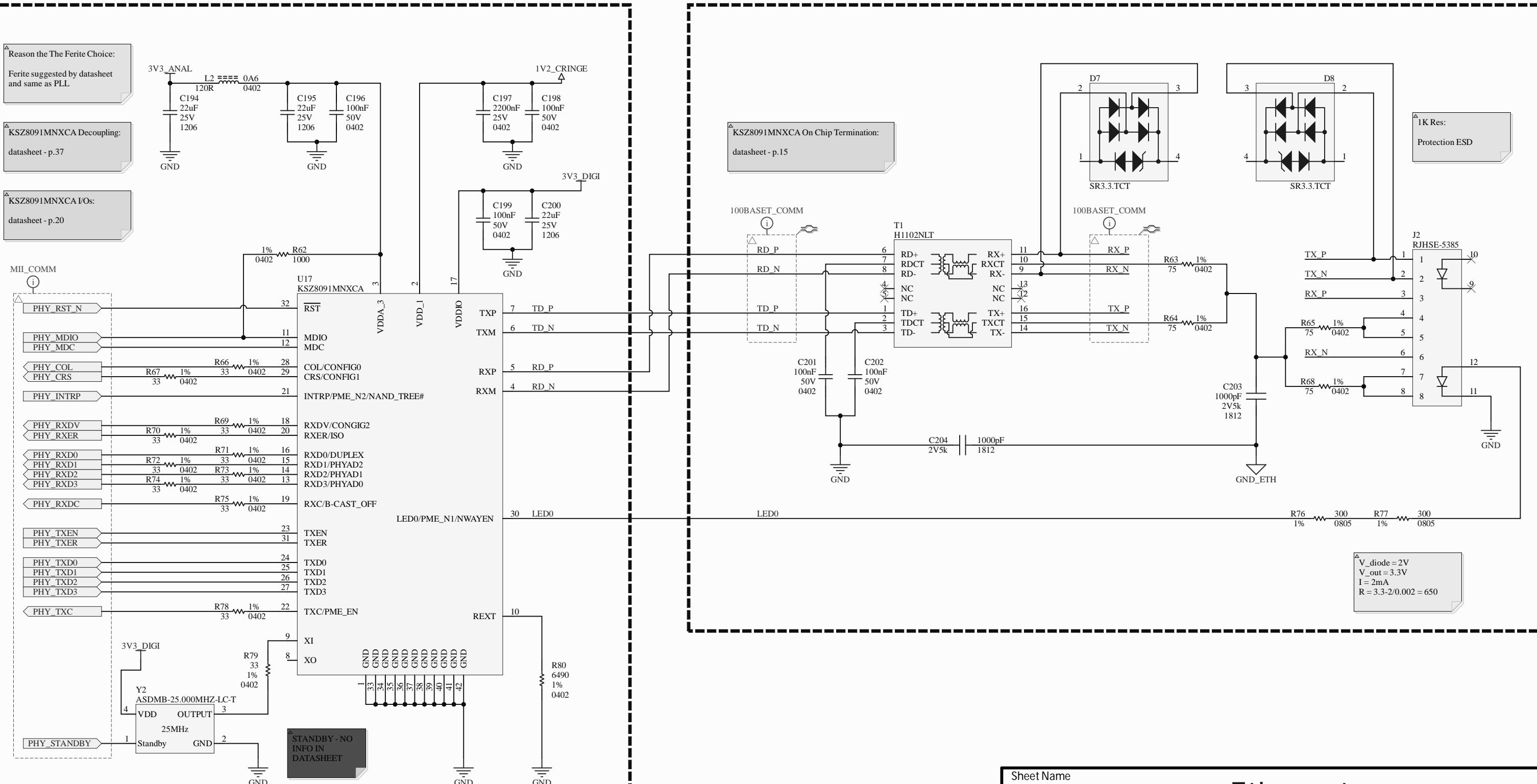
BANK 4



BANK 5

Sheet Name		FPGA Unused Banks	
Project Title		S7CAS-PLEIADES-CARTE-MERE_P20	
Global Project		S7_APP1	
Size	Group	Revision	
11x17		P20: couf1001-norc2802	
Date	Sheet	10	of 20
Filename		Designers	
S7CAS-PLEIADES-CARTE-MERE_P20_FPGA-Unused-Banks.SchDoc		Florent Cournoyer Charles Normandeau	





- KSZ8091MNXCA LED0:
 - LED Mode: datasheet - p.12
 - Output LED Pin: datasheet - p.56

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TOTAL POWER  

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PHY_ANAL = V = 3.3*0.034 = 112.2mW  

PHY_IO: P = V*I = 3.3*0.013 = 42.9mW  

PHY_OSC: P = V*I = 3.3V*0.015 = 49.5mW  

ETH_LED: P = 2*(V*V/R) = 2*3.3*3.3/1000 =  

21.78mW  

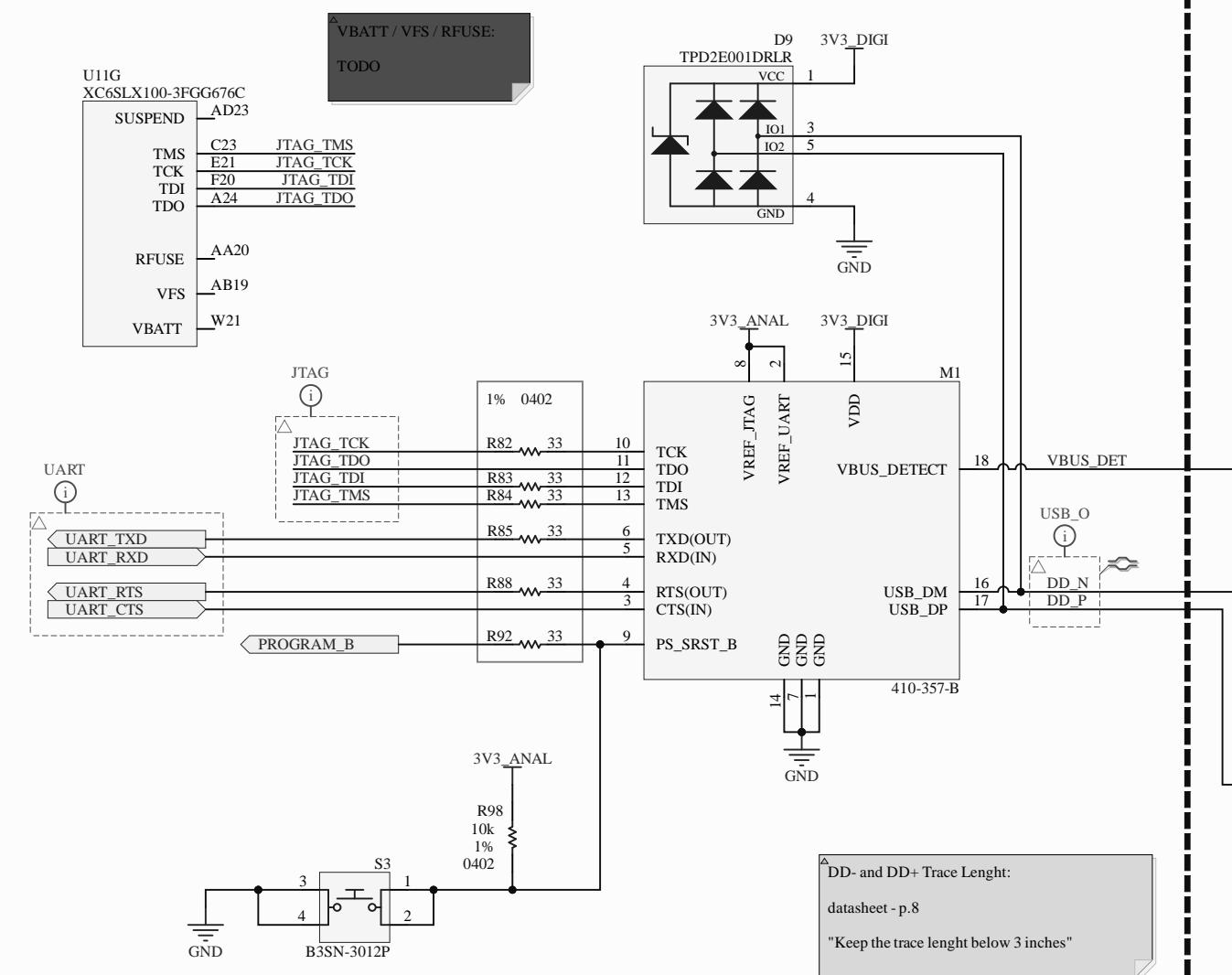
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TOTAL: P = 226.38mW

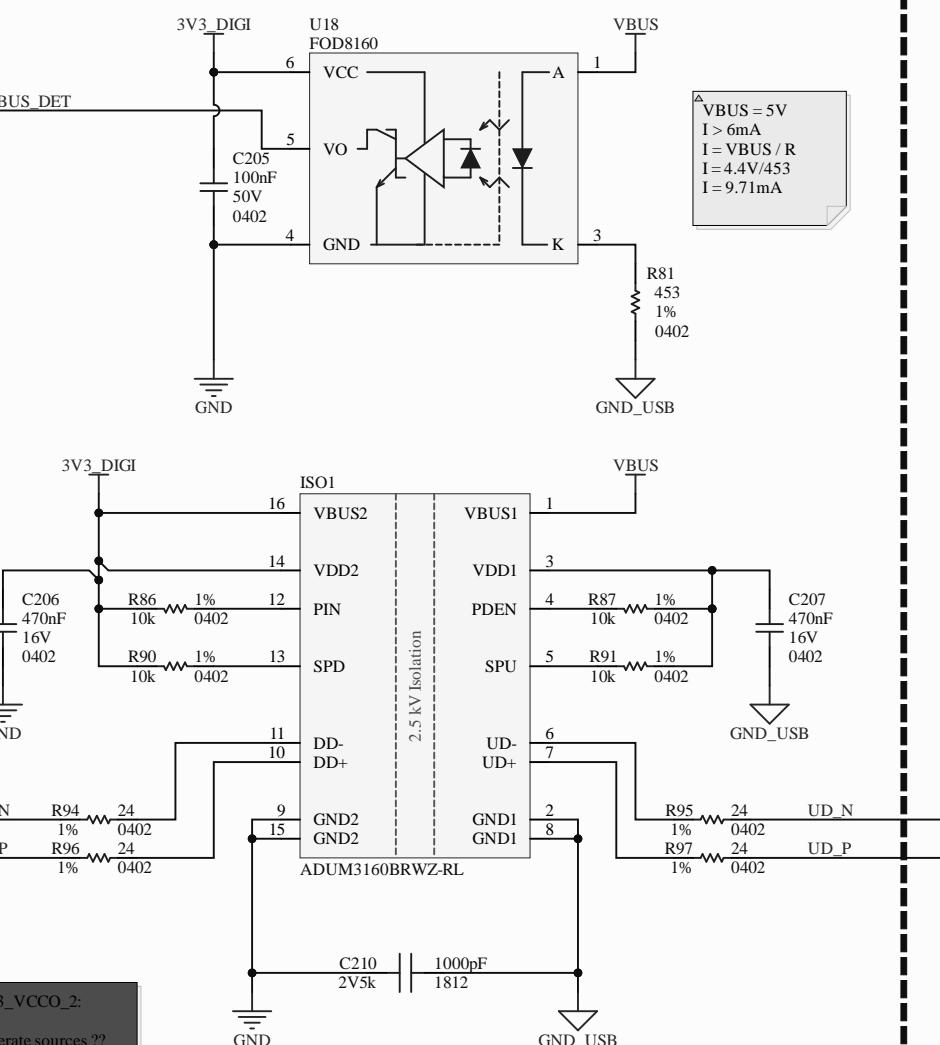
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Global Project	<i>S7_APP1</i>		
Size 11x17	Group P20: couf1001-norc2802	Revision 1.00	
Date 24-01-12	Sheet 12	of 20	
Filename S7CAS-PLEIADES-CARTE-MERE_P20_Ethernet.SchDoc	Designers Florent Cournoyer Charles Normandeau		

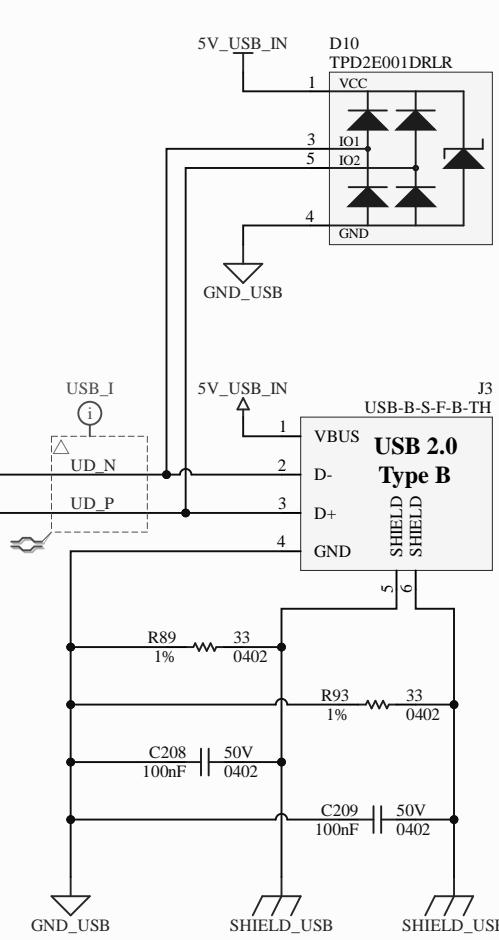
USB to JTAG Interface



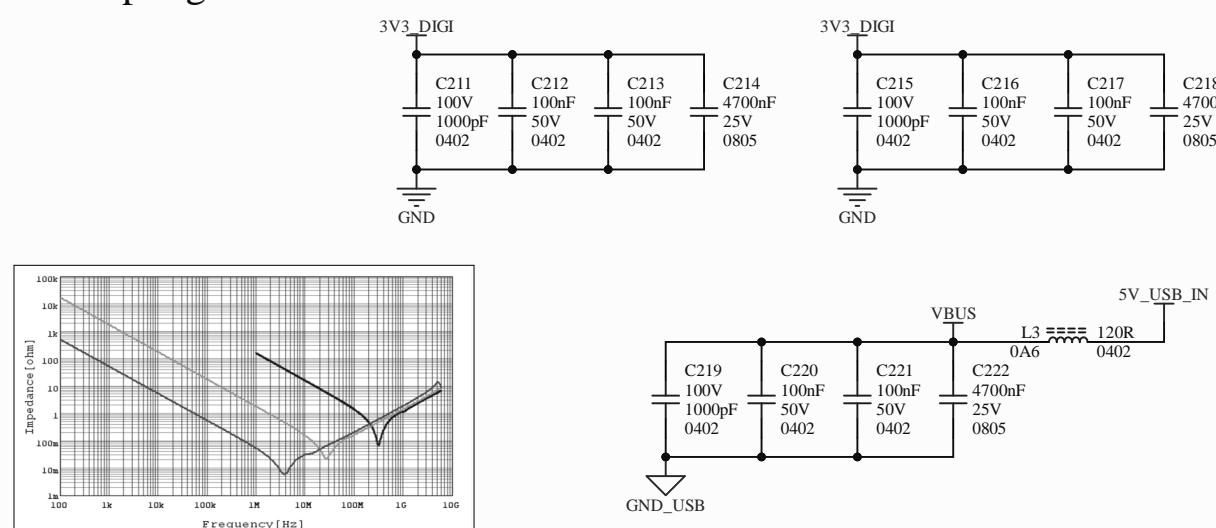
USB Isolation



USB Connector



Decoupling



TOTAL POWER

USB_INT: $P = V \cdot I = 3.3 \cdot 0.1 = 330\text{mW}$

USB_ISO: $P = (V \cdot I) = 3.3 \cdot 0.008 = 26.4\text{mW}$
USB_OPT: $P = 85\text{mW}$

TOTAL: $P = 467.8\text{mW}$

Sheet Name

Project Title

S7CAS-PLEIADES-CARTE-MERE_P20

S7_APP1

Global Project

Size 11x17 Group P20: couf1001-norc2802 Revision 1.00

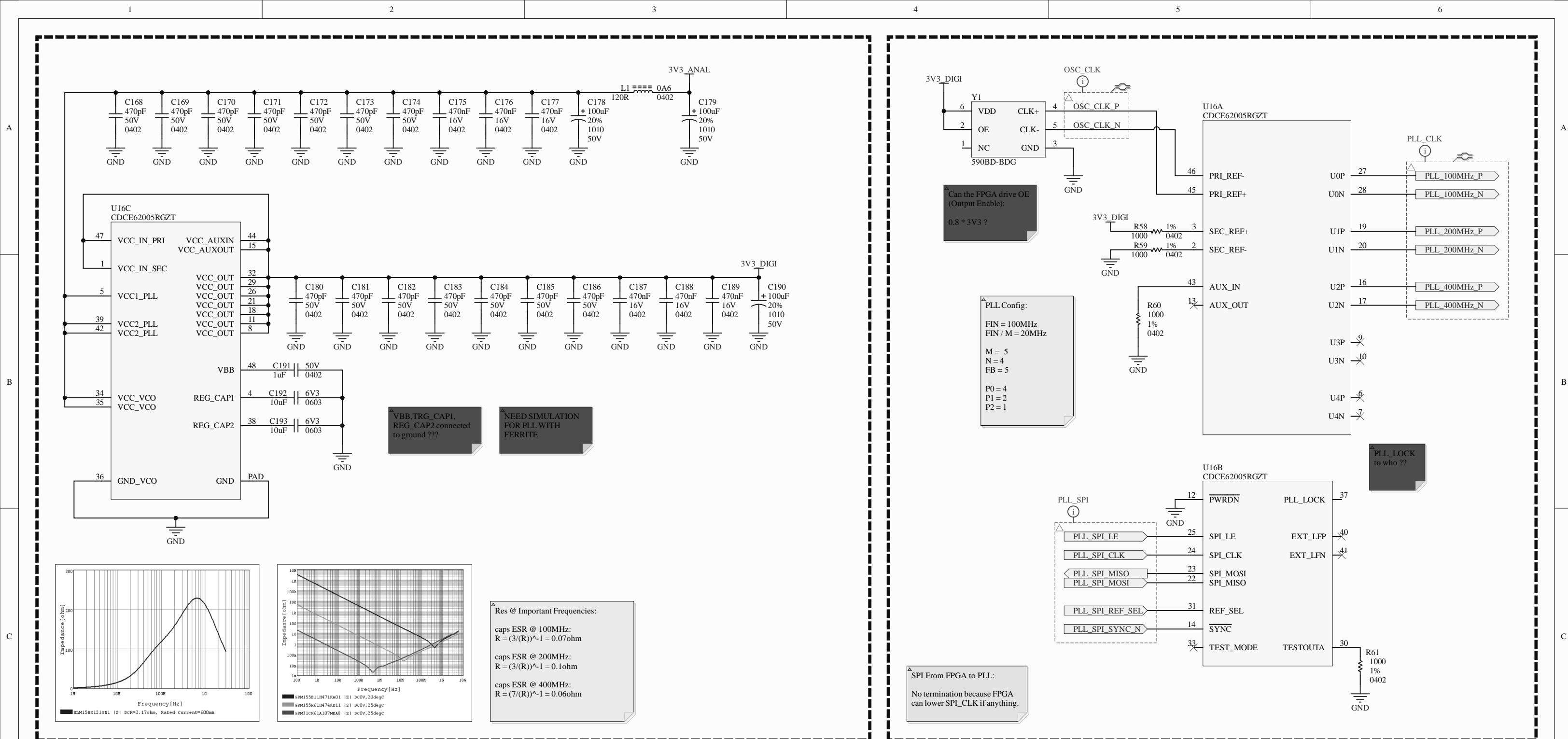
Date 24-01-12

Sheet 13 of 20

Filename

S7CAS-PLEIADES-CARTE-MERE_P20_USB.SchDoc

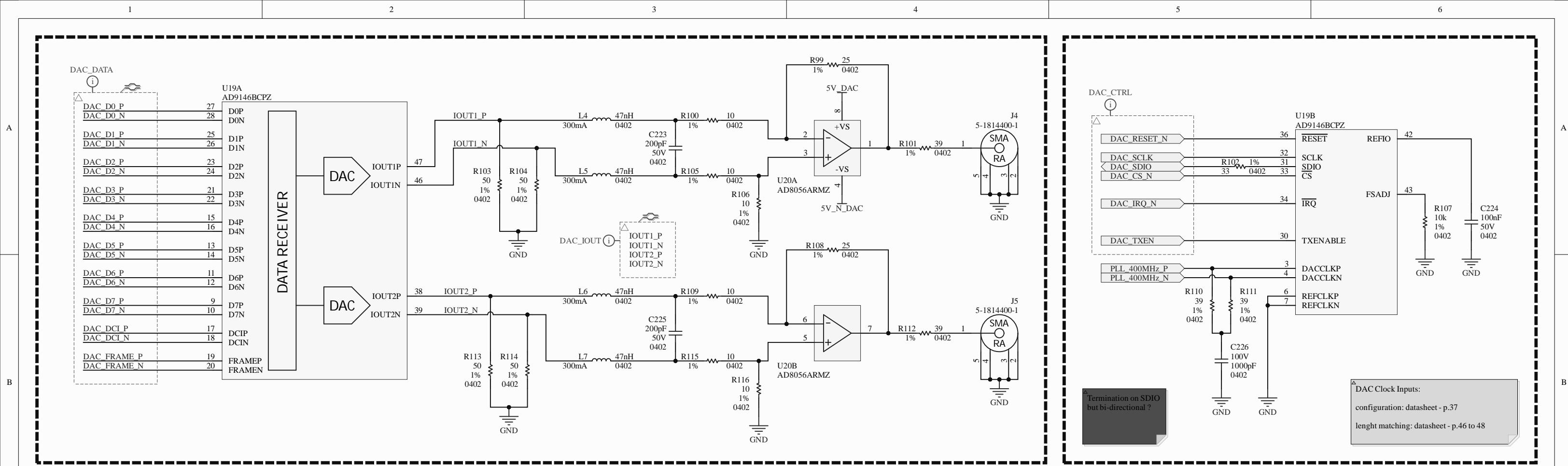
Designers Florent Cournoyer
Charles Normandeau



TOTAL POWER	

PLL_IN_CIRCUIT: $P = 250\text{mW}$	
PLL_ANAL: $P = 500\text{mW}$	
PLL_OUT_DIV: $P = 3 \times 60 + 2 \times 180 = 540\text{mW}$	
PLL_LVDS: $P = 76\text{mW}$	
PLL_OSC: $P = V \times I = 3.3 \times 0.1 = 330\text{mW}$	

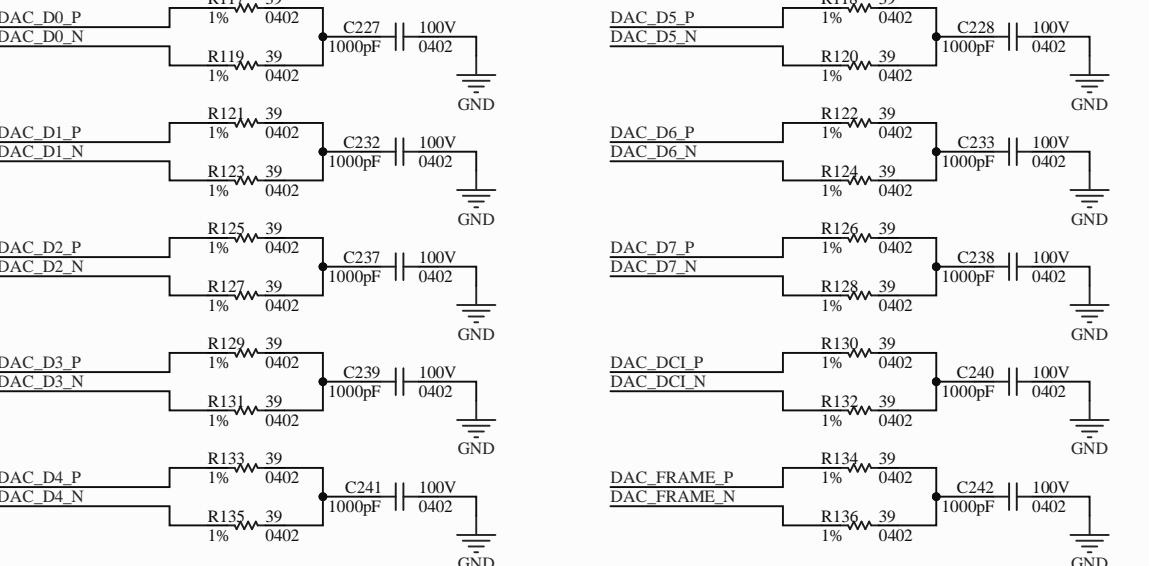
TOTAL: $P = 1696\text{mW}$	



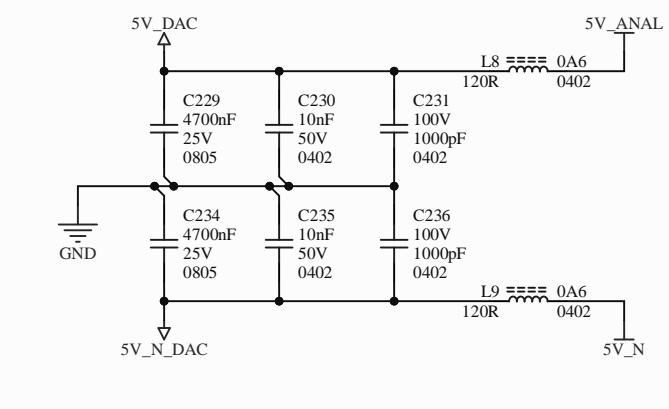
DAC Input Terminations

DAC_D0_P	DAC_D0_P
DAC_D0_N	DAC_D0_N
DAC_D1_P	DAC_D1_P
DAC_D1_N	DAC_D1_N
DAC_D2_P	DAC_D2_P
DAC_D2_N	DAC_D2_N
DAC_D3_P	DAC_D3_P
DAC_D3_N	DAC_D3_N
DAC_DCI_P	DAC_DCI_P
DAC_DCI_N	DAC_DCI_N
DAC_D4_P	DAC_D4_P
DAC_D4_N	DAC_D4_N
DAC_D5_P	DAC_D5_P
DAC_D5_N	DAC_D5_N
DAC_D6_P	DAC_D6_P
DAC_D6_N	DAC_D6_N
DAC_D7_P	DAC_D7_P
DAC_D7_N	DAC_D7_N
DAC_FRAME_P	DAC_FRAME_P
DAC_FRAME_N	DAC_FRAME_N

Terminations:
Is 39ohm ok?
On die terminations?



Op Amp Decoupling



OP Amp Decoupling:
datasheet - p.11

DAC Power Sequencing:
datasheet - p.52
"No specific power supply sequence is required"

TOTAL POWER

DAC_OP_AMP: $P = V \cdot I = 5 \cdot 0.0133 = 66.5mW$

TOTAL: $P = 66.5mW$

DAC

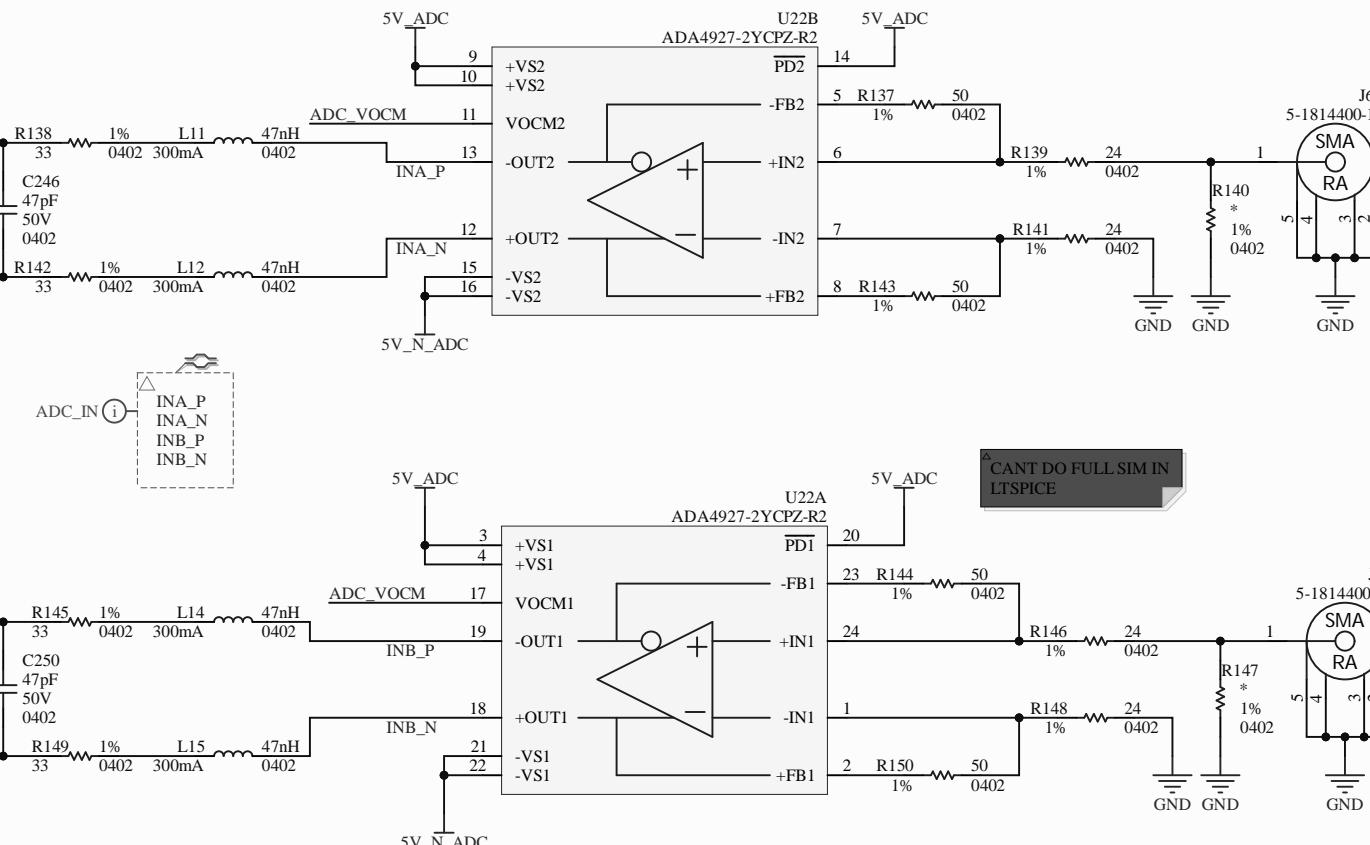
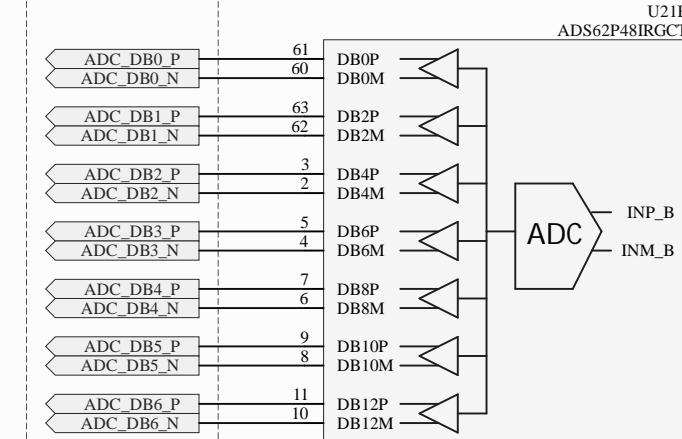
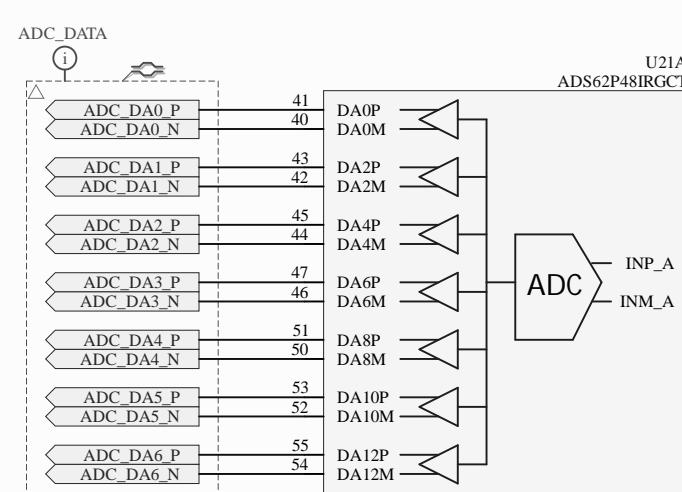
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S7_APP1

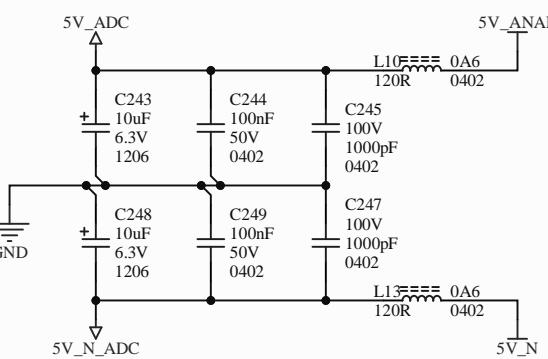
Size: 11x17 Group: P20: couf1001-norc2802 Revision: 1.00

Date: 24-01-12 Sheet: 15 of 20

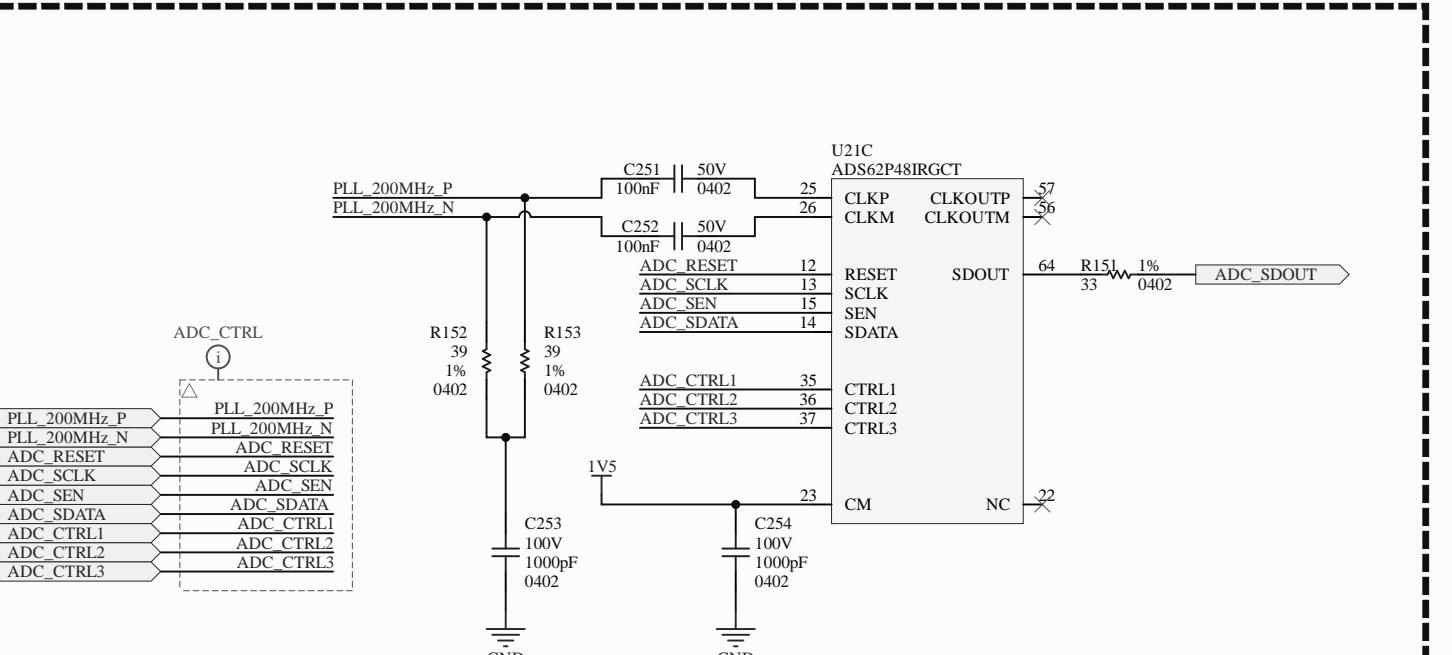
Filename: S7CAS-PLEIADES-CARTE-MERE_P20_DAC.SchDoc Designers: Florent Cournoyer, Charles Normandeau



Op Amp Decoupling



OP Amp Decoupling:
datasheet - p.11

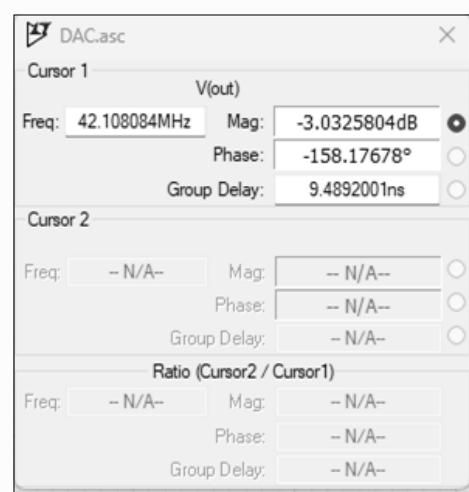
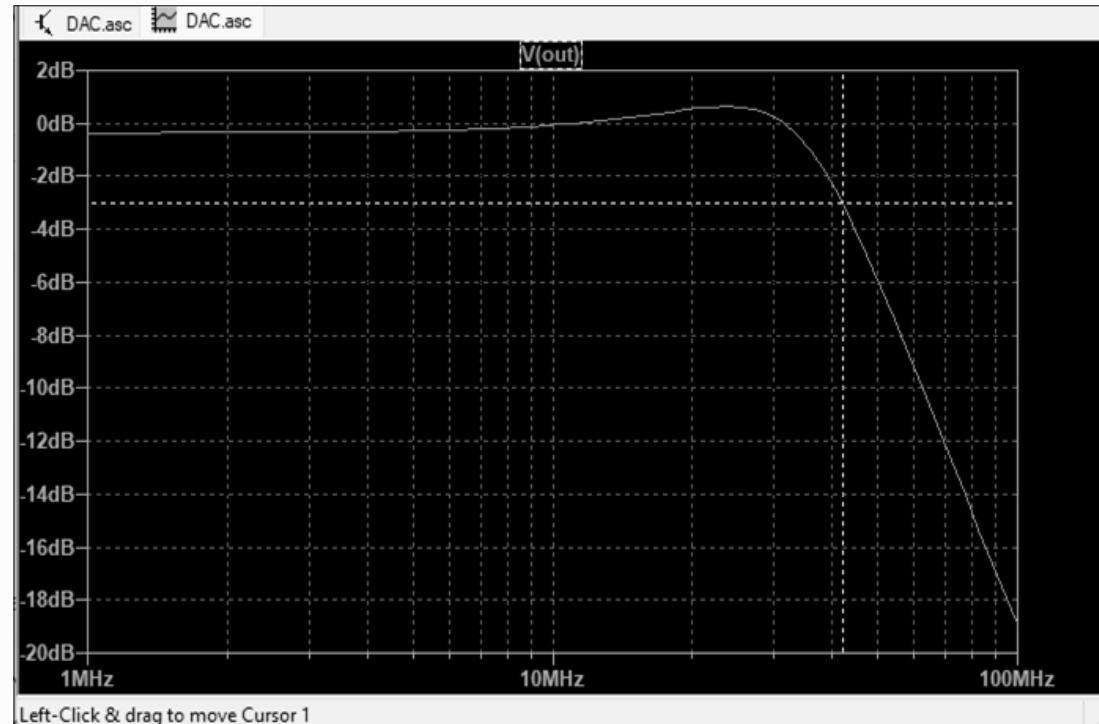
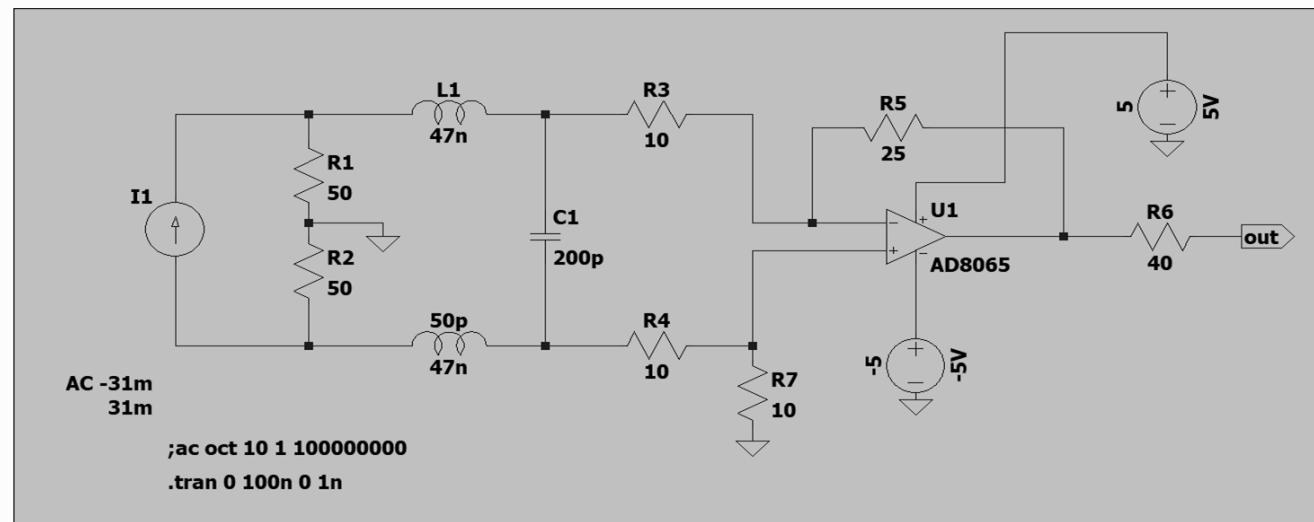


TOTAL POWER
ADC_AMP_OP = V*I = 5*0.0216 = 108mV
TOTAL: P = 108mW

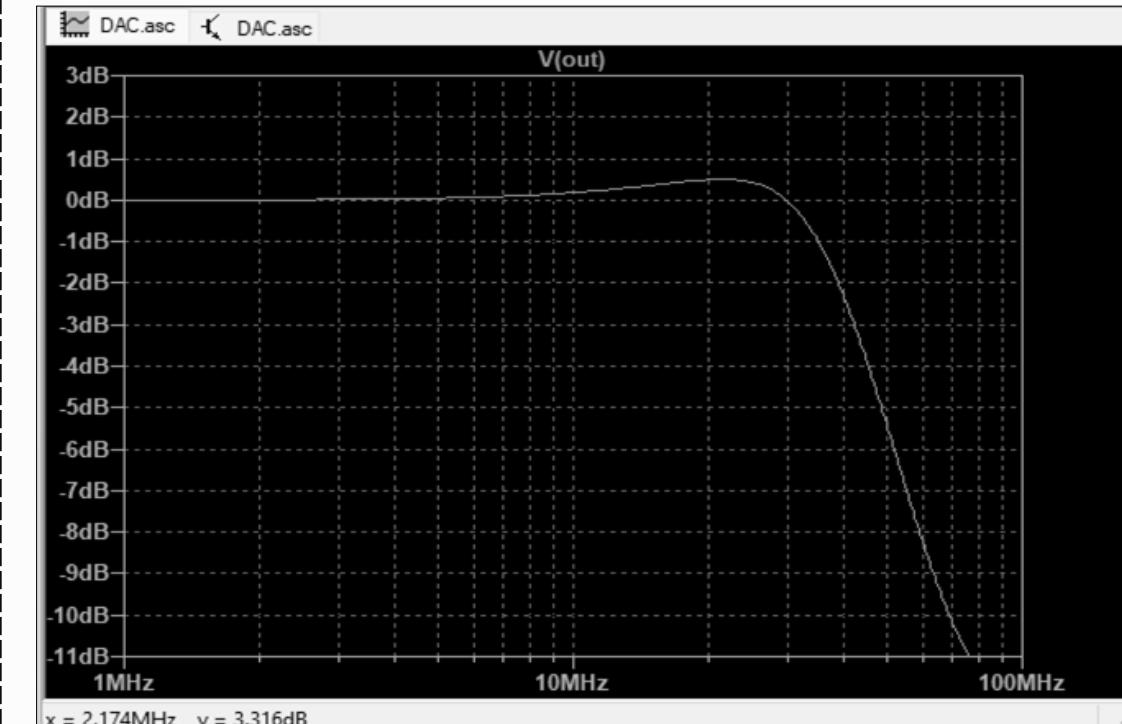
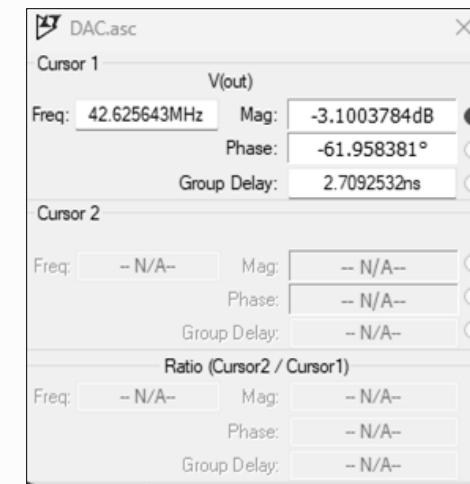
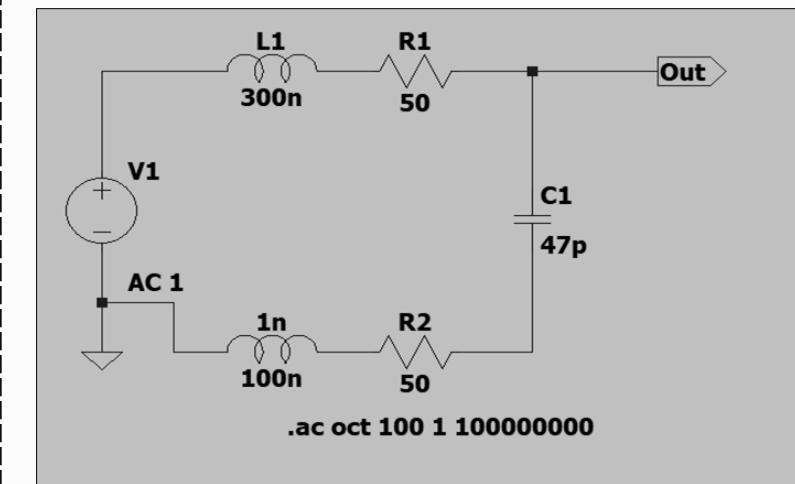
Sheet Name		ADC	
Project Title		S7CAS-PLEIADES-CARTE-MERE_P20	
Global Project		S7_APP1	
Size	Group	P20: couf1001-norc2802	Revision
11x17			1.00
Date	24-01-12	Sheet	16 of 20
Filename	S7CAS-PLEIADES-CARTE-MERE_P20_ADC.SchDoc		
Designers	Florent Cournoyer Charles Normandeau		

ADC Power Up Sequence:
datasheet - p.4
AVDD: Analog supply voltage
DRVDD: Digital supply voltage
"AVDD leads DRVDD during power up"
"DRVDD leads AVDD during power down"

DAC



ADC



C

C

C

C

D

D

Sheet Name
DAC ADC Spice Models

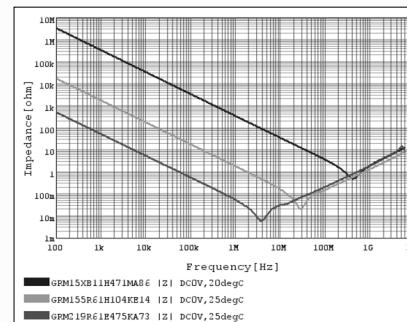
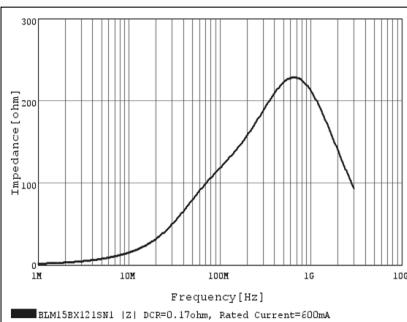
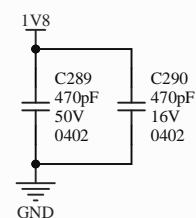
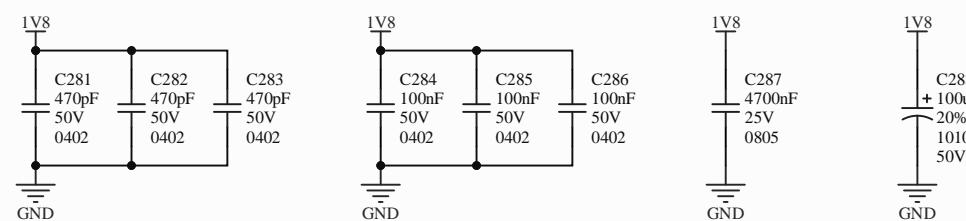
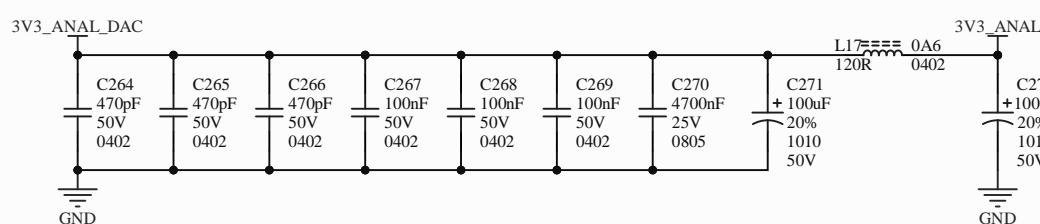
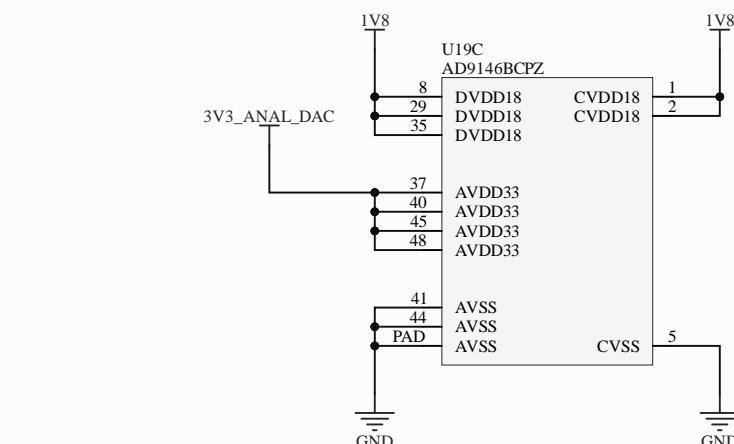
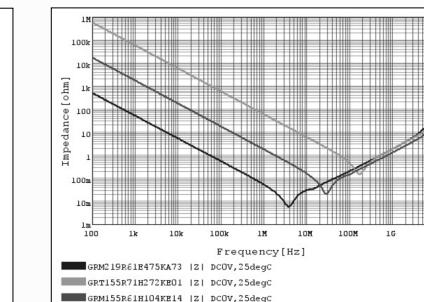
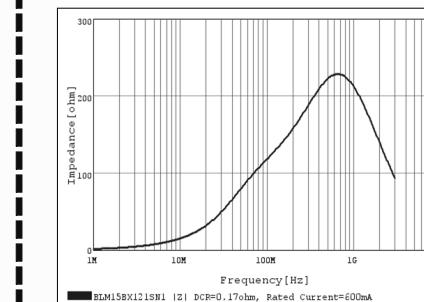
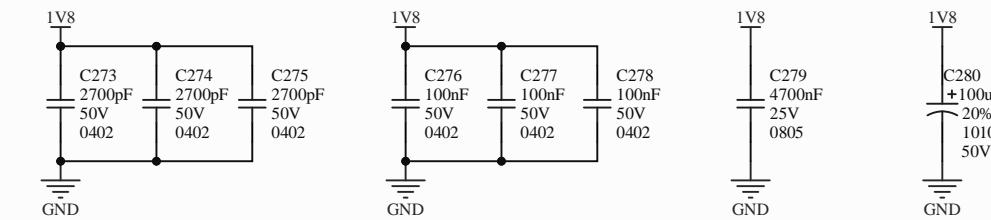
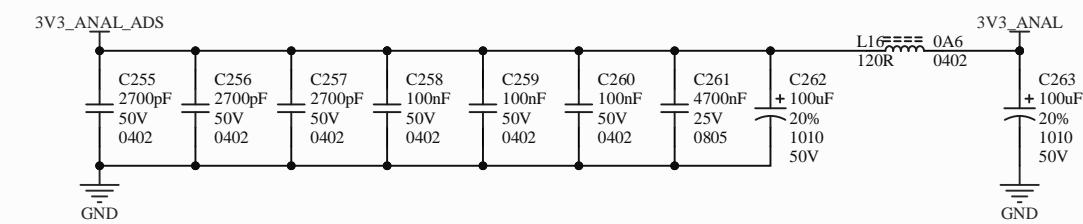
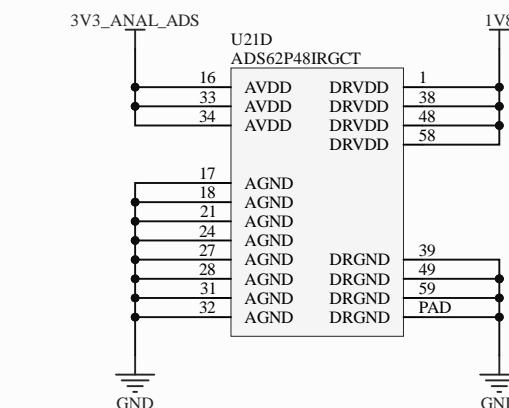
Project Title
S7CAS-PLEIADES-CARTE-MERE_P20

Global Project
S7_APP1

Size 11x17 Group Revision 1.00
P20: couf1001-norc2802

Date 24-01-12 Sheet 17 of 20
24-01-12

Filename Designers
S7CAS-PLEIADES-CARTE-MERE_P20_DAC-ADC-Spice-Models.SchDoc
Florent Cournoyer
Charles Normandeau

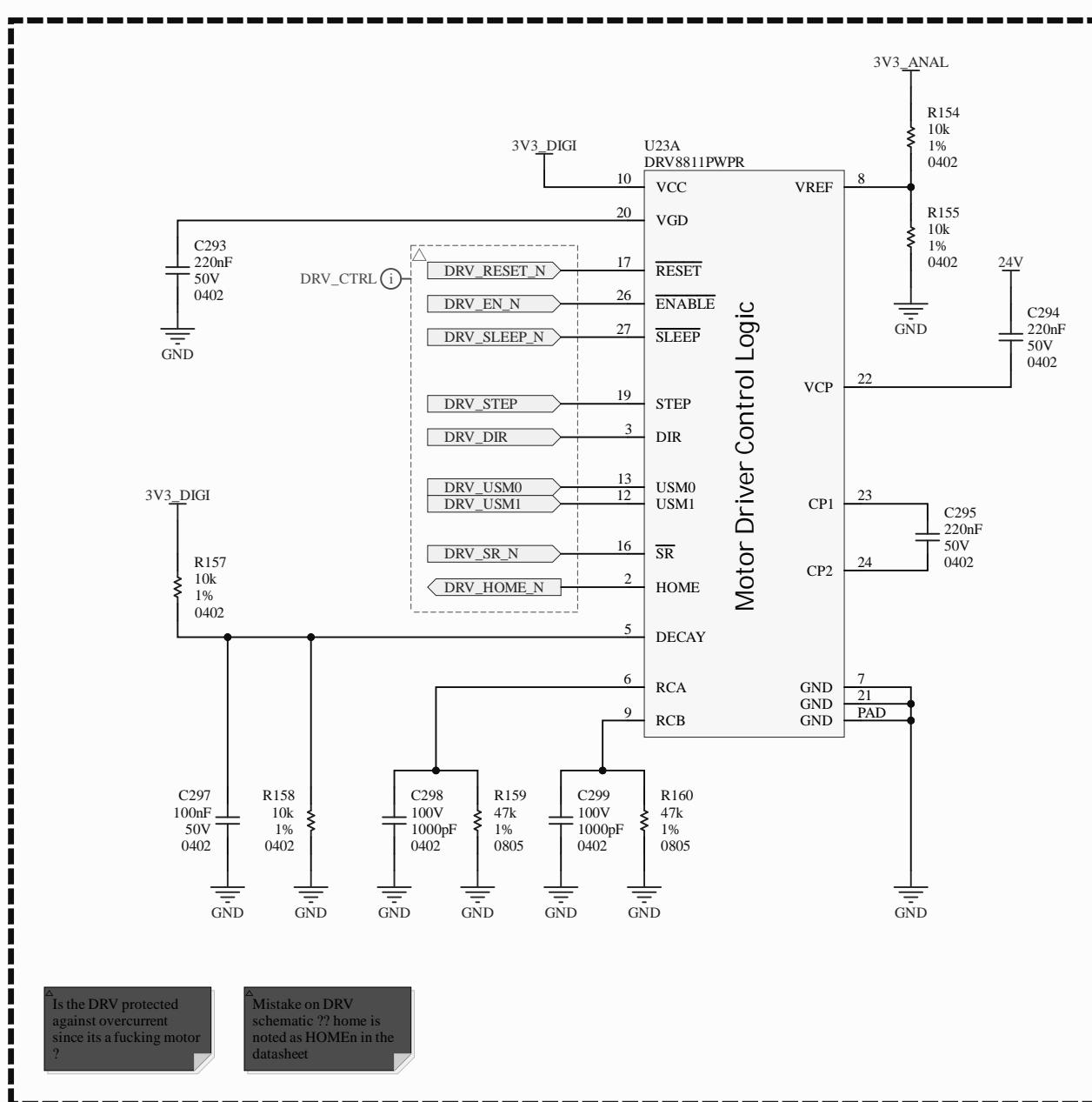
DAC**ADC**

ADC Power Up Sequence:
datasheet - p.4
AVDD: Analog supply voltage
DRVDD: Digital supply voltage
"AVDD leads DRVDD during power up"
"DRVDD leads AVDD during power down"

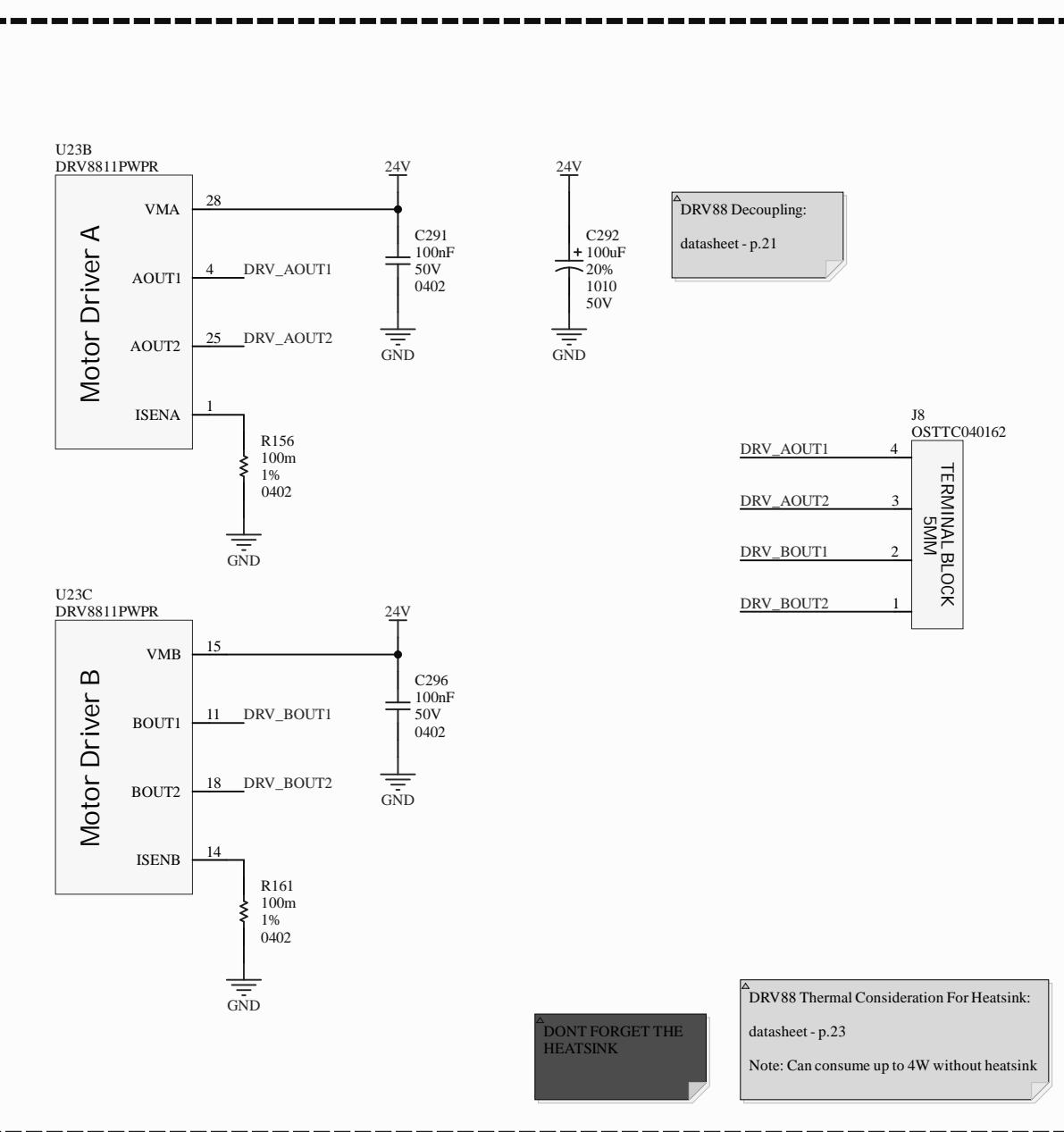
TOTAL POWER	
DAC_AVDD: $P = V \cdot I = 3.3 \cdot 0.056 = 184.8\text{mW}$	
DAC_CVDD: $P = V \cdot I = 1.8 \cdot 0.058 = 104.4\text{mW}$	
DAC_DVDD: $P = V \cdot I = 1.8 \cdot 0.343 = 617.4\text{mW}$	
ADC_AVDD: $P = 1.05\text{W}$	
ADV_DRVDD: $P = 0.3\text{W}$	
TOTAL: $P = 2256.6\text{mW}$	

Sheet Name		DAC ADC Decoupling	
Project Title		S7CAS-PLEIADES-CARTE-MERE_P20	
Global Project		<i>S7_APP1</i>	
Size	Group	P20: couf1001-norc2802	
11x17		Revision 1.00	
Date	24-01-12	Sheet	18 of 20
Filename		Designers Florent Cournoyer Charles Normandeau	
S7CAS-PLEIADES-CARTE-MERE_P20_DAC-ADC-Decoupling.SchDoc			

A



B



C

Is the DRV protected
against overcurrent
since its a fucking motor
?

Mistake on DRV
schematic ?? home is
noted as HOMEn in the
datasheet

DRV88 Current:
 $I_{FS} = V_{REF} / (A_V * R_SENSE)$
 $I_{FS} = 1.65V / (8 * 0.1\Omega)$
 $I_{FS} = 2.0625A$

DRV88 Power Dissipation:
datasheet - p.23

TOTAL POWER

DRV_THERMAL: $P = 4 * (R * I^2) = 4 * RDS * I_{OUT_RMS}^2 = 4 * 0.75 * (0.7 * 2.065)^2 = 6268.41mW$
DRV_MOTOR: $P = V * I = VM * IVM = 24 * (0.008 + 2.065) = 49752mW$
DRV_CTRL: $P = V * I = VCC * IVCC = 3.3 * 0.004 = 13.2mW$

TOTAL: $P = 56033.61mW$

Sheet Name

Motor

Project Title

S7CAS-PLEIADES-CARTE-MERE_P20

Global Project

S7_APP1

Size

11x17

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1.00

Date

24-01-12

Sheet

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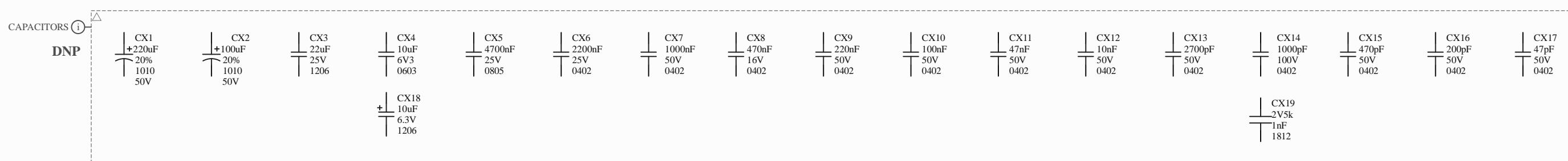
Filename

S7CAS-PLEIADES-CARTE-MERE_P20_Motor.SchDoc

Designers
Florent Cournoyer
Charles Normandeau

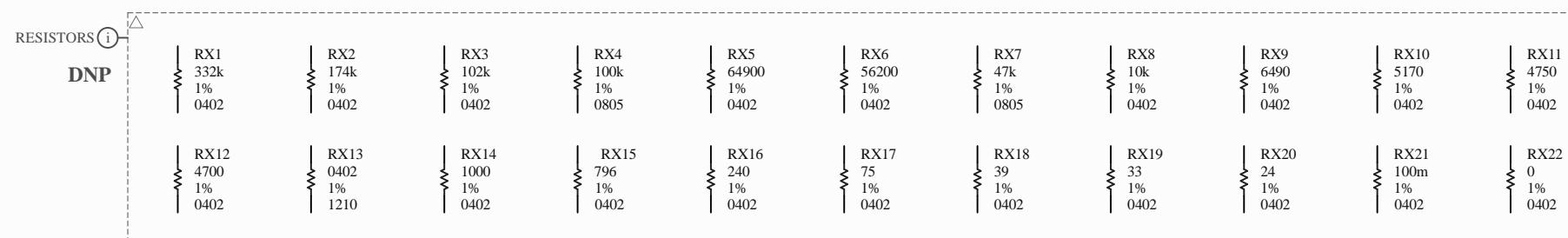
A

CAPACITORS



B

RESISTORS



C

Sheet Name Insert name in Document Parameters		
Project Title S7CAS-PLEIADES-CARTE-MERE_P20		
Global Project S7_APP1		
Size 11x17	Group	Revision P20: couf1001-norc2802
Date 24-01-12	Sheet	20 of 20
Filename S7CAS-PLEIADES-CARTE-MERE_P20_Passive-Components.SchDoc		Designers Florent Cournoyer Charles Normandeau

Board Stack Report

Stack Up		Layer Stack			
Layer	Board Layer Stack	Name	Material	Thickness	Constant
1		Top Paste			
2		Top Overlay			
3		Top Solder	SM-001	2.00mil	4
4		Top Layer	Copper	1.38mil	
5		Dielectric 1	S1170G	3.15mil	4.4
6		Int1 (GND)	Copper	0.69mil	
7		Dielectric 2	S1141	7.87mil	4.6
8		Int2 (Sign)	Copper	0.69mil	
9		Dielectric 3	S1170G	3.15mil	4.4
10		Int3 (GND)	Copper	0.69mil	
11		Dielectric 4	S1141	7.87mil	4.6
12		Int4 (Sign)	Copper	0.69mil	
13		Dielectric 5	S1170G	3.15mil	4.4
14		Int5 (GND)	Copper	0.69mil	
15		Dielectric 6	S1141	7.87mil	4.6
16		Int6 (PWR)	Copper	0.69mil	
17		Dielectric 7	S1170G	3.15mil	4.4
18		Int7 (GND)	Copper	0.69mil	
19		Dielectric 8	S1141	7.87mil	4.6
20		Int8 (GND)	Copper	0.69mil	
21		Dielectric 9	S1170G	3.15mil	4.4
22		Int9 (PWR)	Copper	0.69mil	
23		Dielectric 10	S1141	7.87mil	4.6
24		Int10 (GND)	Copper	0.69mil	
25		Dielectric 11	S1170G	3.15mil	4.4
26		Bottom Layer	Copper	1.38mil	
27		Bottom Solder	SM-001	2.00mil	4
28		Bottom Overlay			
29		Bottom Paste			
	Height : 71.90mil				



MTH3

S7CAS-PLEIADES-CARTE-MERE_P20

S7_APP1

Revision 1.00

Designed by:
Florent Cournoyer
Charles Normandeau

C115
C85
C110
C86
C87
C88
C89
C90
C109
C91
C111
C104 R32
C92
C93
C115
C85
C110
C86
C87
C88
C89
C90
C109
C91
C111
C104 R32
C92
C93

Serial #

R56 R55 R51 R50
D6 D5 D4 D3
C121 S2
R44 R45 C120
S1
R44 C120
S3

