

S7CAS-PLEIADES-CARTE-MERE_P20

S7_APP1

P20: couf1001-norc2802

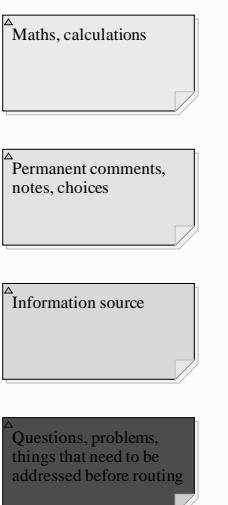
Revision 1.00

Date: 24-01-12

Revision history	

Package size conversion	
Metric	Imperial
1005	0402
1608	0603
2012	0805
3216	1206
3225	1210
6432	2512

Notes Legend



Project Title		
S7CAS-PLEIADES-CARTE-MERE_P20		
Global Project		
S7_APP1		
Size	Group	Revision
11x17	P20: couf1001-norc2802	1.00
Date	Sheet	
24-01-12	1 of 20	
Filename		Designers
S7CAS-PLEIADES-CARTE-MERE_P20_Title.SchDoc		Florent Cournoyer Charles Normandeau

U5 - LDO - TPS7A33 5V_N	
Vin (V)	6.00
Vout (V)	5.00
Iout (ma)	34.90
ADC_OP_AMP	21.60
DAC_OP_AMP	13.30
Pout (mW)	174.50
Eff (%)	0.83
Pdiss (mW)	34.90
Ptot (mW)	209.40

U9 - LDO - TPS7A47 3V3_ANAL	
Vin (V)	5.00
Vout (V)	3.30
Iout (ma)	506.79
PLL_IN_CIRCUIT	75.76
PLL_ANAL	23.03
DAC_AVDD	56.00
ADC_AVDD	318.00
PHY_ANAL	34.00
Pout (mW)	1672.41
Eff (%)	0.66
Pdiss (mW)	861.54
Ptot (mW)	2533.95

U2 - SWR - PTH08T241 3V3_DIGI	
Vin (V)	6.00
Vout (V)	3.30
Iout (ma)	2787.06
PHY_IO	13.00
PHY_OSC	15.00
ETH_LED	6.60
FLASH_PROG	35.00
USB_INT	100.00
USB_ISO	8.00
USB_OCT	25.76
DRV_CTRL	4.00
TEMP_SENS	0.70
I2C	0.66
1V8	629.55
PLL_OUT_DIV	163.64
PLL_LVDS	23.03
PLL_OSC	100.00
1V2_FPGA	1212.12
FPGA_B0	100.00
FPGA_B2	100.00
FPGA_VCCAUX	250
Pout (mW)	9197.30
Eff (%)	0.93
Pdiss (mW)	692.27
Ptot (mW)	9889.57

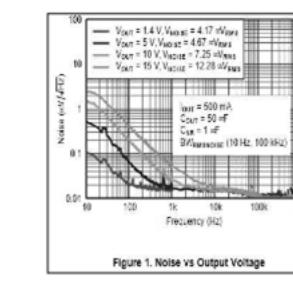
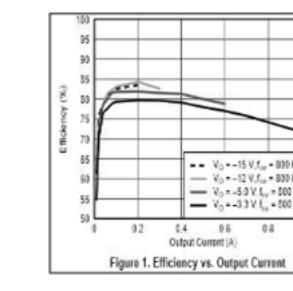
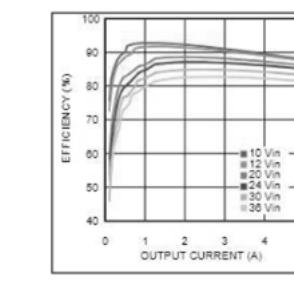
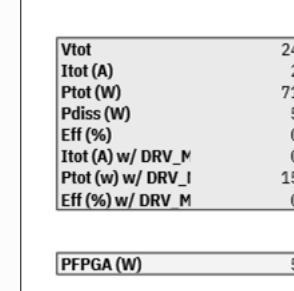
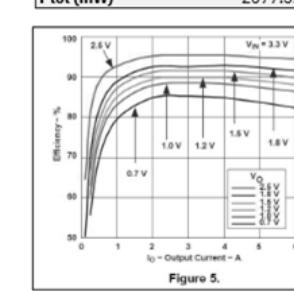
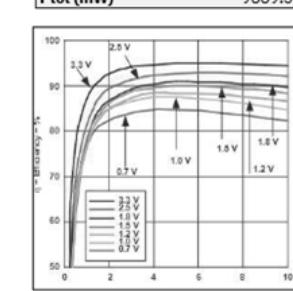
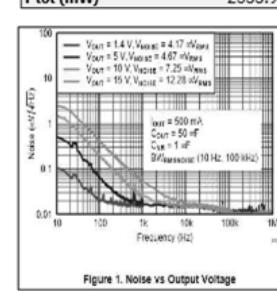
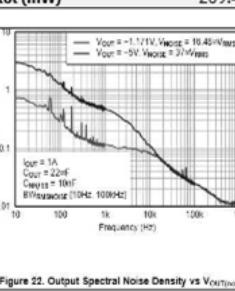
U8 - SWR - PTH04T231 1V8	
Vin (V)	3.30
Vout (V)	1.80
Iout (ma)	981.05
DAC_CVDD	58.00
DAC_DVDD	343.00
1V5	580.05
Pout (mW)	1765.89
Eff (%)	0.85
Pdiss (mW)	311.63
Ptot (mW)	2077.52

PART NUMBER 24V	
Vin (V)	24.00
Vout (V)	24.00
Iout (ma)	2970.79
DRV_THERMAL	261.18
DRV_MOTOR	2073.00
6V	636.61
Pout (mW)	71299.06
Eff (%)	1.00
Pdiss (mW)	0.00
Ptot (mW)	71299.06

U3 - SWR - LMZ23605 6V	
Vin (V)	24.00
Vout (V)	6.00
Iout (ma)	2189.95
6V_N	41.06
5V_ANAL	541.69
3V3_DIGI	1648.26
Pout (mW)	13139.71
Eff (%)	1.00
Pdiss (mW)	0.00
Ptot (mW)	15278.74

U4 - SWR INV - LMZ34002 6V_N	
Vin (V)	6.00
Vout (V)	6.00
Iout (ma)	34.90
ADC_OP_AMP	21.60
DAC_OP_AMP	13.30
3V3_ANAL	506.79
Pout (mW)	209.40
Eff (%)	0.85
Pdiss (mW)	36.95
Ptot (mW)	246.35

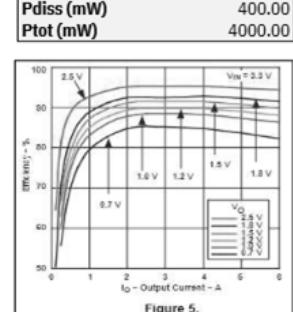
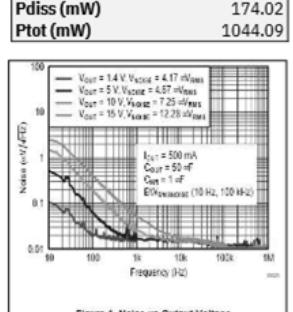
U1 - LDO - TPS7A47 5V_ANAL	
Vin (V)	6.00
Vout (V)	5.00
Iout (ma)	541.69
ADC_OP_AMP	21.60
DAC_OP_AMP	13.30
3V3_ANAL	506.79
Pout (mW)	2708.45
Eff (%)	0.83
Pdiss (mW)	541.69
Ptot (mW)	3250.14



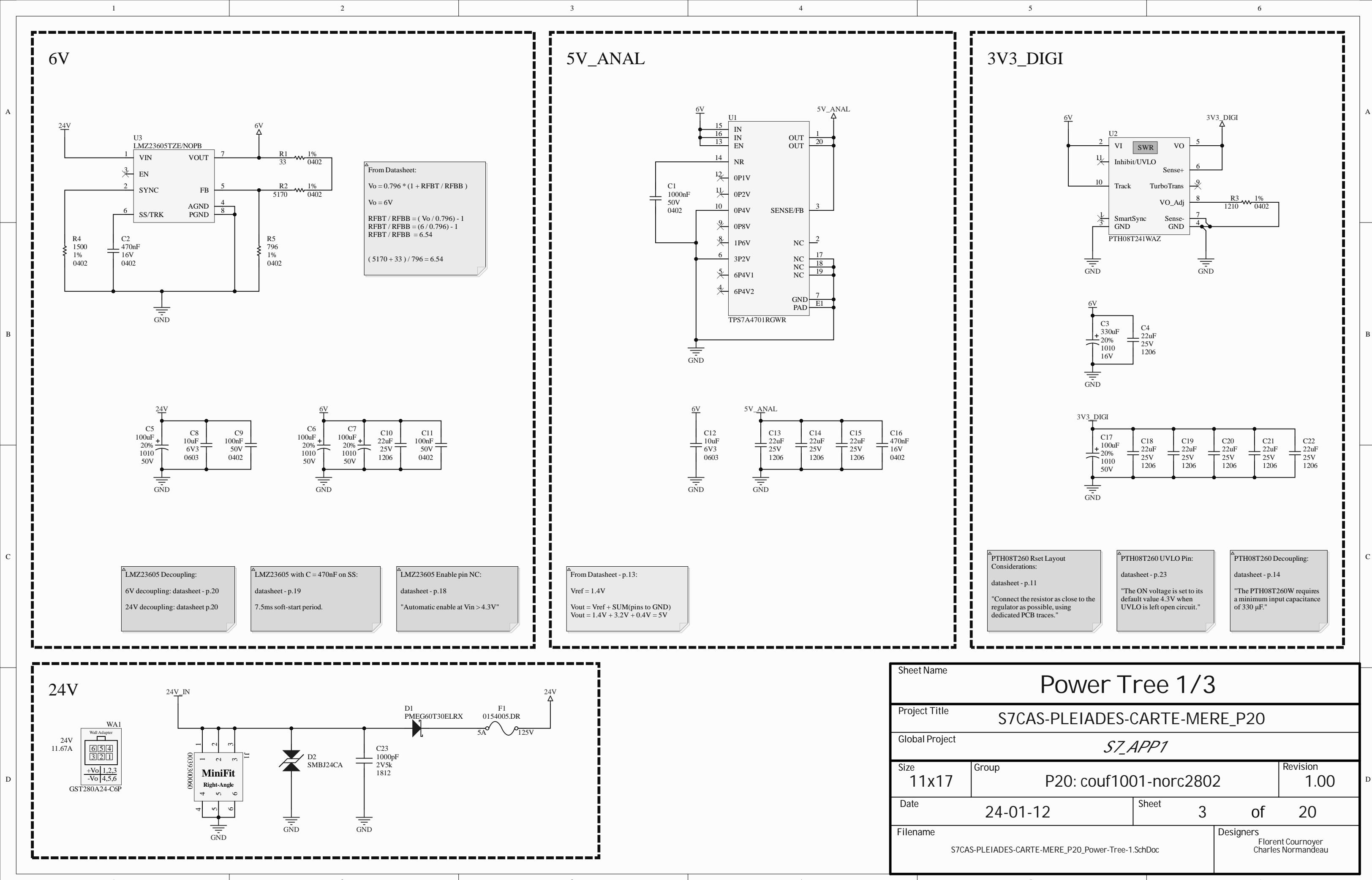
U10 - LDO - TPS7A47 1V5	
Vin (V)	1.80
Vout (V)	1.50
Iout (ma)	580.05
FPGA_B3	300.00
DDR3	181.53
TPS	0.05
0V75	98.47
Pout (mW)	870.08
Eff (%)	0.83
Pdiss (mW)	174.02
Ptot (mW)	1044.09

U7 - SWR - PTH04T231 1V2_FPGA	
Vin (V)	3.30
Vout (V)	1.20
Iout (ma)	3000.00
FPGA_VCCINT	3000.00
Pout (mW)	3600.00
Eff (%)	0.90
Pdiss (mW)	400.00
Ptot (mW)	4000.00

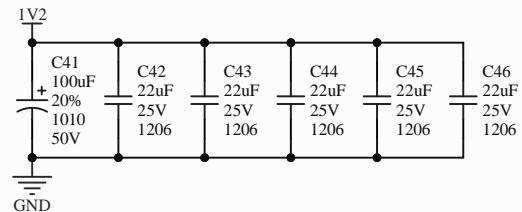
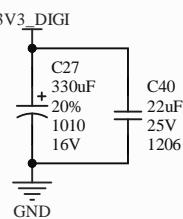
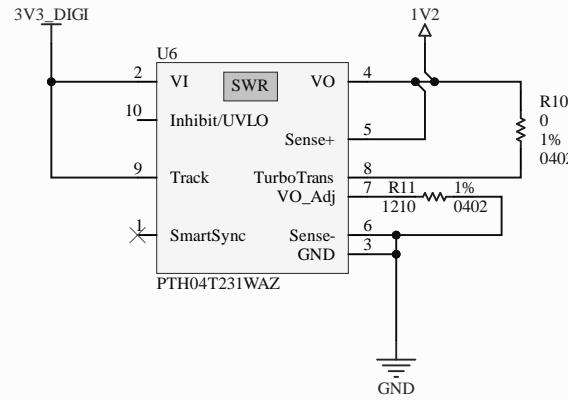
U11 - LDO - TPS51200 0V75	
Vin (V)	1.50
Vout (V)	0.75
Iout (ma)	98.47
RTT	98.47
Pout (mW)	73.85
Eff (%)	0.50
Pdiss (mW)	73.85
Ptot (mW)	147.71



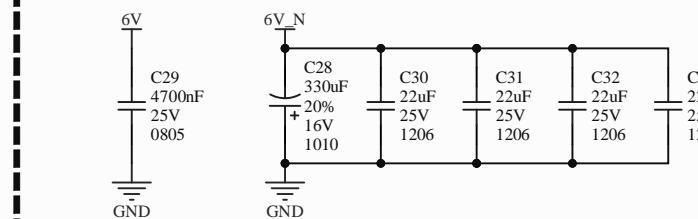
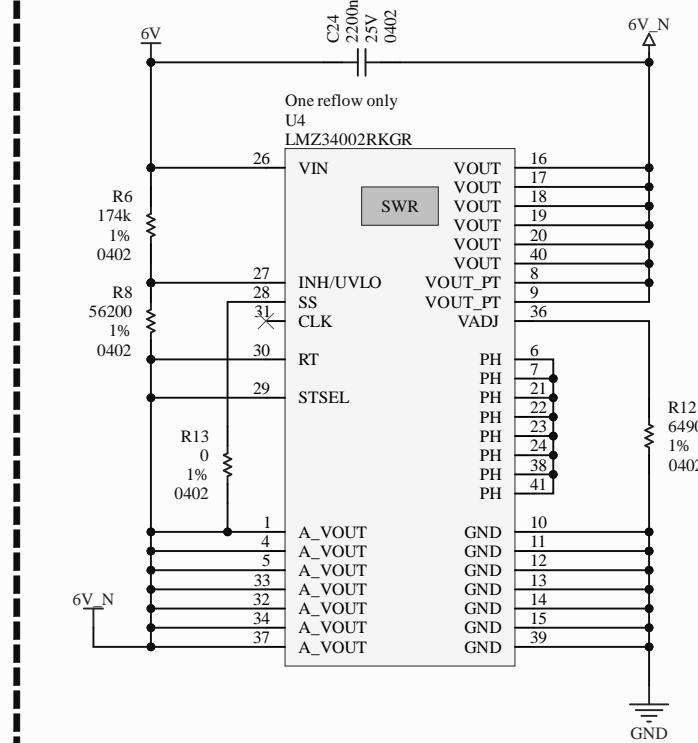
Sheet Name	Power Tree Analysis		
Project Title	S		



1V2

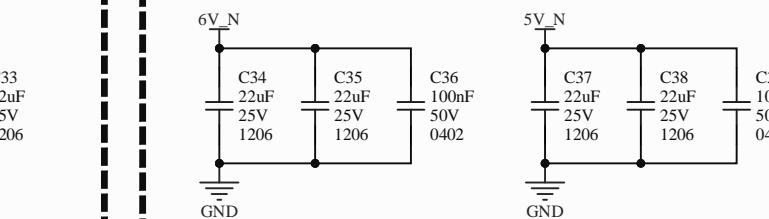
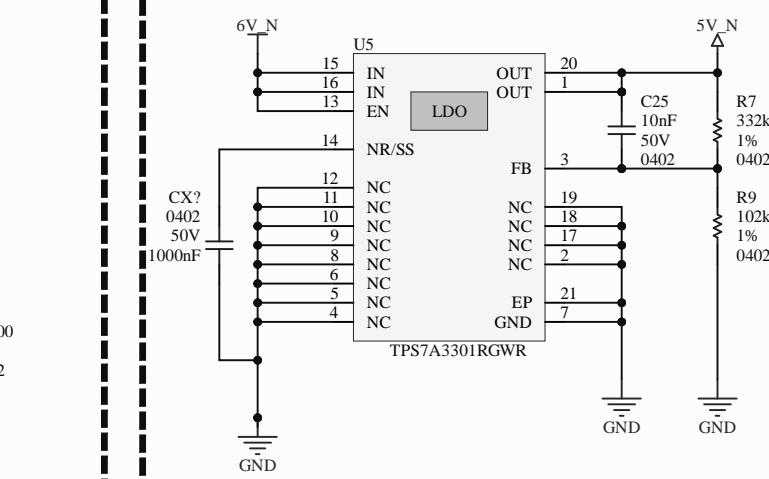


6V_N



[△]LMZ34002RKGR Clock:
datasheet - p.6
"Isolate from any other signal."

5V_N



[△]TPS7A3301RGWR Layout Considerations
datasheet - p.4
"... recommends connecting a 10nF capacitor from FB to OUT as close to the device as possible."

Sheet Name

Power Tree 2/3

Project Title

S7CAS-PLEIADES-CARTE-MERE_P20

Global Project

S7_APP1

Size

11x17

Group

P20: couf1001-norc2802

Revision

1.00

Date

24-01-12

Sheet

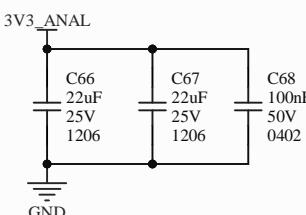
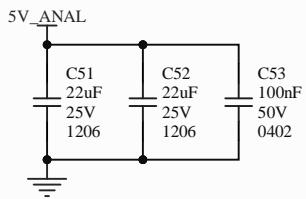
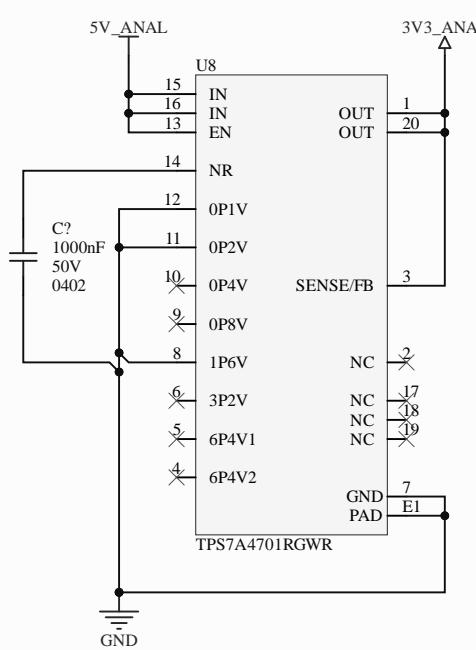
4 of 20

Filename

S7CAS-PLEIADES-CARTE-MERE_P20_Power-Tree-2.SchDoc

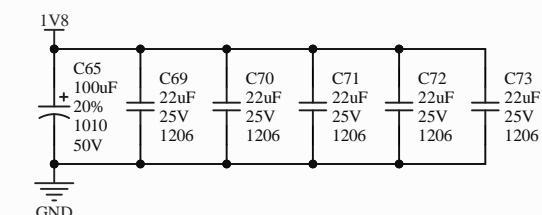
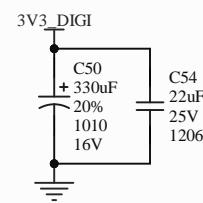
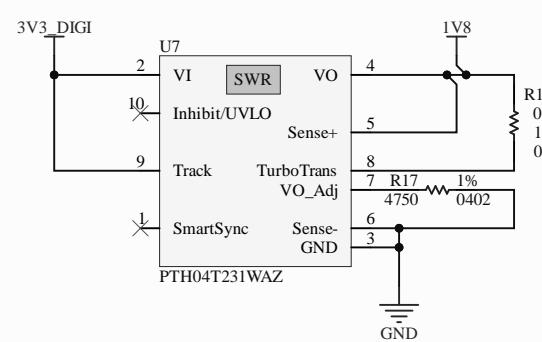
Designers
Florent Cournoyer
Charles Normandeau

3V3_ANAL

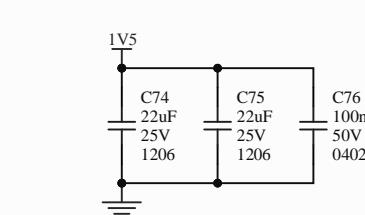
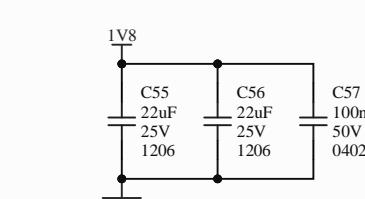
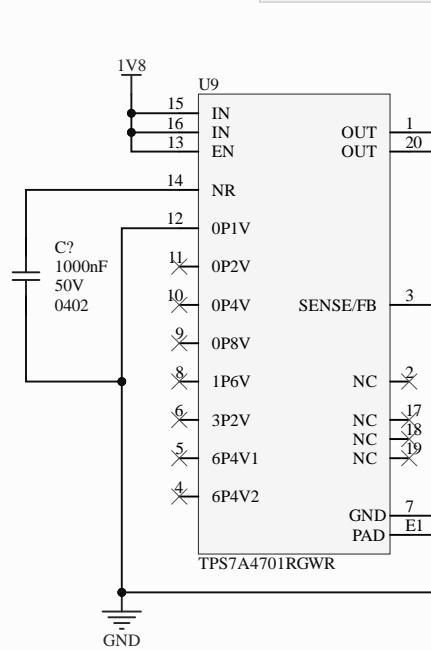


WHAT TO DO WITH
SENSE

1V8



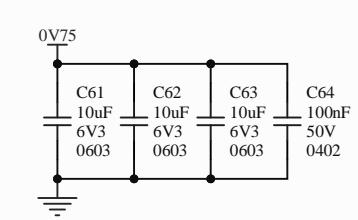
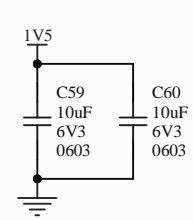
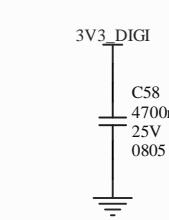
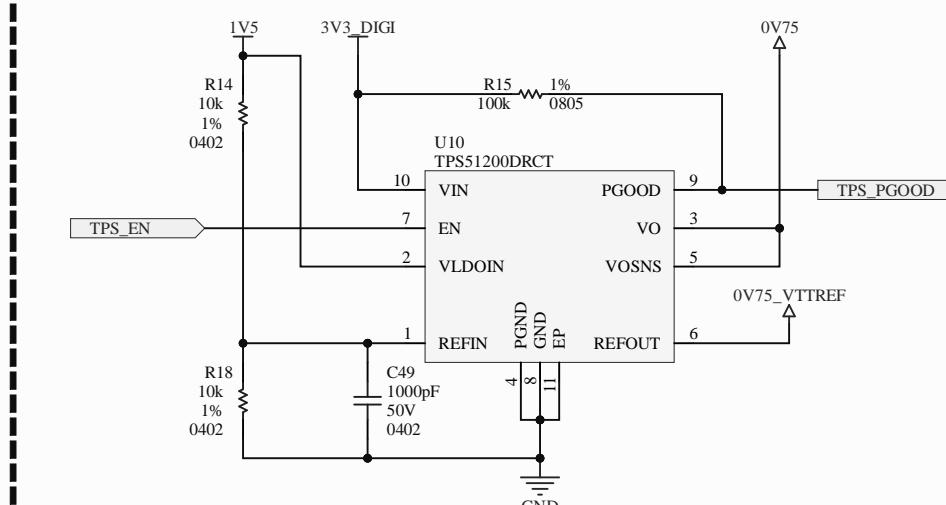
1V5



From Datasheet - p.13:
Vref = 1.4V

Vout = Vref + SUM(pins to GND)
Vout = 1.4V + 0.1V = 1.5V

0V75



TPS5 BOM:
datasheet - p.17
BOM is only for 3.3V which is why we choose 3.3V over 2.5V

TPS5 Pin EN:
desing note - LINK BELOW
"Chip enable can use random FPGA IO."

Sheet Name

Power Tree 3/3

Project Title

S7CAS-PLEIADES-CARTE-MERE_P20

Global Project

S7_APP1

Size

11x17

Group Revision

P20: couf1001-norc2802

1.00

Date

24-01-12

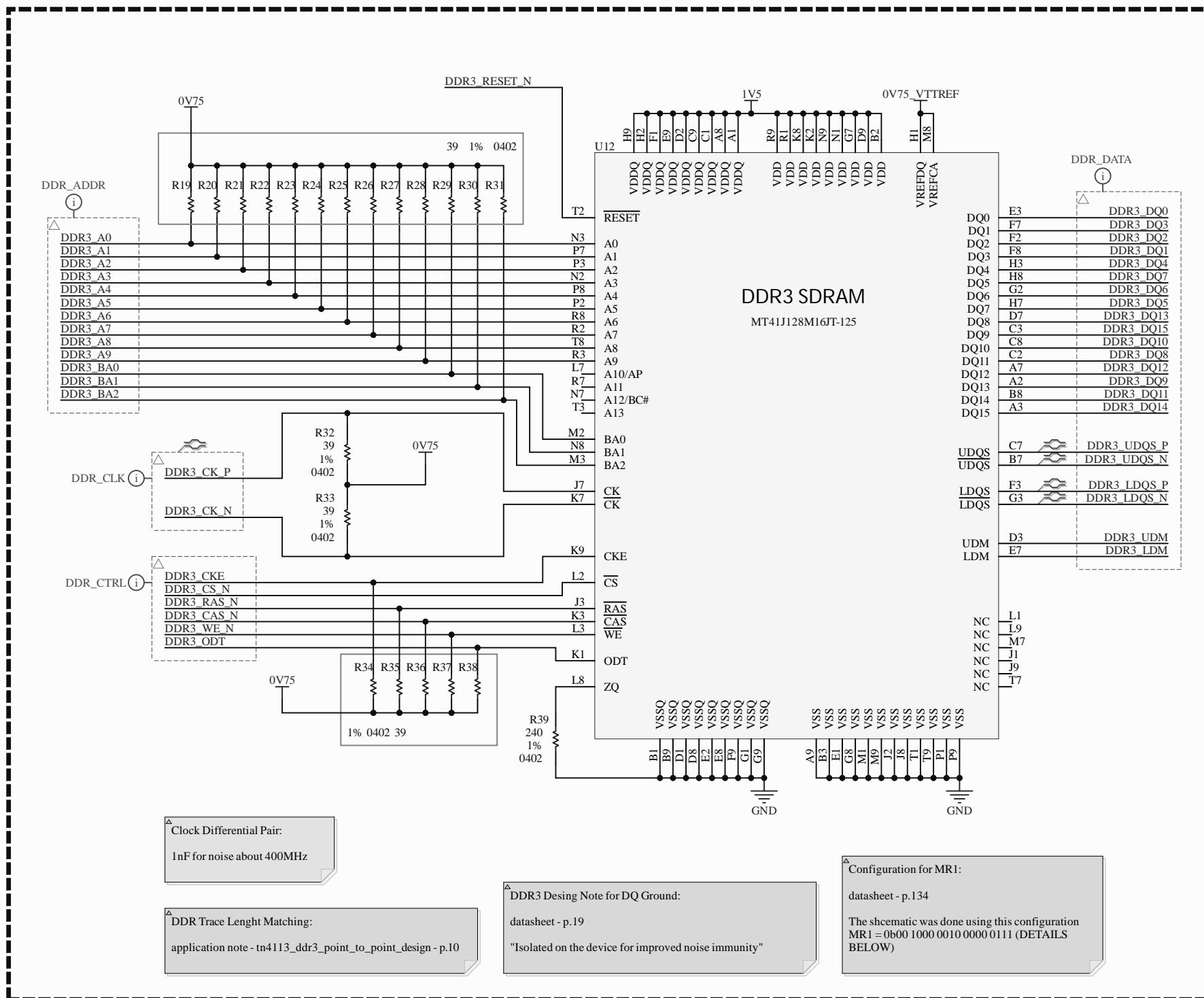
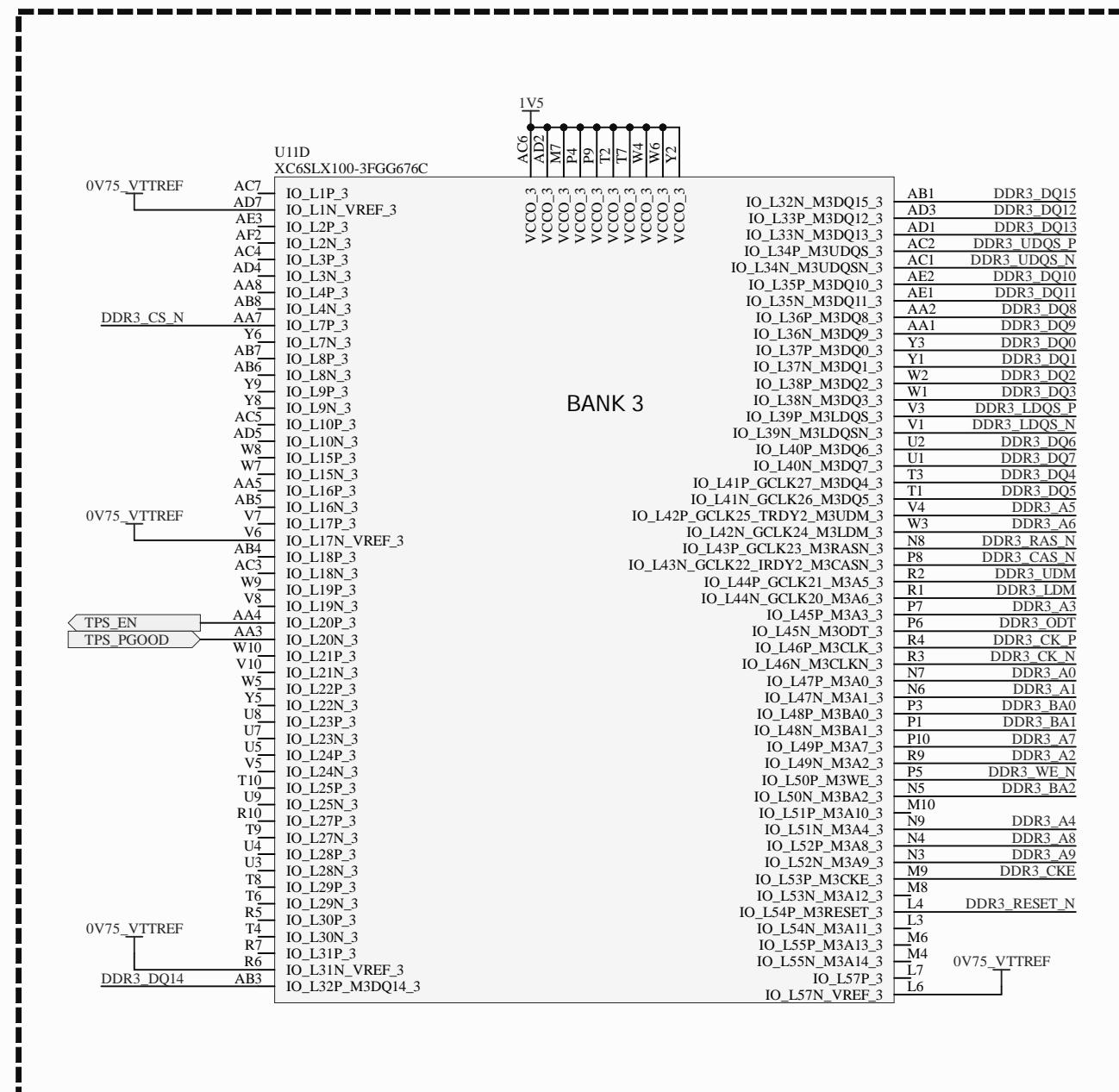
Sheet

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Filename

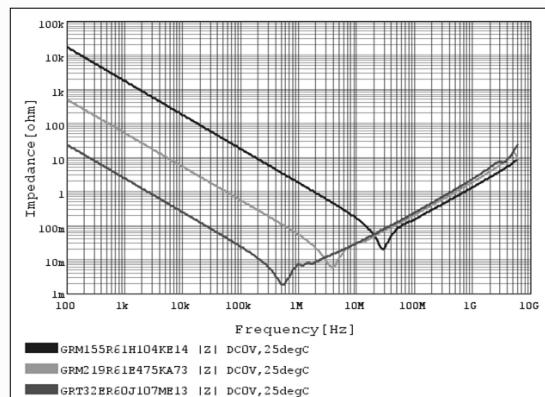
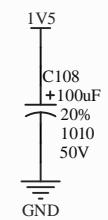
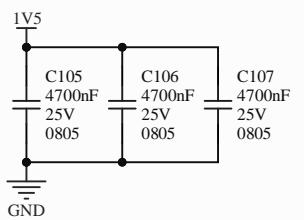
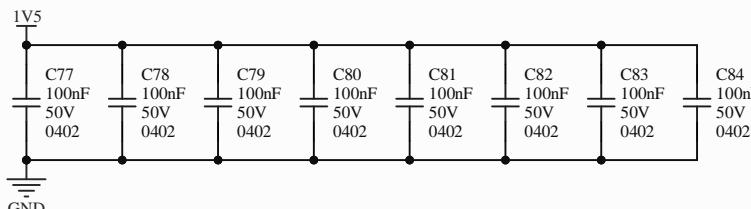
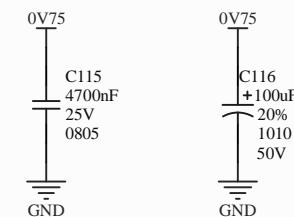
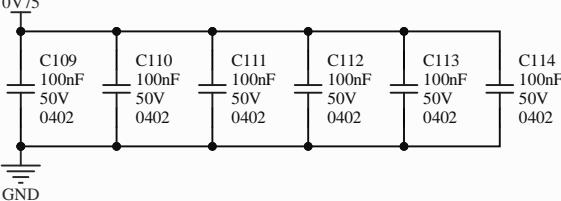
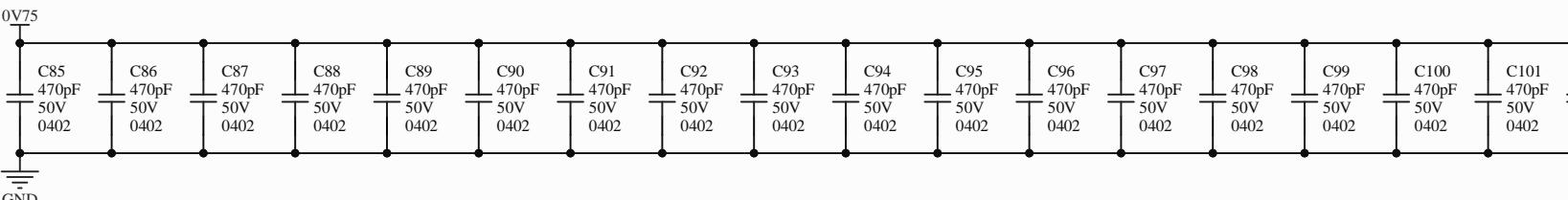
S7CAS-PLEIADES-CARTE-MERE_P20_Power-Tree-3.SchDoc

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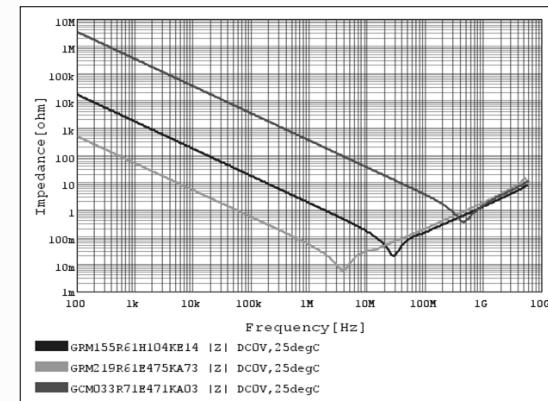
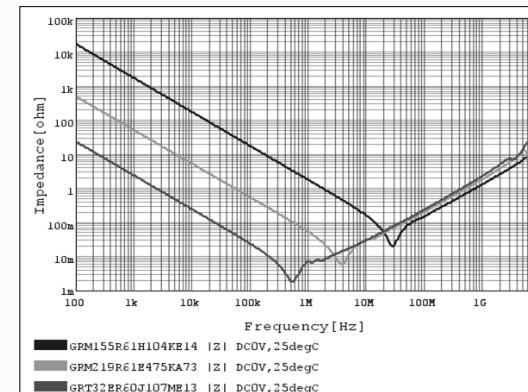
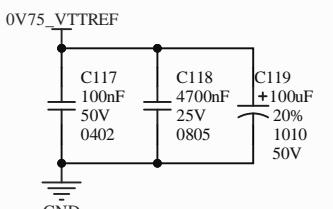


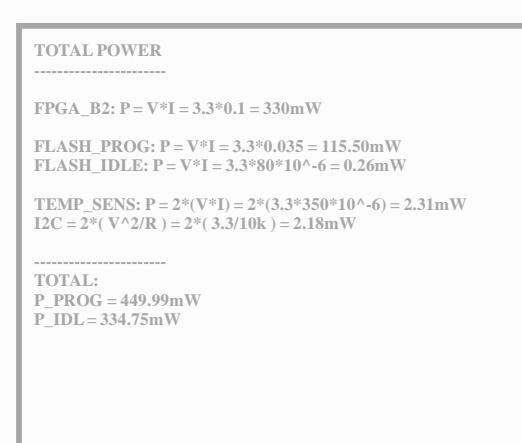
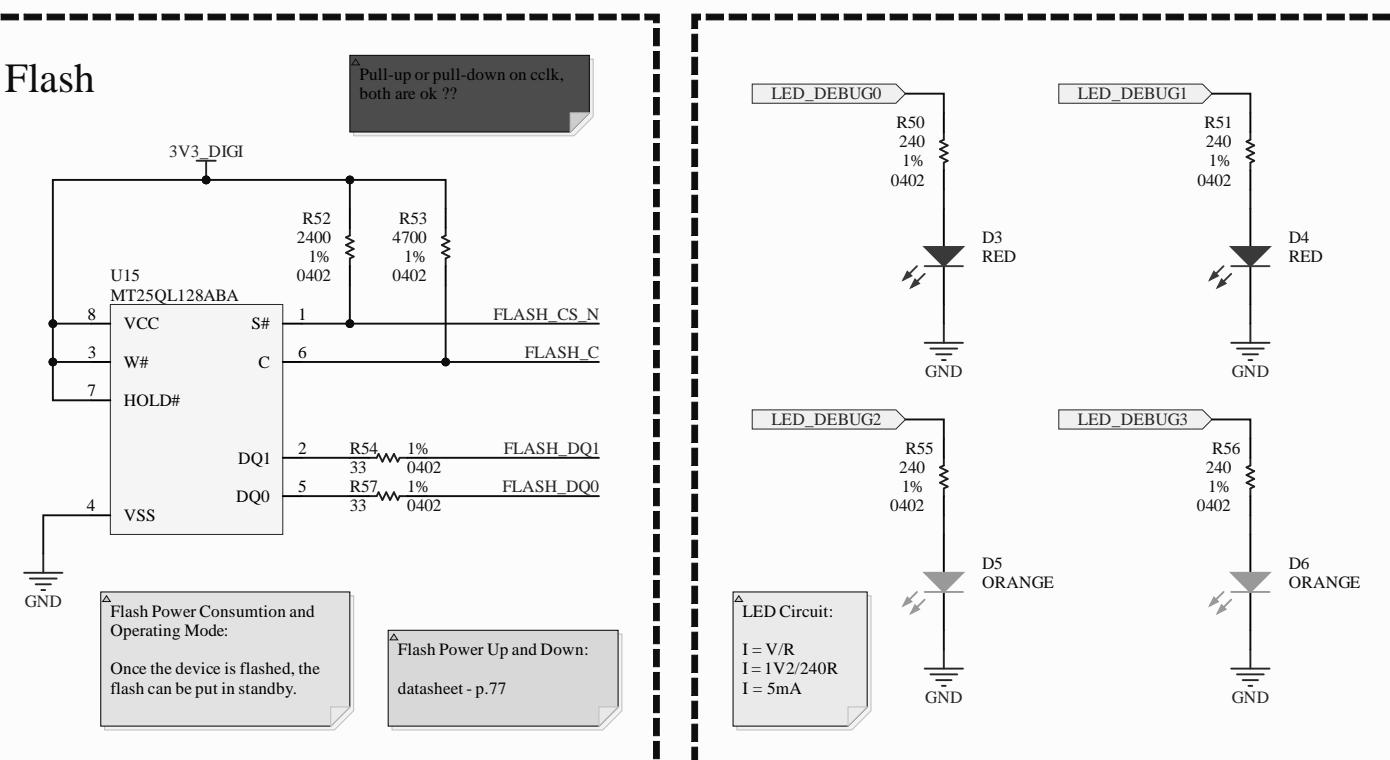
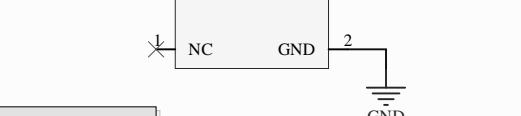
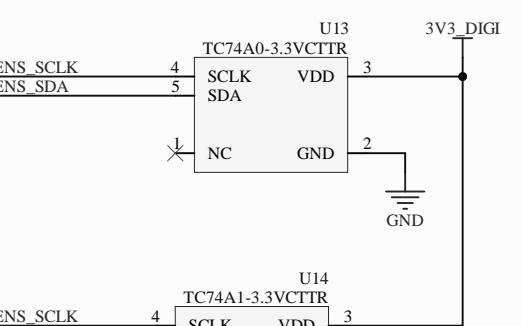
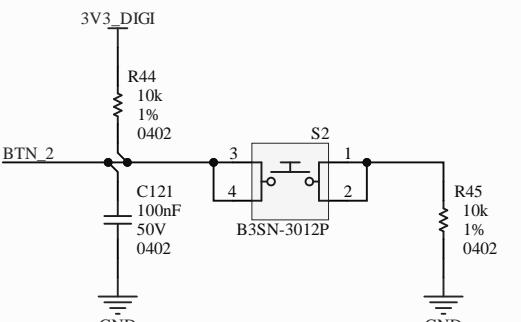
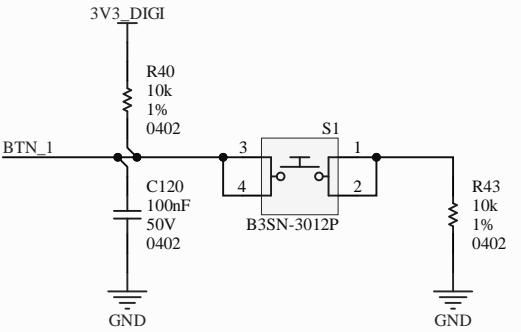
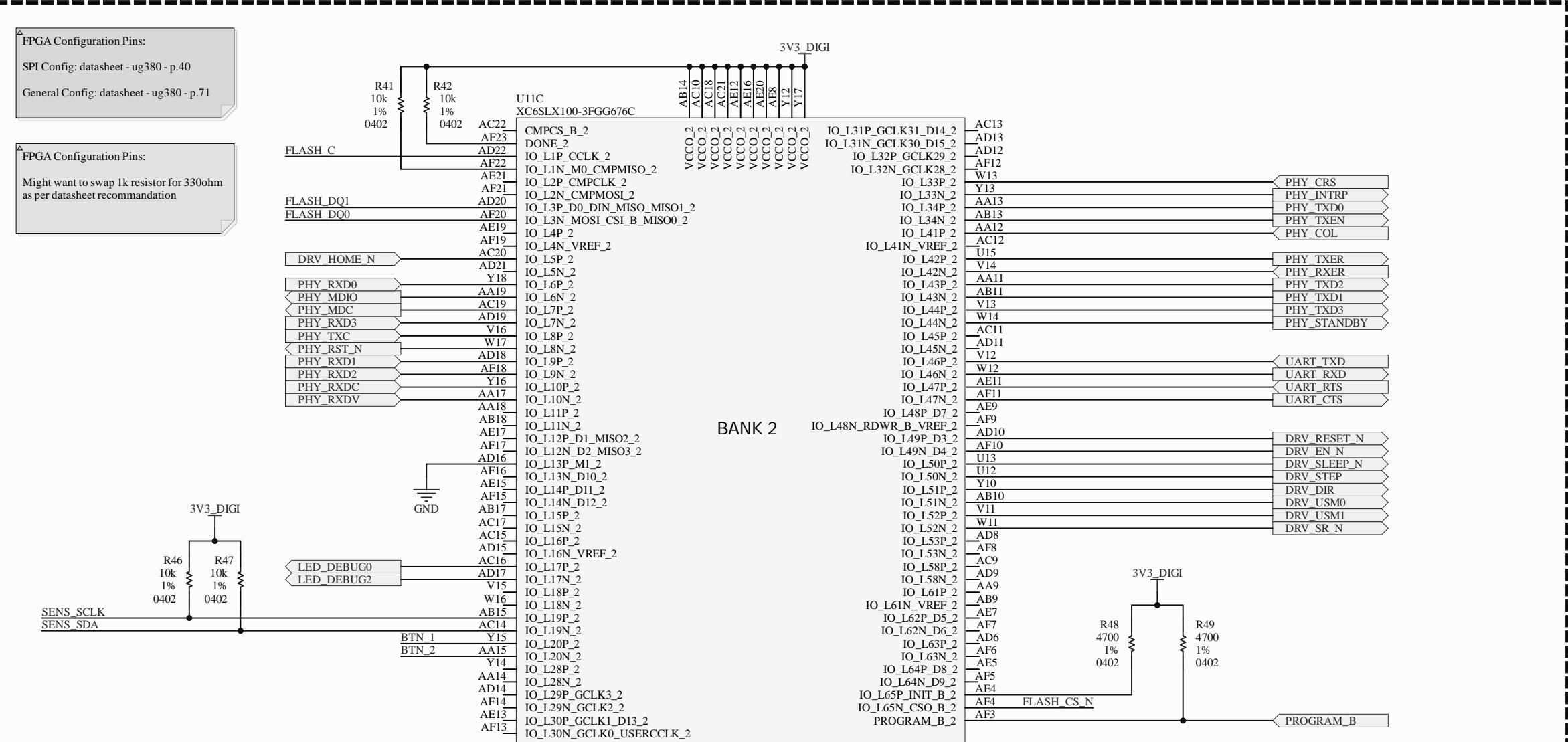
TOTAL POWER	
$R_{TT}: P = NB * (V * V / R) = 18 * (0.4 * 0.4 / 39) = 73.85\text{mW}$	
$FPGA_B3: P = V * I = 1.5 * 0.3 = 450.00\text{mW}$	
$DDR3: P = 272.30\text{mW}$	
$TOTAL: P = 824.95\text{mW}$	

Sheet Name		Project Title	
		S7CAS-PLEIADES-CARTE-MERE_P20	
Global Project		S7_APP1	
Size	Group	P20: couf1001-norc2802	Revision
11x17			1.00
Date	Sheet	24-01-12	6 of 20
Filename	Designers	S7CAS-PLEIADES-CARTE-MERE_P20_DDR3-FPGA-Bank-3.SchDoc	Florent Cournoyer Charles Normandeau

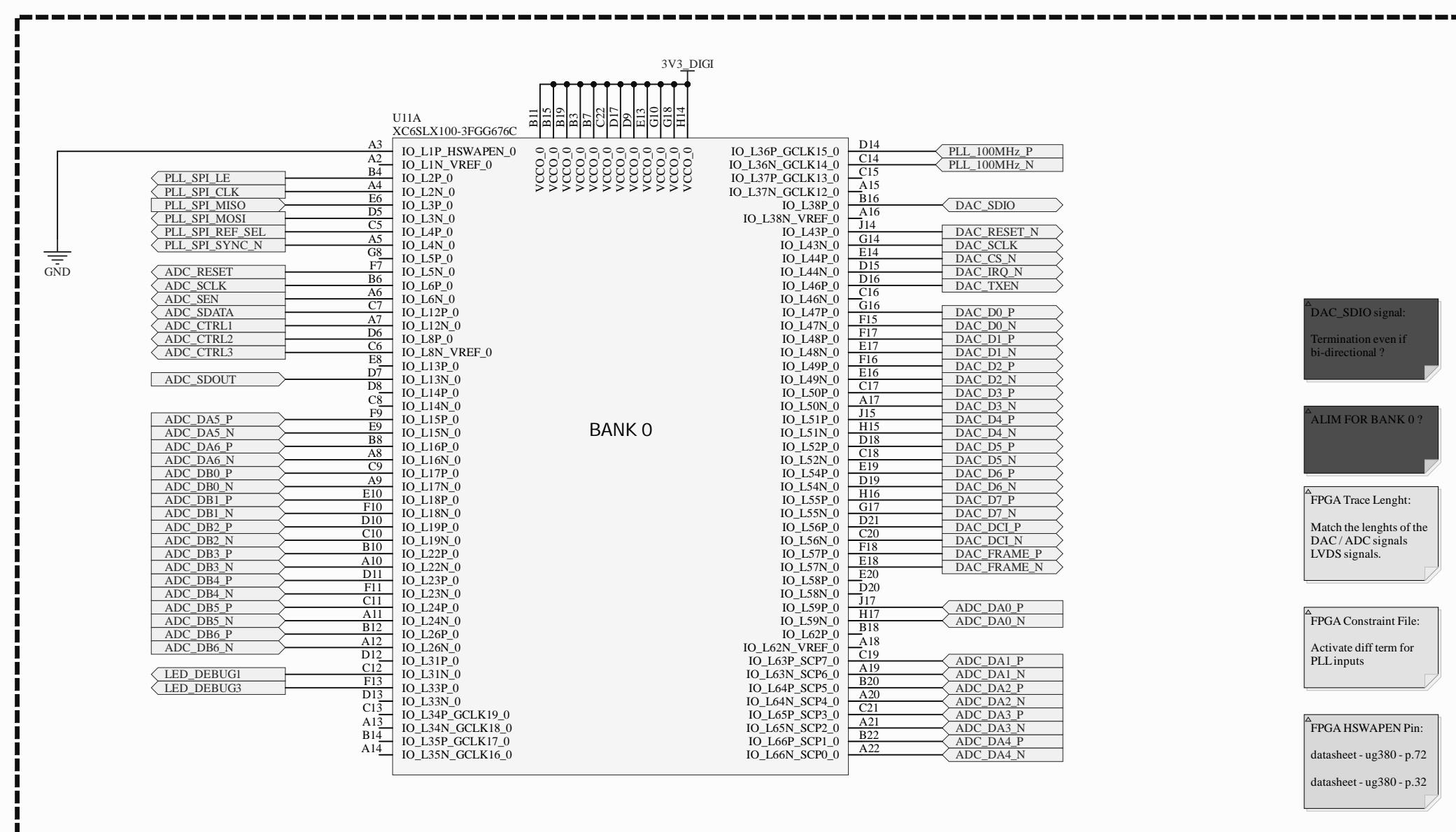
1V5_VDD**0V75**

VTT Cap Placement:
470pF: 1 per pin
100nF: 1 per 3 pin

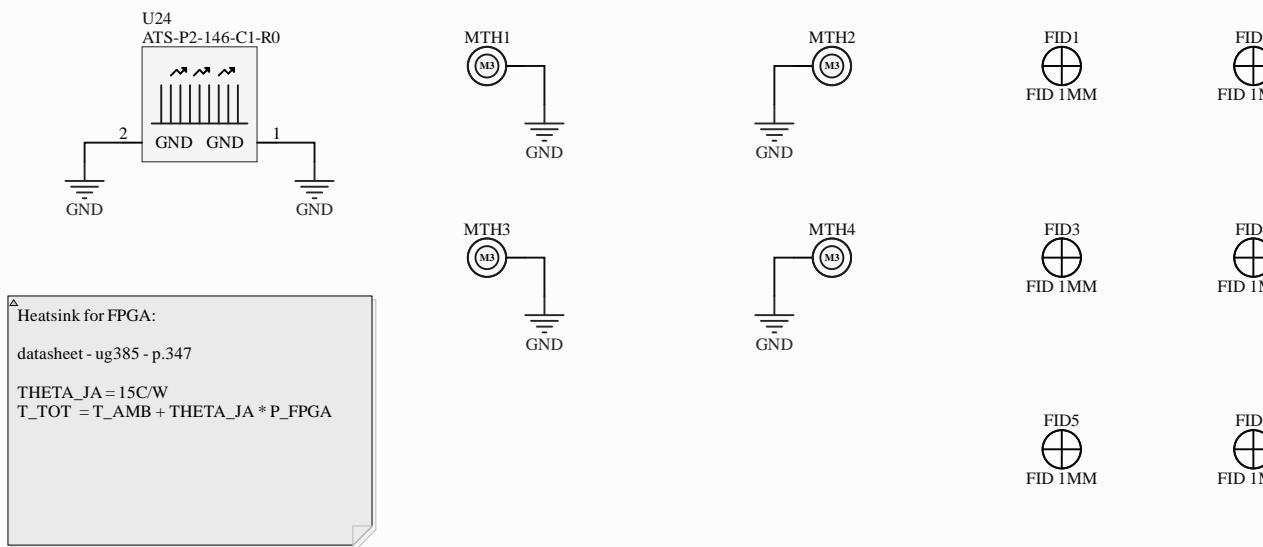
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Charles Normandeau**



Sheet Name	Flash Sensors FPGA Bank 2		
Project Title	S7CAS-PLEIADES-CARTE-MERE_P20		
Global Project	<i>S7APP1</i>		
Size	Group	P20: couf1001-norc2802	Revision
11x17			1.00
Date	24-01-12	Sheet 8	of 20
Filename	S7CAS-PLEIADES-CARTE-MERE_P20_Flash-Sensors-FPGA-bank-2.SchDoc	Designers	Florent Cournoyer Charles Normandeau

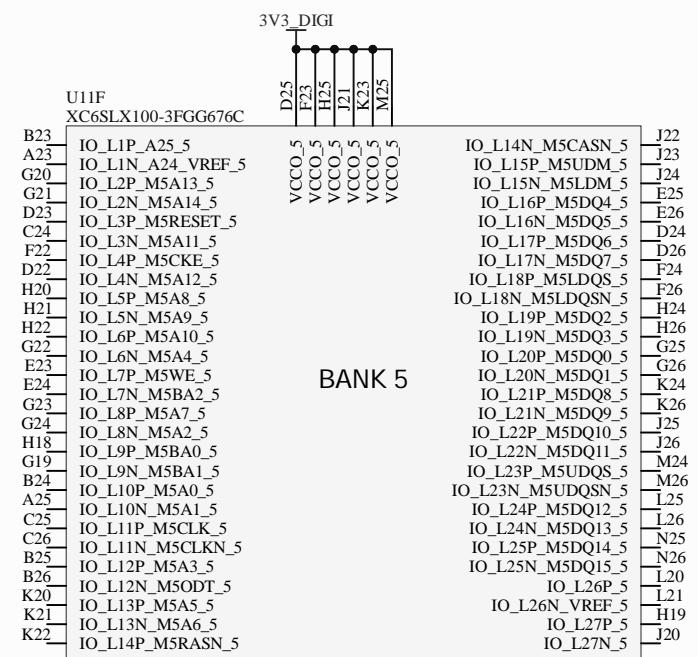
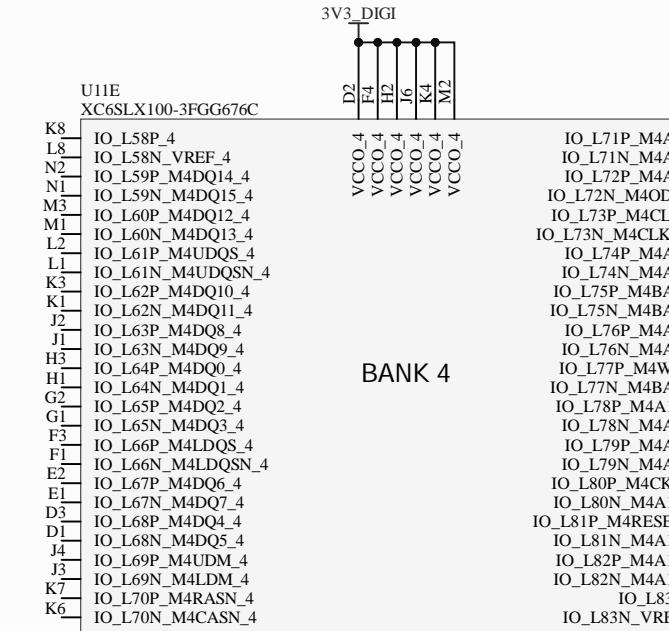
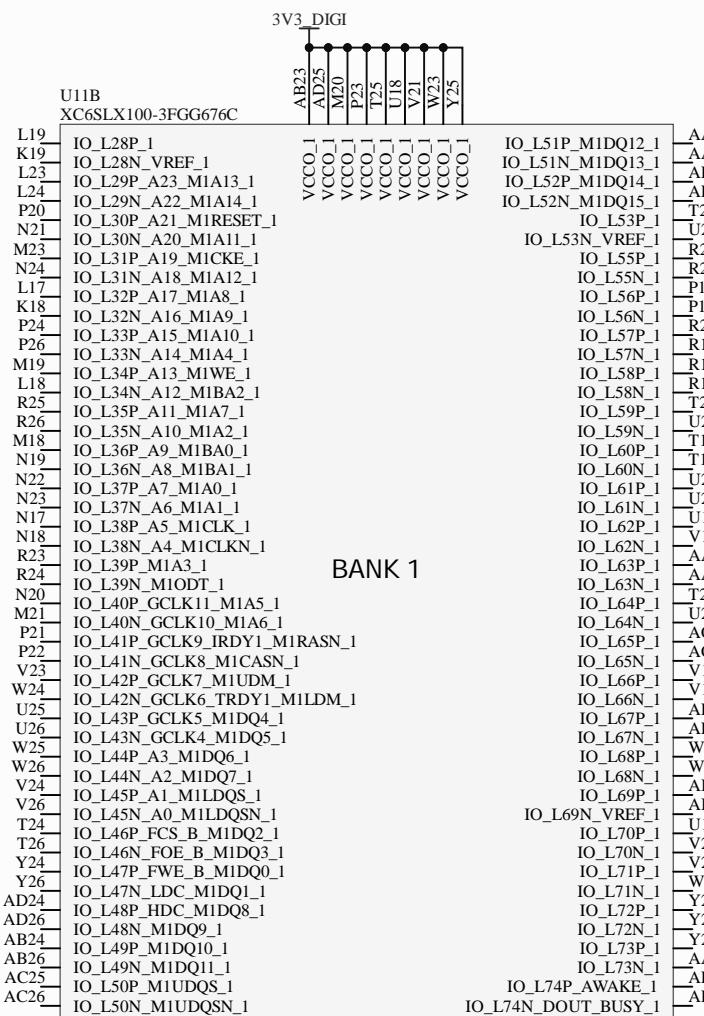


Mechanical



TOTAL POWER	
$P_{\text{FPGA_B0}}: P = V * I = 3.3 * 0.1 = 330\text{mW}$	
TOTAL: $P = 330\text{mW}$	

Sheet Name		Mechanical FPGA Bank 0	
Project Title		S7CAS-PLEIADES-CARTE-MERE_P20	
Global Project		S7_APP1	
Size	11x17	Group	Revision
Date	24-01-12	Sheet	1.00
Filename	S7CAS-PLEIADES-CARTE-MERE_P20_Mechanical-FPGA-Bank-0.SchDoc	Designers	Florent Cournoyer Charles Normandeau



FPGA Unused Banks

Project Title S7CAS-PI FIADES-CARTE-MERE P20

Global Project

CZ_4881

ze

D20: couf1001_norc2802

Revision

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24.01.12

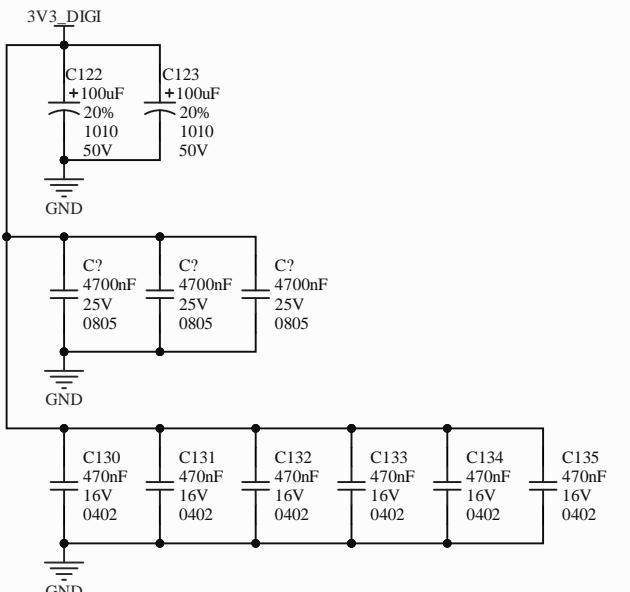
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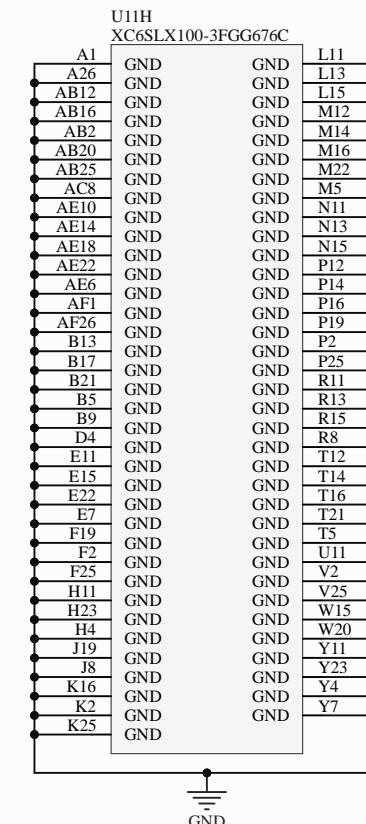
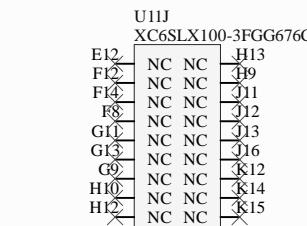
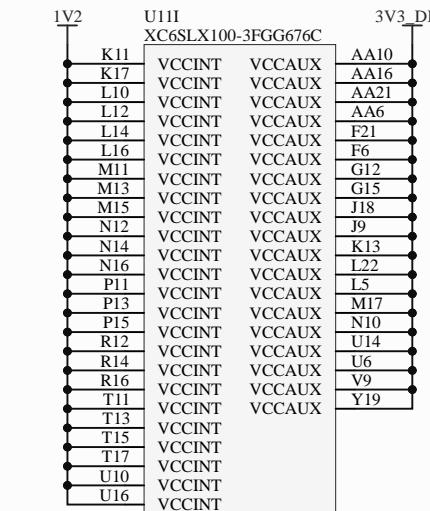
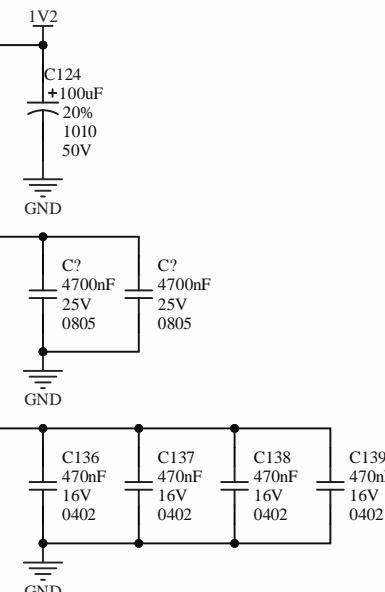
S7CAS PLEIADES CARTE MERÉ P20 ERCA Unused Banks SchDoc

Designers
Florent Cournoyer
Charles Normandeau

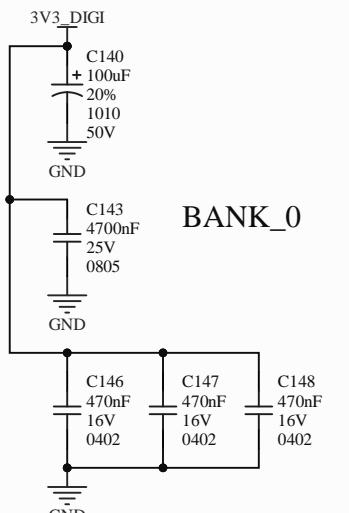
VCCAUX



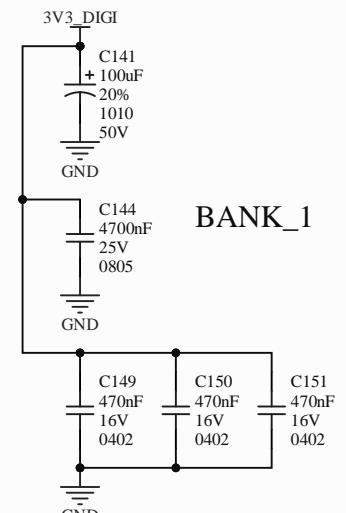
VCCINT



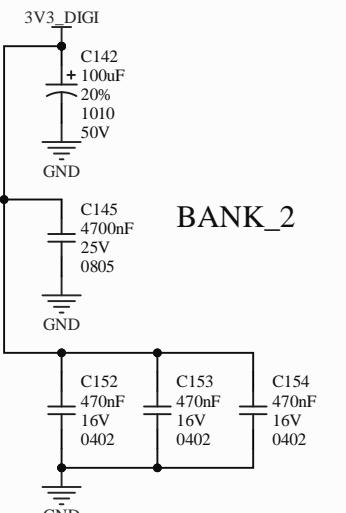
VCO



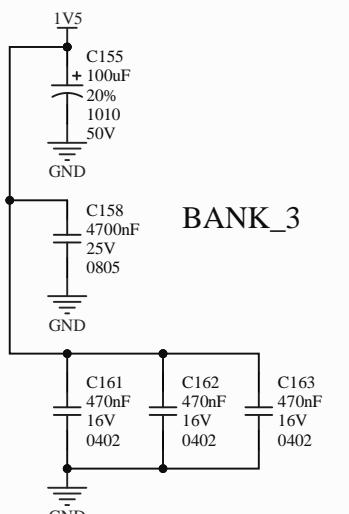
BANK_0



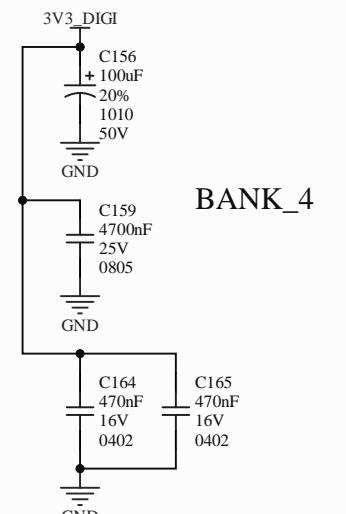
BANK_1



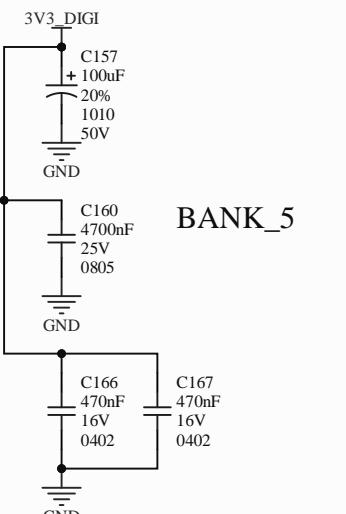
BANK_2



BANK_3



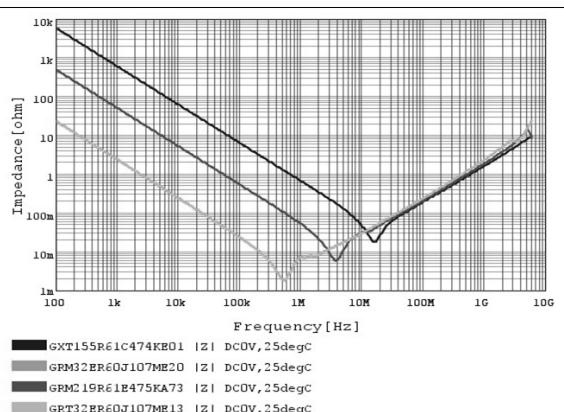
BANK_4



BANK_5

FPGA Capacitor Placement Rules:
datasheet - ug393 - p.17-20
100uF : "As close as possible of the FPGA, but can be anywhere on the PCB."
4.7uF : "As close as possible of the FPGA within 2 inches of the FPGA outer edge."
0.47uF : "Mounted on the PCB backside within the FPGA footprint."

Replacement For Discontinued Parts



Sheet Name

FPGA Decoupling

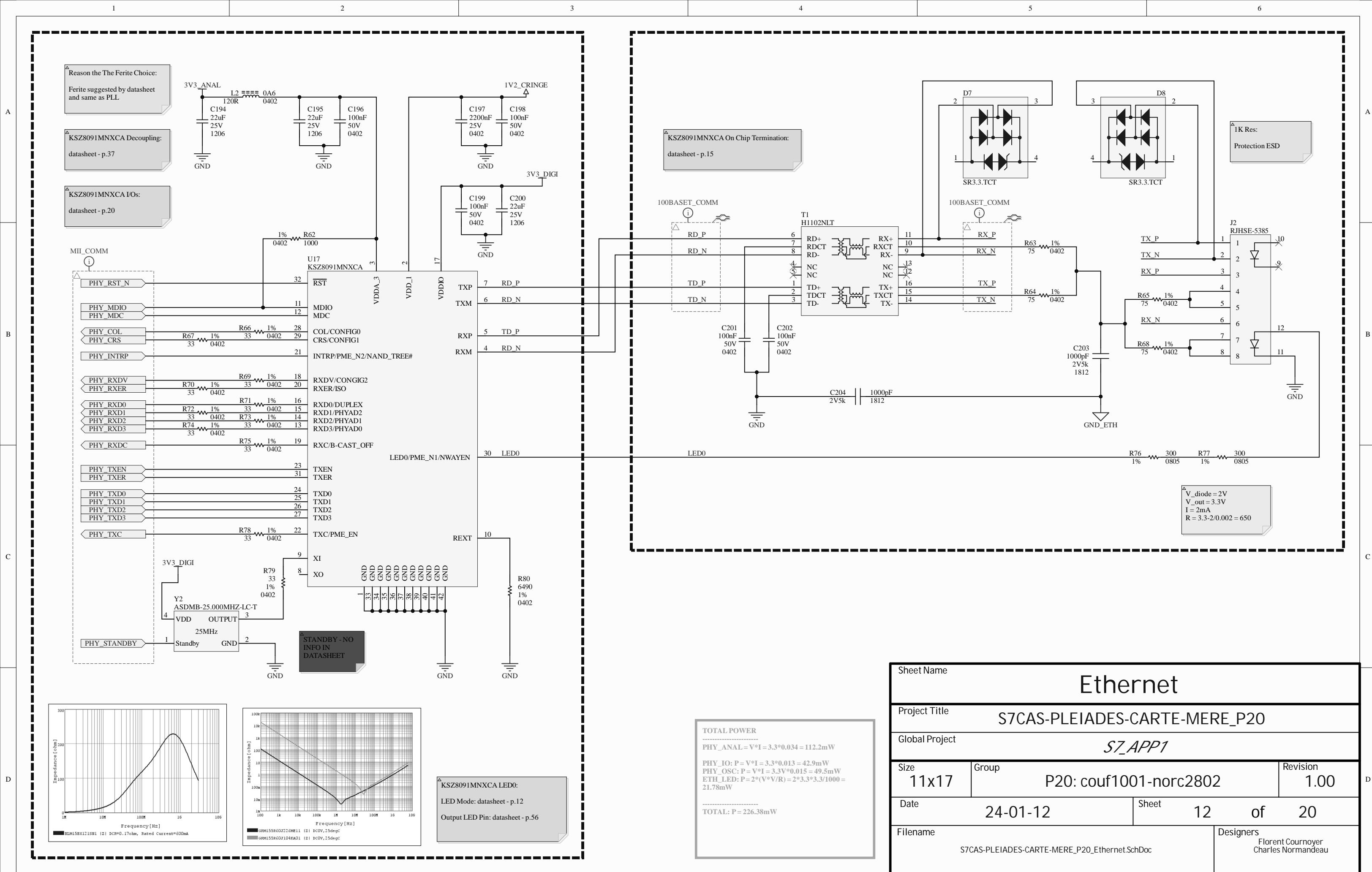
Project Title S7CAS-PLEIADES-CARTE-MERE_P20

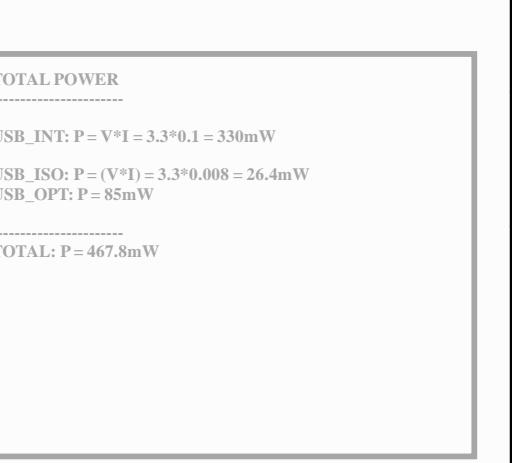
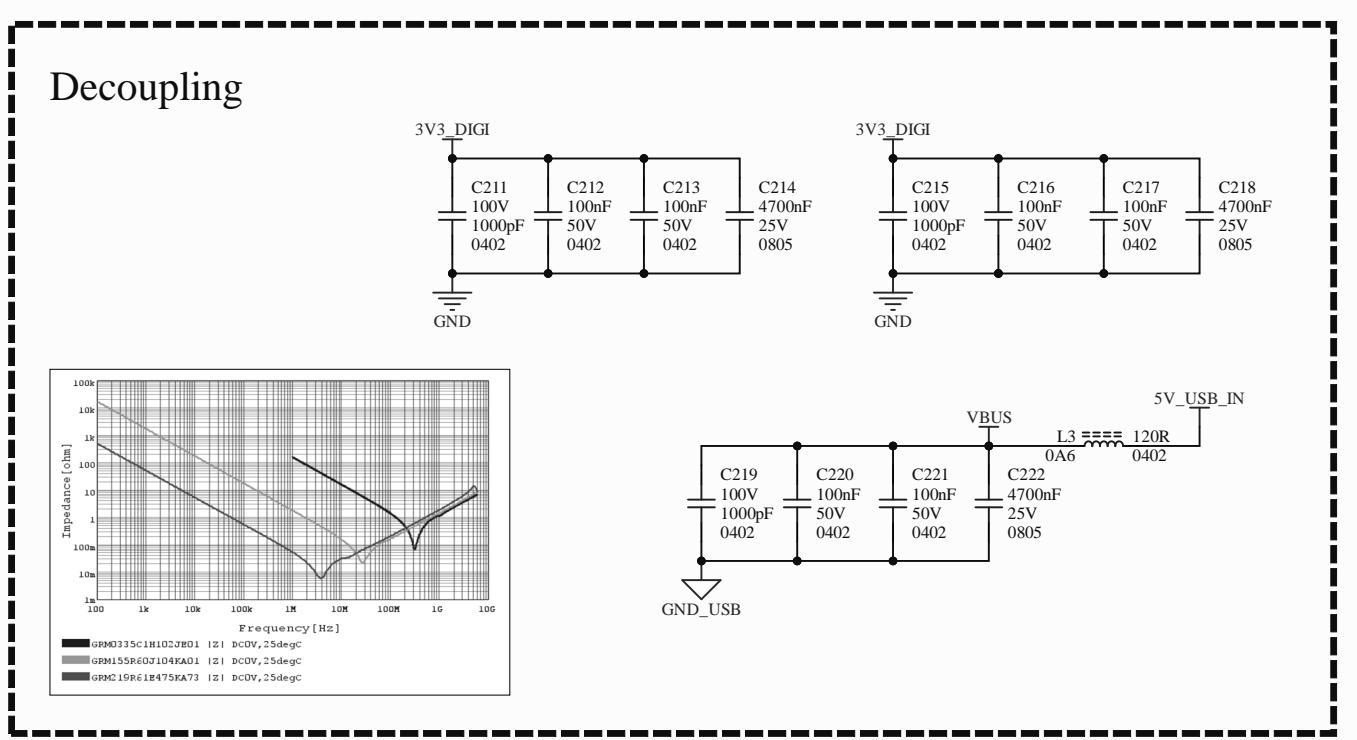
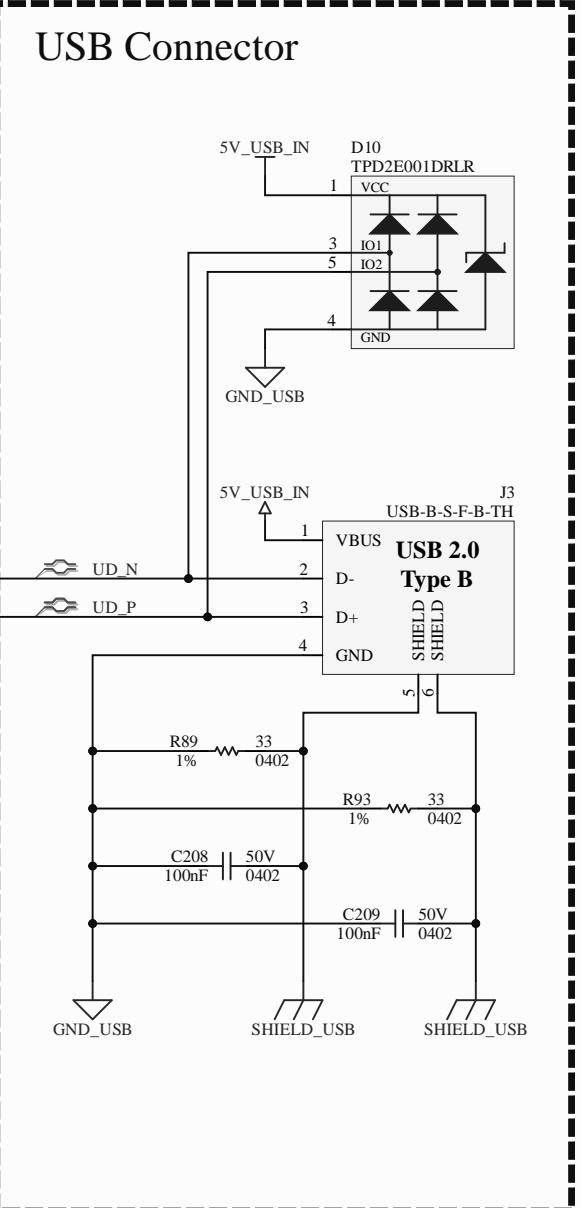
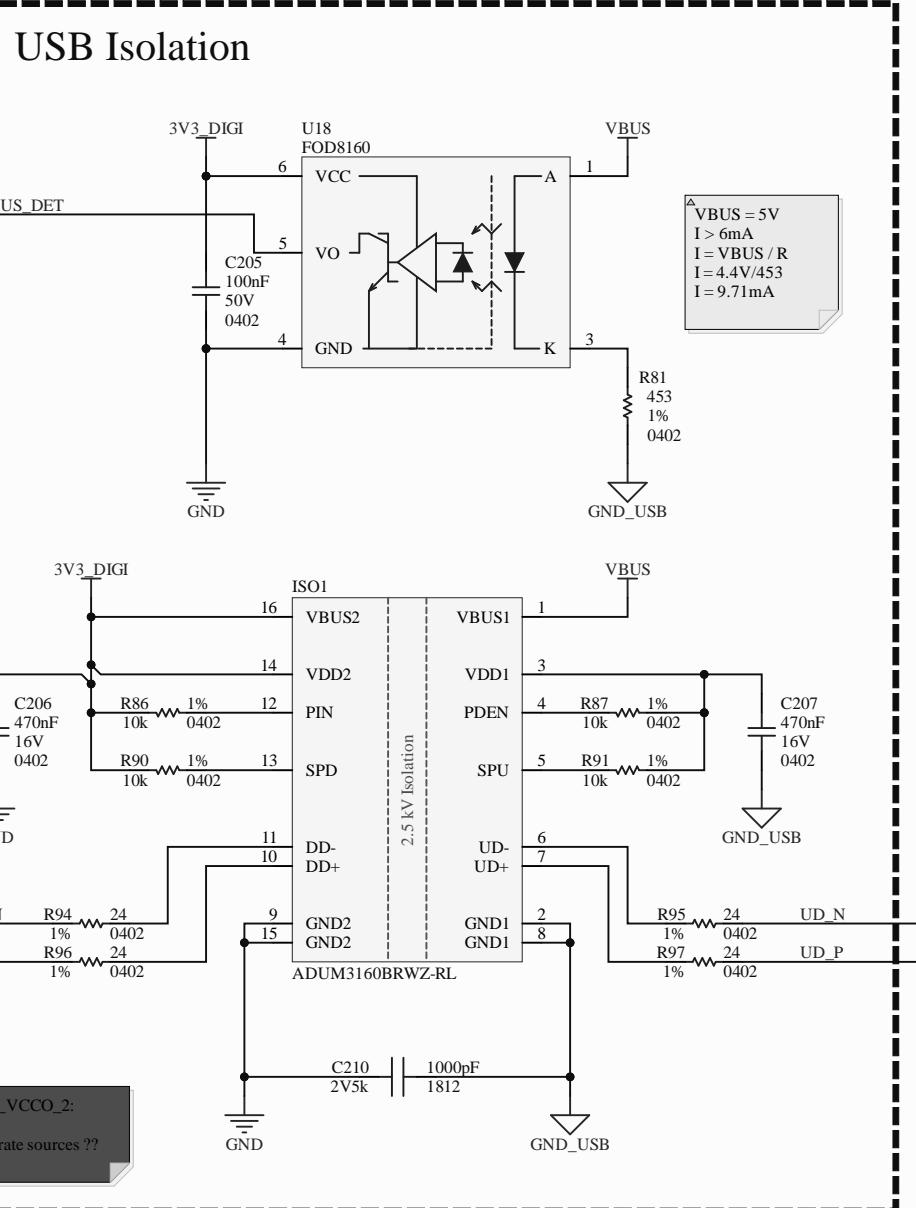
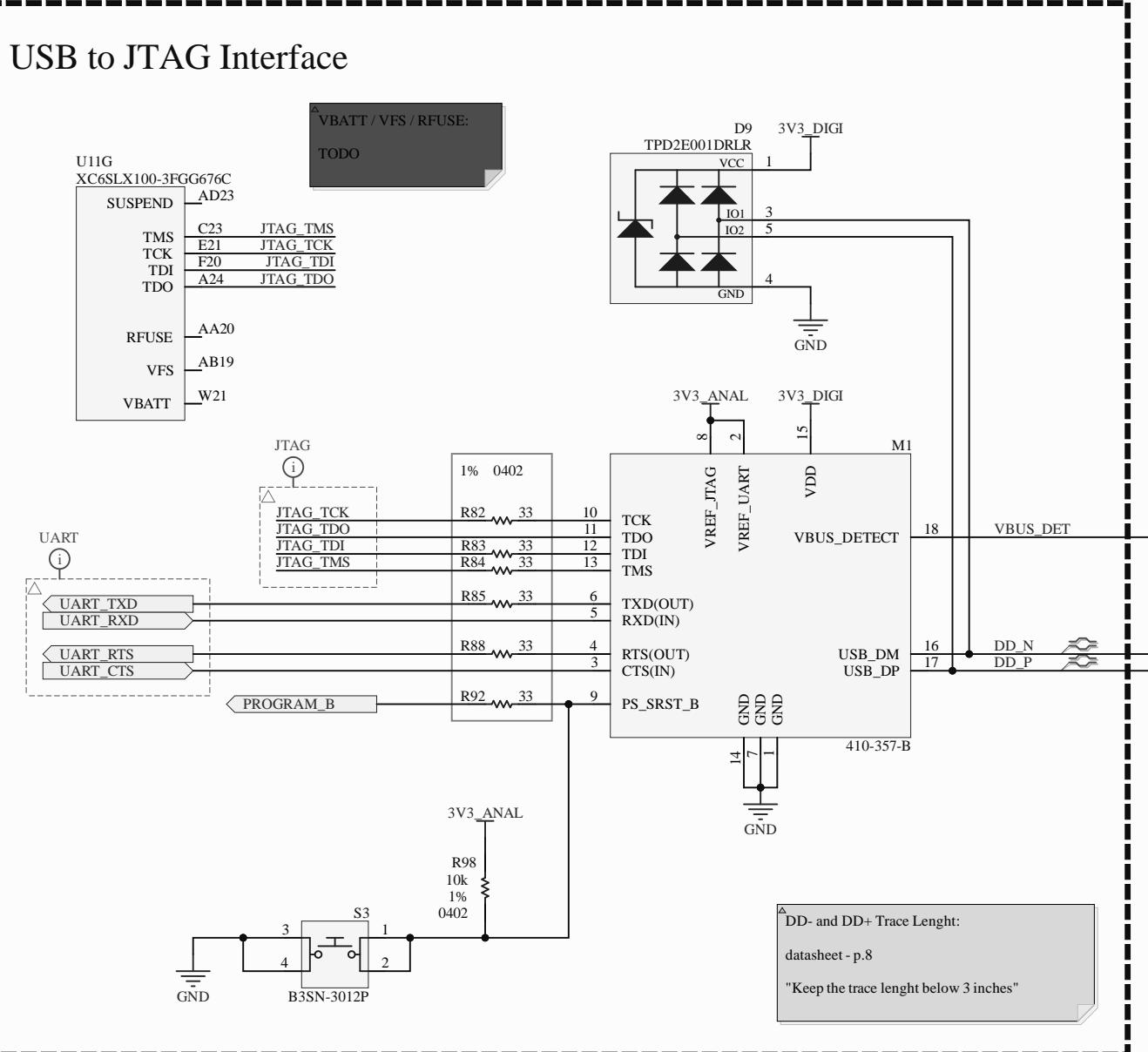
S7_APP1

Size 11x17 Group P20: couf1001-norc2802 Revision 1.00

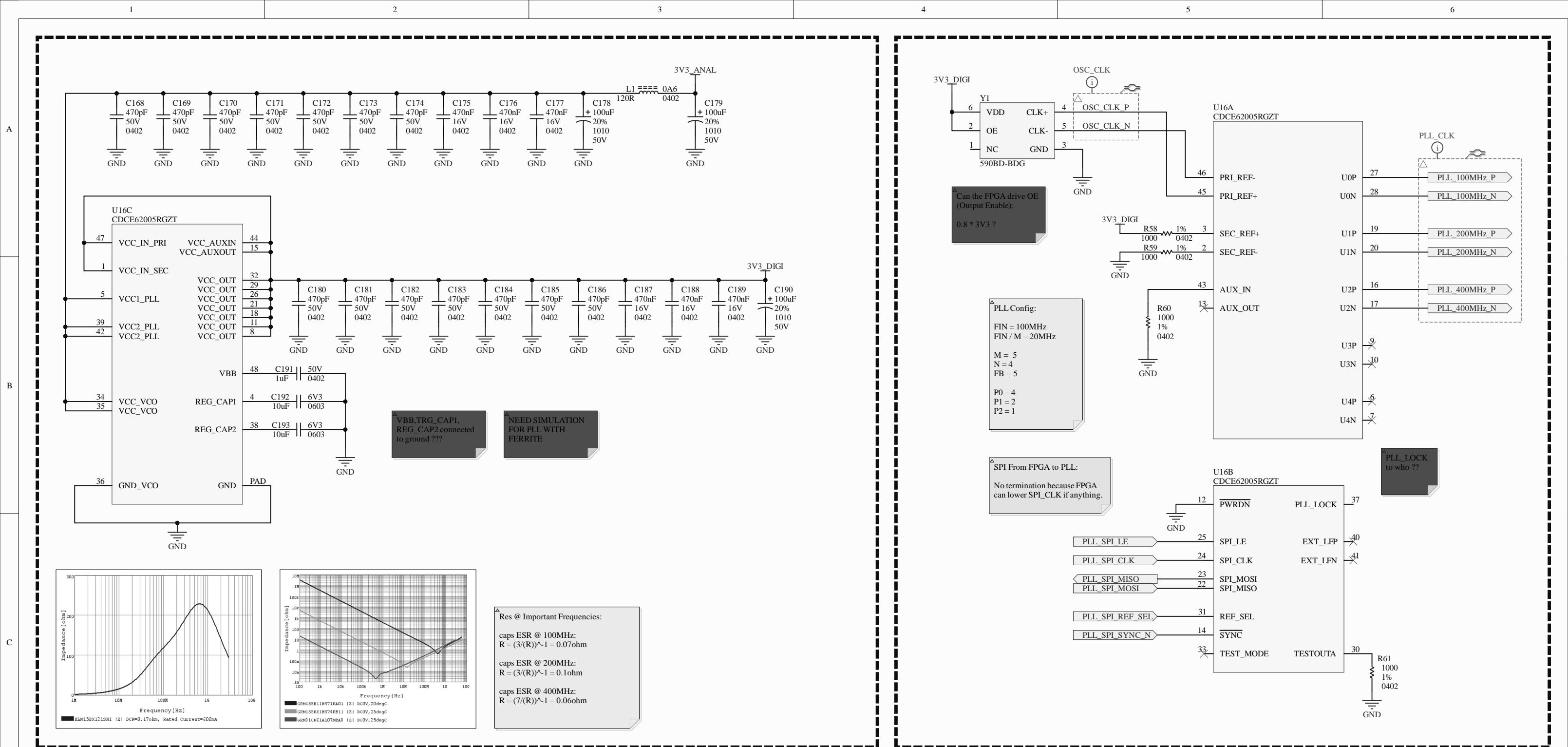
Date 24-01-12 Sheet 11 of 20

Filename S7CAS-PLEIADES-CARTE-MERE_P20_FPGA-Decoupling.SchDoc Designers Florent Cournoyer Charles Normandeau





Sheet Name	USB		
Project Title	S7CAS-PLEIADES-CARTE-MERE_P20		
Global Project	<i>S7APP1</i>		
Size	Group	P20: couf1001-norc2802	Revision
11x17			1.00
Date	24-01-12	Sheet	13 of 20
Filename	S7CAS-PLEIADES-CARTE-MERE_P20_USB.SchDoc		Designers Florent Cournoyer Charles Normandeau



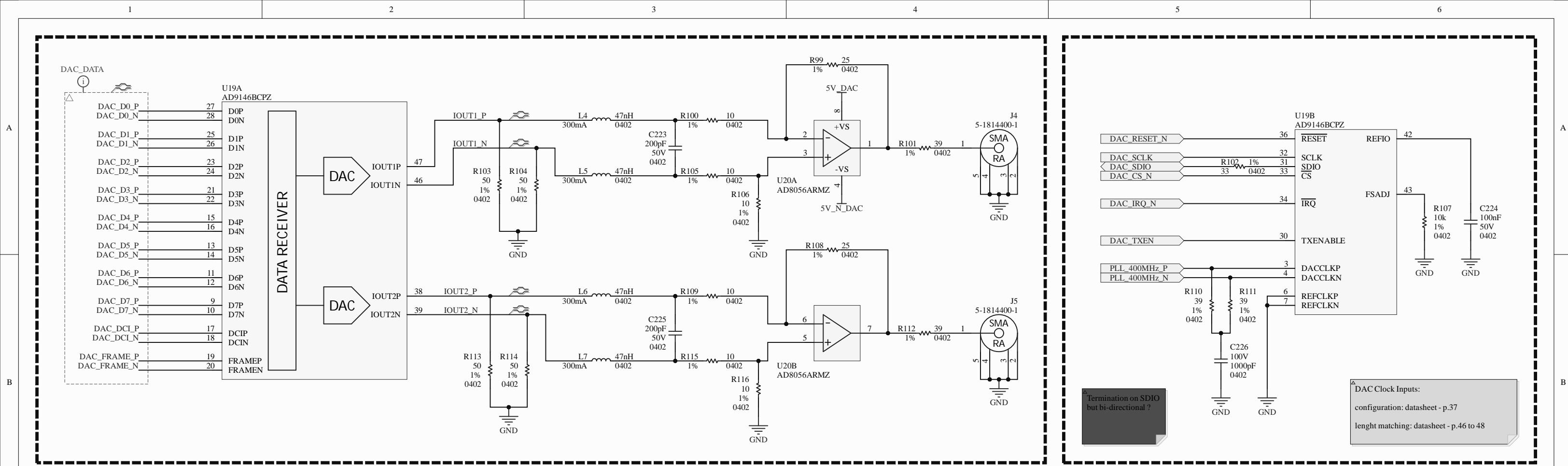
Sheet Name		PLL	
Project Title		S7CAS-PLEIADES-CARTE-MERE_P20	
Global Project		S7_APP1	
Size	Group	P20: couf1001-norc2802	Revision
11x17		1.00	
Date	Sheet	24-01-12	14 of 20
Filename		Designers Florent Cournoyer Charles Normandeau	
S7CAS-PLEIADES-CARTE-MERE_P20_PLL.SchDoc			

TOTAL POWER

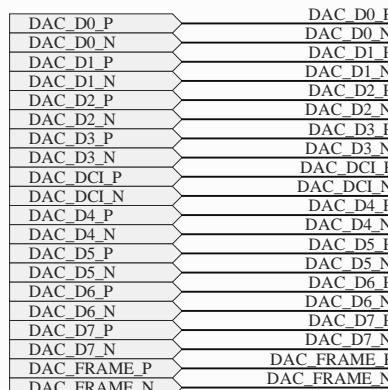
PLL_IN_CIRCUIT: $P = 250\text{mW}$
 PLL_ANAL: $P = 500\text{mW}$
 PLL_OUT_DIV: $P = 3 \times 60 + 2 \times 180 = 540\text{mW}$
 PLL_LVDS: $P = 76\text{mW}$

PLL_OSC: $P = V \times I = 3.3 \times 0.1 = 330\text{mW}$

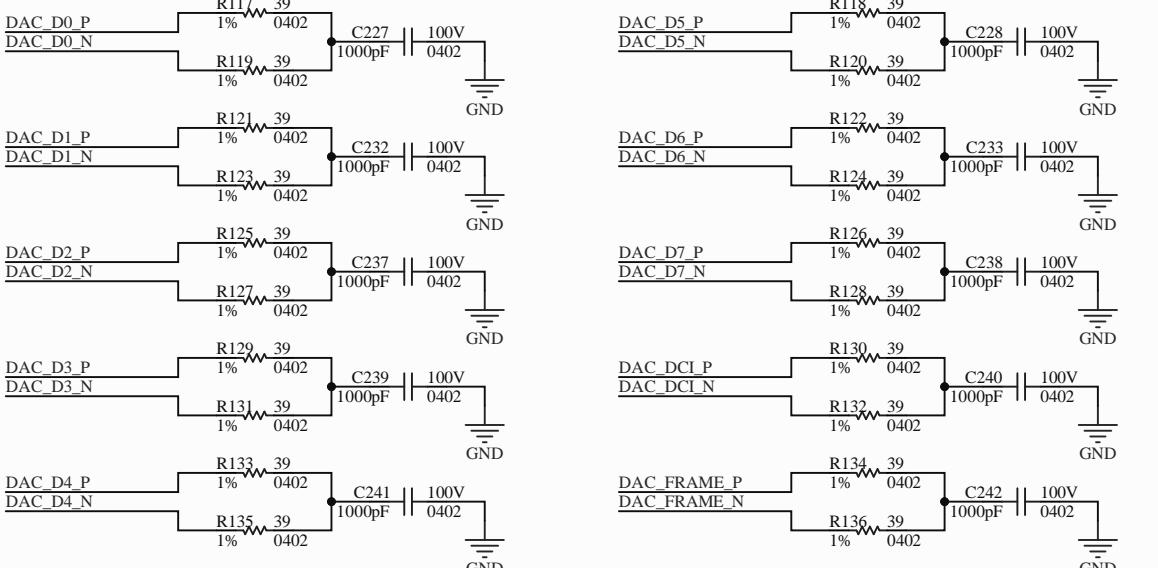
TOTAL: $P = 1696\text{mW}$



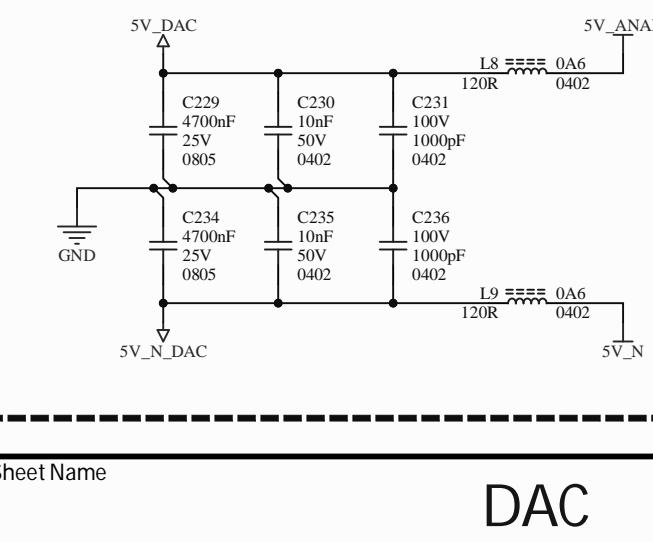
DAC Input Terminations



Terminations:
Is 39ohm ok ?
On die terminations ?



Op Amp Decoupling



OP Amp Decoupling:
datasheet - p.11

DAC Power Sequencing:
datasheet - p.52
"No specific power supply sequence is required"

TOTAL POWER

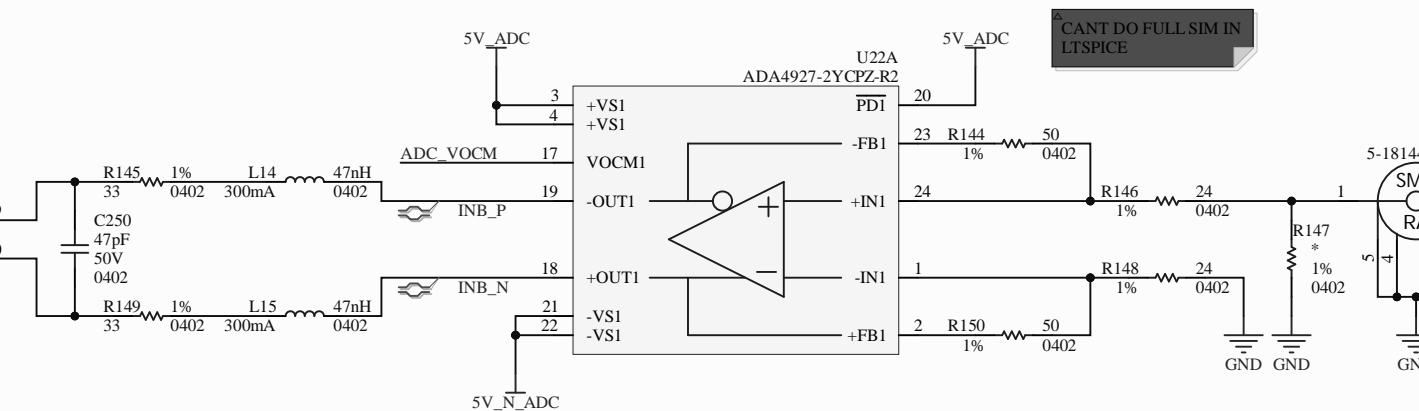
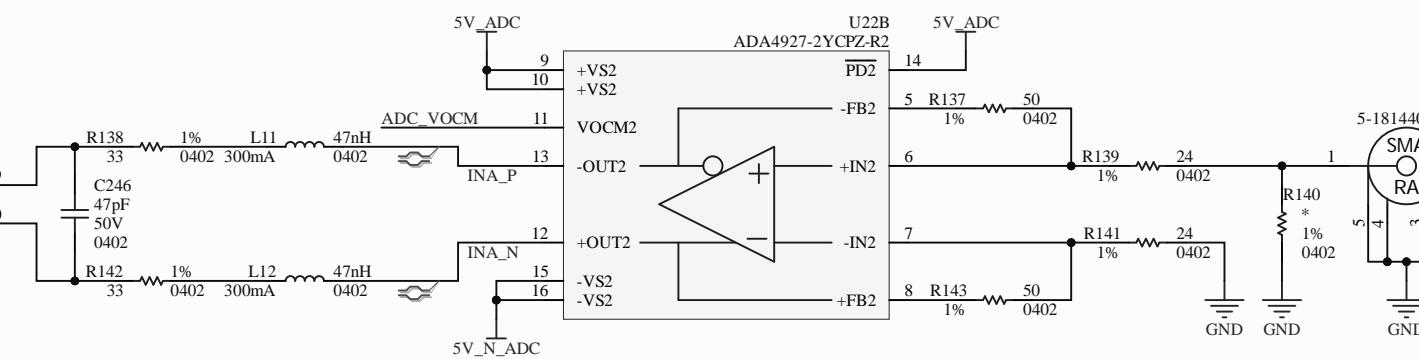
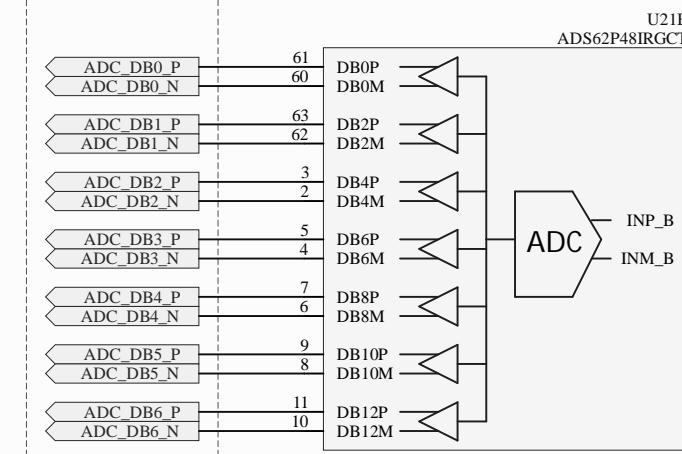
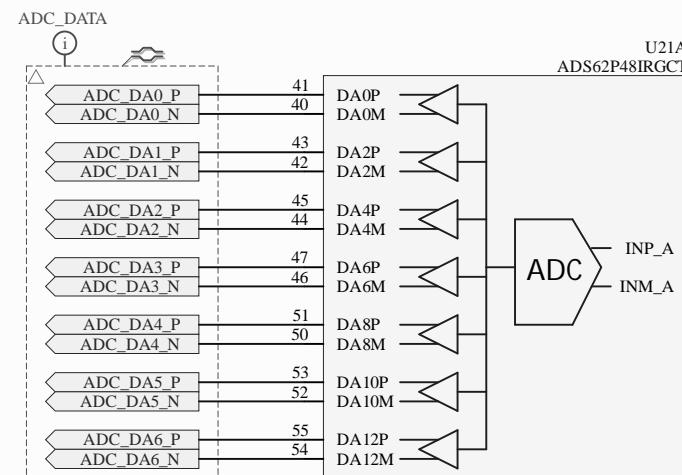
DAC_OP_AMP: $P = V \cdot I = 5 \cdot 0.0133 = 66.5mW$

TOTAL: $P = 66.5mW$

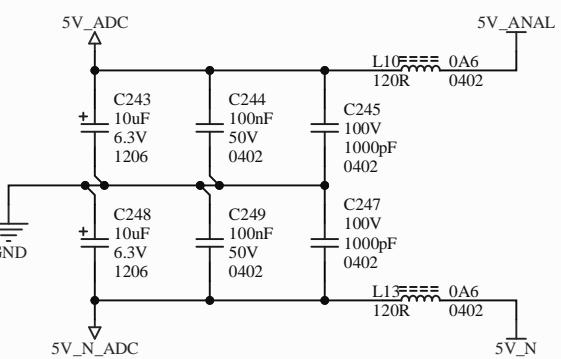
DAC
S7CAS-PLEIADES-CARTE-MERE_P20

S7_APP1

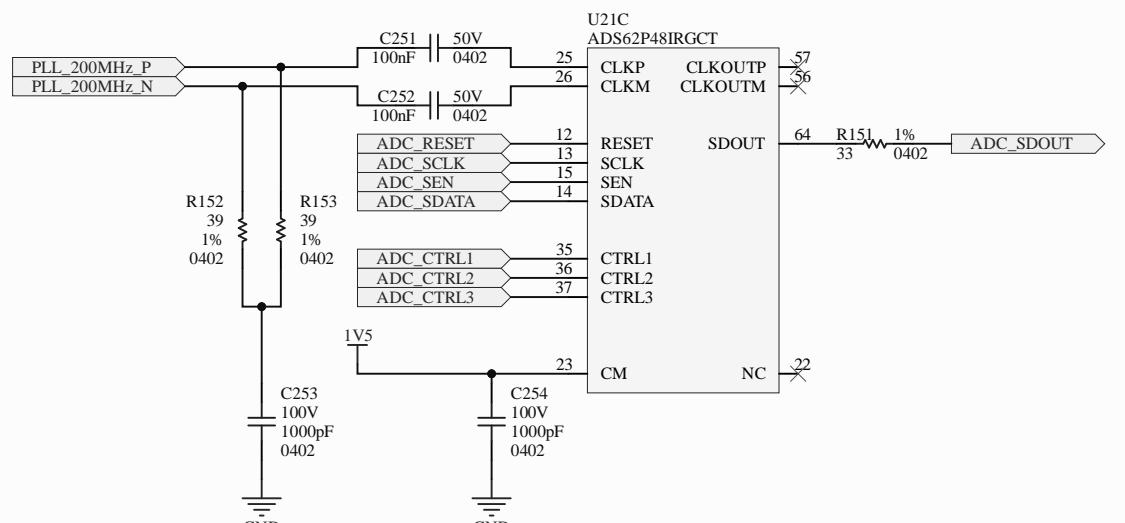
Size	11x17	Group	P20: couf1001-norc2802	Revision	1.00
Date	24-01-12	Sheet	15 of 20		
Filename	S7CAS-PLEIADES-CARTE-MERE_P20_DAC.SchDoc	Designers	Florent Cournoyer Charles Normandeau		



Op Amp Decoupling



OP Amp Decoupling:
datasheet - p.11



TOTAL POWER

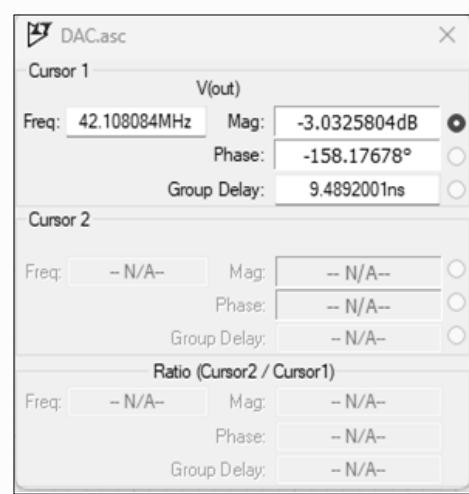
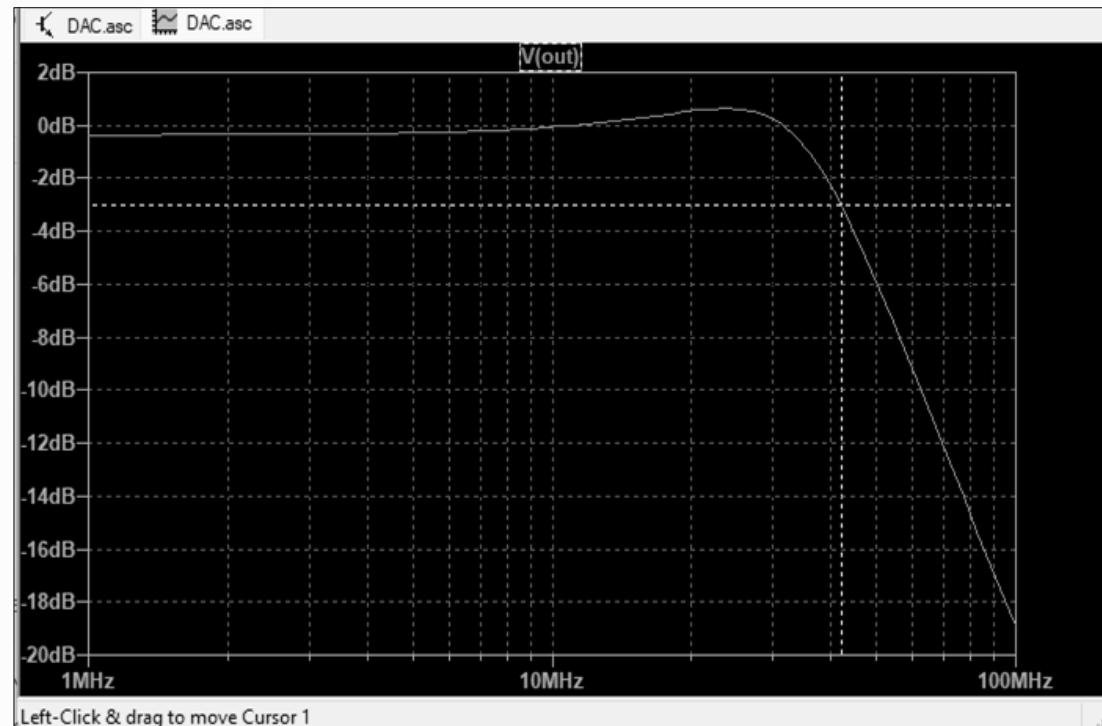
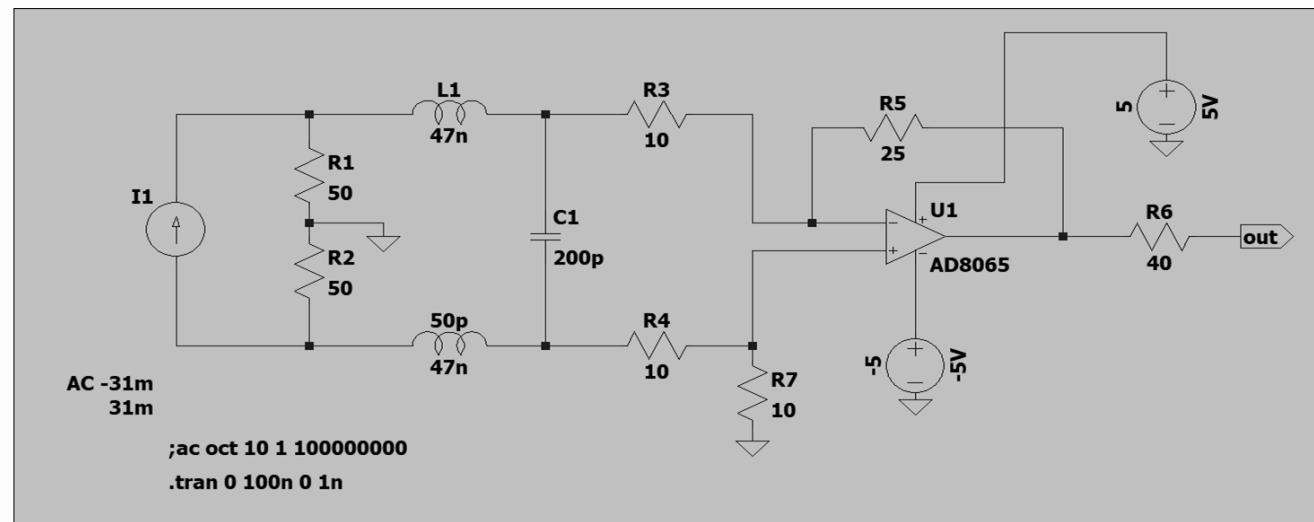
ADC_AMP_OP = V*I = 5*0.0216 = 108mW

TOTAL: P = 108mW

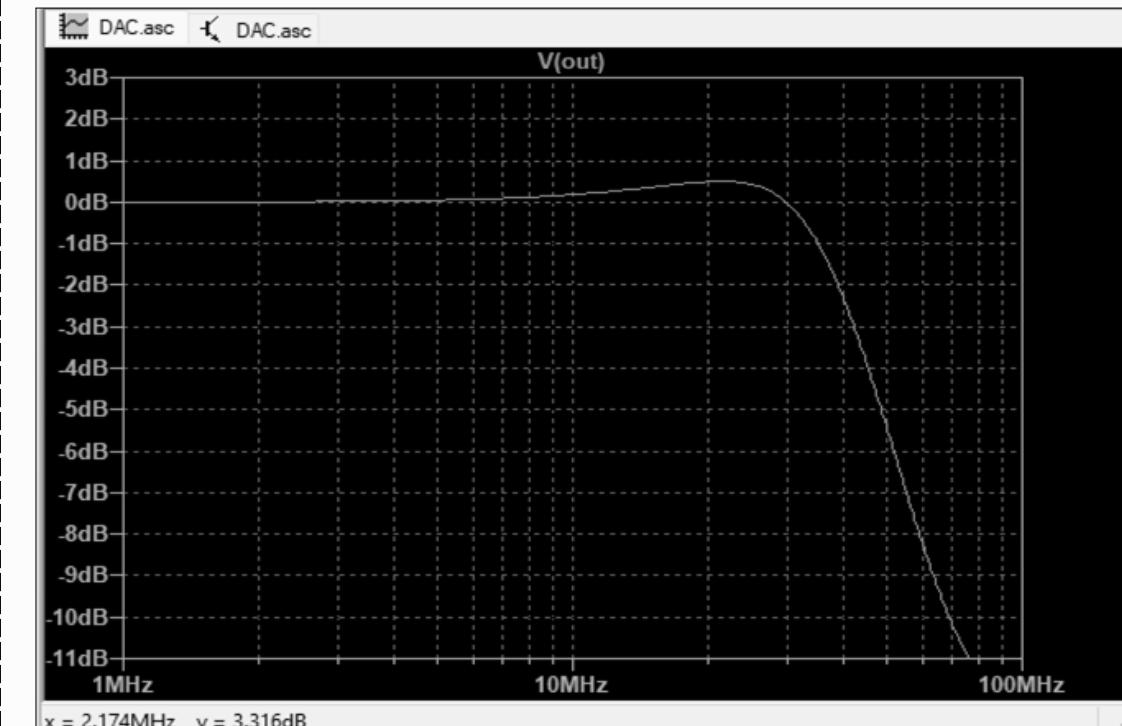
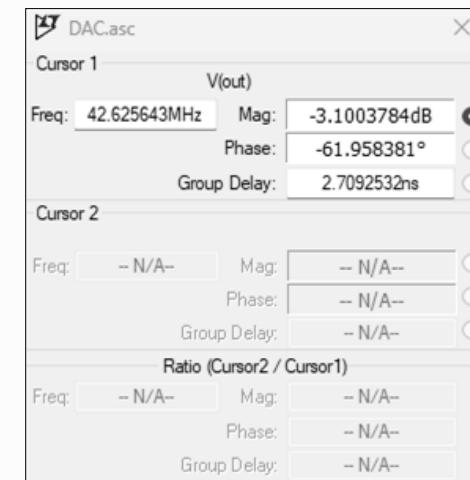
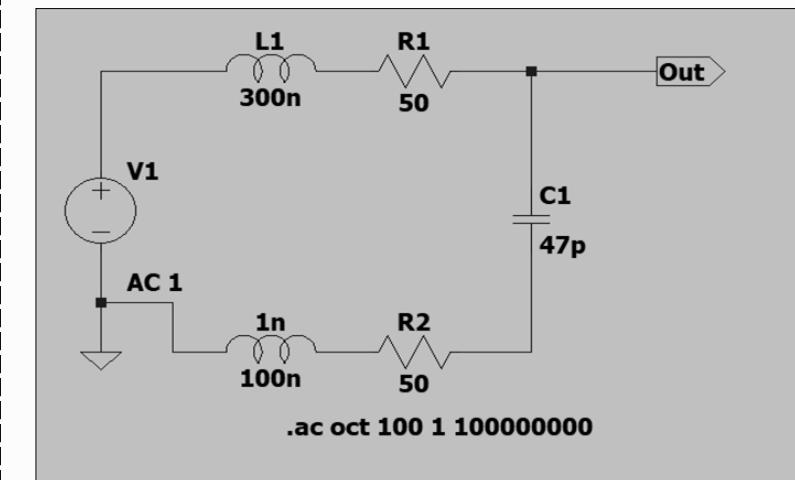
ADC Power Up Sequence:
datasheet - p.4
AVDD: Analog supply voltage
DRVDD: Digital supply voltage
"AVDD leads DRVDD during power up"
"DRVDD leads AVDD during power down"

Sheet Name		ADC	
Project Title		S7CAS-PLEIADES-CARTE-MERE_P20	
Global Project		S7_APP1	
Size	Group	P20: couf1001-norc2802	Revision
11x17			1.00
Date	24-01-12	Sheet	16 of 20
Filename	S7CAS-PLEIADES-CARTE-MERE_P20_ADC.SchDoc		
Designers	Florent Cournoyer Charles Normandeau		

DAC



ADC



C

C

C

D

D

Sheet Name

DAC ADC Spice Models

Project Title

S7CAS-PLEIADES-CARTE-MERE_P20

Global Project

S7_APP1

Size

11x17	Group	P20: couf1001-norc2802	Revision	1.00
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Date

24-01-12

Sheet

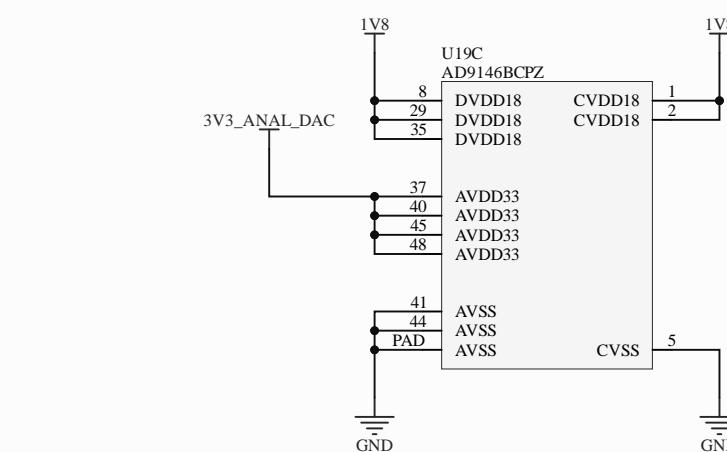
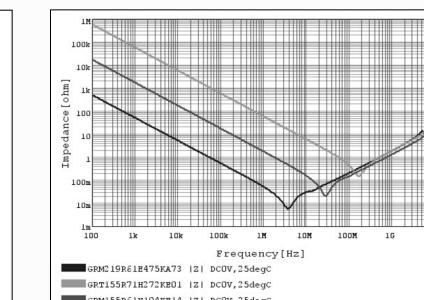
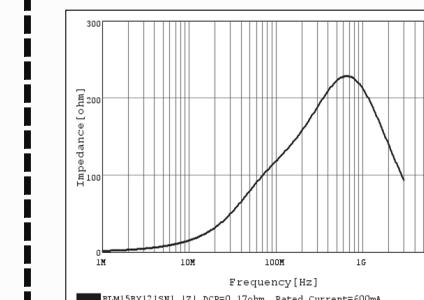
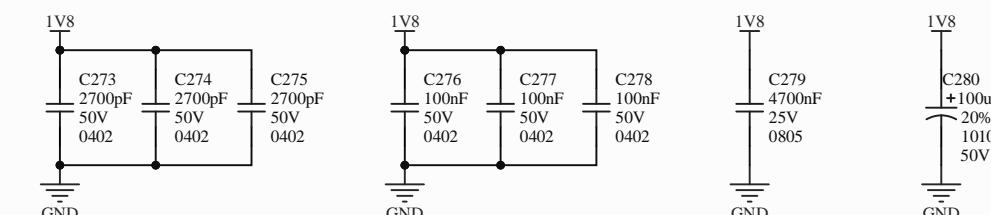
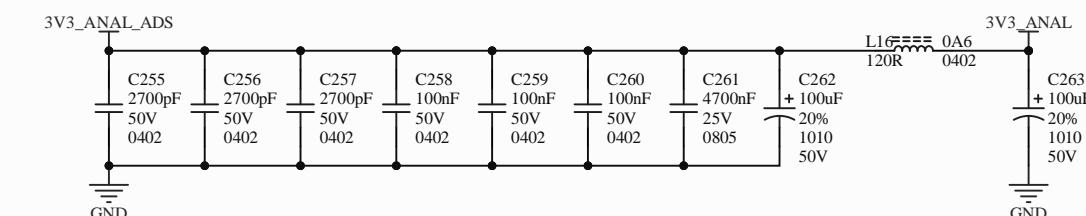
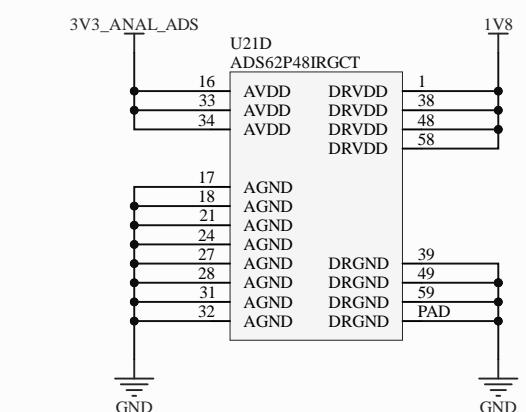
17 of 20

Filename

S7CAS-PLEIADES-CARTE-MERE_P20_DAC-ADC-Spice-Models.SchDoc

Designers

Florent Cournoyer
Charles Normandeau

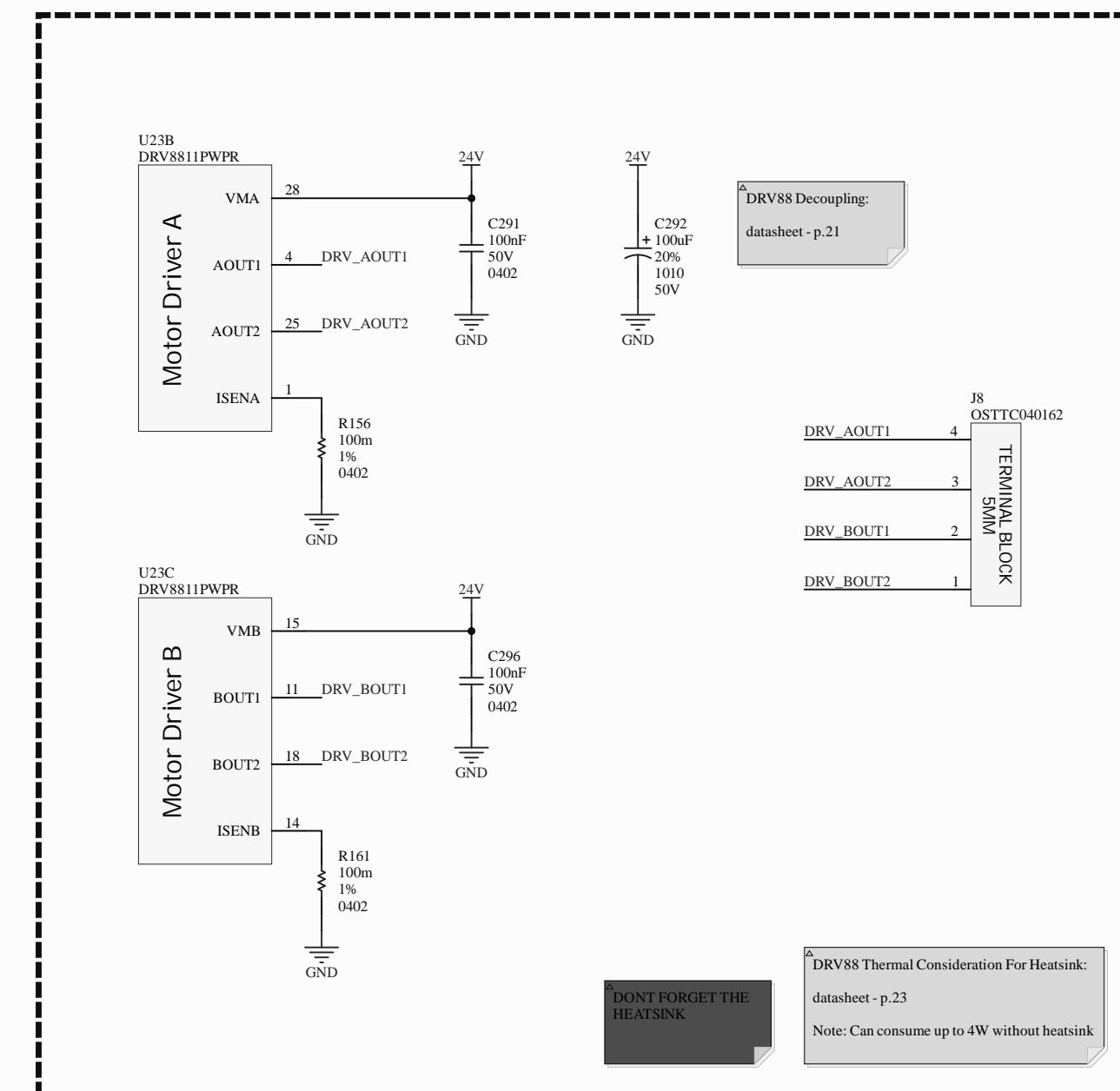
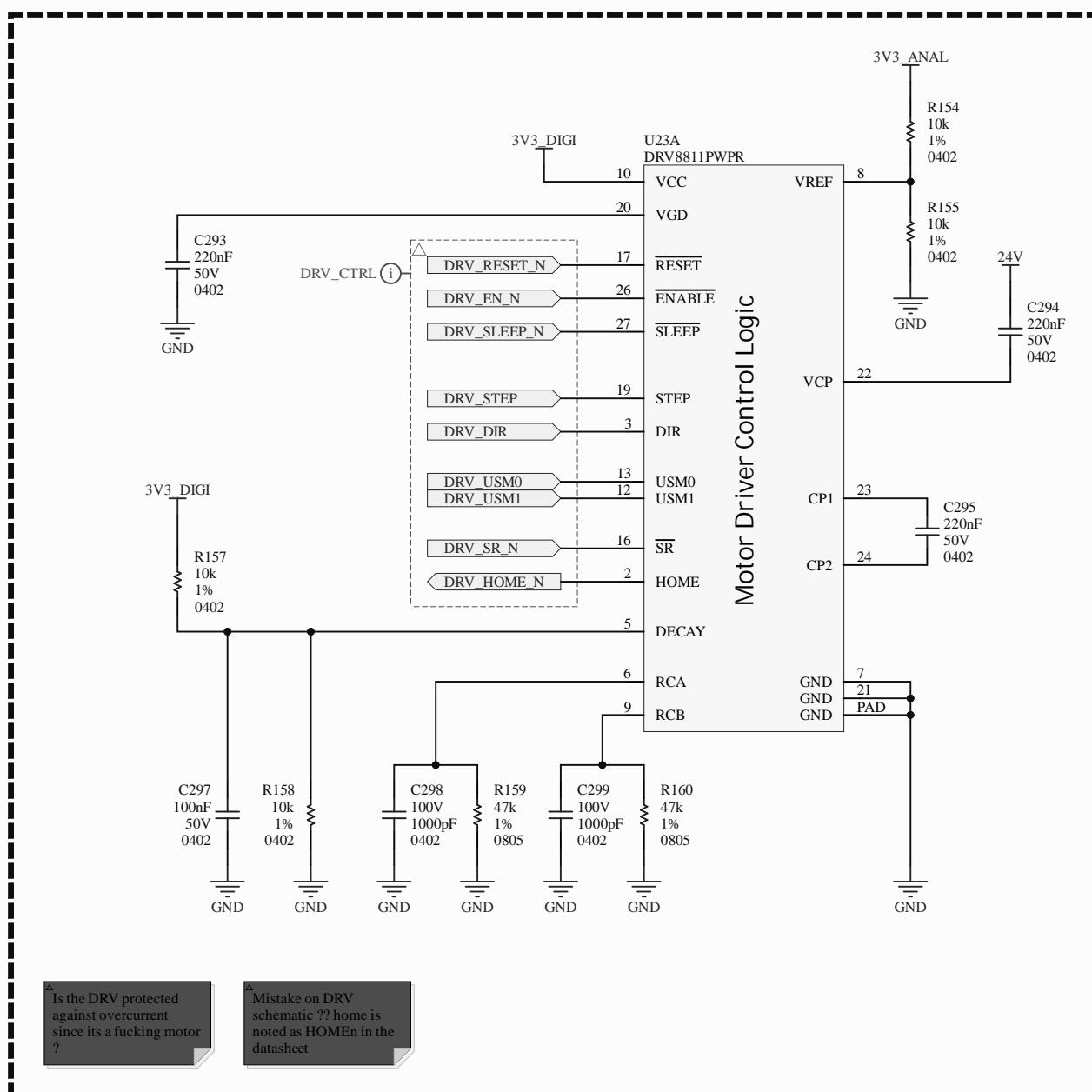
DAC**ADC**

ADC Power Up Sequence:
datasheet - p.4
AVDD: Analog supply voltage
DRVDD: Digital supply voltage
"AVDD leads DRVDD during power up"
"DRVDD leads AVDD during power down"

TOTAL POWER	
DAC_AVDD: $P = V \cdot I = 3.3 \cdot 0.056 = 184.8\text{mW}$	
DAC_CVDD: $P = V \cdot I = 1.8 \cdot 0.058 = 104.4\text{mW}$	
DAC_DVDD: $P = V \cdot I = 1.8 \cdot 0.343 = 617.4\text{mW}$	
ADC_AVDD: $P = 1.05\text{W}$	
ADV_DRVDD: $P = 0.3\text{W}$	
TOTAL: $P = 2256.6\text{mW}$	

Sheet Name		DAC ADC Decoupling	
Project Title		S7CAS-PLEIADES-CARTE-MERE_P20	
Global Project		S7_APP1	
Size	Group	P20: couf1001-norc2802	Revision
11x17			1.00
Date 24-01-12		Sheet 18	of 20
Filename S7CAS-PLEIADES-CARTE-MERE_P20_DAC-ADC-Decoupling.SchDoc		Designers Florent Cournoyer Charles Normandeau	

A



B

C

D

DRV88 Current:
 $I_{FS} = V_{REF} / (A_V * R_{SENSE})$
 $I_{FS} = 1.65V / (8 * 0.1\Omega)$
 $I_{FS} = 2.0625A$

DRV88 Power Dissipation:
 datasheet - p.23

TOTAL POWER

 $DRV_THERMAL: P = 4 * (R * I^2) = 4 * RDS * I_{OUT_RMS}^2 = 4 * 0.75 * (0.7 * 2.065)^2 = 6268.41mW$
 $DRV_MOTOR: P = V * I = VM * IVM = 24 * (0.008 + 2.065) = 49752mW$
 $DRV_CTRL: P = V * I = VCC * IVCC = 3.3 * 0.004 = 13.2mW$

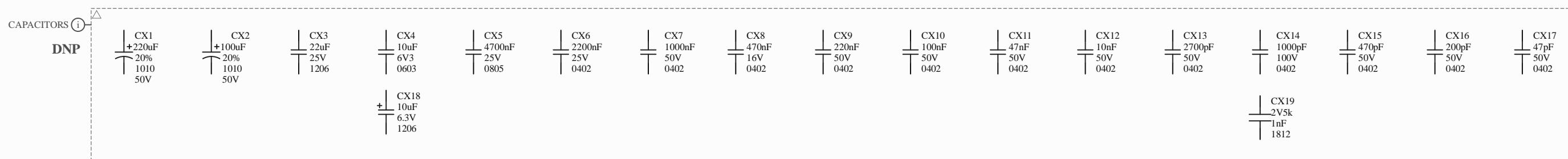
 $TOTAL: P = 56033.61mW$

Sheet Name		Motor	
Project Title		S7CAS-PLEIADES-CARTE-MERE_P20	
Global Project		S7_APP1	
Size	Group	P20: couf1001-norc2802	Revision
11x17			1.00
Date	24-01-12	Sheet	19 of 20
Filename	S7CAS-PLEIADES-CARTE-MERE_P20_Motor.SchDoc		Designers
	Florent Cournoyer Charles Normandeau		

A

A

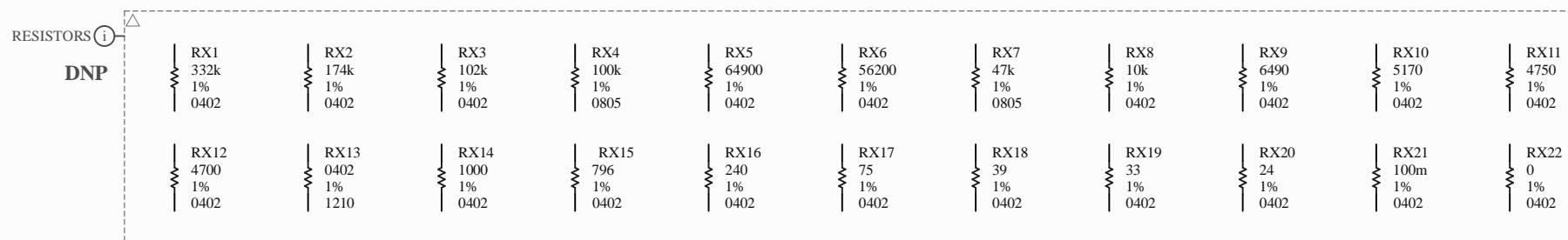
CAPACITORS



B

B

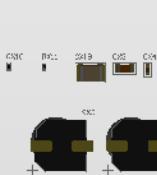
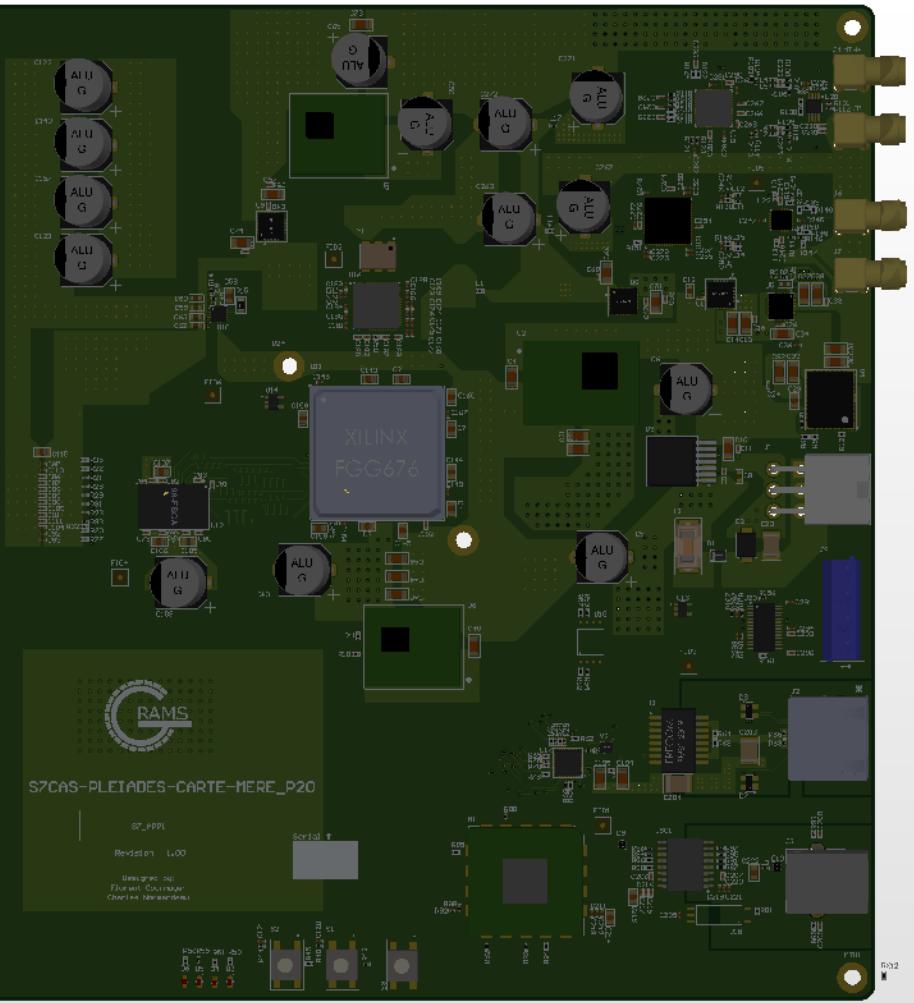
RESISTORS

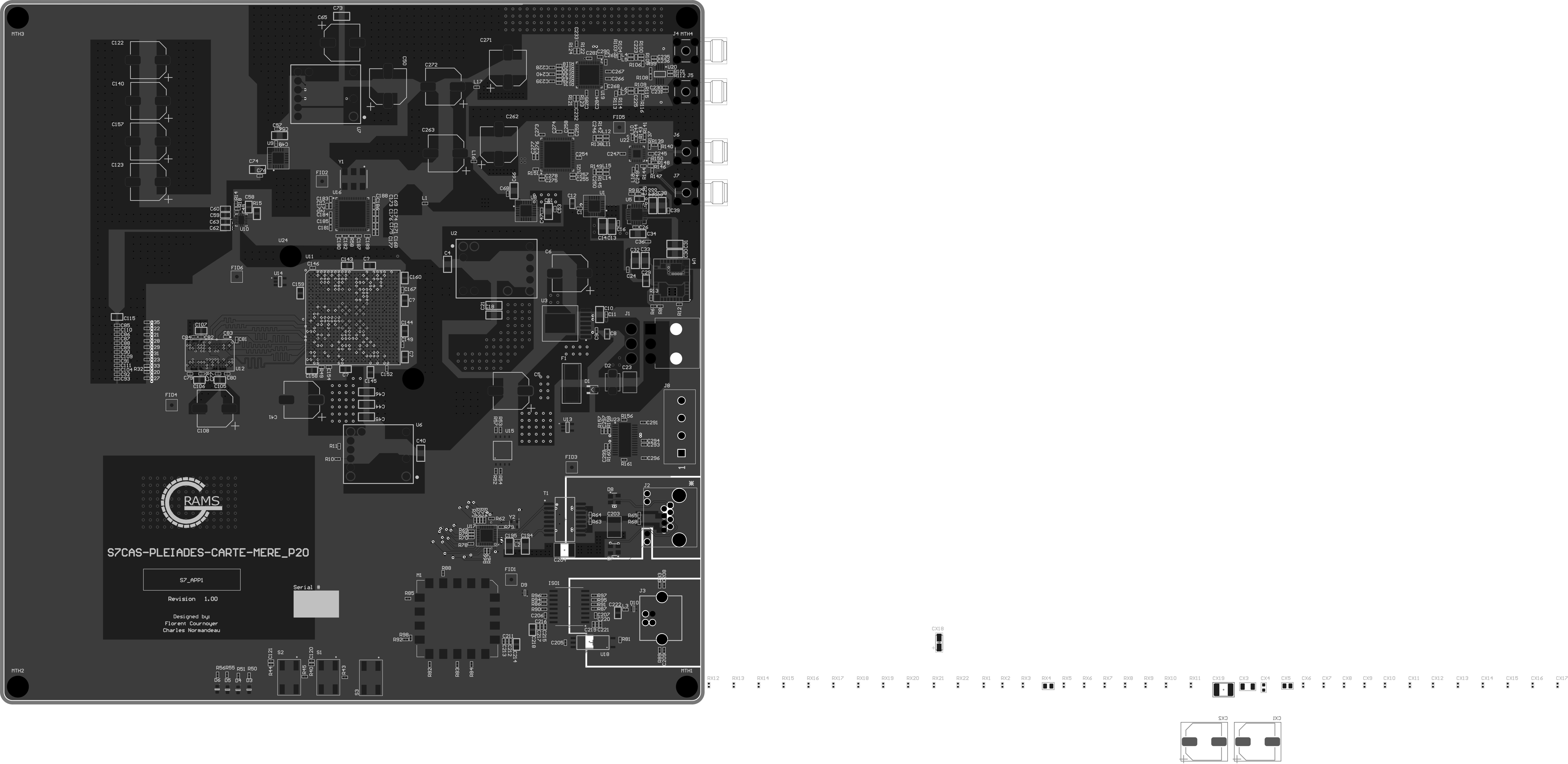


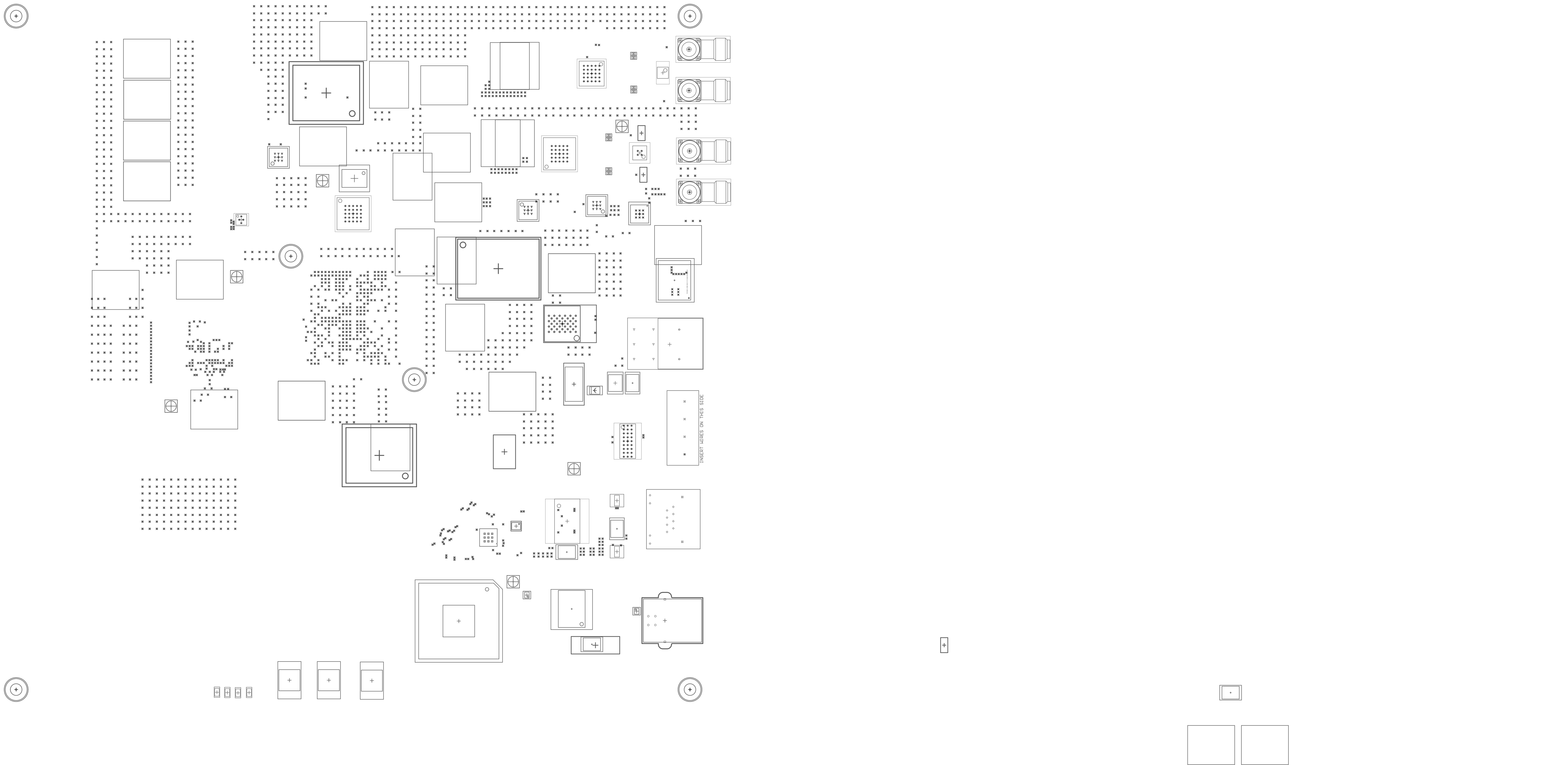
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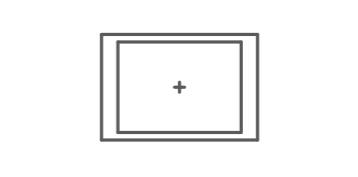
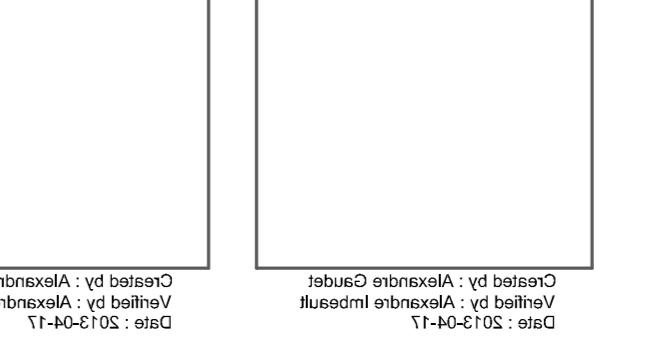
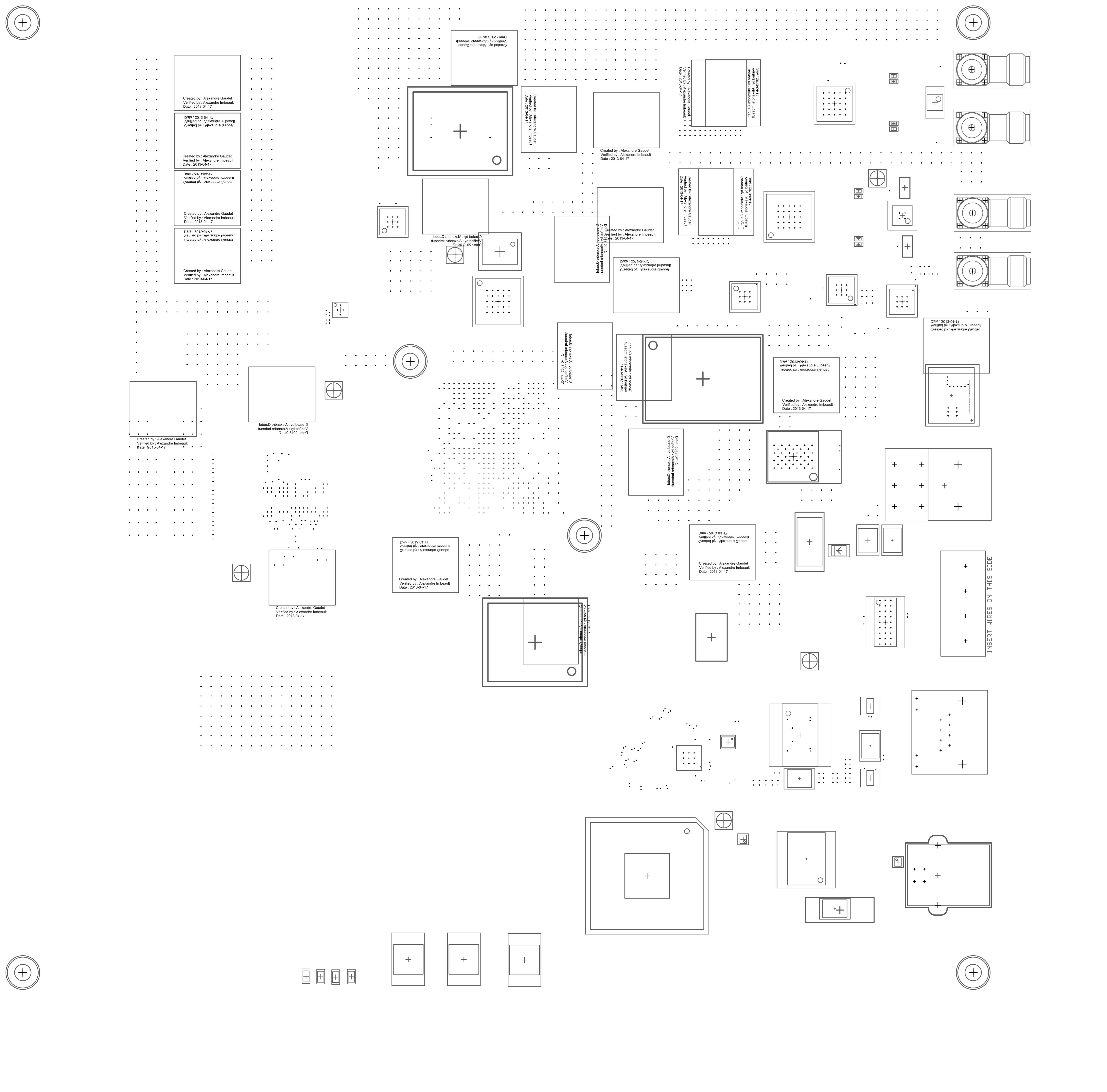
C

Sheet Name Insert name in Document Parameters		
Project Title S7CAS-PLEIADES-CARTE-MERE_P20		
Global Project S7_APP1		
Size 11x17	Group	Revision P20: couf1001-norc2802
Date 24-01-12		Sheet 20 of 20
Filename S7CAS-PLEIADES-CARTE-MERE_P20_Passive-Components.SchDoc		Designers Florent Cournoyer Charles Normandeau









Board Stack Report					
Stack Up		Layer Stack			
Layer	Board Layer Stack	Name	Material	Thickness	Constant
1		Top Paste			
2		Top Overlay			
3		Top Solder	SM-001	2.00mil	4
4		Top Layer	Copper	1.38mil	
5		Dielectric 1	S1170G	3.15mil	4.4
6		Int1 (GND)	Copper	0.69mil	
7		Dielectric 2	S1141	7.87mil	4.6
8		Int2 (Sign)	Copper	0.69mil	
9		Dielectric 3	S1170G	3.15mil	4.4
10		Int3 (GND)	Copper	0.69mil	
11		Dielectric 4	S1141	7.87mil	4.6
12		Int4 (Sign)	Copper	0.69mil	
13		Dielectric 5	S1170G	3.15mil	4.4
14		Int5 (GND)	Copper	0.69mil	
15		Dielectric 6	S1141	7.87mil	4.6
16		Int6 (PWR)	Copper	0.69mil	
17		Dielectric 7	S1170G	3.15mil	4.4
18		Int7 (GND)	Copper	0.69mil	
19		Dielectric 8	S1141	7.87mil	4.6
20		Int8 (GND)	Copper	0.69mil	
21		Dielectric 9	S1170G	3.15mil	4.4
22		Int9 (PWR)	Copper	0.69mil	
23		Dielectric 10	S1141	7.87mil	4.6
24		Int10 (GND)	Copper	0.69mil	
25		Dielectric 11	S1170G	3.15mil	4.4
26		Bottom Layer	Copper	1.38mil	
27		Bottom Solder	SM-001	2.00mil	4
28		Bottom Overlay			
29		Bottom Paste			
	Height : 71.90mil				