

# IC for Online EIS in Automotive Batteries and Hybrid Architecture for High-Current Perturbation in Low-Impedance Cells

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**Abstract**—This paper describes a new custom IC optimised for online Electrochemical Impedance Spectroscopy (EIS) characterisation of battery packs at the cell-level, with 200 mA peak perturbation current. In addition, a new hybrid power architecture is demonstrated that has been designed to be embedded in the battery management system of a new electric pick-up truck. The hybrid architecture consists of 1) a linear current regulator, 2) a small ultracapacitor, and 3) an isolated Cuk converter that is part of the balancing system, which also supplies the 12V auxiliary loads. The architecture leverages the signal processing capabilities of the IC and extends the perturbation range to 40 A peak while limiting the thermal losses. Experimental EIS measurements are performed for four parallel-connected 44 Ah Lithium Nickel-Manganese-Cobalt-oxide pouch cells, each with 1 m $\Omega$  nominal internal resistance, at 40 A peak excitation current.

## I. INTRODUCTION

In 2015, the global stock of Electric Vehicles (EVs) exceeded 1 million for the first time [1]. As the EV industry ramps up from supplying the heavily subsidised early-adopter market to high-volume production, there is a renewed focus on advanced high-reliability Battery Management Systems (BMS). In particular, in order to increase the real-world driving range of EVs, while also reducing the cost, it is critically important to push the battery cell technology to the limits, while maintaining safety and longevity. Increasing the accuracy of estimation of the battery parameters, such as state-of-charge (SOC), power capability, and capacity, is key to reducing the conservative limits that are commonly imposed in today's BMS. Recent work toward this objective involves the introduction of real-time model-based state estimation within the BMS, where an Electrical Circuit Model (ECM), such as the one shown in Fig. 1(a), is often combined with variations of the state observer or Kalman filter. A comprehensive review of battery state estimation techniques is given in [2].

One challenge with real-time model-based state estimation is the accurate determination of time-varying model parameter values. Electrochemical Impedance Spectroscopy (EIS), which involves measurement of the battery's impedance at frequencies from DC to tens of kHz [3], is one method that can be used to directly extract these values. A sinusoidal perturbation

current is injected into the battery and the impedance is calculated based on the current and voltage phasors. Curve-fitting is then used to estimate the circuit parameter values, and a model can be produced for a wide range of operating conditions such as SOC, temperature, and age. Due to the non-linearity of the battery impedance response to current, a trade-off between model accuracy and measurement Signal-to-Noise Ratio (SNR) must be made when selecting the perturbation current amplitude [4]. The amplitude should be small enough to maintain the necessary linearity, and large enough to provide the necessary SNR.

In addition to estimating the voltage dynamics through the ECM, impedance-based battery models have been demonstrated that accurately predict other parameters of interest. In [5], [6] it is shown that the internal temperature of a cell can be estimated through EIS, by identifying the perturbation frequency at which its impedance reaches a certain value. Impedance has also been directly related to the cell SOC and SOH [7], [8], as well as aging [9].

EIS has long been used for offline characterisation with bench-top equipment. However, interest has recently grown in embedding EIS measurement capabilities into the vehicle BMS [10]–[14]. This is due to the potential accuracy improvement that real-time measurements can have on dynamic battery operating limits, which constrain overall battery performance. It is well-known that the weakest series-connected cell in the pack limits performance, for example, the lowest SOC cell limits the discharge of the pack. Therefore it is necessary for any online EIS system to measure the impedance of each series-connected cell. Current perturbation for online EIS has been proposed at both pack and cell levels. Pack-level perturbation is a low-cost solution because it can be carried out by the pack-connected converters that already exist in the vehicle, for example, the charger or traction inverter. However, pack-level parasitic impedances such as those resulting from the layout and wiring of the cells may interfere with the perturbation injection. Furthermore, the challenge of synchronising all cell-level measurements to a pack-level perturbation is significant, especially in the presence of parasitic impedances. In order

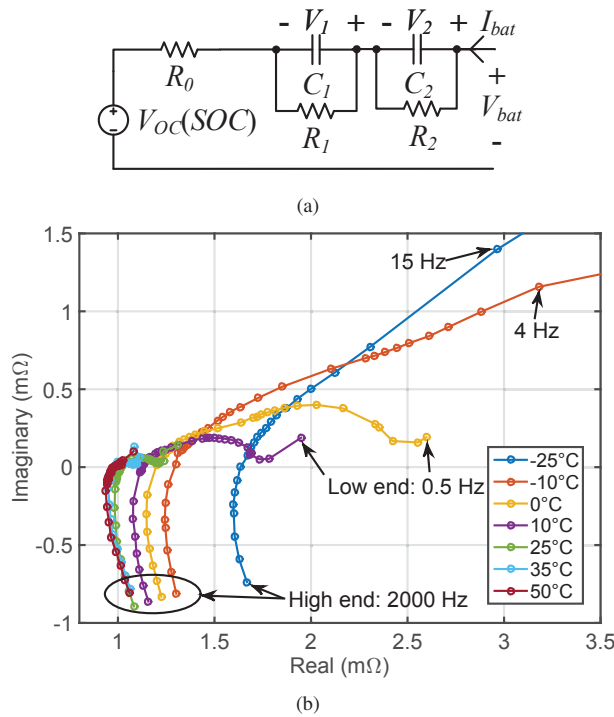


Fig. 1. (a) ECM of a lithium cell. (b) Measured Nyquist plot of the 44 Ah EV cell from 0.5 to 2000 Hz from -25°C to 50°C.

to maximise the benefits of online EIS, it is necessary to maximise the accuracy of measurements. Thus, it is necessary to both perturb and measure at the cell-level.

Due to the cost sensitivity of EV batteries, embedding EIS hardware into the BMS necessitates an integrated solution. However, the EIS power requirement changes significantly based on the cell characteristics, pack architecture, and instrumentation capability. In this work, a large-format 44 Ah Lithium Nickel-Manganese-Cobalt-oxide (NMC) pouch cell with a nominal ESR of 1 m $\Omega$  is considered, and four cells are connected in parallel in the final application. The measured impedance of one cell is shown in Fig. 1(b). It can be seen that impedance has a strong sensitivity to temperature, a characteristic that limits the available cell power [15]. In this work, we describe a new IC optimised for online EIS applications at the cell-level, with a 200 mA peak perturbation current. In addition, we propose a new hybrid power architecture consisting of 1) a linear current regulator, 2) a small ultracapacitor and 3) an isolated switched-mode converter, that can leverage the signal processing capabilities of the IC and extend the perturbation range to 40 A peak. The hybrid architecture online EIS system is part of a new BMS for custom-designed battery modules with liquid thermal management, as shown in Fig. 2(a), which are optimised for a new electric pick-up truck, as shown in Fig. 2(b). This paper is organised as follows: Section II introduces the IC, Section III discusses the system-level context for online EIS in the electric pick-up truck, and Section IV introduces the hybrid architecture operating principle and experimental results.

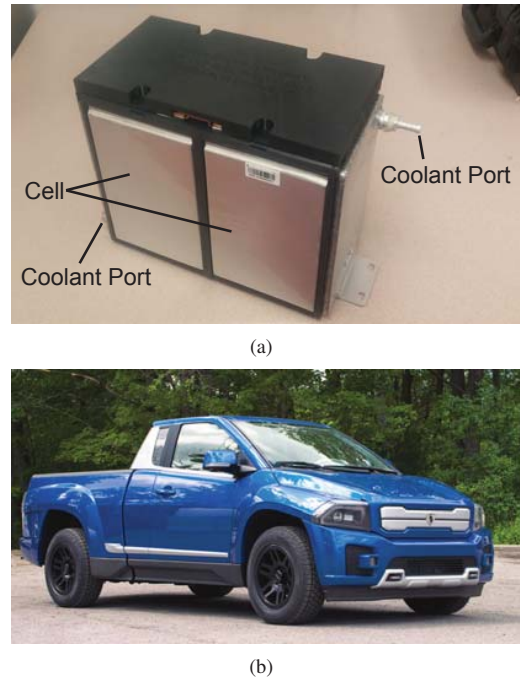


Fig. 2. (a) Custom liquid-cooled battery module. (b) Electric pick-up truck prototype.

## II. BMS IC WITH ONLINE EIS

The BMS IC, referred to as the Single Cell Supervisor IC (SCS), is intended to be mounted very close to the cell, or even inside the cell package, for precise voltage and impedance measurement. A simplified block diagram of an example battery pack built with the SCS is shown in Fig. 3. Each cell in the pack has its own SCS attached to it. The SCS is supplied by the cell that it supervises. The SCSs are connected to each other with a daisy chain that carries information from and to the pack controller. One SCS is connected to a shunt resistor to measure the pack current. Synchronised voltage and current sampling throughout the pack is facilitated by the daisy chain communication protocol. Note that the current measuring SCS is not supplied by a battery cell in the string, as this would cause charge unbalance over time. The power is instead supplied from the auxiliary bus, which is drawn from the entire pack, and does not cause unbalance.

The block diagram of the SCS is shown in Fig. 4. A sigma-delta ADC converts the battery cell voltage into a bitstream. The bitstream is processed in a digital filter block to extract the measurement data: the DC voltage and the real and imaginary part of the cell impedance. A calibration block then corrects the offset and gain errors of the ADC. Each IC is calibrated in the test fab, and the calibration parameters are stored in an on-board One-Time-Programmable memory (OTP). The calibration block also eliminates the errors of the Die Temperature Sensor (DTS). All measurement data is stored in a memory, so it can be retrieved by the pack controller when needed.

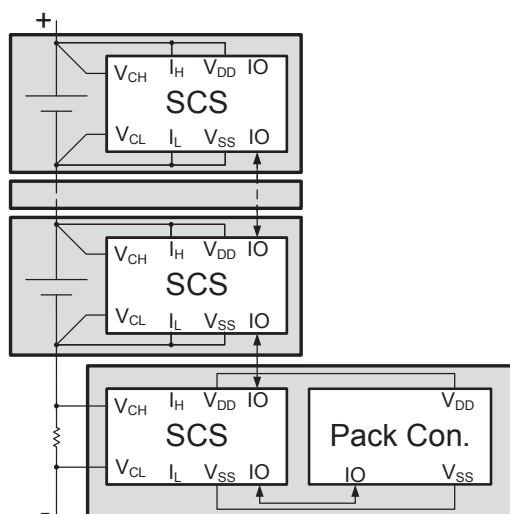


Fig. 3. Battery system architecture using a set of SCSs.

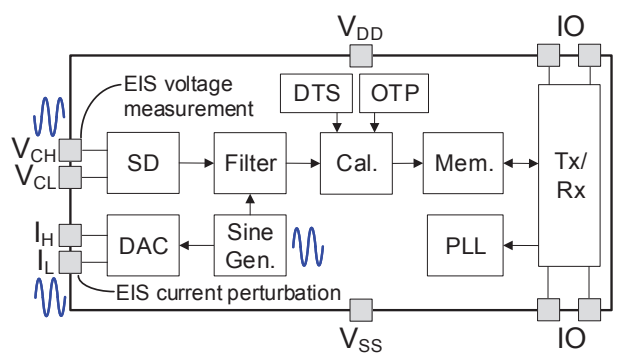


Fig. 4. Block diagram of the SCS.

For passive balancing, a DAC can draw a programmable current from the cell. The same DAC is used to draw a sinusoidal current from the cell during impedance measurements. As the cell impedance is very low, it is crucial to keep the voltage measurement lines and the current lines well separated. Otherwise one is likely to measure the wiring resistance instead of the cell impedance. Having the SCS close to the cell helps keep the wires short and the risk of picking up interference low.

The sine generator is clocked by a PLL which is locked to the clock of the communication daisy chain. The communication protocol allows for the clock to be sent continuously when no commands or data are being transmitted. This keeps the frequency and phase of all ICs extremely accurate and well aligned. The sinusoidal reference that drives the DAC is also sent to the filter block, thus the frequency and phase of the demodulator are exactly the same as those of the modulator. This makes it possible to use filters with a very narrow bandwidth. When a car is driving, its electric motor generates a very high level of interference with a very wide

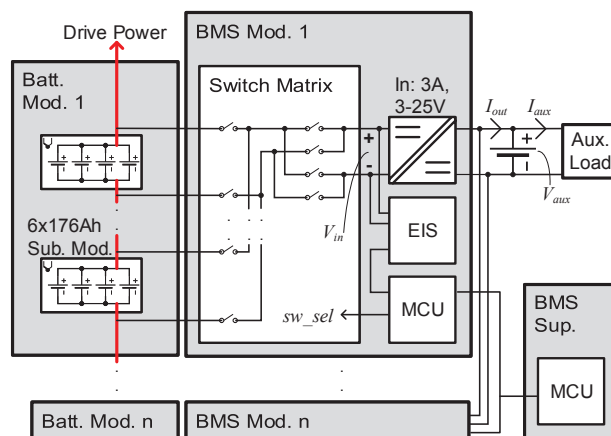


Fig. 5. Electric pickup truck battery system architecture.

bandwidth on the battery cell voltage. By measuring in a very narrow bandwidth, the influence of the interference on the measurement result can be all but eliminated [6]. This measurement system can measure both the real and imaginary parts of the cell impedance. By changing the frequency of the sine generator, it is possible to generate the complete Nyquist curve of the battery cell.

### III. HIGH-CURRENT ONLINE EIS: SYSTEM-LEVEL CONSIDERATIONS

The battery of the EV shown in Fig. 2(b) is composed of 44 Ah NMC pouch cells assembled into series-connected modules, as shown in Fig. 2(a), to form the high-voltage string. The system architecture is shown in Fig. 5. Each module has a 6S4P configuration and contains one BMS module. Each unit of 4 parallel cells is called a sub-module. A BMS supervisor aggregates the sensed sub-module voltages, temperatures, and pack current, and computes the control commands. Each BMS module contains a switch matrix that facilitates connections between the sub-modules and a uni-directional isolated dc-dc converter, implemented as a Ćuk converter. The converter output is connected to the EV's 12V auxiliary bus, which contains a lead-acid battery and serves loads including the electronics involved in the management of the vehicle's thermal, chassis, body, and interior systems. The Ćuk converter serves two roles: 1) deliver the auxiliary supply power from the high-voltage battery, and 2) active cell-balancing. The power management system provides advantages similar to [16], [17] and [18]. However, the fundamental difference is that the converter can draw current from one or all of the cells within the module through the switch matrix. This allows for high auxiliary bus power to be supplied by increasing the converter input voltage rather than current, which achieves cost saving compared to systems with one converter per cell.

Constraining factors in the design of the high-current power-stage for online EIS are: 1) SNR, 2) volume, 3) cost, and 4) level of integration with existing components. This work only considers performing EIS through discharge of the

battery, thus eliminating the need for bi-directional current control. With four cells in parallel, each having a 1 mΩ nominal ESR, a 40 A peak perturbation current (0.22 C) is required to achieve a 10 mV peak signal at the SCS's ADC, which is desirable in this automotive environment. This peak current corresponds to a peak load of 168 W in the EIS circuit at the maximum cell voltage of 4.2 V. Two off-chip options are considered to achieve this perturbation current:

- 1) Dissipation into an external shunt MOSFET in linear mode. This requires the single device to dissipate all measurement power, which adds significantly to the MOSFET cost.
- 2) Use the isolated dc-dc converter to send the perturbation current into the 12V battery. This imposes a costly increase (more than double) on the current rating of magnetic elements, and may cause EMI issues at high perturbation frequencies.

#### IV. HYBRID LINEAR AND SWITCHED-MODE EIS ARCHITECTURE

The new hybrid architecture for high-current online EIS combines both options mentioned in Section III; it includes a switched-mode converter and a linear regulator, as shown in Fig. 6(a). The system is not currently integrated into the switch matrix of the BMS in Fig. 5, however it uses the switch matrix MOSFET as  $Q_{shunt}$ , the shunt MOSFET, and the dc-dc is the same.  $Q_{shunt}$  passes the full perturbation current and is present in the switch matrix. A small ultracapacitor,  $C_{uc}$ , is used to reduce the drain-source voltage of  $Q_{shunt}$ , thus greatly reducing the thermal losses. The isolated dc-dc converter from the BMS also contributes to EIS operation by decreasing the  $C_{uc}$  voltage ripple, further reducing thermal losses. The ultracapacitor maximum voltage rating is 2.7 V, which is lower than the cell voltage of 3-4.2 V. Therefore, the MOSFET  $Q_{uc}$  is used as a switch for voltage blocking while EIS is not operating. The system incurs a minimal incremental cost since the dc-dc converter is already utilised for auxiliary supply, while the 50F ultracapacitor represents 0.03%, 0.001% and 0.2% of the module's volume, energy capacity and cost, respectively.

Table I summarises a comparison of the shunt MOSFET, dc-dc, and proposed hybrid architecture alternatives when operating at 40 A peak perturbation current at a minimum of 1 Hz perturbation frequency. Each online EIS circuit in the pack is used in sequence by all sub-modules in a module through the switch matrix, thus the comparison is done at the module level, and shows the incremental impact on size and cost. It can be seen that the shunt MOSFET option occupies the least volume, but must operate at high power dissipation concentrated into one costly device. Scaling the dc-dc current rating higher would result in the least power dissipation, but adds the most volume. The hybrid system achieves the best balance between the comparison metrics, achieving the necessary reduction in power dissipation to enable the use of MOSFETs already present in the switch matrix, without any increase in the dc-dc volume.

TABLE I. ONLINE EIS DESIGN ALTERNATIVES AND ESTIMATED SYSTEM IMPACT

Design Alternative	RMS Power Loss (W)	Volume (cm <sup>3</sup> )	Cost (USD)
Shunt MOSFET	103	11	20
dc-dc	23	24	4
Hybrid	45	13	4

#### A. Principle of Operation

Key ideal waveforms of the hybrid architecture performing sequential EIS measurements are shown in Fig. 6(b). The order of events is as follows:

- 1) At system startup (not shown),  $C_{uc}$  needs to be precharged to  $V_{uc,start}$ , hence  $Q_{uc}$  is turned *on* and  $Q_{shunt}$  is controlled to regulate the ultracapacitor current according to a constant reference,  $V_{ref,pre}$ .
- 2) Over repeated measurements, prior to extracting the sinusoidal perturbation, the system enters the preconditioning phase,  $T_{pre}$ , where  $V_{uc}$  is discharged by the dc-dc converter down to the measurement start voltage  $V_{uc,start}$ . At the end of this period,  $Q_{uc}$  is turned *off*.
- 3) During the measurement phase,  $T_{measure}$ ,  $Q_{uc}$  is turned *on* again, and  $Q_{shunt}$  is controlled to regulate the battery current according to  $V_{ref,EIS}$ , which is generated by the SCS, and has a fixed amplitude of  $I_{EIS,peak}$  and a period equal to  $T_{EIS}$ .

Multiple  $T_{EIS}$  cycles are included in  $T_{measure}$  to improve the measurement accuracy. In the experimental prototype, the triggering of successive impedance measurements and data aggregation is performed using a PC that acts as the *Coordinator* in place of the pack-level BMS, while the local micro-controller (MCU) controls the Cuk converter within the module.

An optimal design of the hybrid architecture minimises cost and volume by appropriately distributing the energy discharged from the battery during EIS to three locations: 1) the auxiliary bus through the dc-dc converter, 2)  $C_{uc}$ , to be discharged during  $T_{pre}$  by the dc-dc, and 3) losses in  $Q_{shunt}$ . Given a set of EIS parameters,  $I_{EIS,peak}$ ,  $T_{EIS}$ , and  $T_{measure}$ , the necessary capacitance,  $C_{uc}$ , is expressed by

$$C_{uc} = \frac{\int_0^{T_{measure}} I_{uc}(t) dt}{V_{uc,max} - V_{uc,start}}, \quad (1)$$

where the time-varying ultracapacitor current  $I_{uc}$  is expressed by

$$I_{uc}(t) = I_{cell}(t) - I_{conv}, \quad (2)$$

where  $I_{cell}$  is the sinusoidal battery cell current with amplitude  $I_{EIS,peak}$  and period  $T_{EIS}$ , and  $I_{conv}$  is the constant dc-dc converter current during  $T_{measure}$ . The time-varying power dissipated in  $Q_{shunt}$  is defined as  $P_{shunt}$  and is expressed by

$$P_{shunt}(t) = I_{cell}(t)(V_{cell}(t) - V_{uc}(t)). \quad (3)$$



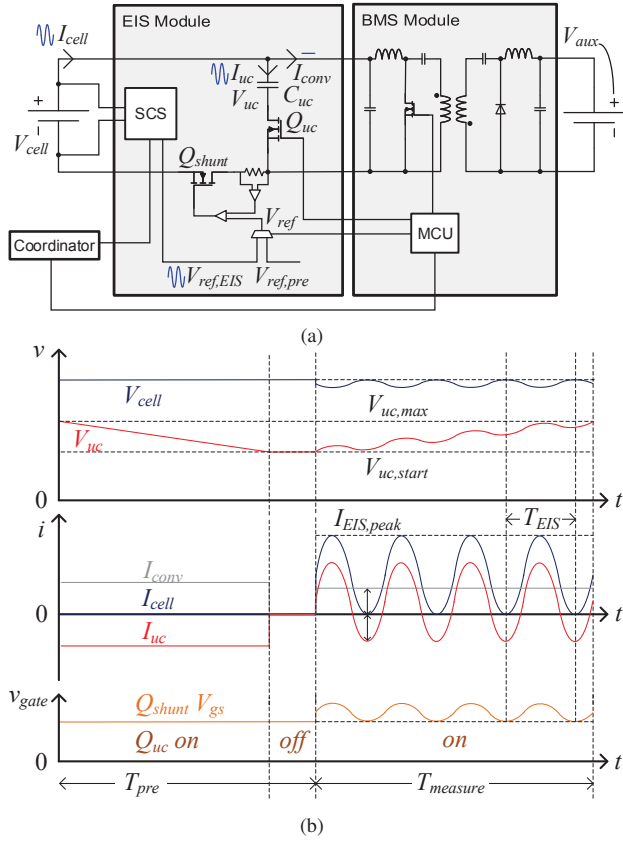


Fig. 6. Proposed hybrid architecture: (a) Prototype implementation, not integrated with switch matrix, the Ćuk converter operates at 300 kHz and is rated for 75 W at 25 V input, (b) ideal operating waveforms.

The component design parameters are:

- 1)  $I_{conv}$ , the dc-dc current,
- 2)  $C_{uc}$ , the ultracapacitor capacitance, and
- 3) the die heat capacity and junction-to-case resistance of  $Q_{shunt}$ .

For a given set of EIS parameters, trade-offs exist between each of the component design parameters. For example,  $C_{uc}$  could be increased to accommodate lower  $I_{conv}$ . Thus, given 1) the EIS parameters, 2) dc-dc current rating, and 3) switch matrix MOSFET thermal ratings in the EV BMS described in section III, it is possible to minimise the incremental cost and volume of introducing online EIS by calculating the minimum necessary ultracapacitor size required in the hybrid power stage. In this work, due to the high EIS current, the ultracapacitor size is limited by the ESR and maximum operating voltage, rather than capacitance.

For a given SNR requirement, the  $T_{measure}$  and  $I_{EIS,peak}$  must be selected according to the power stage thermal limit and the cell linearity. The same SNR can be reached by either 1) using high perturbation current and averaging measurements over fewer cycles, or 2) using low perturbation current and averaging measurements over more cycles. If the measurement removes sufficient charge from the cell to significantly change

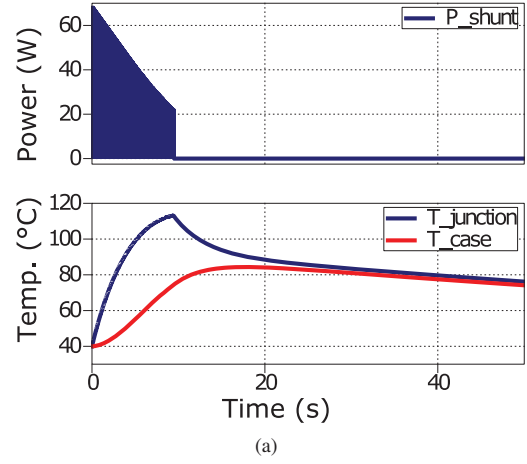


Fig. 7. Thermal-electrical simulation of the hybrid power architecture:  $Q_{shunt}$  power loss and junction and case temperatures.

TABLE II. HYBRID ARCHITECTURE SYSTEM PARAMETERS USED IN THERMAL-ELECTRICAL SIMULATION

Parameter	Value	Unit
EIS peak perturbation current, $I_{EIS,peak}$	30	A
EIS perturbation period, $T_{EIS}$	0.02	s
EIS measurement duration, $T_{measure}$	9	s
dc-dc constant current, $I_{conv}$	6	A
Ultracapacitor capacitance $C_{uc}$	50	F
Ultracapacitor ESR	21	mΩ
Shunt MOSFET $R_{th,jc}$	3	K/W
Shunt MOSFET package	TO-263	

its operating point over the frequency range of interest, then the model accuracy will be reduced. A similar effect is possible with cell self-heating due to perturbation current. To highlight one possible operating scenario,  $P_{shunt}$  and the  $Q_{shunt}$  junction and case temperatures from a thermal-electrical simulation are shown in Fig. 7, for which the parameters are shown in Table II. The listed EIS parameters are the initial test parameters for the prototype system, and are used for the oscilloscope waveforms shown in Section IV-B. The experimental Nyquist plots in Section IV-B are measured using  $I_{EIS,peak} = 40$  A and  $T_{measure} = 1$  s at all  $T_{EIS}$  points. The other system parameters in the simulation are chosen to reflect the system described in section III, and match the experimental setup. An optimal design and calibration of the system considering all relevant parameters is not presented in this paper.

It can be seen in Fig. 7 that as the measurement occurs from 0 to 10s, the amplitude of  $P_{shunt}$  decreases due to the increase in  $V_{uc}$ . The peak junction temperature of 113 °C indicates the system operates near the thermal limit, which is an indicator of optimal component use.

## B. Experimental Results

The experimental setup, as shown Fig. 8, consists of four 44 Ah NMC cells in parallel, the EIS module board, EV battery prototype BMS module board (currently without the switch matrix), SCS communication interface, and an electronic load (not shown) to emulate the 12V auxiliary battery. EIS per-

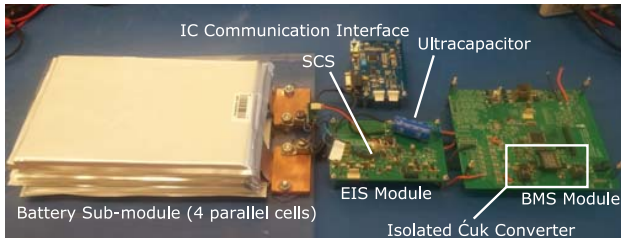


Fig. 8. Hybrid topology experimental setup.

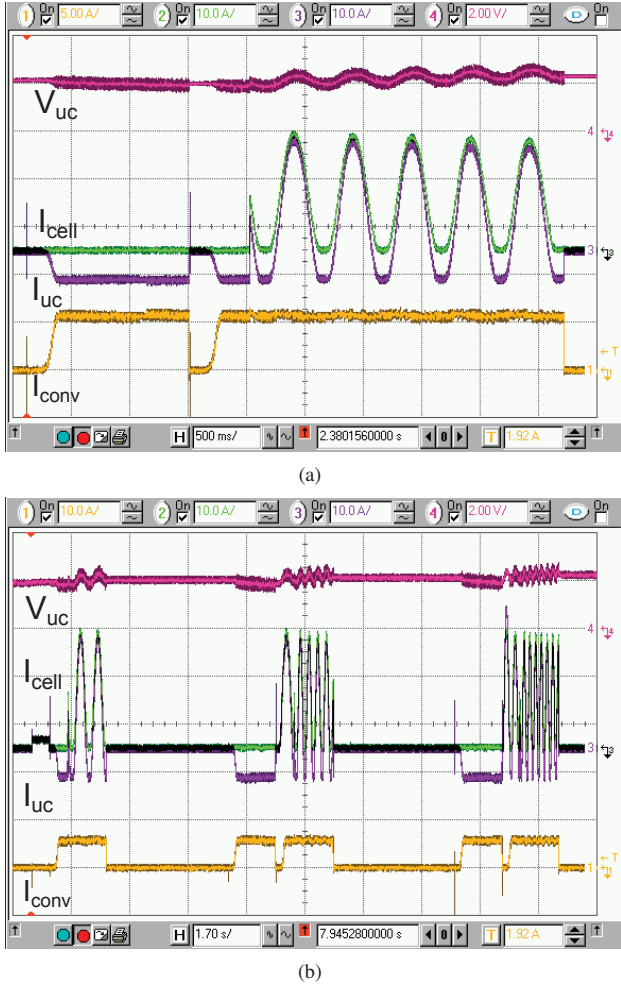


Fig. 9. Hybrid topology experimental results: (a) single impedance measurement cycle, (b) three subsequent impedance measurement cycles.

turbation of a single cell is shown in Fig. 9(a) at a single frequency, and in Fig. 9(b) at multiple frequencies. The EIS current and timings are tuned to showcase system operation. The waveforms match well with Fig. 6(b), except for some noticeable current distortion due to the limited accuracy of the current-loop, as well some switching noise from the converter. The ultracapacitor is operated at 2.4 V peak to stay safely below the 2.7 V rating and prolong its lifetime.

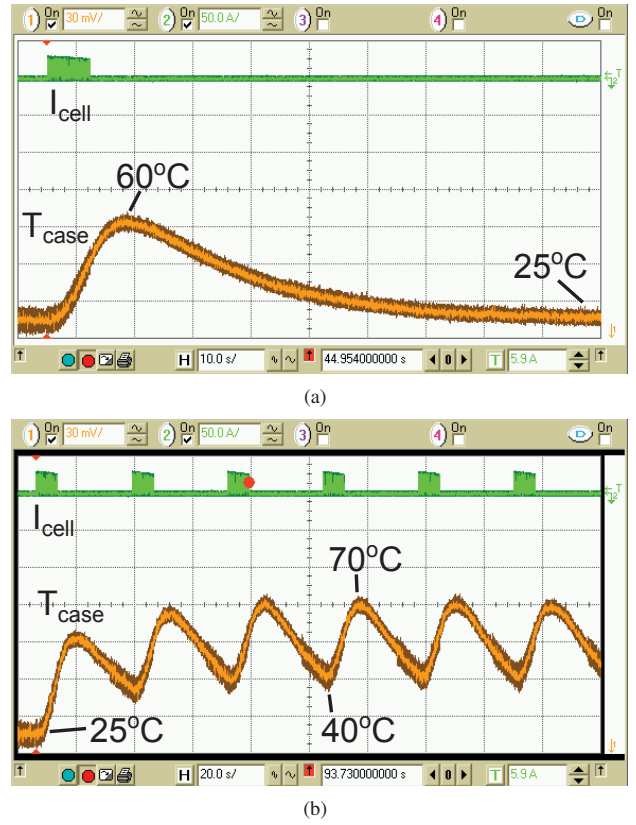


Fig. 10. Hybrid topology experimental results: (a) MOSFET case temperature over single 50 Hz impedance measurement cycle, and (b) MOSFET case temperature over 6 impedance measurement cycles with 25 s delay between each.

To highlight the thermal challenge imposed by EIS measurement at such high perturbation currents, the case temperature of the shunt MOSFET from two calibration experiments is shown in Figs. 10(a) and 10(b). During repeated measurement cycles, the steady-state temperature rise from ambient is 45°C, and the maximum rise rate is 3°C/s. It can be seen that the temperature rise directly impacts the maximum measurement speed. The case temperature curve shows consistency in shape with the simulation from Fig. 7. The discrepancy in temperature could be due to inaccuracy in both the measurement and thermal model. In a system with only the shunt MOSFET and without the ultracapacitor, the maximum heat dissipation would be approximately double under the same conditions, which provides a strong motivation for the hybrid approach.

Nyquist curves of EIS measurements taken with the hybrid power stage are shown in Fig. 11. All measurements are taken with the same power stage operating with  $I_{cell} = 40$  A,  $T_{measure} = 1$  s, and frequency varying from 2 to 2000 Hz. Fig. 11(a) shows two Nyquist curves of a single cell. The curves correspond to measurements made with either 1) an oscilloscope, or 2) the SCS. The oscilloscope measurement setup consists of a *Preamble Instruments 1855* differential

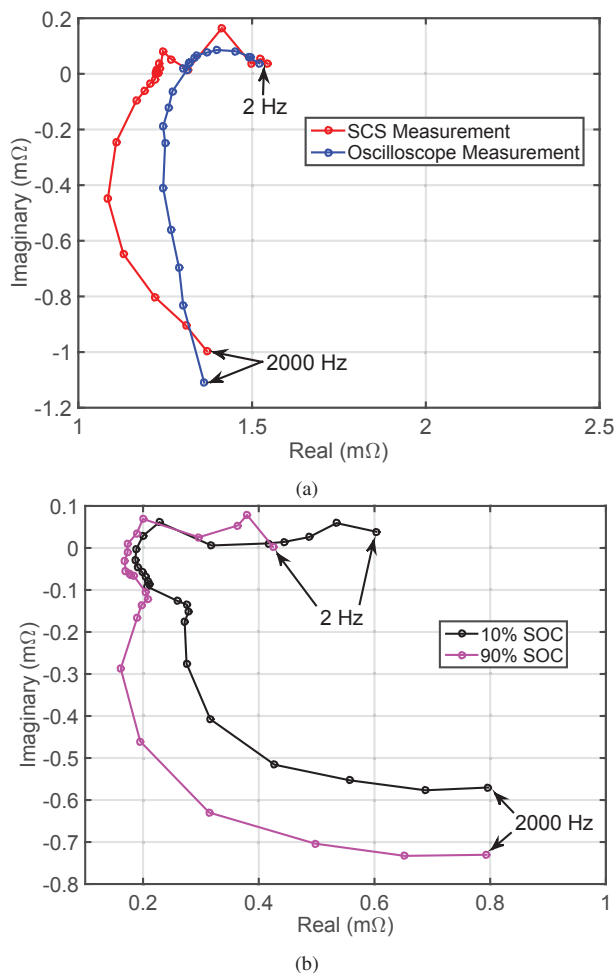


Fig. 11. Hybrid topology experimental results: (a) Nyquist plots of a single 44 Ah cell using hybrid topology perturbation and measurement with oscilloscope and SCS, (b) Nyquist plots of four parallel 44 Ah cells at two SOC points using hybrid topology perturbation and measurement with SCS.

amplifier with *LeCroy DXC 100A* differential probe for voltage measurement, and *Tektronix TCP303* current probe with *TCPA300* amplifier for current. While the oscilloscope instrumentation setup is meant for precision measurements, it should not be considered an ideal reference. The discrepancy between the two curves in Fig. 11(a) indicates that further tuning and verification of the accuracy and precision of all instrumentation used is necessary. The impedance of four cells in parallel, measured at two SOC points with the hybrid power stage and SCS, is shown in Fig. 11(b). The measured real impedance at low frequency is higher at 10% SOC compared to 90%, which is consistent with what is described in [8].

## V. CONCLUSION

The IC presented in this paper facilitates next-generation BMS architectures with embedded EIS at 200 mA. The low-impedance cells used in larger EVs impose a high SNR requirement for EIS. The proposed hybrid architecture presents

one method to meet this requirement, by significantly increasing the perturbation current amplitude. By introducing a small ultracapacitor in each battery module, and leveraging the isolated dc-dc converter that is used for auxiliary supply, the thermal loss on the shunt device is reduced. This enables the addition of high-perturbation-current online EIS to the BMS presented here at minimal incremental impact to system size and cost. The hybrid architecture has been successfully used to measure the impedance of a 44 Ah, 1 mΩ nominal ESR Lithium NMC cell, as well as four such cells connected in parallel.

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