IfElsePkg Package User Guide

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Ву

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1 IfElsePkg Overview

IfElsePkg provides a function that returns one of two input values based on a conditional. It is a stand in for the "when else" language capability that is in VHDL-2019 (but is not currently supported by all simulators).

2 IfElse Function

IfElse function returns the value from parameter A when the expression is true, otherwise, it returns the value from parameter B. AType can be string, std_logic, std_logic_vector, integer, or boolean.

```
function IfElse(Expr : boolean ; A, B : AType) return AType ;
```

The targeted use of IfElse is in an constant expression, such as shown below.

3 About IfElsePkg

IfElsePkg is part of the OSVVM Utility library.

IfElsePkg was created by Jim Lewis of SynthWorks. Please support our work by buying your VHDL Training from SynthWorks.

IfElsePkg.vhd is a work in progress and will be updated from time to time. Caution, undocumented items are experimental and may be removed in a future version.

4 Compiling and Using OSVVM Utility Library

Reference all packages in the OSVVM Utility library by using the context declaration:

```
library OSVVM ;
  context osvvm.OsvvmContext ;
```

Compilation order for OSVVM Utility Library is in OSVVM_release_notes.pdf. Rather than learning this, we recommend using the OSVVM compilation scripts.

OSVVM Utility library is released under the Apache open source license. It is free (both to download and use - there are no license fees). You can download it from osvvm.org or from our development area on GitHub (https://github.com/OSVVM/OSVVM).

If you add features to the package, please donate them back under the same license as candidates to be added to the standard version of the package. If you need features, be sure to contact us.

We also support the OSVVM user community and blogs through http://www.osvvm.org. Interested in sharing about your experience using OSVVM? Let us know, you can blog about it at osvvm.org.

5 About the Author - Jim Lewis

Jim Lewis, the founder of SynthWorks, has thirty plus years of design, teaching, and problem solving experience. In addition to working as a Principal Trainer for SynthWorks, Mr Lewis has done ASIC and FPGA design, custom model development, and consulting.

Mr. Lewis is chair of the IEEE 1076 VHDL Working Group (VASG) and is the primary developer of the Open Source VHDL Verification Methodology (OSVVM.org) packages. Neither of these activities generate revenue.

Please support our volunteer efforts by buying your VHDL training from SynthWorks.

If you find bugs these packages or would like to request enhancements, you can reach me at jim@synthworks.com.